HEWLETT PACKARD

Isolation and Control Components Designer's Catalog

HEWLETT® PACKARD

Hewlett-Packard: A Leader in Components

A Brief Sketch

Founded in 1961, and headquartered in San Jose, California, the Hewlett-Packard Company's Components Group is the world's largest independent supplier of communications components. Today the group has approximately 9500 employees, and had fiscal 1995 revenues of $856 million.

The Components Group incorporates three major divisions–Optoelectronics, Optical Communication and Communications Components–and serves six major markets: communications, computer/office, industrial, transportation, consumer and government/military. Included in the Components Group's extensive line of more than 9,000 components are visible and infrared LED lamps; visible LED displays, light bars and arrays; Infrared Data Association (IrDA)-compliant infrared transceiver modules; fiber-optic transceivers, transmitters and receivers meeting most of today's industry standards; motion control devices; optocouplers and related optically-isolated control components; bar-code components; RF and microwave semiconductors; and communications amplifiers and assemblies. HP offers the world's brightest LEDs and is a technical leader for visible III-V products.

The Components Group markets products through a sales force of 300 technically-educated sales professionals located in about 40 countries. HP components are also sold through a worldwide distributor network with more than 150 locations. Altogether, 95 percent of sales revenues are from customers external to HP.

The Components Group maintains five marketing centers worldwide in San Jose, California; Boeblingen, Germany; Tokyo, Japan; Frimley, UK; and Singapore. Each is fully staffed with product application and support engineers and each is responsible for regional decision making. A design center in Tokyo is specifically chartered to develop products for the Japanese market.

Local decision-making is central to HP's transnational business strategy which focuses on customer satisfaction. In addition to providing the right product with superior quality and reliability, the Components Group strives to ensure worldwide product availability, accurate on-time delivery and up-to-date technical information for its customers.

Quality and Reliability

Quality and reliability are very important concepts to Hewlett-Packard in maintaining the commitment to product performance.

At Hewlett-Packard, quality is integral to product development, manufacturing, and final introduction. HP's commitment to quality means that there is a continuous process of improvement and tightening of quality standards. Manufacturing quality circles and quality testing programs are important ingredients in HP products.

Reliability testing is also required for the introduction of new HP components. Lifespan calculations in "mean-time-between-failure" (MTBF) terms are published and available as reliability data sheets. HP's stringent reliability testing assures long component lifetimes and consistent product performance.

Information about the Components Group and its products can be found on the World Wide Web at **http.//www.hp.com/go/components**

The body of this book is printed on recycled paper.

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About This Catalog

About This Catalog

To help you choose and design with Hewlett-Packard optoelectronic components, this catalog contains detailed product specifications. The catalog is divided into four product sections:

1. Optocouplers
2. Motion Sensing and Control Products
3. Fiber-Optic Components
4. Bar Code Components

How to Find the Right Information

- The Table of Contents helps you locate the product sections as well as the Data Sheet Index and selection guides for each product section.
- The Alphanumeric Index lists every component in this catalog and the page number on which the corresponding data sheet is located.
- Data Sheet Indexes list all of the data sheets in the product section.
- Selection Guides allow you to quickly select products most suitable for your application.

How to Order

To order any component in this catalog, call your nearest HP authorized distributor or HP sales office.

A complete listing of HP authorized distributors is located on page 6-3. These distributors can offer off-the-shelf delivery for most HP components.

Service and Support

For technical assistance or for the location of your nearest HP sales office, distributor or representative call (US and Canada only): 1-800-235-0312 or 408-654-8675.

Elsewhere in the world, call your local Hewlett-Packard sales office. Ask for a Components representative.

For Additional Information

In the US/Canada, technical literature is available from the Hewlett-Packard Components Group fax-back service at: 1-800-450-9455, or from the Components Sales Response Center at 1-800-235-0312.

Elsewhere in the world, call your local HP sales office. Ask for a Components representative.

Information regarding Hewlett-Packard Components Group products is available on the World Wide Web at **http://www.hp.com/go/components**

Literature is available regarding other HP Components Group products not listed in this catalog:

- *High Performance Fiber-Optic data communications and telecommunications products*
- *LED Lamps and Displays*
- *Infrared Products*
- *RF & Microwave Products*

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*See Hermetic and Hi-Rel Data Sheets.

Bold type = new product

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Optocouplers

- **Plastic Optocouplers**
- **Isolation Amplifiers**
- **Solid State Relays**
- **Hermetic Optocouplers**

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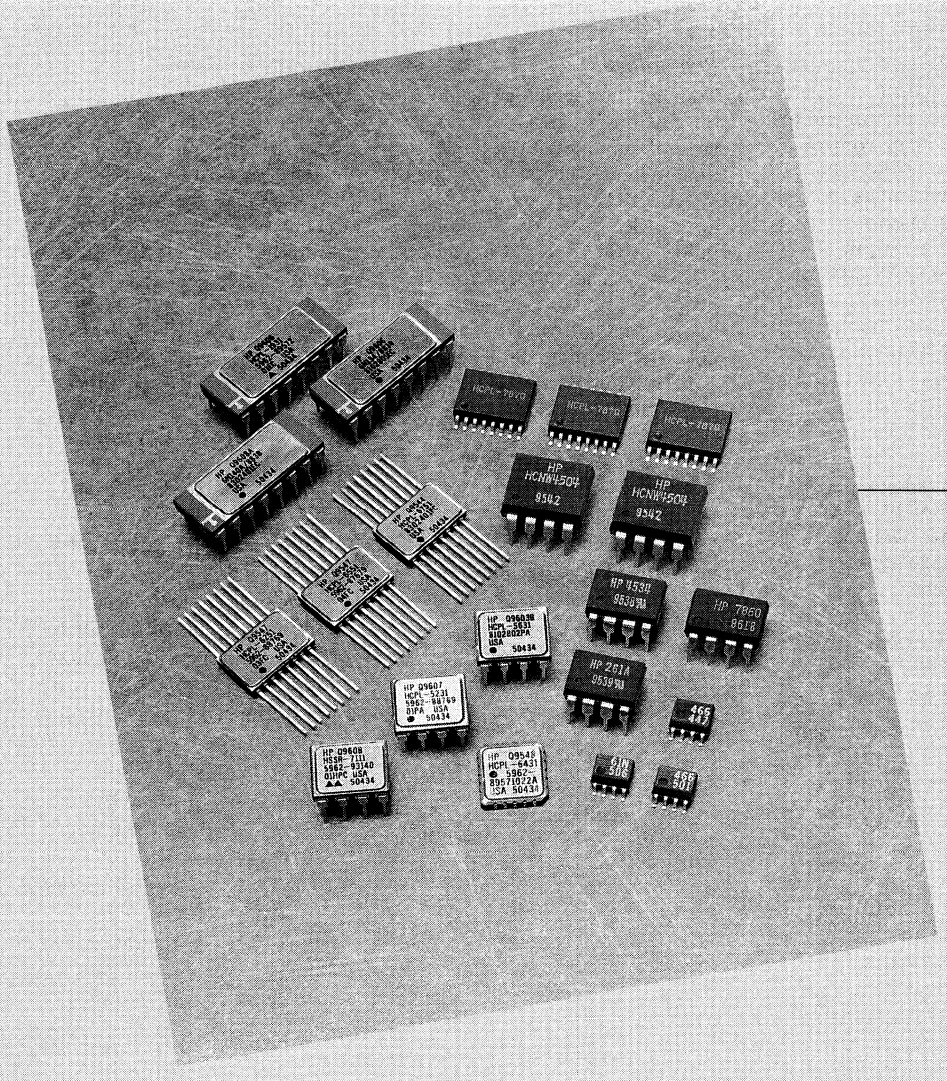


Optocouplers

With Hewlett-Packard's broad line of optically coupled isolation products you can put an end to erroneous data, false control signals and damaged circuits. HP has six primary families of optocouplers to choose from: 1 MBd Transistor Output, 100 KBd High gain Transistor Output, 5 MBd Logic Gate, 10 MBd Logic Gate, Integrated Gate Drive, and Miniature Isolation Amplifiers. In addition, HP offers a wide array of application specific devices for applications like line receivers and wideband analog/video, as well as isolated A/D Converters. Most families are available in a variety of package styles to fit your design needs.

NEW High Performance Optocouplers from HP!

High Common Mode Rejection

If you are designing in a noisy environment, HP optocouplers lead the industry in performance. Common mode rejection levels of 15,000 V/µs can be achieved using HP's high performance optocouplers. Look in the selection guide for a wide array of performance choices.

Regulatory

To meet the regulatory needs of our customers, HP has expanded several families with 400 mil dual in line packages providing V_{IORM}=1414 V_{PEAK} and VDE approval. Look in the selection guide for these parts prefixed "HCNW". In addition, many products are now available with an optional 630 V_{PEAK} VDE approval (Option #060). These parts are indicated with an "A" under the VDE column of the selection guide.

Low input current

HP has expanded the 10 MBd Logic Gate family with several new, low input current alternatives. These parts can be driven from HCMOS gates directly and may eliminate extra drive circuitry and reduce the size of the power supply needed. Look for these parts in the 10 MBd Logic gate section of the selection guide with suffixes "A" or "N". In addition, HP introduced a 100 KBd high gain transistor output part with 40 µA drive current, the lowest in the industry.

Motor Control Optocouplers

Hewlett-Packard also offers a complete line of optocouplers designed specifically to address the needs of isolated gate drive and current sensing applications within the motor control market.

Gate Drive

The most recent additions to our family of gate drive optocouplers include the HCPL-3120 and HCPL-3150. Optimized for directly driving IGBTs with ratings up to 1200 V/100 A or 1200 V/50 A respectively, each optocoupler provides the following application critical performance:

- 2.0 A and 0.5 A, respectively, Minimum Peak Output Currents
- 15 kV/µs Minimum Common Mode Rejection (CMR)
- -40°C to +100°C Performance Guarantees
- Under Voltage Lockout Protection with Hysteresis
- 500 ns Maximum Switching Speeds
- UL, VDE and CSA Regulatory Approval
- 15 to 30 V V_{CC} Operating Range
- Low Level Output Voltage
- 5 mA Maximum Supply Current

By incorporating an integrated fault feedback optocoupler, our soon to be introduced **HCPL-3160** will provide even lower cost, area efficient IGBT gate drive by offering desaturation or over-current detection and local IGBT shutdown.

For interfacing to an Intelligent Power Module's (IPM) power transistor gate drive circuitry, HP introduced the **HCPL-4506** family of optocouplers. Available in several 8-pin package styles, the HCPL-4506 (PDIP), **HCPL-0466** (SO8), and **HCNW4506** (Widebody PDIP) provide significant performance advantages for such design critical specifications as current transfer ratio, propagation delay, and common mode rejection.

Current Sense

As extensions to its family of HCPL-7800 Analog Isolation Amplifiers for motor drive current sensing, HP introduced the **HCPL-7820**, **HCPL-7825,** and **HCPL-7840**. Each offers a breakthrough combination of unequaled CMR performance, compact size, -40°C to +100°C performance guarantees, and overall lower solution cost as compared to the predominant form of competition.

Most recently, HP introduced the **HCPL-7860** and **HCPL-7870**, which together form an **Isolated 15-bit Programmable A/D Converter** that delivers the reliability, small size, superior isolation and over temperature performance motor drive designers need to accurately measure current at half the price of traditional solutions. Peformance features include:

- 12-bit Linearity
- Resolution/Speed trade-off with 5 different Conversion Modes
- 12-bit effective resolution with 18 µs signal delay
- 14-bit effective resolution with 95 µs signal delay
- Fast 3 µs Over-Range Detection
- ± 200 mV Input Range with single 5 V supply
- Internal Reference Voltage
- Offset Calibration
- -40°C to +85°C Operating Temperature Range
- 15 kV/µs Isolation Transient Immunity
- UL, CSA and VDE Regulatory Approval

Product Safety Regulations and Optocouplers

Optocouplers optically transfer a signal from one circuit to another circuit within or between electrical equipment. In addition to providing common-mode signal isolation, optocouplers are often used to provide high voltage insulation. This is done by preventing voltage transients on a signal line from affecting the equipment, and by protecting the operator from high voltage which may be present inside the equipment.

Because optocouplers perform a safety function, they are tested and qualified for use in each country, usually through national third party safety agencies, both at the component level and system level. Third party safety agencies are often private organizations which have governmental authority and develop standards for many aspects of equipment manufacture (e.g., safety, electromagnetic interference reduction, protecting the environment).

In Europe, standardization for equipment specifications is well in progress. The European Economic Community (EEC) established a target date of January 1, 1992 for all member countries and manufacturers to be in compliance with the EEC directives. Transitional periods have been established by each member country when they will begin enforcing and accepting the European norms(EN), by creating national laws. The EEC is now known as the European Union(EU), composed of 15 countries.

At this time, optocouplers have not had the benefit of harmonized test requirements, i.e., agreement among countries and their respective national agencies. Testing, approval, recognition and certification must still be obtained from each country where optocouplers will be used. Each country tests optocouplers to different standards, either component based or system/equipment based.

Each Hewlett-Packard optocoupler data sheet provides the design engineer with sufficient information to determine which optocouplers are suitable for an application. Although some equipment standards are more specific than others and definitions may vary, each

Testing Level	Country	Standard/Specification	Agency
Component	Germany	VDE 0884 (June 1992 revision)	Verband Deutscher Elektrotechniker (VDE)
	United States	UL 1577	Underwriters Laboratories (UL)
	Canada	CSA Component Acceptance Notice No. 5	Canadian Standards Association (CSA)
System/ Equipment	United Kingdom	BS 415 BS EN60950 BS 7002 BS EN41003	British Standards Institute (BSI)

standard will specify the safety related requirements for a particular type of equipment.

Certain parameters are used to determine where Hewlett-Packard optocouplers fit in your applications. These parameters are found in each Hewlett-Packard data sheet and are noted by **bold print** in the common definitions provided below. A summary of these parameters is provided as well.

Common Parameters and Definitions

Comparative Tracking Index (CTI)

CTI is a measure of the optocoupler mold material and its relative insulating capability. The surface of the mold material is subjected to an alternating low-voltage stress, which produces a small current flow. When the current flow reaches a predetermined value, the corresponding numerical value of the applied voltage is the **CTI** value. **CTI** impacts both **External Creepage** and maximum allowable **Working Voltage**, where higher **CTI** values allow more **Working Voltage** for the same value of **External Creepage** distance.

Material Group

Because the behavior of insulating materials is very complex under various contaminants and voltages, direct correlation between deterioration of the insulating material and formation of conductive paths on the insulation surface is not practical. Correlation between the **Comparative Tracking Index** (**CTI**) and ranking performance of insulating materials has been found by empirical observation. Consequently, **CTI** values can be used to categorize insulation materials:

Material Group I
600 < CTI

Material Group II
400 < CTI < 600

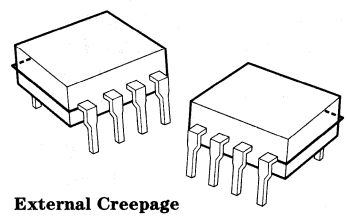
Material Group IIIa
175 < CTI < 400

Material Group IIIb
100 < CTI < 175

In some equipment specifications, Material Group is used in conjunction with **Pollution Degree**, **Creepage** distance, and **Working Voltage** tables.

Creepage, External

External Creepage is the shortest distance path along the outside surface of an optocoupler, between the input and output leads, usually measured in mm. **External Creepage** plus **Pollution Degree** plus **Material Group** (**CTI**) determine the maximum allowable **Working Voltage** applied to an optocoupler.



External Creepage

Clearance, External

External Clearance is the shortest distance through air, between two conductive leads, input to output, usually measured in mm. **Clearance** determines the maximum **Transient Overvoltage** that can be applied to an optocoupler with respect to the equipment **Mains Voltage** and **Installation Class**.

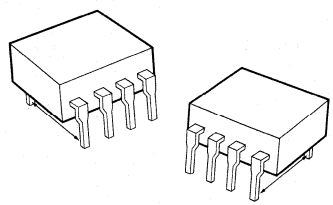
However, once mounted on a printed circuit board, minimum creepage and clearance requirements must be met as specified for individual equipment standards. For creepage, the shortest distance path along the surface of a printed circuit board between the solder fillets of the input and output leads must be considered. There are recommended techniques such as grooves and ribs which may be used on a printed circuit board to achieve desired creepage and clearances.

Clearance, Internal (Distance through Solid Insulation)

As applied to optocouplers, this is the direct distance between the photoemitter and photodetector inside the optocoupler cavity. Some equipment standards require a minimum 0.4 mm distance through solid insulation for reinforced levels.

Pollution Degree Environment

Pollution Degree is determined by the equipment-use environment. **Pollution Degree 2** is typically used as a "benchmark" to establish test voltages, especially for VDE 0884 qualification. Higher **Pollution Degrees** (3, 4) indicate dirtier, more contaminated environments.



External Clearance

Dielectric Withstand-Voltage

Capability of a device to withstand without breakdown for 60 seconds, a potential difference equal to the dielectric insulation voltage applied between the input and output leads of an optocoupler. This is a safety parameter and is also known as **Input-Output Momentary Withstand Voltage**. This is a dielectric voltage rating in V_{rms} and is not to be interpreted as an input-output continuous **Working Voltage** rating. For the continuous voltage rating, refer to your equipment level safety specification. See also **Working Voltage**.

Working Voltage

Working Voltage is the maximum continuous voltage which may be applied to the insulation of an optocoupler under normal operating conditions. **Working Voltage** is not the same as the 60 second **Dielectric Withstand-Voltage**. **Working Voltage** is determined by a combination of numerous factors such as **External Creepage**, equipment mains voltage, insulation level (e.g., basic or reinforced), **Pollution Degree, and Material Group**.

Endurance Voltage

Endurance Voltage is the ability of an optocoupler insulating material to endure continuous voltage over long periods of time without damaging the optocoupler. It is an empirical measure of the robustness and reliability of the optocoupler. Endurance Voltage must not be confused with or replace **Working Voltage**, which is defined by equipment standards. In all cases where regulatory compliance is required, **Working Voltage** sets the maximum allowable steady-state, input-output voltage. See Hewlett-Packard's application note on Optocoupler Input-Output Endurance Voltage (AN 1074). Our current data sheets provide sufficient information to determine the suitability of Hewlett-Packard optocouplers for your applications. Our engineers are also available to assist you in determining which optocoupler best fits your need. For more detailed information and guidance, contact your local Hewlett-Packard sales representative.

Common Optocoupler Parameters Equipment Installation Requirements

Product Family	External Creepage	External Clearance	Internal Clearance	Material Group	Pollution Degree	Dielectric Withstand Voltage, Vrms, 1 min.	Country Regulatory Approvals
HCNW/HCNR Series "Wide Body" 8-pin DIP or Surface Mount	10.0	9.6 mm	1.0	IIIa CTI = 200	2 (Typical)	5,000 V	United States-UL Canada-CSA Germany-VDE United Kingdom-BSI
HCPL-7XXX Series 8-pin DIP or Surface Mount	8.0 mm	7.4 mm	0.5 mm	IIIa CTI = 175	2 (Typical)	3,750 V	United States-UL Canada-CSA Germany-VDE
HCPL-XXXX Series 8-pin DIP or Surface Mount	7.4 mm	7.1 mm	0.08 mm	IIIa CTI - 200	2 (Typical)	2,500 V and 5,000 V (See specific data sheet)	United States-UL Canada-CSA Germany-VDE
HCPL-0XXX Series 8-pin SO8 Surface Mount	4.8 mm	4.9 mm	0.08 mm	IIIa CTI = 200	2 (Typical)	2,500 V	United States-UL Canada-CSA
HCPL-MXXX Series 5-pin Miniflat Surface Mount	5.0 mm	5.5 mm	0.08 mm	IIIa CTI = 200	2 (Typical)	2,500 V	United States-UL Canada-CSA

Optocouplers for Safe Electrical Separation per VDE 0884

Optocouplers providing safe electrical separation per VDE 0884 (June 1992) do so only within the safety-limiting values to which they are qualified. Protective cut-out switches must be used to ensure that the safety limits are not exceeded. The insulation characteristics for each VDE approved optocoupler are shown in the Insulation Characteristics Table, which includes the permitted installation classes vs. equipment mains voltage, maximum allowable transient overvoltage, maximum allowable working voltage, climatic classification and safety limiting values.

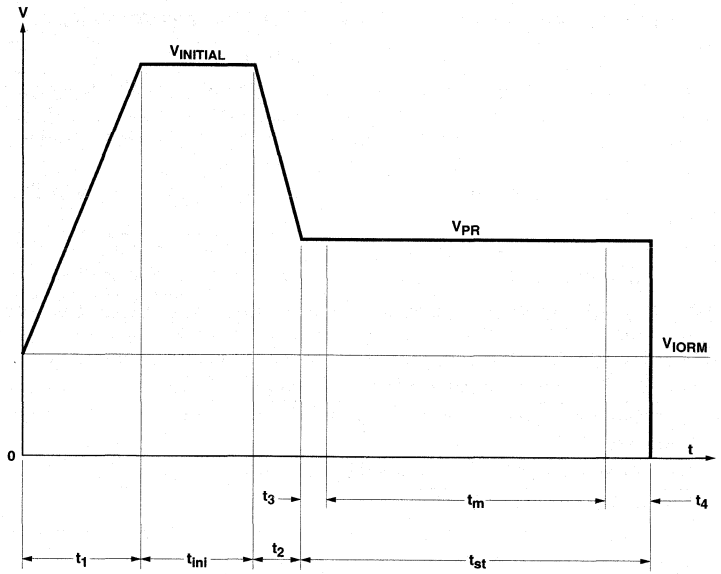
Partial discharge measurement per VDE 0884 (June 1992) is a technique to evaluate the insulation integrity of optocouplers. VDE's philosophy is that partial discharge testing replaces the common dielectric withstand voltage test, because any dielectric voltage test may predamage the insulation of an optocoupler. Although successful partial discharge testing qualifies an optocoupler for reinforced insulation applications, some equipment standards may impose specific restrictions for reinforced insulation such as internal clearance and doubling the external creepage value. The profiles below describe the partial discharge test for type and sampling (Procedure A) and for 100% production (Procedure B) testing in accordance with VDE 0884:

PROCEDURE A:
(FOR TYPE AND SAMPLING TESTS, DESTRUCTIVE TESTS)

t_1, t_2 = 1 to 10 s
t_3, t_4 = 1 s

t_m (MEASURING TIME FOR PARTIAL DISCHARGE) = 60 s

t_{st} = 62 s
t_{ini} = 10 s

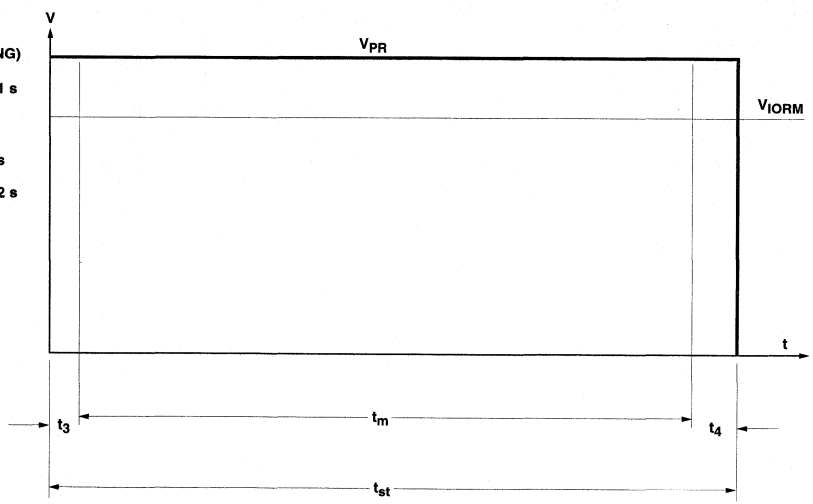


PROCEDURE B:
(FOR 100% PRODUCTION TESTING)

t_3, t_4 = 0.1 s

t_m (MEASURING TIME FOR PARTIAL DISCHARGE) = 1 s

t_{st} = 1.2 s



Definitions of Terms Used in VDE 0884 Partial Discharge Testing

Term	Definitions
$V_{INITIAL}$	Maximum test voltage for the partial discharge test. It is also the maximum transient overvoltage occurring in a rated mains voltage and service class. At this initial voltage partial discharge (but no breakdown) may occur. $V_{INITIAL}$ also equals V_{IOTM} (transient overvoltage) which is listed in the applicable VDE insulated related characteristics sections of this catalog. Preferred values for $V_{INITIAL}$ are shown in Table 1 below (from Table 2 of VDE 0884, June 1992 revision).
V_{PR}	Partial discharge test voltage applied to an optocoupler and maintained for a specific time period, t_{st}. During this time, partial discharge is measured at a specific time interval, t_m. V_{PR} = 1.5 X V_{IORM} for Procedure A and V_{PR} = 1.875 X V_{IORM} for Procedure B.
V_{IORM}	Working voltage (maximum service insulation voltage) – this is the maximum continuous permitted voltage which may be applied to an optocoupler. This value is specified in each applicable VDE insulated related characteristics section of this catalog.
t_m	Test time for partial discharge and equals 60 seconds for Procedure A, 1 second for Procedure B.
t_{ini}	Time beginning at $V_{INITIAL}$ test voltage and equals 10 seconds.
t_1, t_2, t_3, t_4	Test voltage initialization times.
Pass/Fail Criteria	No leakage failures and no optocoupler to have more than 5 pC Partial Discharge during partial discharge test time, t_m.

Table 1. (from VDE 0884-June 1992, Table 2)

	Preferred Insulation Test Voltages for Service Class (V Initial)			
Rated Mains Voltage up to and Including Vrms or Vdc	**I PEAK**	**II PEAK**	**III PEAK**	**IV PEAK**
50	330	500	800	1500
100	500	800	1500	2500
150	800	1500	2500	4000
300	1500	2500	4000	6000
600	2500	4000	6000	8000
1000	4000	6000	8000	12000

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- High CMR, High Speed Optocouplers 1-33
- Intelligent Power Module and Gate Drive Interface Optocouplers 1-49
- Dual Channel, High Speed Optocouplers 1-63
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- Low Input Current, High Gain Optocouplers 1-77
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- Dual Channel Low Input Current, High Gain Optocouplers 1-108
- Low Input Current, Logic Gate Optocouplers 1-120
- Very High CMR, Wide V_{CC} Logic Gate Optocouplers 1-131
- High CMR, High Speed TTL Compatible Optocouplers 1-146
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- 2.0 Amp Output Current IGBT Gate Drive Optocoupler 1-182
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- High CMR Analog Isolation Amplifiers 1-233
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- 20 MBd High CMR Logic Gate Optocouplers 1-300
- High CMR Line Receiver Optocouplers 1-314
- Power Based Transistor Base Drive Optocouplers 1-329
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- Optically Coupled 20 mA Current Loop Transmitter 1-361
- Optically Coupled 20 mA Current Loop Receiver 1-373
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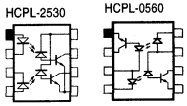
- 40 ns Prop. Delay, SO-8 Optocoupler 1-416
- High-Linearity Analog Optocouplers 1-418
- High-Gain Darlington Output Optocouplers 1-434
- 60 V/0.7 Ohm, General Purpose, 1 Form A, Solid State Relay 1-441
- 200 V/160 Ohm, 1 Form A, Small-Signal Solid State Relay 1-454
- 400 V/10 Ohm, General Purpose, 1 Form A, Solid State Relay 1-465
- Optocoupler Option for 5000 V rms/1 Minute Requirement 1-478
- VDE 0884 V_{IORM} = 630 V peak Option for Plastic Optocouplers 1-480
- Gull Wing Surface Mount Option for Optocouplers and Solid State Relays 1-482
- Tape and Reel Packaging Option for Optocouplers and Solid State Relays 1-485
- Hermetic & Hi Rel Optocouplers Data Sheet Index 1-492

Single Channel 1 MBd Transistor Output Optocoupler (6N135/6 Type)

Part Number	Package 300 mil DIP	Package SO8	Package 400 mil DIP	I_f mA	Prop Delay t_{PHL} µs (max.)	Prop Delay t_{PLH} µs (max.)	CTR Min. %	CTR Max. %	CMR – V/µs (V_{CM}) 1000 (10 V)	CMR – V/µs (V_{CM}) 10000 (1.5 kV)	CMR – V/µs (V_{CM}) 15000 (1.5 kV)	VDE V_{IORM} 630 Vp	VDE V_{IORM} 1414 Vp	Insulation UL = 1 min. 2500 V	Insulation UL = 1 min. 5000 V	Page No.
6N135	✓			16	2.0	2.0	7	50	✓					✓	B	1-16
HCPL-0500		✓		16	2.0	2.0	7	50	✓					✓		
HCNW135			✓	16	2.0	2.0	7	150	✓				✓		✓	
6N136	✓			16	1.0	1.0	19	50	✓					✓	B	
HCPL-0501		✓		16	1.0	1.0	19	50	✓					✓		
HCNW136			✓	16	1.0	1.0	19	150	✓				✓		✓	
HCPL-4502[1]	✓			16	1.0	1.0	19	50	✓					✓	B	
HCPL-0452[1]		✓		16	1.0	1.0	19	50	✓					✓		
HCNW4502[1]			✓	16	1.0	1.0	19	150	✓				✓		✓	
HCPL-4503[1]	✓			16	1.0	1.0	19	50			✓	A		✓	B	
HCPL-0453[1]		✓		16	1.0	1.0	19	50			✓			✓		
HCNW4503[1]			✓	16	1.0	1.0	19	150			✓		✓		✓	
HCPL-4504[1]	✓			12	1.0	1.4	26	65		✓		A		✓	B	1-33
HCPL-0454[1]		✓		12	1.0	1.4	26	65		✓				✓		
HCNW4504[1]			✓	12	1.0	1.4	25	65		✓			✓		✓	
HCPL-4506[2]	✓			10	0.4	0.55	44	>90			✓	A		✓	B	1-49
HCPL-0466[2]		✓		10	0.4	0.55	44	>90			✓			✓		
HCNW4506[2]			✓	10	0.4	0.55	44	>90			✓		✓		✓	

Notes:
1. Pin 7 not connected.
2. Pin 7 connected to internal 20 K pull-up resistor.

HCPL-2530 HCPL-0560



Dual Channel 1 MBd Transistor Output Optocoupler (6N135/6 Type)

Part Number	Package 300 mil DIP	Package SO8	Package 400 mil DIP	I_f mA	Prop Delay t_{PHL} µs (max.)	Prop Delay t_{PLH} µs (max.)	CTR Min. %	CTR Max. %	CMR – V/µs (V_{CM}) 1000 (10 V)	CMR – V/µs (V_{CM}) 10000 (1.5 kV)	CMR – V/µs (V_{CM}) 15000 (1.5 kV)	VDE V_{IORM} 630 Vp	VDE V_{IORM} 1414 Vp	Insulation UL = 1 min. 2500 V	Insulation UL = 1 min. 5000 V	Page No.
HCPL-2530	✓			16	2.0	2.0	7	50	✓					✓	B	1-63
HCPL-0530		✓		16	2.0	2.0	7	50	✓					✓		
HCPL-2531	✓			16	1.0	1.0	19	50	✓					✓	B	
HCPL-0531		✓		16	1.0	1.0	19	50	✓					✓		
HCPL-4534	✓			16	1.0	1.0	19	50			✓			✓	B	
HCPL-0534		✓		16	1.0	1.0	19	50			✓			✓		
HCPL-0560*		✓		16	1.0	1.0	19	50	✓					✓	B	1-74
HCPL-0561*		✓		16	1.0	1.0	19	50	✓					✓		

Bold Type = New Product

*coming soon

A = Option 060
B = Option 020

Single Channel 100 KBd High Gain Transistor Output Optocoupler (6N138/9 Type)

Part Number	Package: 300 mil DIP	Package: SO8	Package: 400 mil DIP	I_F-min: 40 µA	I_F-min: 0.5 mA	I_F-min: 1.6 mA	CTR: Min. %	VDE V_{IORM}: 630 Vp	VDE V_{IORM}: 1414 Vp	Insulation UL = 1 min.: 2500 V	Insulation UL = 1 min.: 5000 V	Page No.
6N138	✓					✓	300			✓	B	1-77
HCPL-0700		✓				✓	300			✓		
HCNW138			✓			✓	300		✓		✓	
6N139	✓				✓		400			✓	B	
HCPL-0701		✓			✓		400			✓		
HCNW139			✓		✓		400		✓		✓	
HCPL-4701	✓			✓			800	A		✓	B	1-92
HCPL-070A		✓		✓			800			✓		

Dual Channel 100 KBd High Gain Transistor Output Optocoupler (6N138/9 Type)

Part Number	Package: 300 mil DIP	Package: SO8	Package: 400 mil DIP	I_F-min: 40 µA	I_F-min: 0.5 mA	I_F-min: 1.6 mA	CTR: Min. %	VDE V_{IORM}: 630 Vp	VDE V_{IORM}: 1414 Vp	Insulation UL = 1 min.: 2500 V	Insulation UL = 1 min.: 5000 V	Page No.
HCPL-2730	✓					✓	300			✓	B	1-108
HCPL-0730		✓				✓	300			✓		
HCPL-2731	✓				✓		400			✓	B	
HCPL-0731		✓			✓		400			✓		
HCPL-4731	✓			✓			800			✓	B	1-92
HCPL-073A		✓		✓			800			✓		

Single Channel 5 MBd Logic Gate Optocoupler (HCPL-2200 Type)

Part Number	Package: 300 mil DIP	Package: SO8	Package: 400 mil DIP	I_F-min: 1.6 mA	I_F-min: 1.8 mA	CMR-V/µs (V_{CM}): 1000 (50 V)	CMR-V/µs (V_{CM}): 2500 (400 V)	CMR-V/µs (V_{CM}): 5000 (1 kV)	VDE V_{IORM}: 630 Vp	VDE V_{IORM}: 1414 Vp	Insulation UL = 1 min.: 2500 V	Insulation UL = 1 min.: 5000 V	Page No.
HCPL-2200	✓			✓		✓					✓		1-120
HCPL-2219	✓			✓			✓		A		✓		
HCPL-2201[3]	✓			✓		✓					✓		1-131
HCPL-2202[3,4]	✓			✓		✓					✓		
HCPL-0201[3]		✓		✓		✓					✓		
HCNW2201[3]			✓	✓		✓				✓		✓	
HCPL-2211[3]	✓			✓				✓	A		✓		
HCPL-2212[3,4]	✓			✓				✓	A		✓		
HCPL-0211[3]		✓		✓				✓			✓		
HCNW2211[3]			✓	✓				✓		✓		✓	

Notes:

3. Pin 6 not connected.
4. Pins 6 and 7 reversed.

Bold Type = New Product

A = Option 060
B = Option 020

Dual Channel 5 MBd Logic Gate Optocoupler (HCPL-2200 Type)

Part Number	Package: 300 mil DIP	Package: SO8	Package: 400 mil DIP	I_F-min: 1.6 mA	I_F-min: 1.8 mA	CMR-V/µs (V_{CM}): 1000 (50 V)	CMR-V/µs (V_{CM}): 2500 (400 V)	CMR-V/µs (V_{CM}): 5000 (1 kV)	VDE V_{IORM}: 630 Vp	VDE V_{IORM}: 1414 Vp	Insulation UL = 1 min.: 2500 V	Insulation UL = 1 min.: 5000 V	Page No.
HCPL-2231	✓				✓	✓					✓		1-131
HCPL-2232	✓				✓			✓			✓		

Single Channel 10 MBd Logic Gate Optocoupler (6N137 Type)

Part Number	Package: 300 mil DIP	Package: SO8	Package: 400 mil DIP	I_F-min: 2 mA	I_F-min: 5mA	CMR-V/µs (V_{CM}): 100 (50 V)	CMR-V/µs (V_{CM}): 5000 (50 V)	CMR-V/µs (V_{CM}): 10000 (1 kV)	VDE V_{IORM}: 630 Vp	VDE V_{IORM}: 1414 Vp	Insulation UL = 1 min.: 2500 V	Insulation UL = 1 min.: 5000 V	Page No.
6N137	✓				✓	✓					✓	B	1-146
HCPL-0600		✓			✓	✓					✓		
HCNW137			✓		✓	✓				✓		✓	
HCPL-2601	✓				✓		✓				✓	B	
HCPL-0601		✓			✓		✓				✓		
HCNW2601			✓		✓		✓			✓		✓	
HCPL-2611	✓				✓			✓	A		✓	B	
HCPL-0611		✓			✓			✓			✓		
HCNW2611			✓		✓			✓		✓		✓	
HCPL-261A	✓			✓			✓		A		✓	B	1-166
HCPL-061A		✓		✓			✓				✓		
HCPL-261N	✓			✓				✓	A		✓	B	
HCPL-061N		✓		✓				✓			✓		

Dual Channel 10 MBd Logic Gate Optocoupler (6N137 Type)

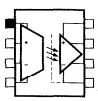
Part Number	Package: 300 mil DIP	Package: SO8	Package: 400 mil DIP	I_F-min: 2 mA	I_F-min: 5mA	CMR-V/µs (V_{CM}): 100 (50 V)	CMR-V/µs (V_{CM}): 5000 (50 V)	CMR-V/µs (V_{CM}): 10000 (1 kV)	VDE V_{IORM}: 630 Vp	VDE V_{IORM}: 1414 Vp	Insulation UL = 1 min.: 2500 V	Insulation UL = 1 min.: 5000 V	Page No.
HCPL-2630	✓				✓	✓					✓	B	1-146
HCPL-0630		✓			✓	✓					✓		
HCPL-2631	✓				✓		✓				✓	B	
HCPL-0631		✓			✓		✓				✓		
HCPL-4661	✓				✓			✓			✓	B	
HCPL-0661		✓			✓			✓			✓		
HCPL-263A	✓			✓			✓				✓	B	1-166
HCPL-063A		✓		✓			✓				✓		
HCPL-263N	✓			✓				✓			✓	B	
HCPL-063N		✓		✓				✓			✓		

Bold Type = New Product

A = Option 060
B = Option 020

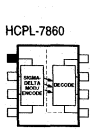
Integrated Gate Drive Optocouplers

Part Number	I_f (on) mA	Iout A (min.)	Prop Delay t_{PHL} µs (max.)	Prop Delay t_{PLH} µs (max.)	PWD µs (max.)	V_{CC} V (max.)	CMR-V/µs	Page No.
HCPL-3000	8	0.6	2.0	5.0	–	13	1.5 kV/µs @ V_{CM} = 600 V	1-329
HCPL-3100	12	0.1		2.0	–	24	1.5 kV/µs @ V_{CM} = 600 V	1-338
HCPL-3101	16	0.1		0.5	–	24	1.5 kV/µs @ V_{CM} = 600 V	
HCPL-3120	7	2	0.5	0.5	0.3	30	15 kV/µs @ V_{CM} = 1500 V	1-182
HCPL-3150	7	0.5	0.5	0.5	0.3	30	15 kV/µs @ V_{CM} = 1500 V	1-197
HCPL-3160	2.0 A with Integrated Over-Current Protection and Fault Feedback							1-212



Miniature Isolation Amplifiers

Part Number	Gain Tolerance (max. %)	Non-Linearity (max. %)	Prop Delay µs (max.)	CMR-V/µs (V_{CM}) 10000 (1000)	CMR-V/µs (V_{CM}) 20000 (1000)	VDE V_{IORM} 600 V	Page No.
HCPL-7800	5	0.35	9.9	✓		✓	1-216
HCPL-7800A/B	1	0.35	9.9	✓		✓	
HCPL-7820	3	0.15	4.1		✓	✓	1-233
HCPL-7825	5	0.15	4.1		✓	✓	
HCPL-7840	5	0.2	9.9	✓			1-248

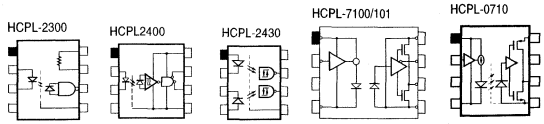


Isolated Analog-to-Digital (A/D) Converters

Part Number	Gain Tolerance (max. %)	Integral Non-Linearity (max. %)	SNR (dB)	Effective Radiation (bits)	Signal Delay (µs)	Signal Bandwidth (kHz)	CMR V/µs (V_{CM}) 15000 (1000)	Page No.
HCPL-7860 **HCPL-7870** **HCPL-0870**	1%	0.15	83	12	19	22	✓	1-260

Bold Type = New Product

A = Option 060
B = Option 020

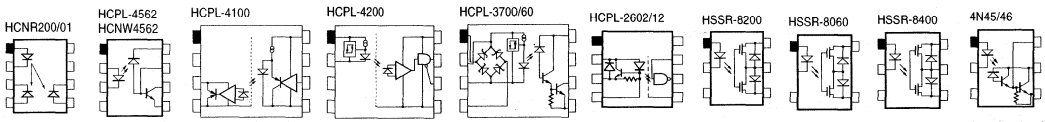


Other High Speed Logic Gate Optocouplers

Part Number	I_f - mA max.	I_f - mA min.	Prop Delay max.	CMR V/µs/V_{CM}	VDE V_{IORM} V_{PEAK}	Insulation UL = 1-min. Vac	Page No.
HCPL-2300	0.5		200 ns	1000 V/µs@V_{CM} = 50 V	630[1]	2500	1-288
HCPL-2400	4		60 ns	1000 V/µs@V_{CM} = 300 V	630[1]	2500	1-300
HCPL-2430	4		60 ns	1000 V/µs@V_{CM} = 50 V		2500	
HCPL-7100	0.001	[2]	70 ns	2000 V/µs@V_{CM} = 200 V	848	3750	1-402
HCPL-7101	0.001	[2]	40 ns	2000 V/µs@V_{CM} = 200 V	848	3750	
HCPL-0710	0.001	[2]	40 ns	10,000 V/µs@V_{CM} = 1000 V	N/A	2500	1-416

Notes:

1. Available with Option 060.
2. Value given is max. input current for a CMOS buffer which drives the LED. Requires isolated input power supply.



Other Application Specific Optocouplers

Description	Part Number	Page No.
High Linearity Analog	**HCNR200/01**	1-418
Wide Analog/Video	HCPL-4562 HCNW-4562	1-385
20 mA Current Loop Transmitter	HCPL-4100	1-361
20 mA Current Loop Receiver	HCPL-4200	1-373
AC/DC to Logic Interface	HCPL-3700/60	1-348
Line Receiver	HCPL-2602/12	1-314
200 V, 160 Ω Solid State Relays	HSSR-8200	1-454
60 V, 0.7 Ω Solid State Relay	HSSR-8060	1-441
400 V, 10 Ω Solid State Relay	HSSR-8400	1-465
High CTR-6 pin	4N45/46	1-434

Optocoupler & Solid State Relay Options

Option Number	Description	Eligible Optocouplers & Solid State Relays	Page No.
001	Commercial Burn-in	All 7.6 mm (300 mil) wide plastic products. Contact factory for availability.	
002	100% Screening Program	All 7.6 mm (300 mil) wide plastic products. Contact factory for availability.	
020	5000 Vac/1 min. UL Rating	See Note 1 for list of part numbers.	1-478
060	630 V, VDE	See Note 2 for list of part numbers.	1-480
300	Gull Wing Surface Mount	Available on most plastic products. Contact factory for list of part numbers.	1-482
500	Tape and Reel Packaging	Available on all plastic DIP and surface mount products. Contact factory for list of part numbers.	1-485

Notes:
1. Option 020 is available for 6N135, 6N136, 6N137, 6N138, 6N139, HCPL-2502, HCPL-2601, HCPL-2611, HCPL-4502, HCPL-4503, and HCPL-4562.
2. Option 060 is available for HCPL-4701, HCPL-2219, HCPL-2211, HCPL-2212, HCPL-4503, HCPL-4504, HCPL-4506, HCPL-2611, HCPL-261A, HCPL-261N, HCPL-2400, HCPL-3120, HCPL-2300, HCPL-3150.

Hermetic and Hi-Rel Optocouplers Selection Guide	Page No.
	1-493

HEWLETT® PACKARD

Single Channel, High Speed Optocouplers

Technical Data

6N135/6
HCNW135/6
HCNW4502/3
HCPL-0452/3
HCPL-0500/1
HCPL-4502/3

Features

- **15 kV/μs Minimum Common Mode Transient Immunity at V_{CM} = 1500 V (4503/0453)**
- **High Speed: 1 Mb/s**
- **TTL Compatible**
- **Available in 8-Pin DIP, SO-8, Widebody Packages**
- **Open Collector Output**
- **Guaranteed Performance from Temperature: 0°C to 70°C**
- **Safety Approval**
  UL Recognized – 2500 V rms for 1 minute (5000 V rms for 1 minute for HCNW and Option 020 devices) per UL1577
  CSA Approved
  VDE 0884 Approved
  $-V_{IORM}$ = 630 V peak for HCPL-4503#060
  $-V_{IORM}$ = 1414 V peak for HCNW devices
  BSI Certified
  (HCNW devices only)
- **Dual Channel Version Available (253X/4534/053X/0534)**
- **MIL-STD-1772 Version Available (55XX/65XX/4N55)**

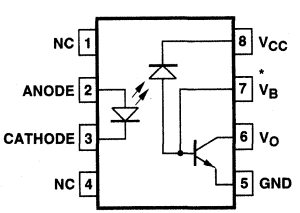
Applications

- **High Voltage Insulation**
- **Video Signal Isolation**
- **Power Transistor Isolation in Motor Drives**
- **Line Receivers**
- **Feedback Element in Switched Mode Power Supplies**
- **High Speed Logic Ground Isolation – TTL/TTL, TTL/CMOS, TTL/LSTTL**
- **Replaces Pulse Transformers**
- **Replaces Slow Phototransistor Isolators**
- **Analog Signal Ground Isolation**

Description

These diode-transistor optocouplers use an insulating layer between a LED and an integrated photodetector to provide electrical insulation between input and output. Separate connections for the photodiode bias and output-transistor collector increase the speed up to a hundred times that of a conventional phototransistor coupler by reducing the base-collector capacitance.

Functional Diagram



* NOTE: FOR 4502/3, 0452/3, PIN 7 IS NOT CONNECTED.

TRUTH TABLE (POSITIVE LOGIC)

LED	V_O
ON	LOW
OFF	HIGH

A 0.1 μF bypass capacitor must be connected between pins 5 and 8.

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

These single channel optocouplers are available in 8-Pin DIP, SO-8 and Widebody package configurations.

The 6N135, HCPL-0500, and HCNW135 are for use in TTL/CMOS, TTL/LSTTL or wide bandwidth analog applications. Current transfer ratio (CTR) for these devices is 7% minimum at I_F = 16 mA.

The 6N136, HCPL-0501, and HCNW136 are designed for high speed TTL/TTL applications. A standard 16 mA TTL sink current through the input LED will provide enough output current for 1 TTL load and a 5.6 kΩ pull-up resistor. CTR for these devices is 19% minimum at I_F = 16 mA.

The HCPL-4502, HCPL-0452, and HCNW4502 provide the electrical and switching performance of the 6N136, HCPL-0501, and HCNW136 with increased ESD protection.

The HCPL-4503, HCPL-0453, and HCNW4503 are similar to the HCPL-4502, HCPL-0452, and HCNW4502 optocouplers but have increased common mode transient immunity of 15 kV/μs minimum at V_{CM} = 1500 V guaranteed.

Selection Guide

Minimum CMR			8-Pin DIP (300 Mil)		Small-Outline SO-8		Widebody (400 Mil)	Hermetic
dV/dt (V/μs)	V_{CM} (V)	Current Transfer Ratio (%)	Single Channel Package	Dual Channel Package*	Single Channel Package	Dual Channel Package*	Single Channel Package	Single and Dual Channel Packages*
1,000	10	7	6N135	HCPL-2530	HCPL-0500	HCPL-0530	HCNW135	
		19	6N136 HCPL-4502†	HCPL-2531	HCPL-0501 HCPL-0452†	HCPL-0531	HCNW136 HCNW4502†	
15,000	1500	19	HCPL-4503†	HCPL-4534	HCPL-0453†	HCPL-0534	HCNW4503†	
1,000	10	9						HCPL-55XX HCPL-65XX 4N55

*Technical data for these products are on separate HP publications.
†Pin 7, transistor base, is not connected.

Ordering Information

Specify Part Number followed by Option Number (if desired).

Example:

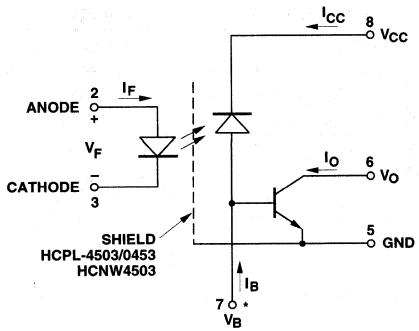
HCPL-4503#XXX

- 020 = UL 5000 V rms/1 Minute Option*
- 060 = VDE 0884 V_{IORM} = 630 V peak Option**
- 300 = Gull Wing Surface Mount Option†
- 500 = Tape and Reel Packaging Option

Option data sheets available. Contact your Hewlett-Packard sales representative or authorized distributor for information.

*For 6N135/6 and HCPL-4502/3 only.
**For HCPL-4503 only. Combination of Option 020 and Option 060 is not available.
†Gull wing surface mount option applies to through hole parts only.

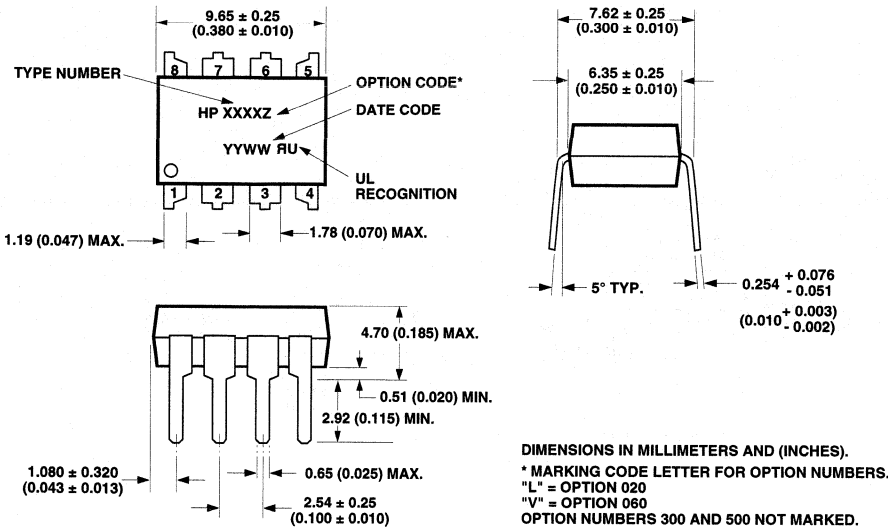
Schematic



* NOTE: FOR HCPL-4502/-3, HCPL-0452/3, HCNW4502/3, PIN 7 IS NOT CONNECTED.

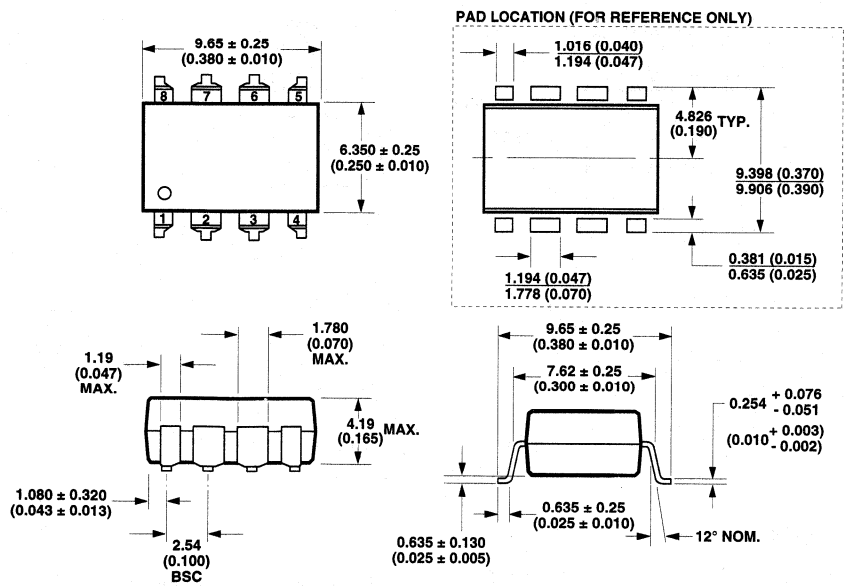
Package Outline Drawings

8-Pin DIP Package (6N135/6, HCPL-4502/3)



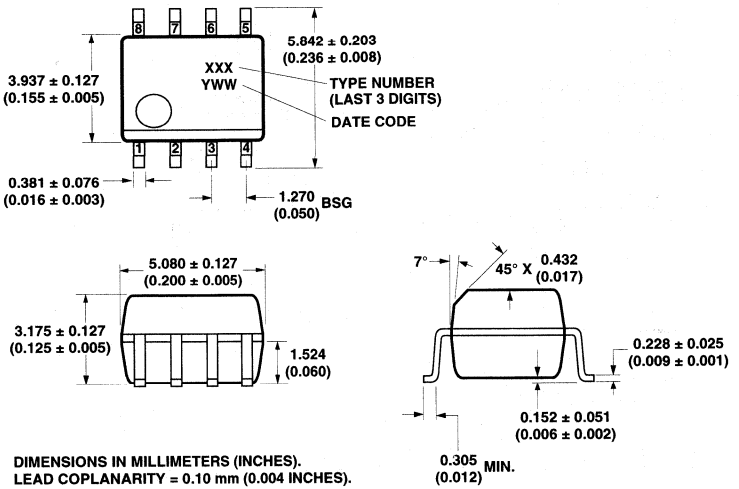
DIMENSIONS IN MILLIMETERS AND (INCHES).
* MARKING CODE LETTER FOR OPTION NUMBERS.
"L" = OPTION 020
"V" = OPTION 060
OPTION NUMBERS 300 AND 500 NOT MARKED.

8-Pin DIP Package with Gull Wing Surface Mount Option 300 (6N135/6, HCPL-4502/3)

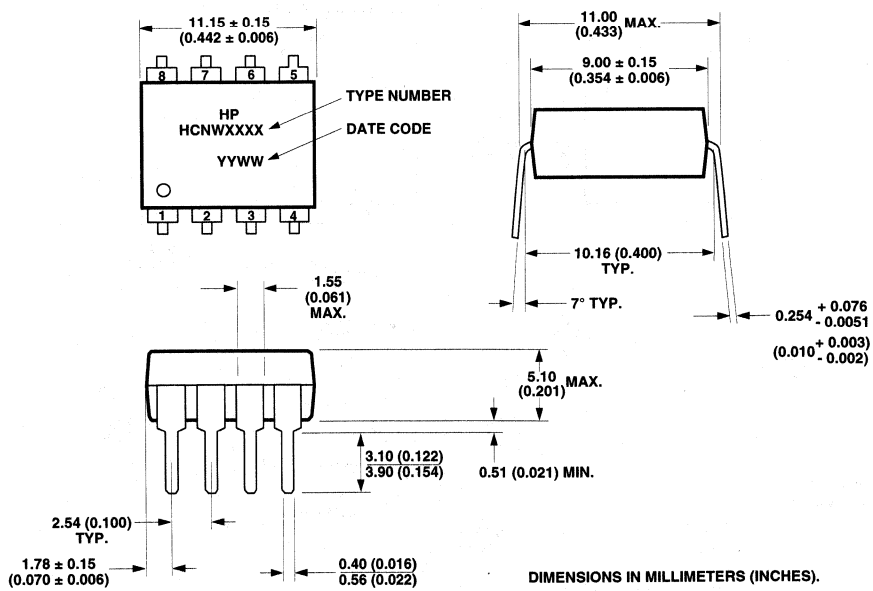


DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES).

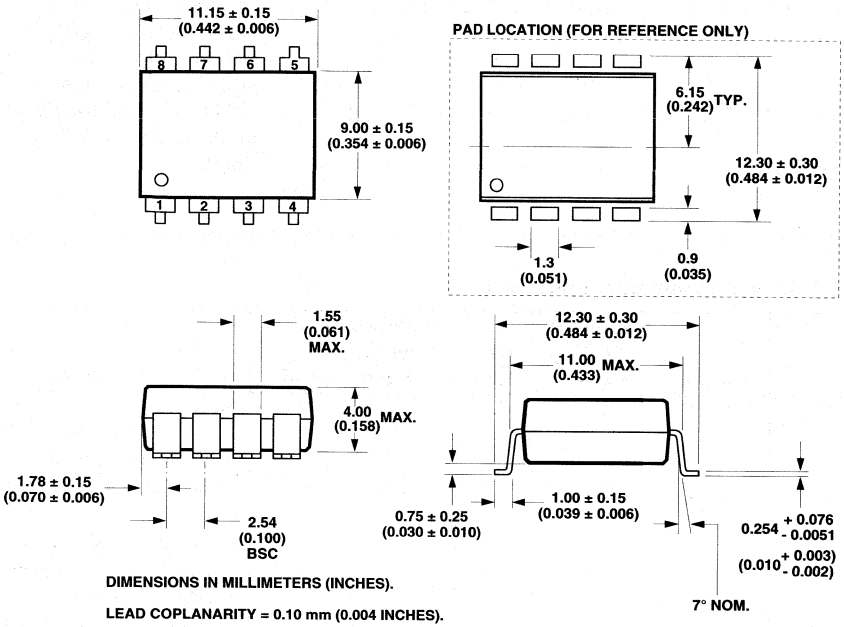
Small Outline SO-8 Package (HCPL-0500/1, HCPL-0452/3)



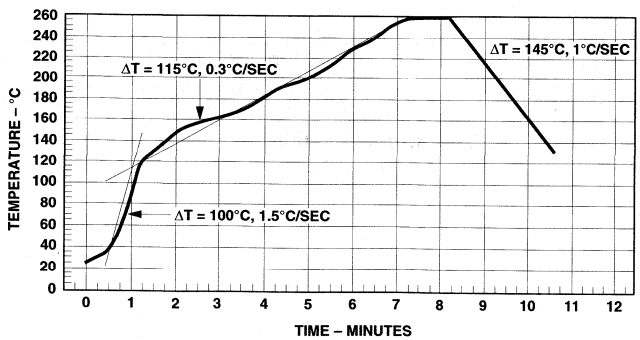
8-Pin Widebody DIP Package (HCNW135/6, HCNW4502/3)



8-Pin Widebody DIP Package with Gull Wing Surface Mount Option 300 (HCNW135/6, HCNW4502/3)



Solder Reflow Temperature Profile (HCPL-0500/1, HCPL-0452/3, and Gull Wing Surface Mount Option Parts)



Note: Use of Non-Chlorine Activated Fluxes is Recommended.

Regulatory Information

The devices contained in this data sheet have been approved by the following organizations:

UL

Recognized under UL 1577, Component Recognition Program, File E55361.

CSA

Approved under CSA Component Acceptance Notice #5, File CA 88324.

VDE

Approved according to VDE 0884/06.92 (HCNW and Option 060 devices only).

BSI

Certification according to BS451:1994, (BS EN60065:1994); BS EN60950:1992 (BS7002:1992) and EN41003:1993 for Class II applications (HCNW devices only).

Insulation and Safety Related Specifications

Parameter	Symbol	8-Pin DIP (300 Mil) Value	SO-8 Value	Widebody (400 Mil) Value	Units	Conditions
Minimum External Air Gap (External Clearance)	L(101)	7.1	4.9	9.6	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L(102)	7.4	4.8	10.0	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	0.08	1.0	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity.
Minimum Internal Tracking (Internal Creepage)		NA	NA	4.0	mm	Measured from input terminals to output terminals, along internal cavity.
Tracking Resistance (Comparative Tracking Index)	CTI	200	200	200	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa	IIIa	IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Option 300 - surface mount classification is Class A in accordance with CECC 00802.

VDE 0884 Insulation Related Characteristics (HCPL-4503 OPTION 060 ONLY)

Description	Symbol	Characteristic	Units
Installation classification per DIN VDE 0110/1.89, Table 1			
for rated mains voltage ≤ 300 V rms		I-IV	
for rated mains voltage ≤ 450 V rms		I-III	
Climatic Classification		55/100/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	630	V peak
Input to Output Test Voltage, Method b* V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial Discharge < 5 pC	V_{PR}	1181	V peak
Input to Output Test Voltage, Method a* V_{IORM} x 1.5 = V_{PR}, Type and sample test, t_m = 60 sec, Partial Discharge < 5 pC	V_{PR}	945	V peak
Highest Allowable Overvoltage* (Transient Overvoltage, t_{ini} = 10 sec)	V_{IOTM}	6000	V peak
Safety Limiting Values (Maximum values allowed in the event of a failure, also see Figure 9, Thermal Derating curve.)			
Case Temperature	T_S	175	°C
Input Current	$I_{S,INPUT}$	230	mA
Output Power	$P_{S,OUTPUT}$	600	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	≥ 10^9	Ω

VDE 0884 Insulation Related Characteristics (HCNW135/6, HCNW4502/3 ONLY)

Description	Symbol	Characteristic	Units
Installation classification per DIN VDE 0110/1.89, Table 1			
for rated mains voltage ≤ 600 V rms		I-IV	
for rated mains voltage ≤ 1000 V rms		I-III	
Climatic Classification		55/85/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	1414	V peak
Input to Output Test Voltage, Method b* V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial Discharge < 5 pC	V_{PR}	2652	V peak
Input to Output Test Voltage, Method a* V_{IORM} x 1.5 = V_{PR}, Type and sample test, t_m = 60 sec, Partial Discharge < 5 pC	V_{PR}	2121	V peak
Highest Allowable Overvoltage* (Transient Overvoltage, t_{ini} = 10 sec)	V_{IOTM}	8000	V peak
Safety Limiting Values (Maximum values allowed in the event of a failure, also see Figure 9, Thermal Derating curve.)			
Case Temperature	T_S	150	°C
Input Current	$I_{S,INPUT}$	400	mA
Output Power	$P_{S,OUTPUT}$	700	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	≥ 10^9	Ω

*Refer to the front of the optocoupler section of the current catalog, under Product Safety Regulations section (VDE 0884), for a detailed description.

Note: Isolation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuits in application.

Absolute Maximum Ratings

Parameter	Symbol	Device	Min.	Max.	Units	Note
Storage Temperature*	T_S		-55	125	°C	
Operating Temperature*	T_A	8-Pin DIP SO-8	-55	100	°C	
		Widebody	-55	85		
Average Forward Input Current*	$I_{F(AVG)}$			25	mA	1
Peak Forward Input Current* (50% duty cycle, 1 ms pulse width)	$I_{F(PEAK)}$	8-Pin DIP SO-8		50	mA	2
(50% duty cycle, 1 ms pulse width)		Widebody		40		
Peak Transient Input Current* (≤ 1 µs pulse width, 300 pps)	$I_{F(TRANS)}$	8-Pin DIP SO-8		1	A	
		Widebody		0.1		
Reverse LED Input Voltage* (Pin 3-2)	V_R	8-Pin DIP SO-8		5	V	
		Widebody		3		
Input Power Dissipation*	P_{IN}	8-Pin DIP SO-8		45	mW	3
		Widebody		40		
Average Output Current* (Pin 6)	$I_{O(AVG)}$			8	mA	
Peak Output Current*	$I_{O(PEAK)}$			16	mA	
Emitter-Base Reverse Voltage* (Pin 5-7, except 4502/3, 0452/3)	V_{EBR}			5	V	
Supply Voltage (Pin 8-5)	V_{CC}		-0.5	30	V	
Output Voltage (Pin 6-5)	V_O		-0.5	20	V	
Supply Voltage* (Pin 8-5)	V_{CC}		-0.5	15	V	
Output Voltage* (Pin 6-5)	V_O		-0.5	15	V	
Base Current* (Pin 7, except 4502/3, 0452/3)	I_B			5	mA	
Output Power Dissipation*	P_O			100	mW	4
Lead Solder Temperature* (Through-Hole Parts Only) 1.6 mm below seating plane, 10 seconds	T_{LS}	8-Pin DIP		260	°C	
up to seating plane, 10 seconds		Widebody		260	°C	
Reflow Temperature Profile	T_{RP}	SO-8 and Option 300	See **Package Outline Drawings** section			

*Data has been registered with JEDEC for the 6N135/6N136.

Electrical Specifications (DC)

Over recommended temperature (T_A = 0°C to 70°C) unless otherwise specified. See note 13.

Parameter	Symbol	Device	Min.	Typ.**	Max.	Units	Test Conditions			Fig.	Note
Current Transfer Ratio	CTR*	6N135	7	18	50	%	T_A = 25°C	V_O = 0.4 V	I_F = 16 mA, V_{CC} = 4.5 V	1, 2, 4	5, 11
		HCPL-0500 HCNW135	5	19				V_O = 0.5 V			
		6N136 HCPL-4502/3 HCPL-0501	19	24	50		T_A = 25°C	V_O = 0.4 V			
		HCPL-0452/3 HCNW136 HCNW4502/3	15	25				V_O = 0.5 V			
Logic Low Output Voltage	V_{OL}	6N135		0.1	0.4	V	T_A = 25°C	I_O = 1.1 mA	I_F = 16 mA, V_{CC} = 4.5 V		
		HCPL-0500 HCNW135		0.1	0.5			I_O = 0.8 mA			
		6N136		0.1	0.4		T_A = 25°C	I_O = 3.0 mA			
		HCPL-4502/3 HCPL-0501 HCPL-0452/3 HCNW136 HCNW4502/3		0.1	0.5			I_O = 2.4 mA			
Logic High Output Current	I_{OH}*			0.003	0.5	µA	T_A = 25°C	V_O = V_{CC} = 5.5 V	I_F = 0 mA	7	
				0.01	1		T_A = 25°C	V_O = V_{CC} = 15 V			
					50						
Logic Low Supply Current	I_{CCL}			50	200	µA	I_F = 16 mA, V_O = Open, V_{CC} = 15 V				13
Logic High Supply Current	I_{CCH}*			0.02	1	µA	T_A = 25°C	I_F = 0 mA, V_O = Open, V_{CC} = 15 V			13
					2						
Input Forward Voltage	V_F*	8-Pin DIP		1.5	1.7	V	T_A = 25°C	I_F = 16 mA		3	
		SO-8			1.8						
		Widebody	1.45	1.68	1.85		T_A = 25°C	I_F = 16 mA			
			1.35		1.95						
Input Reverse Breakdown Voltage	BV_R*	8-Pin DIP SO-8	5			V	I_R = 10 µA				
		Widebody	3				I_R = 100 µA				
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$	8-Pin DIP SO-8		-1.6		mV/°C	I_F = 16 mA				
		Widebody		-1.9							
Input Capacitance	C_{IN}	8-Pin DIP SO-8		60		pF	f = 1 MHz, V_F = 0 V				
		Widebody		90							
Transistor DC Current Gain	h_{FE}	8-Pin DIP		150			V_O = 5 V, I_O = 3 mA				
		SO-8		130			V_O = 0.4 V, I_B = 20 µA				
		Widebody		180			V_O = 5 V, I_O = 3 mA				
				160			V_O = 0.4 V, I_B = 20 µA				

*For JEDEC registered parts.
**All typicals at T_A = 25°C.

Switching Specifications (AC)

Over recommended temperature (T_A = 0°C to 70°C), V_{CC} = 5 V, I_F = 16 mA unless otherwise specified.

Parameter	Sym.	Device	Min.	Typ.**	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to Logic Low at Output	t_{PHL}*	6N135		0.2	1.5	µs	T_A = 25°C, R_L = 4.1 kΩ	5, 6, 11	8, 9
		IICPL-0500			2.0				
		HCNW135							
		6N136		0.2	0.8		T_A = 25°C, R_L = 1.9 kΩ		
		HCPL-4502/3							
		HCPL-0501							
		HCPL-0452/3			1.0				
		HCNW136							
		HCNW4502/3							
Propagation Delay Time to Logic High at Output	t_{PLH}*	6N135		1.3	1.5	µs	T_A = 25°C, R_L = 4.1 kΩ	5, 6, 11	8, 9
		HCPL-0500			2.0				
		HCNW135							
		6N136		0.6	0.8		T_A = 25°C, R_L = 1.9 kΩ		
		HCPL-4502/3							
		HCPL-0501							
		HCPL-0452/3			1.0				
		HCNW136							
		HCNW4502/3							
Common Mode Transient Immunity at Logic High Level Output	$\|CM_H\|$	6N135		1		kV/µs	R_L = 4.1 kΩ, I_F = 0 mA, T_A = 25°C, V_{CM} = 10 V_{p-p}, C_L = 15 pF	12	7, 8, 9
		HCPL-0500							
		HCNW135							
		6N136		1			R_L = 1.9 kΩ		
		HCPL-4502							
		HCPL-0501							
		HCPL-0452							
		HCNW4502							
		HCPL-4503	15	30			R_L = 1.9 kΩ, I_F = 0 mA, T_A = 25°C, V_{CM} = 1500 V_{p-p}, C_L = 15 pF		
		HCPL-0453							
		HCNW4503							
Common Mode Transient Immunity at Logic Low Level Output	$\|CM_L\|$	6N135		1		kV/µs	R_L = 4.1 kΩ, I_F = 16 mA, T_A = 25°C, V_{CM} = 10 V_{p-p}, C_L = 15 pF	12	7, 8, 9
		HCPL-0500							
		HCNW135							
		6N136		1			R_L = 1.9 kΩ		
		HCPL-4502							
		HCPL-0501							
		HCPL-0452							
		HCNW4502							
		HCPL-4503	15	30			R_L = 1.9 kΩ, I_F = 16 mA, T_A = 25°C, V_{CM} = 1500 V_{p-p}, C_L = 15 pF		
		HCPL-0453							
		HCNW4503							
Bandwidth	BW	6N135/6		9		MHz	See Test Circuit	8, 10	10
		HCPL-0500/1							
		HCNW135/6		11					

*For JEDEC registered parts.
**All typicals at T_A = 25°C.

Package Characteristics

Over recommended temperature (T_A = 0°C to 70°C) unless otherwise specified.

Parameter	Sym.	Device	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage**	V_{ISO}	8-Pin DIP SO-8	2500			V rms	RH < 50%, t = 1 min., T_A = 25°C		6, 14
		Widebody	5000						6, 15
		8-Pin DIP (Option 020)	5000						6, 12, 15
	I_{I-O}	8-Pin DIP			1	μA	45% RH, t = 5 s, V_{I-O} = 3 kVdc, T_A = 25°C		6, 16
Input-Output Resistance	R_{I-O}	8-Pin DIP SO-8		10^{12}		Ω	V_{I-O} = 500 Vdc		6
		Widebody	10^{12}	10^{13}			T_A = 25°C		
			10^{11}				T_A = 100°C		
Input-Output Capacitance	C_{I-O}	8-Pin DIP SO-8		0.6		pF	f = 1 MHz		6
		Widebody		0.5	0.6				

*All typicals at T_A = 25°C.

**The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the VDE 0884 Insulation Related Characteristics Table (if applicable), your equipment level safety specification or HP Application Note 1074 entitled "Optocoupler Input-Output Endurance Voltage," publication number 5963-2203E.

Notes:

1. Derate linearly above 70°C free-air temperature at a rate of 0.8 mA/°C (8-Pin DIP).
   Derate linearly above 85°C free-air temperature at a rate of 0.5 mA/°C (SO-8).
2. Derate linearly above 70°C free-air temperature at a rate of 1.6 mA/°C (8-Pin DIP).
   Derate linearly above 85°C free-air temperature at a rate of 1.0 mA/°C (SO-8).
3. Derate linearly above 70°C free-air temperature at a rate of 0.9 mW/°C (8-Pin DIP).
   Derate linearly above 85°C free-air temperature at a rate of 1.1 mW/°C (SO-8).
4. Derate linearly above 70°C free-air temperature at a rate of 2.0 mW/°C (8-Pin DIP).
   Derate linearly above 85°C free-air temperature at a rate of 2.3 mW/°C (SO-8).
5. CURRENT TRANSFER RATIO in percent is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100.
6. Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.
7. Common mode transient immunity in a Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic High state (i.e., V_O > 2.0 V). Common mode transient immunity in a Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., V_O < 0.8 V).
8. The 1.9 kΩ load represents 1 TTL unit load of 1.6 mA and the 5.6 kΩ pull-up resistor.
9. The 4.1 kΩ load represents 1 LSTTL unit load of 0.36 mA and 6.1 kΩ pull-up resistor.
10. The frequency at which the ac output voltage is 3 dB below its mid-frequency value.
11. The JEDEC registration for the 6N136 specifies a minimum CTR of 15%. HP guarantees a minimum CTR of 19%.
12. See Option 020 data sheet for more information.
13. Use of a 0.1 μf bypass capacitor connected between pins 5 and 8 is recommended.
14. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 3000 V rms for 1 second (leakage detection current limit, I_{I-O} ≤ 5 μA). This test is performed before the 100% Production test shown in the VDE 0884 Insulation Related Characteristics Table if applicable.
15. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 6000 V rms for 1 second (leakage detection current limit, I_{I-O} ≤ 5 μA). This test is performed before the 100% Production test shown in the VDE 0884 Insulation Related Characteristics Table if applicable.
16. This rating is equally validated by an equivalent ac proof test.

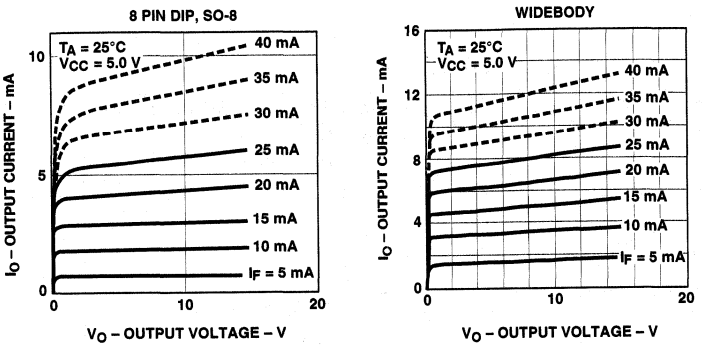


Figure 1. DC and Pulsed Transfer Characteristics.

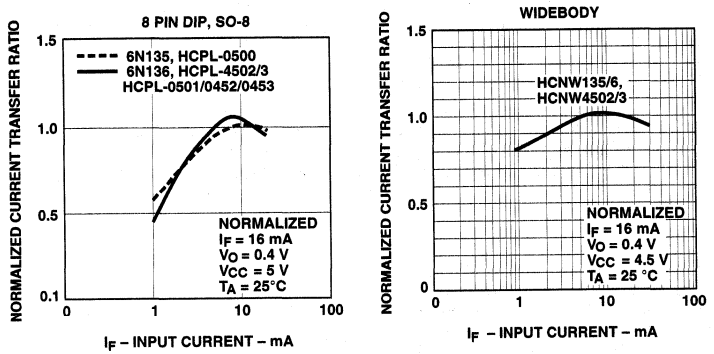


Figure 2. Current Transfer Ratio vs. Input Current.

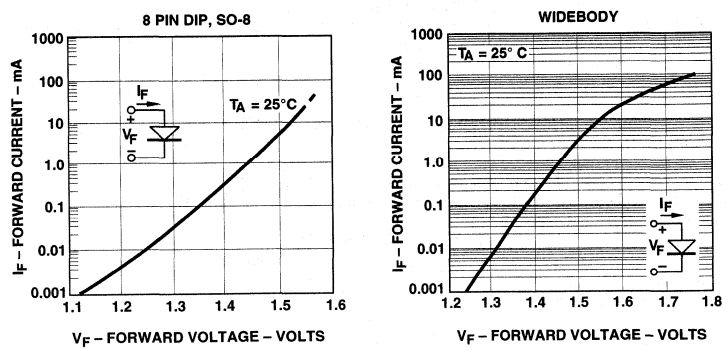


Figure 3. Input Current vs. Forward Voltage.

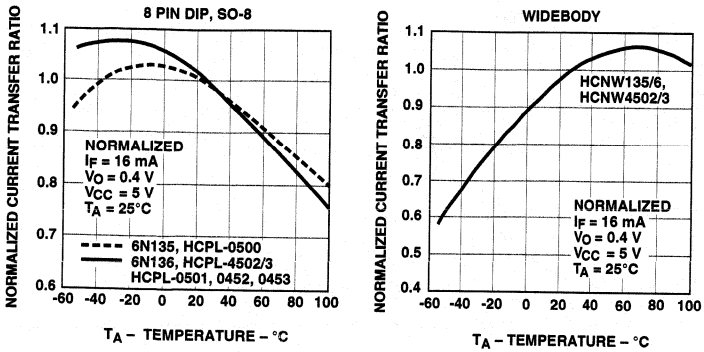


Figure 4. Current Transfer Ratio vs. Temperature.

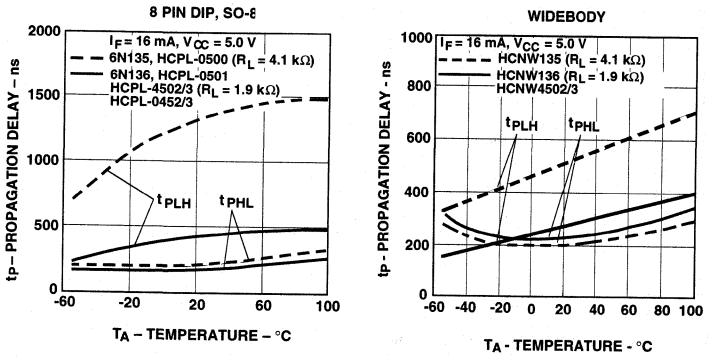


Figure 5. Propagation Delay vs. Temperature.

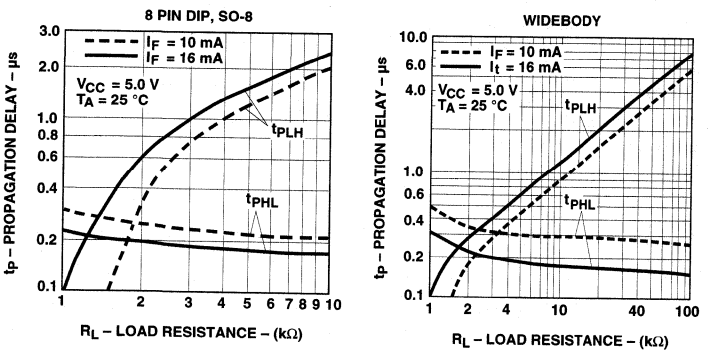


Figure 6. Propagation Delay Time vs. Load Resistance.

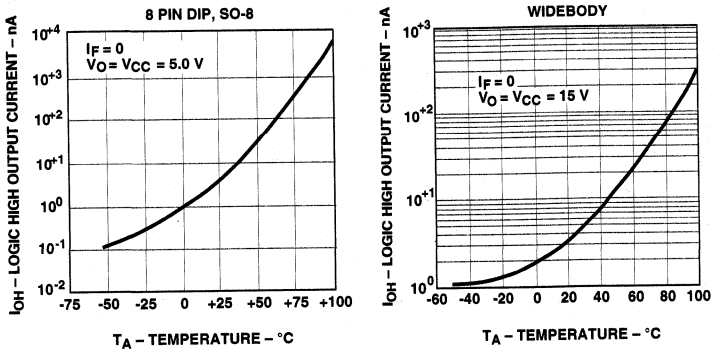


Figure 7. Logic High Output Current vs. Temperature.

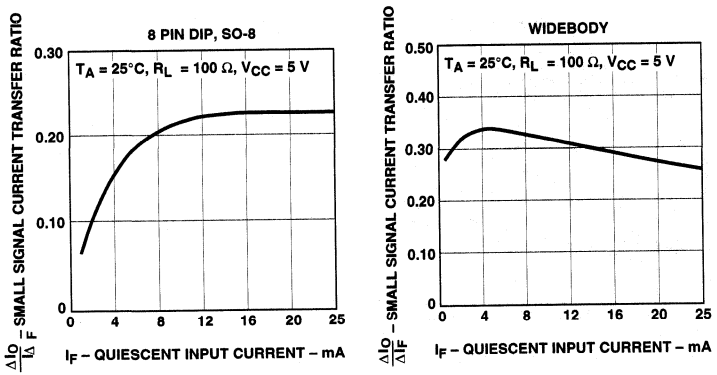


Figure 8. Small-Signal Current Transfer Ratio vs. Quiescent Input Current.

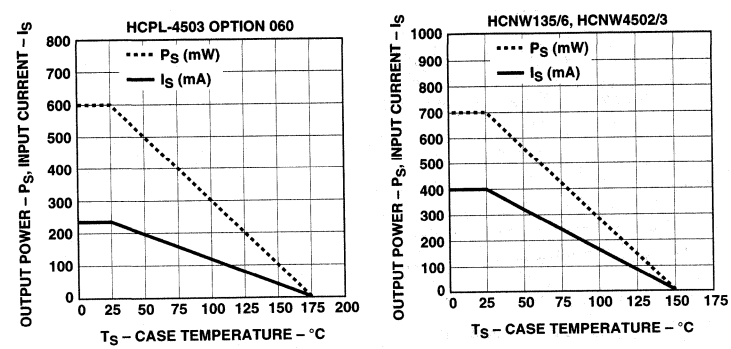
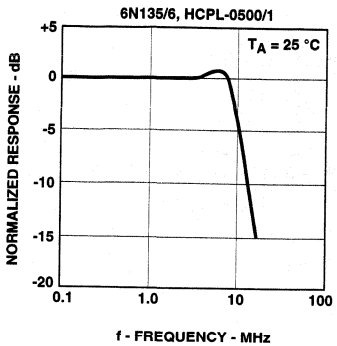
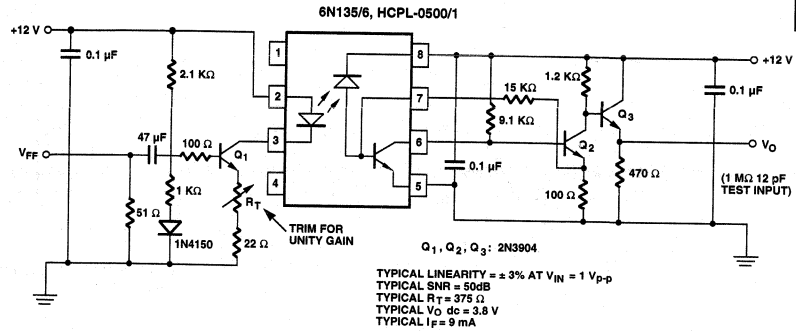
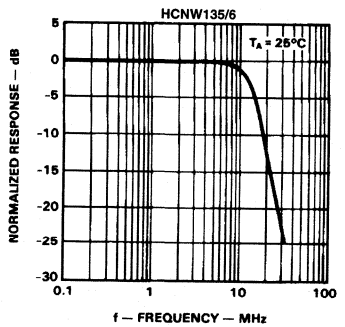


Figure 9. Thermal Derating Curve, Dependence of Safety Limiting Value with Case Temperature per VDE 0884.







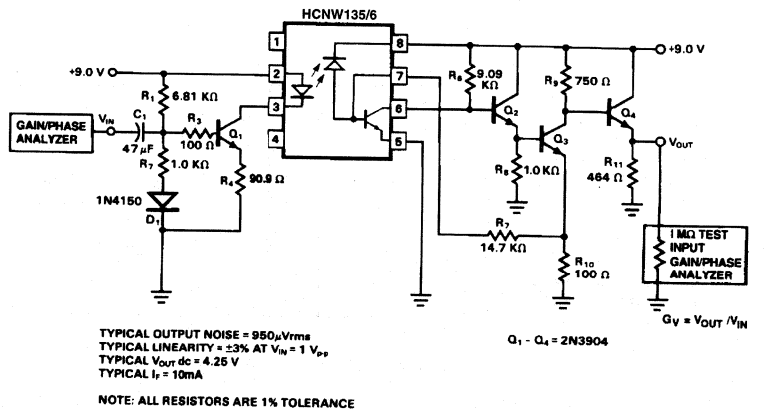


Figure 10. Frequency Response.

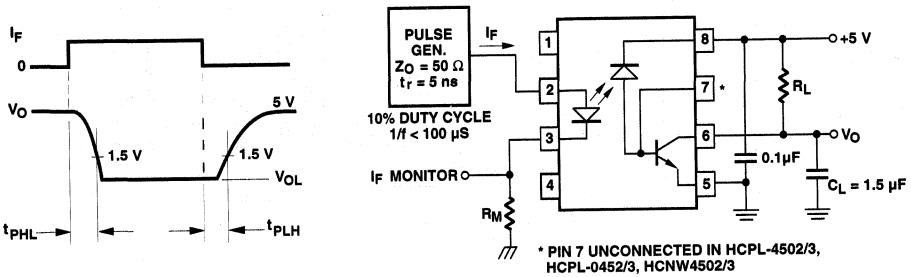


Figure 11. Switching Test Circuit.

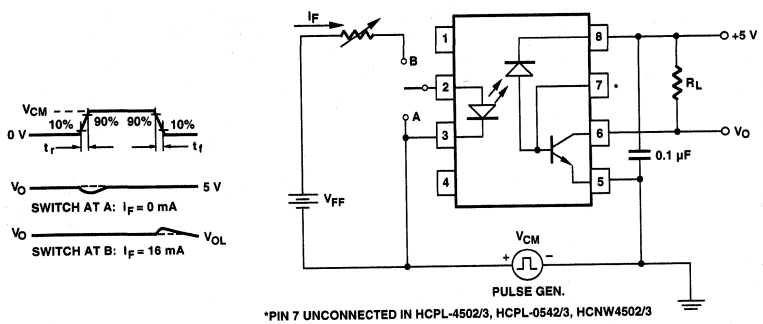


Figure 12. Test Circuit for Transient Immunity and Typical Waveforms.

High CMR, High Speed Optocouplers

Technical Data

HCPL-4504
HCPL-0454
HCNW4504

Features

- **Short Propagation Delays for TTL and IPM Applications**
- **15 kV/μs Minimum Common Mode Transient Immunity at V_{CM} = 1500 V for TTL/Load Drive**
- **High CTR at T_A = 25°C**
  >25% for HCPL-4504/0454
  >23% for HCNW4504
- **Electrical Specifications for Common IPM Applications**
- **TTL Compatible**
- **Guaranteed Performance from 0°C to 70°C**
- **Open Collector Output**
- **Safety Approval**
  UL Recognized - 2500 V rms for 1 minute (5000 V rms for 1 minute for HCPL-4504#020 and HCNW4504)per UL1577
  CSA Approved
  VDE 0884 Approved
  -V_{IORM} = 630 V peak for HCPL-4504#060
  -V_{IORM} = 1414 V peak for HCNW4504
  BSI Certified (HCNW4504)
- **Available in 8-Pin DIP, SO-8, Widebody Packages**

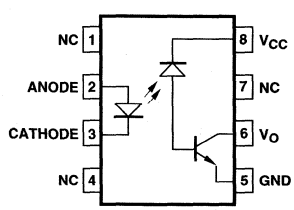
Applications

- **Inverter Circuits and Intelligent Power Module (IPM) interfacing -**
  High Common Mode Transient Immunity (> 10 kV/μs for an IPM load/drive) and (t_{PLH} - t_{PHL}) Specified (See Power Inverter Dead Time section)
- **Line Receivers -**
  Short Propagation Delays and Low Input-Output Capacitance
- **High Speed Logic Ground Isolation - TTL/TTL, TTL/CMOS, TTL/LSTTL**
- **Replaces Pulse Transformers -**
  Save Board Space and Weight
- **Analog Signal Ground Isolation -**
  Integrated Photodetector Provides Improved Linearity over Phototransistors

Description

These optocouplers are similar to HP's other high speed transistor optocouplers but with shorter propagation delays and higher CTR. The HCPL-4504/0454 and HCNW4504 also have a guaranteed propagation delay difference (t_{PLH} - t_{PHL}). These features make these optocouplers an excellent solution to IPM inverter dead time and other switching problems.

Functional Diagram



TRUTH TABLE

LED	V_O
ON	LOW
OFF	HIGH

A 0.1 μF bypass capacitor between pins 5 and 8 is recommended.

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

The HCPL-4504/0454 and HCNW4504 CTR, propagation delay, and CMR are specified for both TTL and IPM load/drive conditions. Specifications and typical performance plots for both TTL and IPM conditions are provided for ease of application.

These single channel, diode-transistor optocouplers are available in 8-Pin DIP, SO-8, and Widebody package configurations. An insulating layer between a LED and an integrated photodetector provide electrical insulation between input and output. Separate connections for the photodiode bias and output-transistor collector increase the speed up to a hundred times that of a conventional phototransistor coupler by reducing the base collector capacitance.

Selection Guide

Single Channel Packages		
8-Pin DIP (300 Mil)	**Small Outline SO-8**	**Widebody (400 Mil)**
HCPL-4504	HCPL-0454	HCNW4504

Ordering Information

Specify Part Number followed by Option Number (if desired).

Example:

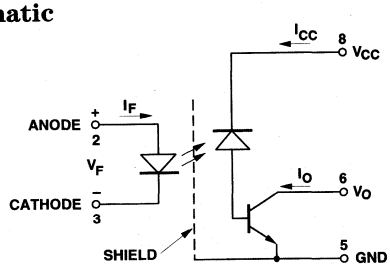
HCPL-4504#XXX

- 020 = UL 5000 V rms/1 Minute Option*
- 060 = VDE 0884 V_{IORM} = 630 V peak Option*
- 300 = Gull Wing Surface Mount Option†
- 500 = Tape and Reel Packaging Option

Option data sheets available. Contact your Hewlett-Packard sales representative or authorized distributor for information.

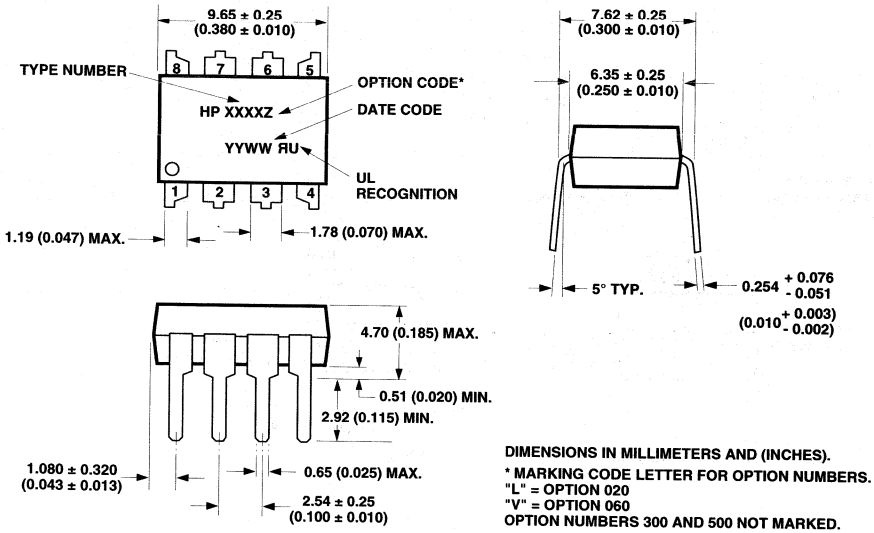
*For HCPL-4504 only. Combination of Option 020 and Option 060 is not available.
†Gull wing surface mount option applies to through hole parts only.

Schematic



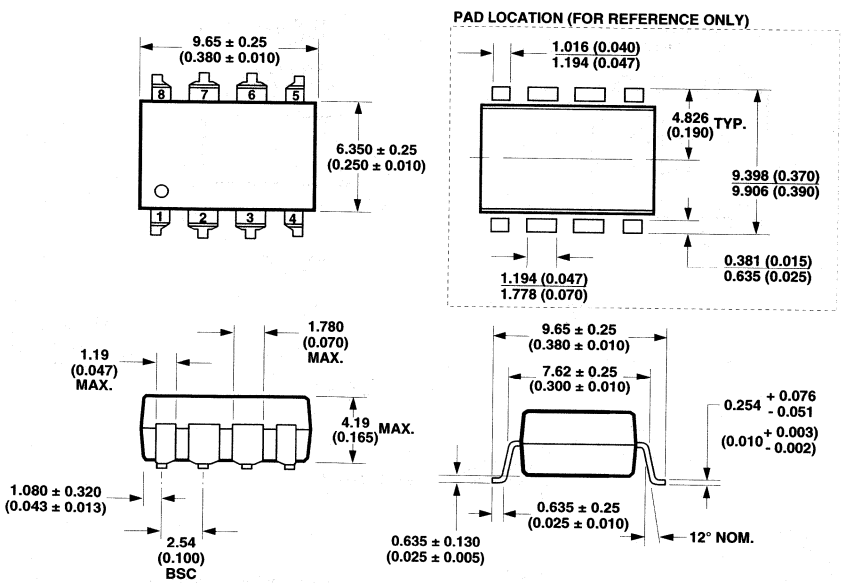
Package Outline Drawings

8-Pin DIP Package (HCPL-4504)



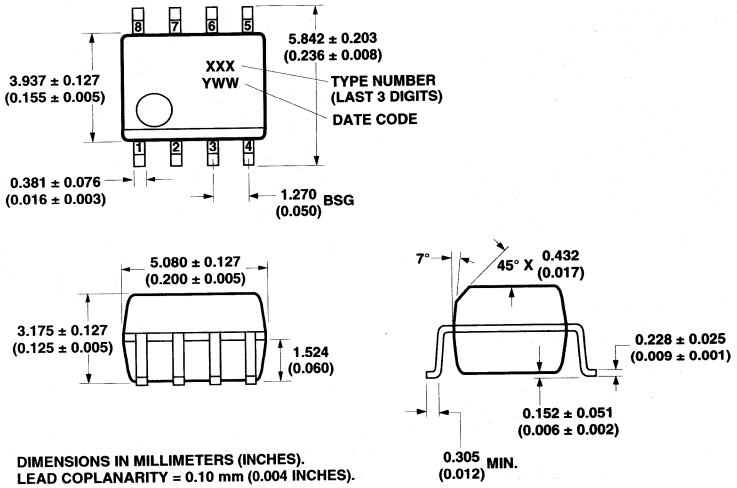
DIMENSIONS IN MILLIMETERS AND (INCHES).
* MARKING CODE LETTER FOR OPTION NUMBERS.
"L" = OPTION 020
"V" = OPTION 060
OPTION NUMBERS 300 AND 500 NOT MARKED.

8-Pin DIP Package with Gull Wing Surface Mount Option 300 (HCPL-4504)



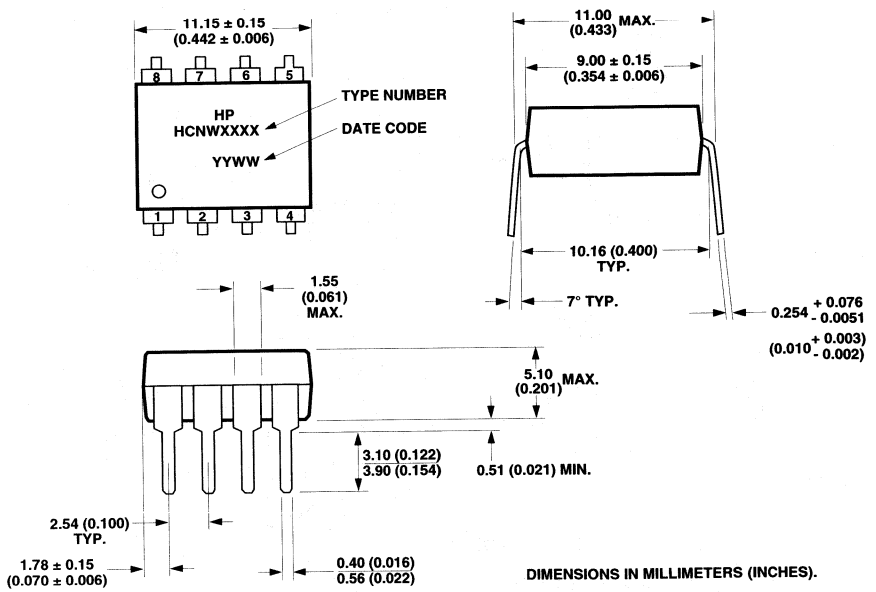
DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES).

Small Outline SO-8 Package (HCPL-0454)



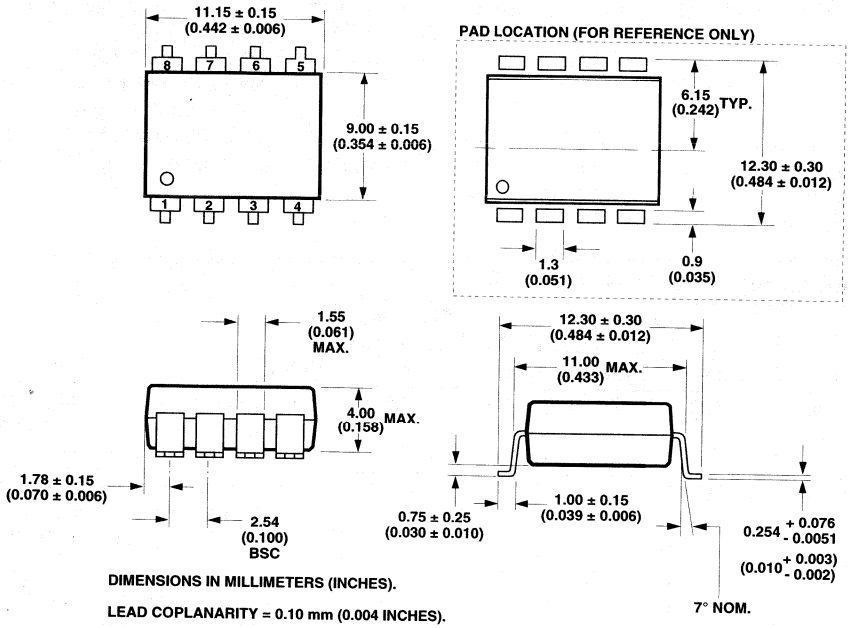
DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES).

8-Pin Widebody DIP Package (HCNW4504)

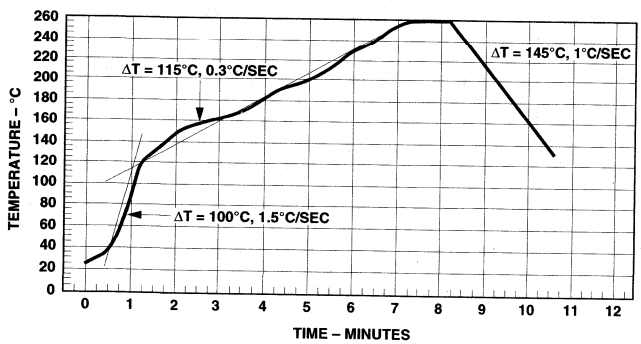


DIMENSIONS IN MILLIMETERS (INCHES).

8-Pin Widebody DIP Package with Gull Wing Surface Mount Option 300 (HCNW4504)



Solder Reflow Temperature Profile (HCPL-0454 and Gull Wing Surface Mount Option Parts)



Note: Use of nonchlorine activated fluxes is highly recommended.

Regulatory Information

The devices contained in this data sheet have been approved by the following organizations:

UL

Recognized under UL 1577, Component Recognition Program, File E55361.

CSA

Approved under CSA Component Acceptance Notice #5, File CA 88324.

VDE

Approved according to VDE 0884/06.92 (HCNW4504 and HCPL-4504#060 only).

BSI

Certification according to BS451:1994, (BS EN60065:1994); BS EN60950:1992 (BS7002:1992) and EN41003:1993 for Class II applications (HCNW4504 only).

Insulation and Safety Related Specifications

Parameter	Symbol	8-Pin DIP (300 Mil) Value	SO-8 Value	Widebody (400 Mil) Value	Units	Conditions
Minimum External Air Gap (External Clearance)	L(101)	7.1	4.9	9.6	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L(102)	7.4	4.8	10.0	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	0.08	1.0	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity.
Minimum Internal Tracking (Internal Creepage)		NA	NA	4.0	mm	Measured from input terminals to output terminals, along internal cavity.
Tracking Resistance (Comparative Tracking Index)	CTI	200	200	200	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa	IIIa	IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Option 300 - surface mount classification is Class A in accordance with CECC 00802.

VDE 0884 Insulation Related Characteristics (HCPL-4504 OPTION 060 ONLY)

Description	Symbol	Characteristic	Units
Installation classification per DIN VDE 0110/1.89, Table 1 for rated mains voltage ≤ 300 V rms		I-IV	
for rated mains voltage ≤ 450 V rms		I-III	
Climatic Classification		55/100/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	630	V peak
Input to Output Test Voltage, Method b* V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial Discharge < 5 pC	V_{PR}	1181	V peak
Input to Output Test Voltage, Method a* V_{IORM} x 1.5 = V_{PR}, Type and sample test, t_m = 60 sec, Partial Discharge < 5 pC	V_{PR}	945	V peak
Highest Allowable Overvoltage* (Transient Overvoltage, t_{ini} = 10 sec)	V_{IOTM}	6000	V peak
Safety Limiting Values (Maximum values allowed in the event of a failure, also see Figure 15, Thermal Derating curve.)			
Case Temperature	T_S	175	°C
Input Current	$I_{S,INPUT}$	230	mA
Output Power	$P_{S,OUTPUT}$	600	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	≥ 10^9	Ω

VDE 0884 Insulation Related Characteristics (HCNW4504 ONLY)

Description	Symbol	Characteristic	Units
Installation classification per DIN VDE 0110/1.89, Table 1 for rated mains voltage ≤ 600 V rms		I-IV	
for rated mains voltage ≤ 1000 V rms		I-III	
Climatic Classification		55/85/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	1414	V peak
Input to Output Test Voltage, Method b* V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial Discharge < 5 pC	V_{PR}	2652	V peak
Input to Output Test Voltage, Method a* V_{IORM} x 1.5 = V_{PR}, Type and sample test, t_m = 60 sec, Partial Discharge < 5 pC	V_{PR}	2121	V peak
Highest Allowable Overvoltage* (Transient Overvoltage, t_{ini} = 10 sec)	V_{IOTM}	8000	V peak
Safety Limiting Values (Maximum values allowed in the event of a failure, also see Figure 15, Thermal Derating curve.)			
Case Temperature	T_S	150	°C
Input Current	$I_{S,INPUT}$	400	mA
Output Power	$P_{S,OUTPUT}$	700	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	≥ 10^9	Ω

*Refer to the front of the optocoupler section of the current catalog under Product Safety Regulations section (VDE 0884), for a detailed description.

Note: Isolation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuits in application.

Absolute Maximum Ratings

Parameter	Symbol	Device	Min.	Max.	Units	Note
Storage Temperature	T_S		-55	125	°C	
Operating Temperature	T_A	HCPL-4504 HCPL-0454	-55	100	°C	
		HCNW4504	-55	85		
Average Forward Input Current	$I_{F(AVG)}$			25	mA	1
Peak Forward Input Current (50% duty cycle, 1 ms pulse width)	$I_{F(PEAK)}$	HCPL-4504 HCPL-0454		50	mA	2
(50% duty cycle, 1 ms pulse width)		HCNW4504		40		
Peak Transient Input Current (≤ 1 µs pulse width, 300 pps)	$I_{F(TRANS)}$	HCPL-4504 HCPL-0454		1	A	
		HCNW4504		0.1		
Reverse LED Input Voltage (Pin 3-2)	V_R	HCPL-4504 HCPL-0454		5	V	
		HCNW4504		3		
Input Power Dissipation	P_{IN}	HCPL-4504 HCPL-0454		45	mW	3
		HCNW4504		40		
Average Output Current (Pin 6)	$I_{O(AVG)}$			8	mA	
Peak Output Current	$I_{O(PEAK)}$			16	mA	
Supply Voltage (Pin 8-5)	V_{CC}		-0.5	30	V	
Output Voltage (Pin 6-5)	V_O		-0.5	20	V	
Output Power Dissipation	P_O			100	mW	4
Lead Solder Temperature (Through-Hole Parts Only) 1.6 mm below seating plane, 10 seconds up to seating plane, 10 seconds	T_{LS}	HCPL-4504		260	°C	
		HCNW4504		260	°C	
Reflow Temperature Profile	T_{RP}	HCPL-0454 and Option 300	See **Package Outline Drawings** section			

Electrical Specifications (DC)

Over recommended temperature (T_A = 0°C to 70°C) unless otherwise specified. See note 12.

Parameter	Symbol	Device	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR	HCPL-4504	25	32	60	%	T_A = 25°C, V_O = 0.4 V, I_F = 16 mA, V_{CC} = 4.5 V	1, 2, 4	5
		HCPL-0454	21	34			V_O = 0.5 V		
		HCNW4504	23	29	60		T_A = 25°C, V_O = 0.4 V		
			19	31	63		V_O = 0.5 V		
Current Transfer Ratio	CTR	HCPL-4504	26	35	65	%	T_A = 25°C, V_O = 0.4 V, I_F = 12 mA, V_{CC} = 4.5 V	1, 2, 4	5
		HCPL-0454	22	37			V_O = 0.5 V		
		HCNW4504	25	33	65		T_A = 25°C, V_O = 0.4 V		
			21	35	68		V_O = 0.5 V		
Logic Low Output Voltage	V_{OL}	HCPL-4504		0.2	0.4	V	T_A = 25°C, I_O = 4.0 mA, I_F = 16 mA, V_{CC} = 4.5 V		
		HCPL-0454			0.5		I_O = 3.3 mA		
		HCNW4504		0.2	0.4		T_A = 25°C, I_O = 3.6 mA		
					0.5		I_O = 3.0 mA		
Logic High Output Current	I_{OH}			0.003	0.5	µA	T_A = 25°C, V_O = V_{CC} = 5.5 V, I_F = 0 mA	5	
				0.01	1		T_A = 25°C, V_O = V_{CC} = 15 V		
					50				
Logic Low Supply Current	I_{CCL}			50	200	µA	I_F = 16 mA, V_O = Open, V_{CC} = 15 V		12
Logic High Supply Current	I_{CCH}			0.02	1	µA	T_A = 25°C, I_F = 0 mA, V_O = Open, V_{CC} = 15 V		12
					2				
Input Forward Voltage	V_F	HCPL-4504		1.5	1.7	V	T_A = 25°C, I_F = 16 mA	3	
		HCPL-0454			1.8				
		HCNW4504	1.45	1.59	1.85		T_A = 25°C, I_F = 16 mA		
			1.35		1.95				
Input Reverse Breakdown Voltage	BV_R	HCPL-4504	5			V	I_R = 10 µA		
		HCPL-0454							
		HCNW4504	3				I_R = 100 µA, T_A = 25°C		
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$	HCPL-4504		-1.6		mV/°C	I_F = 16 mA		
		HCPL-0454							
		HCNW4504		-1.4					
Input Capacitance	C_{IN}	HCPL-4504		60		pF	f = 1 MHz, V_F = 0 V		
		HCPL-0454							
		HCNW4504		70					

*All typicals at T_A = 25°C.

AC Switching Specifications

Over recommended temperature (T_A = 0°C to 70°C) unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions		Fig.	Note
Propagation Delay Time to Logic Low at Output	t_{PHL}		0.2	0.3	µs	T_A = 25°C	Pulse: f = 20 kHz, Duty Cycle = 10%, I_F = 16 mA, V_{CC} = 5.0 V, R_L = 1.9 kΩ, C_L = 15 pF, V_{THHL} = 1.5 V	6, 8, 9	9
			0.2	0.5					
		0.2	0.5	0.7		T_A = 25°C	Pulse: f = 10 kHz, Duty Cycle = 50%, I_F = 12 mA, V_{CC} = 15.0 V, R_L = 20 kΩ, C_L = 100 pF, V_{THHL} = 1.5 V	6, 10-14	10
		0.1	0.5	1.0					
Propagation Delay Time to Logic High at Output	t_{PLH}		0.3	0.5	µs	T_A = 25°C	Pulse: f = 20 kHz, Duty Cycle = 10%, I_F = 16 mA, V_{CC} = 5.0 V, R_L = 1.9 kΩ, C_L = 15 pF, V_{THLH} = 1.5 V	6, 8, 9	9
			0.3	0.7					
		0.3	0.8	1.1		T_A = 25°C	Pulse: f = 10 kHz, Duty Cycle = 50%, I_F = 12 mA, V_{CC} = 15.0 V, R_L = 20 kΩ, C_L = 100 pF, V_{THLH} = 2.0 V	6, 10-14	10
		0.2	0.8	1.4					
Propagation Delay Difference Between Any 2 Parts	t_{PLH}-t_{PHL}	-0.4	0.3	0.9	µs	T_A = 25°C	Pulse: f = 10 kHz, Duty Cycle = 50%, I_F = 12 mA, V_{CC} = 15.0 V, R_L = 20 kΩ, C_L = 100 pF, V_{THHL} = 1.5 V, V_{THLH} = 2.0 V	6, 10-14	15
		-0.7	0.3	1.3					
Common Mode Transient Immunity at Logic High Level Output	$\|CM_H\|$	15	30		kV/µs	T_A = 25°C	V_{CC} = 5.0 V, R_L = 1.9 kΩ, C_L = 15 pF, I_F = 0 mA	7	7, 9
		15	30			V_{CM} = 1500 V_{P-P}	V_{CC} = 15.0 V, R_L = 20 kΩ, C_L = 100 pF, I_F = 0 mA	7	8, 10
Common Mode Transient Immunity at Logic Low Level Output	$\|CM_L\|$	15	30		kV/µs	T_A = 25°C	V_{CC} = 5.0 V, R_L = 1.9 kΩ, C_L = 15 pF, I_F = 16 mA	7	7, 9
		10	30			V_{CM} = 1500 V_{P-P}	V_{CC} = 15.0 V, R_L = 20 kΩ, C_L = 100 pF, I_F = 12 mA	7	8, 10
		15	30				V_{CC} = 15.0 V, R_L = 20 kΩ, C_L = 100 pF, I_F = 16 mA	7	8, 10

*All typicals at T_A = 25°C.

Package Characteristics

Over recommended temperature (T_A = 0°C to 25°C) unless otherwise specified.

Parameter	Sym.	Device	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage†	V_{ISO}	HCPL-4504 HCPL-0454	2500			V rms	RH ≤ 50%, t = 1 min., T_A = 25°C		6, 13
		HCNW4504	5000						6, 14
		HCPL-4504 (Option 020)	5000						6, 11, 14
Input-Output Resistance	R_{I-O}	HCPL-4504 HCPL-0454		10^{12}		Ω	V_{I-O} = 500 Vdc		6
		HCNW4504	10^{12}	10^{13}			T_A = 25°C		
			10^{11}				T_A = 100°C		
Input-Output Capacitance	C_{I-O}	HCPL-4504 HCPL-0454		0.6		pF	f = 1 MHz		6
		HCNW4504		0.5	0.6				

*All typicals at T_A = 25°C..

†The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the VDE 0884 Insulation Related Characteristics Table (if applicable), your equipment level safety specification or HP Application Note 1074 entitled "Optocoupler Input-Output Endurance Voltage."

Notes:

1. Derate linearly above 70°C free-air temperature at a rate of 0.8 mA/°C (8-Pin DIP).
   Derate linearly above 85°C free-air temperature at a rate of 0.5 mA/°C (SO-8).
2. Derate linearly above 70°C free-air temperature at a rate of 1.6 mA/°C (8-Pin DIP).
   Derate linearly above 85°C free-air temperature at a rate of 1.0 mA/°C (SO-8).
3. Derate linearly above 70°C free-air temperature at a rate of 0.9 mW/°C (8-Pin DIP).
   Derate linearly above 85°C free-air temperature at a rate of 1.1 mW/°C (SO-8).
4. Derate linearly above 70°C free-air temperature at a rate of 2.0 mW/°C (8-Pin DIP).
   Derate linearly above 85°C free-air temperature at a rate of 2.3 mW/°C (SO-8).
5. CURRENT TRANSFER RATIO in percent is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100.
6. Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.
7. Under TTL load and drive conditions: Common mode transient immunity in a Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (i.e., V_O > 2.0 V). Common mode transient immunity in a Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., V_O < 0.8 V).
8. Under IPM (Intelligent Power Module) load and LED drive conditions: Common mode transient immunity in a Logic High level is the maximum tolerable dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (i.e., V_O > 3.0 V). Common mode transient immunity in a Logic Low level is the maximum tolerable dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., V_O < 1.0 V).
9. The 1.9 kΩ load represents 1 TTL unit load of 1.6 mA and the 5.6 kΩ pull-up resistor.
10. The R_L = 20 kΩ, C_L = 100 pF load represents an IPM (Intelligent Power Module) load.
11. See Option 020 data sheet for more information.
12. Use of a 0.1 µF bypass capacitor connected between pins 5 and 8 is recommended.
13. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 3000 V rms for 1 second (leakage detection current limit, I_{i-o} ≤ 5 µA). This test is performed before the 100% Production test shown in the VDE 0884 Insulation Related Characteristics Table, if applicable.
14. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 6000 V rms for 1 second (leakage detection current limit, I_{i-o} ≤ 5 µA). This test is performed before the 100% Production test shown in the VDE 0884 Insulation Related Characteristics Table, if applicable.
15. The difference between t_{PLH} and t_{PHL} between any two devices (same part number) under the same test condition. (See Power Inverter Dead Time and Propagation Delay Specifications section.)

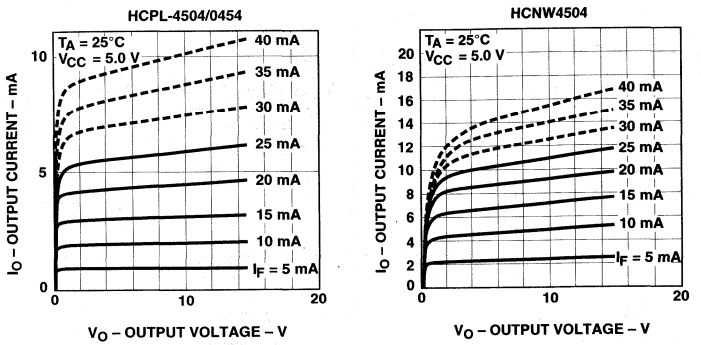


Figure 1. DC and Pulsed Transfer Characteristics.

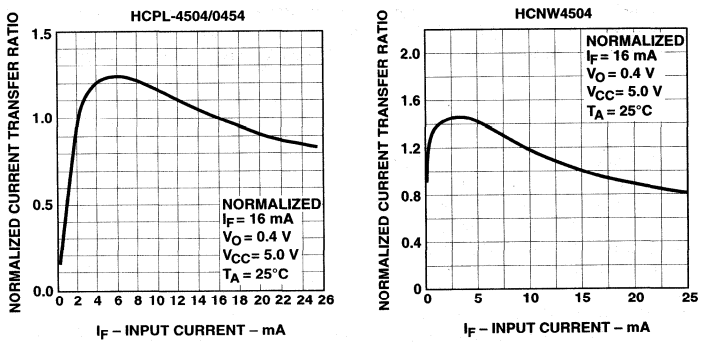


Figure 2. Current Transfer Ratio vs. Input Current.

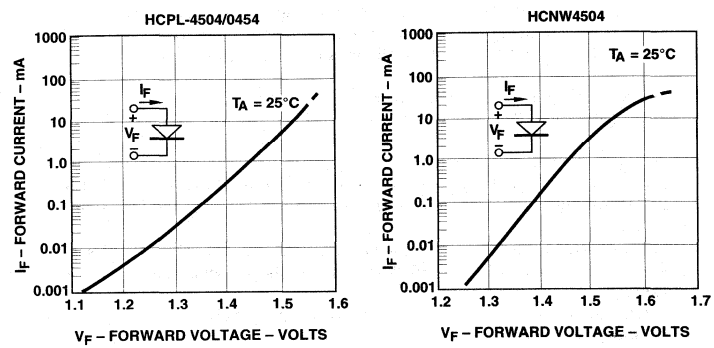
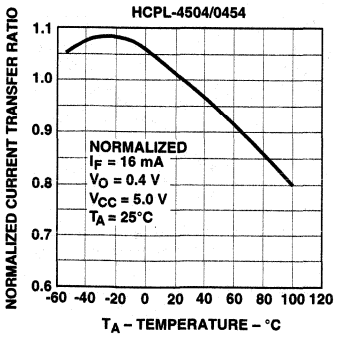


Figure 3. Input Current vs. Forward Voltage.



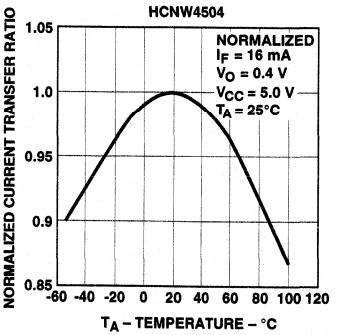


Figure 4. Current Transfer Ratio vs. Temperature.

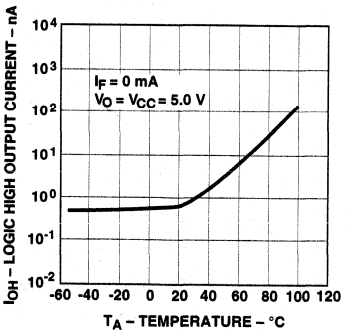
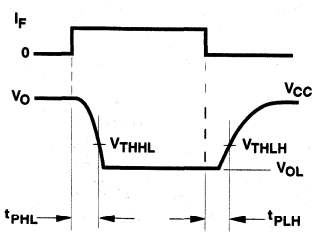


Figure 5. Logic High Output Current vs. Temperature.



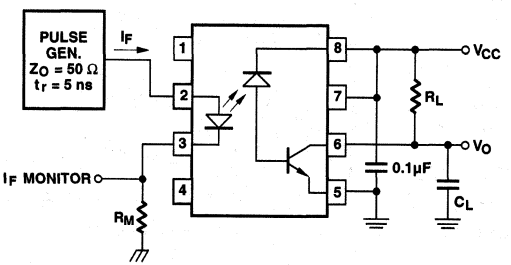
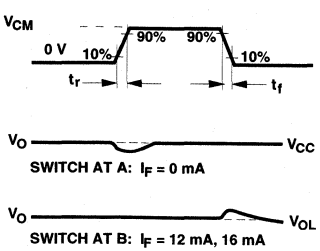


Figure 6. Switching Test Circuit.



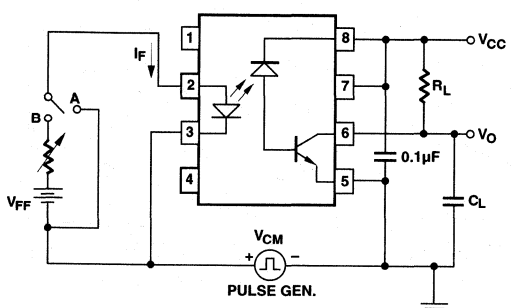


Figure 7. Test Circuit for Transient Immunity and Typical Waveforms.

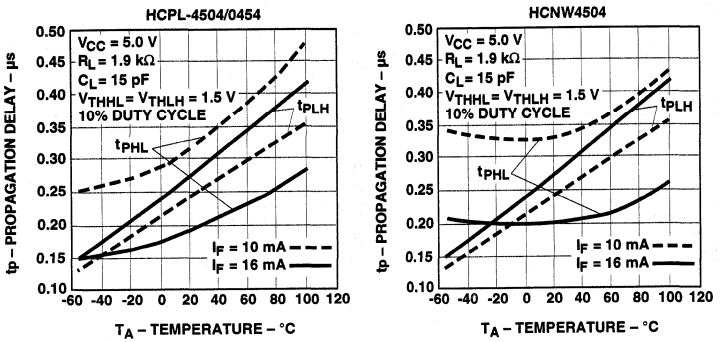


Figure 8. Propagation Delay Time vs. Temperature.

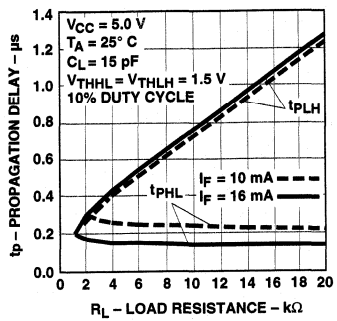


Figure 9. Propagation Delay Time vs. Load Resistance.

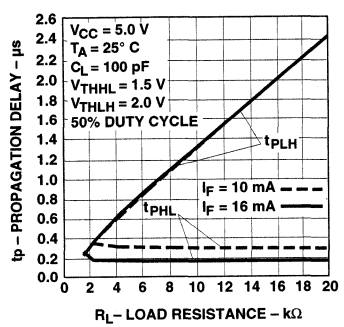


Figure 10. Propagation Delay Time vs. Load Resistance.

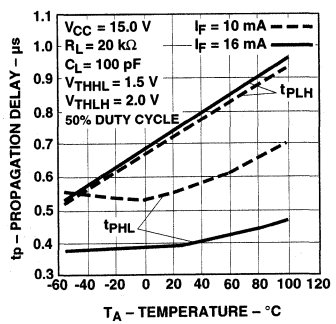


Figure 11. Propagation Delay Time vs. Temperature.

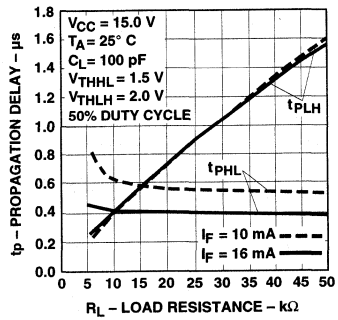


Figure 12. Propagation Delay Time vs. Load Resistance.

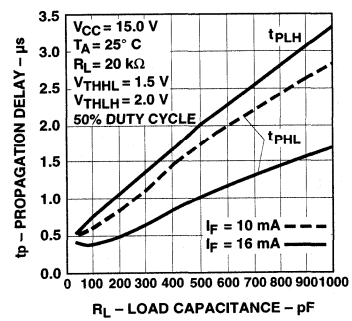


Figure 13. Propagation Delay Time vs. Load Capacitance.

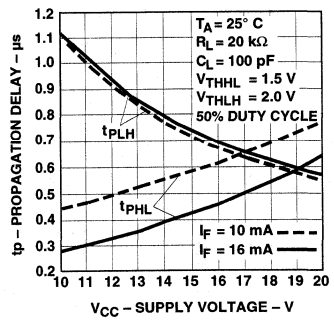


Figure 14. Propagation Delay Time vs. Supply Voltage.

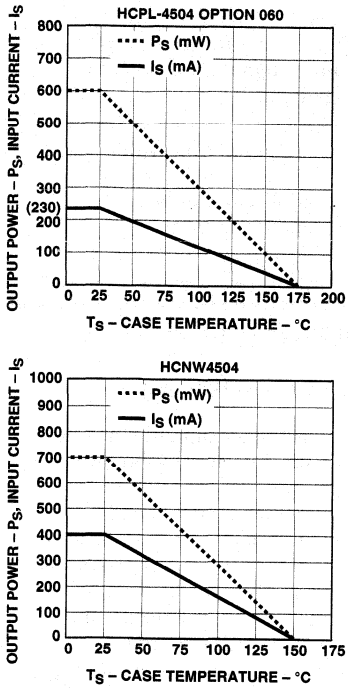


Figure 15. Thermal Derating Curve, Dependence of Safety Limiting Valve with Case Temperature per VDE 0884.

Power Inverter Dead Time and Propagation Delay Specifications

The HCPL-4504/0454 and HCNW4504 include a specification intended to help designers minimize "dead time" in their power inverter designs. The new "propagation delay difference" specification ($t_{PLH} - t_{PHL}$) is useful for determining not only how much optocoupler switching delay is needed to prevent "shoot-through" current, but also for determining the best achievable worst-case dead time for a given design.

When inverter power transistors switch (Q1 and Q2 in Figure 17), it is essential that they never

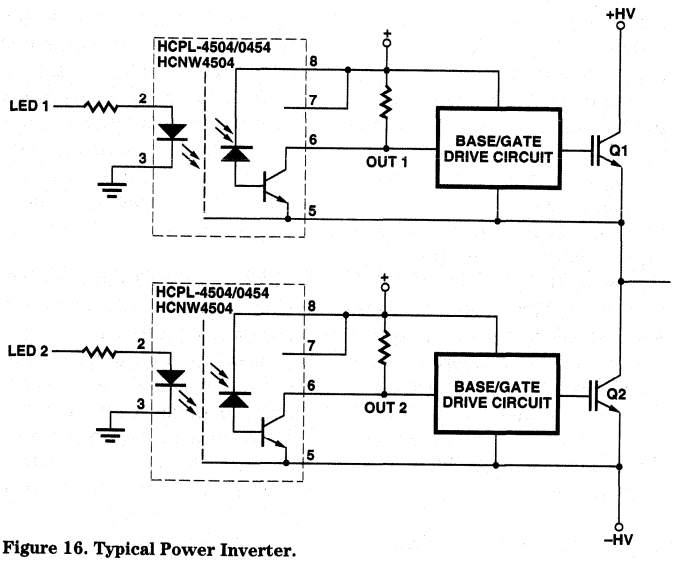


Figure 16. Typical Power Inverter.

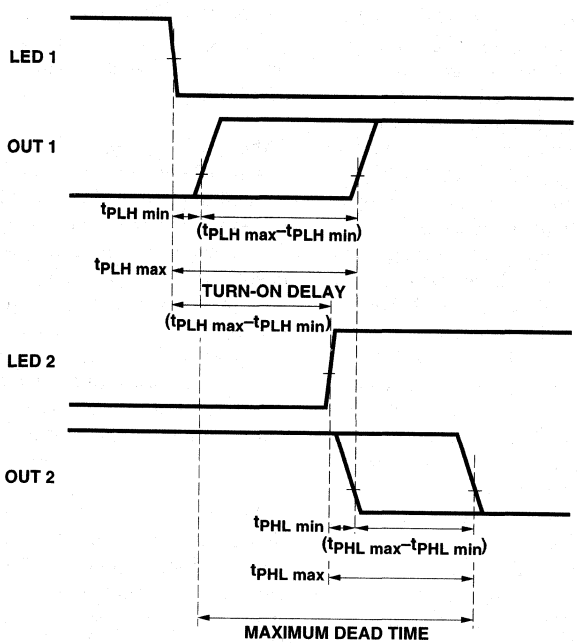


Figure 17. LED Delay and Dead Time Diagram.

conduct at the same time. Extremely large currents will flow if there is any overlap in their conduction during switching transitions, potentially damaging the transistors and even the surrounding circuitry. This "shoot-through" current is eliminated by delaying the turn-on of one transistor (Q2) long enough to ensure that the opposing transistor (Q1) has completely turned off. This delay introduces a small amount of "dead time" at the output of the inverter during which both transistors are off during switching transitions. Minimizing this dead time is an important design goal for an inverter designer.

The amount of turn-on delay needed depends on the propagation delay characteristics of the optocoupler, as well as the characteristics of the transistor base/gate drive circuit. Considering only the delay characteristics of the optocoupler (the characteristics of the base/gate drive circuit can be analyzed in the same way), it is important to know the minimum and maximum turn-on (t_{PHL}) and turn-off (t_{PLH}) propagation delay specifications, preferably over the desired operating temperature range. The importance of these specifications is illustrated in Figure 17. The waveforms labeled "LED1", "LED2", "OUT1", and "OUT2" are the input and output voltages of the optocoupler circuits driving Q1 and Q2 respectively. Most inverters are designed such that the power transistor turns on when the optocoupler LED turns on; this ensures that both power transistors will be off in the event of a power loss in the control circuit. Inverters can also be designed such that the power transistor turns off when the optocoupler LED turns on; this type of design, however, requires additional fail-safe circuitry to turn off the power transistor if an over-current condition is detected. The timing illustrated in Figure 17 assumes that the power transistor turns on when the optocoupler LED turns on.

The LED signal to turn on Q2 should be delayed enough so that an optocoupler with the very fastest turn-on propagation delay (t_{PHLmin}) will never turn on before an optocoupler with the very slowest turn-off propagation delay (t_{PLHmax}) turns off. To ensure this, the turn-on of the optocoupler should be delayed by an amount no less than (t_{PLHmax} - t_{PHLmin}), which also happens to be the maximum data sheet value for the propagation delay difference specification, (t_{PLH} - t_{PHL}). The HCPL-4504/0454 and HCNW4504 specify a maximum (t_{PLH} - t_{PHL}) of 1.3 µs over an operating temperature range of 0-70°C.

Although $(t_{PLH}-t_{PHL})_{max}$ tells the designer how much delay is needed to prevent shoot-through current, it is insufficient to tell the designer how much dead time a design will have. Assuming that the optocoupler turn-on delay is exactly equal to $(t_{PLH} - t_{PHL})_{max}$, the minimum dead time is zero (i.e., there is zero time between the turn-off of the very slowest optocoupler and the turn-on of the very fastest optocoupler).

Calculating the maximum dead time is slightly more complicated. Assuming that the LED turn-on delay is still exactly equal to $(t_{PLH} - t_{PHL})_{max}$, it can be seen in Figure 17 that the maximum dead time is the sum of the maximum difference in turn-on delay plus the maximum difference in turn-off delay,

$$[(t_{PLHmax}-t_{PLHmin})+(t_{PHLmax}-t_{PHLmin})].$$

This expression can be rearranged to obtain

$$[(t_{PLHmax}-t_{PHLmin})-(t_{PHLmin}-t_{PHLmax})],$$

and further rearranged to obtain

$$[(t_{PLH}-t_{PHL})_{max}-(t_{PLH}-t_{PHL})_{min}],$$

which is the maximum minus the minimum data sheet values of (t_{PLH}-t_{PHL}). The difference between the maximum and minimum values depends directly on the total spread in propagation delays and sets the limit on how good the worst-case dead time can be for a given design. Therefore, optocouplers with tight propagation delay specifications (and not just shorter delays or lower pulse-width distortion) can achieve short dead times in power inverters. The HCPL-4504/0454 and HCNW4504 specify a minimum (t_{PLH} - t_{PHL}) of -0.7 µs over an operating temperature range of 0-70°C, resulting in a maximum dead time of 2.0 µs when the LED turn-on delay is equal to $(t_{PLH}-t_{PHL})_{max}$, or 1.3 µs.

It is important to maintain accurate LED turn-on delays because delays shorter than $(t_{PLH} - t_{PHL})_{max}$ may allow shoot-through currents, while longer delays will increase the worst-case dead time.

Intelligent Power Module and Gate Drive Interface Optocouplers

Technical Data

HCPL-4506
HCPL-0466
HCNW4506

Features

- **Performance Specified for Common IPM Applications over Industrial Temperature Range: -40°C to 100°C**
- **Fast Maximum Propagation Delays**
  t_{PHL} = 400 ns
  t_{PLH} = 550 ns
- **Minimized Pulse Width Distortion (PWD = 450 ns)**
- **15 kV/µs Minimum Common Mode Transient Immunity at V_{CM} = 1500 V**
- **CTR > 44% at I_F = 10 mA**
- **Safety Approval**
  UL Recognized - 2500 V rms for 1 minute (5000 V rms for 1 minute for HCNW4506 and HCPL-4506 Option 020) per UL1577
  CSA Approved
  VDE 0884 Approved
  -V_{IORM} = 630 V peak for HCPL-4506 Option 060
  -V_{IORM} = 1414 V peak for HCNW4506
  BSI Certified (HCNW4506)

Applications

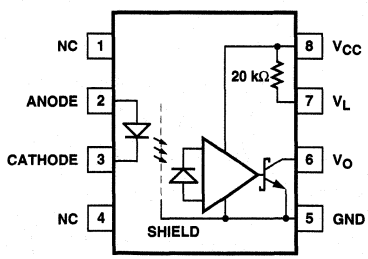
- **IPM Isolation**
- **Isolated IGBT/MOSFET Gate Drive**
- **AC and Brushless DC Motor Drives**
- **Industrial Inverters**

Description

The HCPL-4506 and HCPL-0466 contain a GaAsP LED while the HCNW4506 contains an AlGaAs LED. The LED is optically coupled to an integrated high gain photo detector. Minimized propagation delay difference between devices make these optocouplers excellent solutions for improving inverter efficiency through reduced switching dead time.

An on chip 20 kΩ output pull-up resistor can be enabled by shorting output pins 6 and 7, thus eliminating the need for an external pull-up resistor in common IPM applications. Specifications and performance plots are given for typical IPM applications.

Functional Diagram



Truth Table

LED	V_O
ON	L
OFF	H

Selection Guide

Operating Temperature T_A [°C]		Single Channel Packages			
Min.	Max.	8-Pin DIP (300 Mil)	Small Outline SO-8	Widebody (400 Mil)	Hermetic*
-40	100	HCPL-4506	HCPL-0466	HCNW4506	
-55	125				HCPL-5300 HCPL-5301

*Technical data for these products are on separate HP publications.

The connection of a 0.1 µF bypass capacitor between pins 5 and 8 is recommended.

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Ordering Information

Specify Part Number followed by Option Number (if desired).

Example:

HCPL-4506#XXX

- 020 = UL 5000 V rms/1 Minute Option*
- 060 = VDE 0884 V_{IORM} = 630 V peak Option*
- 300 = Gull Wing Surface Mount Option†
- 500 = Tape and Reel Packaging Option

*For HCPL-4506 only. Combination of Option 020 and Option 060 is not available.

†Gull wing surface mount option applies to through hole parts only.

Option data sheets are available. Contact your Hewlett-Packard sales representative or authorized distributor for information.

Package Outline Drawings

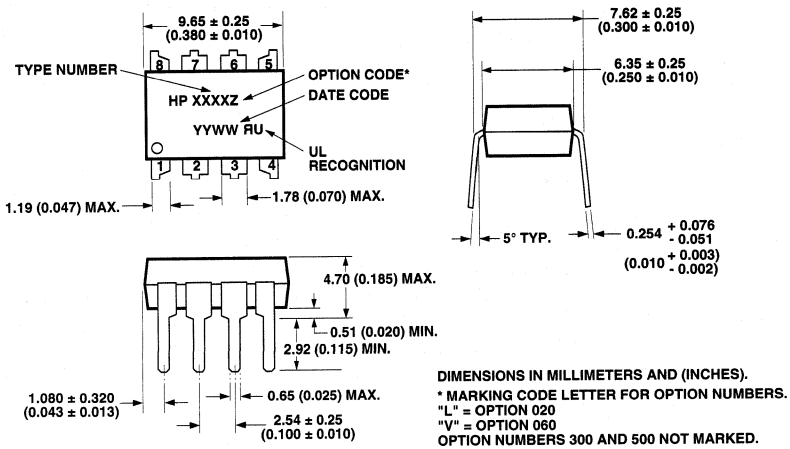


Figure 1. HCPL-4506 Outline Drawing (Standard DIP Package).

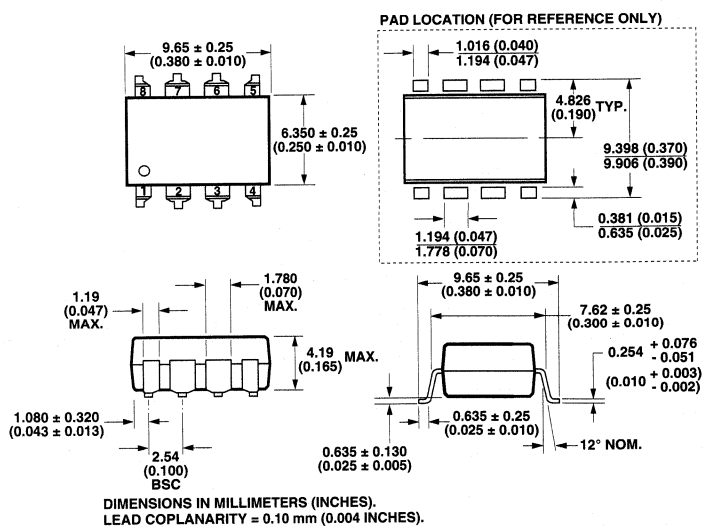


Figure 2. HCPL-4506 Gull Wing Surface Mount Option #300 Outline Drawing.

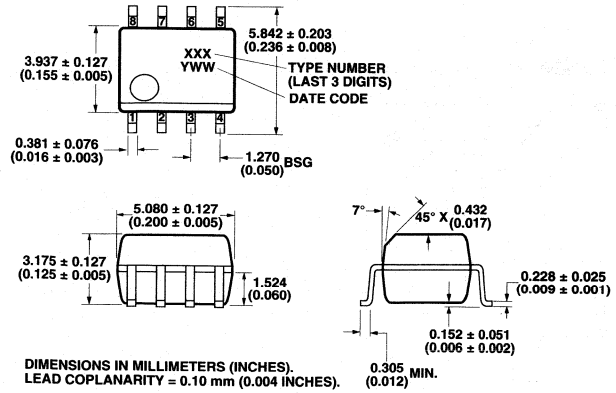


Figure 3. HCPL-0466 Outline Drawing (8-Pin Small Outline Package).

Pin Location (for reference only)

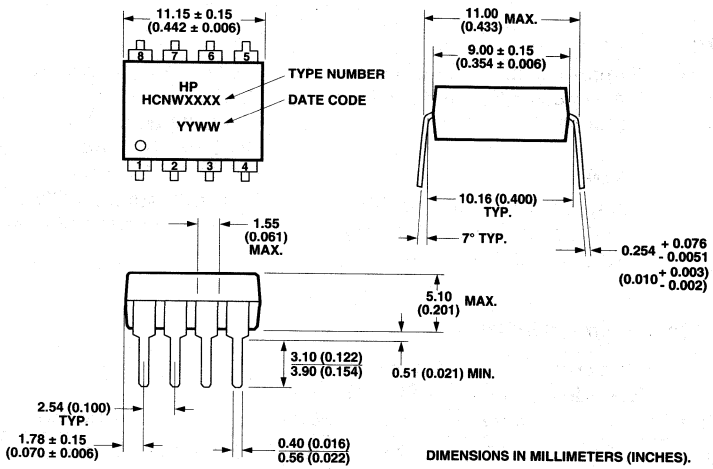


Figure 4a. HCNW4506 Outline Drawing (8-Pin Widebody Package).

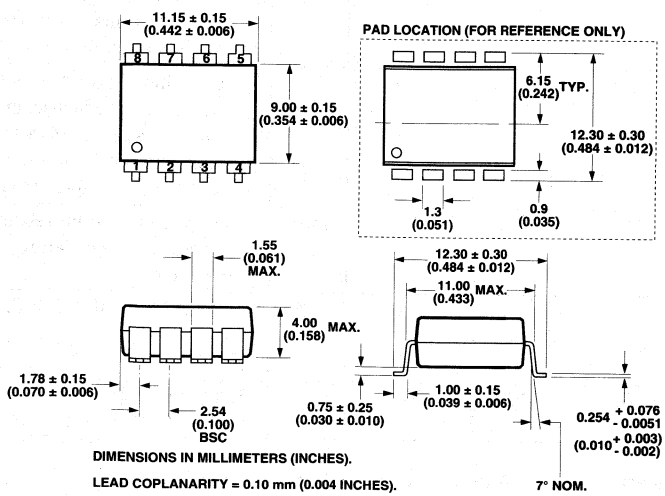
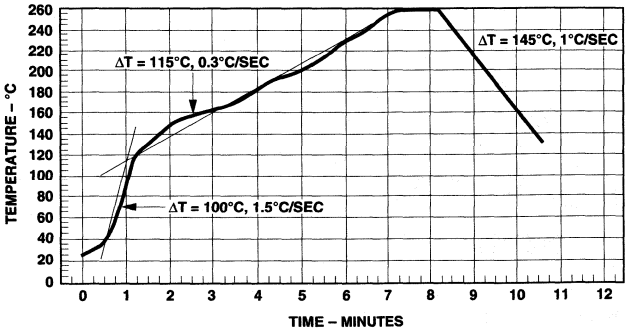


Figure 4b. HCNW4506 Outline Drawing (8-Pin Widebody Package with Gull Wing Surface Mount Option 300).

Solder Reflow Temperature Profile



Note: Use of nonchlorine activated fluxes is recommended.

Regulatory Information

The devices contained in this data sheet have been approved by the following organizations:

UL

Recognized under UL 1577, Component Recognition Program, File E55361.

CSA

Approved under CSA Component Acceptance Notice #5, File CA 88324.

VDE

Approved according to VDE 0884/06.92 (HCNW4506 and HCPL-4506 Option 060 only).

BSI

Certification according to BS451:1994 (BS EN60065:1994); BS EN60950:1992 (BS7002:1992) and EN41003:1993 for Class II applications (HCNW4506 only).

Insulation and Safety Related Specifications

Parameter	Symbol	8-Pin DIP (300 Mil) Value	SO-8 Value	Widebody (400 Mil) Value	Units	Conditions
Minimum External Air Gap (External Clearance)	L(101)	7.1	4.9	9.6	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L(102)	7.4	4.8	10.0	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	0.08	1.0	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity.
Minimum Internal Tracking (Internal Creepage)		NA	NA	4.0	mm	Measured from input terminals to output terminals, along internal cavity.
Tracking Resistance (Comparative Tracking Index)	CTI	200	200	200	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa	IIIa	IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Option 300 - surface mount classification is Class A in accordance with CECC 00802.

VDE 0884 Insulation Related Characteristics (HCPL-4506 OPTION 060 ONLY)

Description	Symbol	Characteristic	Units
Installation classification per DIN VDE 0110/1.89, Table 1			
for rated mains voltage ≤ 300 V rms		I-IV	
for rated mains voltage ≤ 450 V rms		I-III	
Climatic Classification		55/100/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	630	V peak
Input to Output Test Voltage, Method b* V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial Discharge < 5 pC	V_{PR}	1181	V peak
Input to Output Test Voltage, Method a* V_{IORM} x 1.5 = V_{PR}, Type and sample test, t_m = 60 sec, Partial Discharge < 5 pC	V_{PR}	945	V peak
Highest Allowable Overvoltage* (Transient Overvoltage, t_{ini} = 10 sec)	V_{IOTM}	6000	V peak
Safety Limiting Values (Maximum values allowed in the event of a failure, also see Figure 18, Thermal Derating curve.)			
Case Temperature	T_S	175	°C
Input Current	$I_{S,INPUT}$	230	mA
Output Power	$P_{S,OUTPUT}$	600	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	≥ 10^9	Ω

VDE 0884 Insulation Related Characteristics (HCNW4506 ONLY)

Description	Symbol	Characteristic	Units
Installation classification per DIN VDE 0110/1.89, Table 1			
for rated mains voltage ≤ 600 V rms		I-IV	
for rated mains voltage ≤ 1000 V rms		I-III	
Climatic Classification		55/100/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	1414	V peak
Input to Output Test Voltage, Method b* V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial Discharge < 5 pC	V_{PR}	2652	V peak
Input to Output Test Voltage, Method a* V_{IORM} x 1.5 = V_{PR}, Type and sample test, t_m = 60 sec, Partial Discharge < 5 pC	V_{PR}	2121	V peak
Highest Allowable Overvoltage* (Transient Overvoltage, t_{ini} = 10 sec)	V_{IOTM}	8000	V peak
Safety Limiting Values (Maximum values allowed in the event of a failure, also see Figure 18, Thermal Derating curve.)			
Case Temperature	T_S	150	°C
Input Current	$I_{S,INPUT}$	400	mA
Output Power	$P_{S,OUTPUT}$	700	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	≥ 10^9	Ω

*Refer to the front of the optocoupler section of the current catalog, under Product Safety Regulations section (VDE 0884), for a detailed description.

Note: Isolation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuits in application.

Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Units
Storage Temperature		T_S	-55	125	°C
Operating Temperature		T_A	-40	100	°C
Average Input Current[1]		$I_{F(avg)}$		25	mA
Peak Input Current[2] (50% duty cycle, ≤ 1 ms pulse width)		$I_{F(peak)}$		50	mA
Peak Transient Input Current (<1 µs pulse width, 300 pps)		$I_{F(tran)}$		1.0	A
Reverse Input Voltage (Pin 3-2)	HCPL-4506, HCPL-0466	V_R		5	Volts
	HCNW4506			3	
Average Output Current (Pin 6)		$I_{O(avg)}$		15	mA
Resistor Voltage (Pin 7)		V_7	-0.5	V_{CC}	Volts
Output Voltage (Pin 6-5)		V_O	-0.5	30	Volts
Supply Voltage (Pin 8-5)		V_{CC}	-0.5	30	Volts
Output Power Dissipation[3]		P_O		100	mW
Total Power Dissipation[4]		P_T		145	mW
Lead Solder Temperature (HCPL-4506)		260°C for 10 s, 1.6 mm below seating plane			
Lead Solder Temperature (HCNW4506)		260°C for 10 s (up to seating plane)			
Infrared and Vapor Phase Reflow Temperature (HCPL-0466 and Option 300)		See **Package Outline Drawings** Section			

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage	V_{CC}	4.5	30	Volts
Output Voltage	V_O	0	30	Volts
Input Current (ON)	$I_{F(on)}$	10	20	mA
Input Voltage (OFF)	$V_{F(off)}$*	-5	0.8	V
Operating Temperature	T_A	-40	100	°C

*Recommended $V_{F(OFF)}$ = -3 V to 0.8 V for HCNW4506.

Electrical Specifications

Over recommended operating conditions unless otherwise specified:
T_A = -40°C to +100°C, V_{CC} = +4.5 V to 30 V, $I_{F(on)}$ = 10 mA to 20 mA, $V_{F(off)}$ = -5 V to 0.8 V†

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions		Fig.	Note
Current Transfer Ratio	CTR	44	90		%	I_F = 10 mA, V_O = 0.6 V			5
Low Level Output Current	I_{OL}	4.4	9.0		mA	I_F = 10 mA, V_O = 0.6 V		5,6	
Low Level Output Voltage	V_{OL}		0.3	0.6	V	I_O = 2.4 mA			
Input Threshold Current	I_{TH}		1.5	5.0	mA	V_O = 0.8 V, I_O = 0.75 mA		5	14
High Level Output Current	I_{OH}		5	50	µA	V_F = 0.8 V		7	
High Level Supply Current	I_{CCH}		0.6	1.3	mA	V_F = 0.8 V, V_O = Open			14
Low Level Supply Current	I_{CCL}		0.6	1.3	mA	I_F = 10 mA, V_O = Open			14
Input Forward Voltage	V_F		1.5	1.8	V	HCPL-4506 HCPL-0466	I_F = 10 mA	8	
			1.6	1.85		HCNW4506		9	
Temperature Coefficient of Forward Voltage	$\Delta V_F/\Delta T_A$		-1.6		mV/°C	HCPL-4506 HCPL-0466	I_F = 10 mA		
			-1.3			HCNW4506			
Input Reverse Breakdown Voltage	BV_R	5			V	HCPL-4506 HCPL-0466	I_R = 100 µA		
		3				HCNW4506			
Input Capacitance	C_{IN}		60		pF	HCPL-4506 HCPL-0466	f = 1 MHz, V_F = 0 V		
			72			HCNW4506			
Internal Pull-up Resistor	R_L	14	20	25	kΩ	T_A = 25°C			10,11
Internal Pull-up Resistor Temperature Coefficient	$\Delta R_L/\Delta T_A$		0.014		kΩ/°C				

*All typical values at 25°C, V_{CC} = 15 V.
†$V_{F(off)}$ = -3 V to 0.8 V for HCNW4506.

Switching Specifications (R_L = 20 kΩ External)

Over recommended operating conditions unless otherwise specified:
T_A = -40°C to +100°C, V_{CC} = +4.5 V to 30 V, $I_{F(on)}$ = 10 mA to 20 mA, $V_{F(off)}$ = -5 V to 0.8 V†

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions		Fig.	Note
Propagation Delay Time to Low Output Level	t_{PHL}	30	200	400	ns	C_L = 100 pF	$I_{F(on)}$ = 10 mA, $V_{F(off)}$ = 0.8 V, V_{CC} = 15.0 V,	10, 12, 14-17	9, 12, 14
			100		ns	C_L = 10 pF			
Propagation Delay Time to High Output Level	t_{PLH}	270	400	550	ns	C_L = 100 pF	V_{THLH} = 2.0 V, V_{THHL} = 1.5 V		
			130			C_L = 10 pF			
Pulse Width Distortion	PWD		200	450	ns	C_L = 100 pF			18
Propagation Delay Difference Between Any 2 Parts	t_{PLH}-t_{PHL}	-150	200	450	ns				15
Output High Level Common Mode Transient Immunity	$\|CM_H\|$	15	30		kV/μs	I_F = 0 mA, V_O > 3.0 V	V_{CC} = 15.0 V, C_L = 100 pF, V_{CM} = 1500 V_{P-P}	11	16
Output Low Level Common Mode Transient Immunity	$\|CM_L\|$	15	30		kV/μs	I_F = 10 mA V_O < 1.0 V	T_A = 25°C		17

Switching Specifications (R_L = Internal Pull-up)

Over recommended operating conditions unless otherwise specified:
T_A = -40°C to +100°C, V_{CC} = +4.5 V to 30 V, $I_{F(on)}$ = 10 mA to 20 mA, $V_{F(off)}$ = -5 V to 0.8 V†

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions		Fig.	Note
Propagation Delay Time to Low Output Level	t_{PHL}	20	200	400	ns	$I_{F(on)}$ = 10 mA, $V_{F(off)}$ = 0.8 V, V_{CC} = 15.0 V, C_L = 100 pF, V_{THLH} = 2.0 V, V_{THHL} = 1.5 V		10, 13	9-12, 14
Propagation Delay Time to High Output Level	t_{PLH}	220	450	650	ns				
Pulse Width Distortion	PWD		250	500	ns				18
Propagation Delay Difference Between Any 2 Parts	t_{PLH}-t_{PHL}	-150	250	500	ns				15
Output High Level Common Mode Transient Immunity	$\|CM_H\|$		30		kV/μs	I_F = 0 mA, V_O > 3.0 V	V_{CC} = 15.0 V, C_L = 100 pF, V_{CM} = 1500 V_{P-P},	11	16
Output Low Level Common Mode Transient Immunity	$\|CM_L\|$		30		kV/μs	I_F = 16 mA, V_O < 1.0 V	T_A = 25°C		17
Power Supply Rejection	PSR		1.0		V_{P-P}	Square Wave, t_{RISE}, t_{FALL} > 5 ns, no bypass capacitors			14

*All typical values at 25°C, V_{CC} = 15 V.
†$V_{F(off)}$ = -3 V to 0.8 V for HCNW4506.

Package Characteristics

Over recommended temperature (T_A = -40°C to 100°C) unless otherwise specified.

Parameter	Sym.	Min.	Typ.*	Max.	Units	Test Conditions		Fig.	Note
Input-Output Momentary Withstand Voltage†	V_{ISO}	2500			V rms	HCPL-4506 HCPL-0466	RH < 50%, t = 1 min. T_A = 25°C		6, 7, 8
		5000				HCNW4506 Option 020			6, 8, 13
		5000				HCNW4506			6, 8
Resistance (Input-Output)	R_{I-O}		10^{12}		Ω	HCPL-4506 HCPL-0466	V_{I-O} = 500 Vdc		6
		10^{12}	10^{13}			HCNW4506			
Capacitance (Input-Output)	C_{I-O}		0.6		pF	HCPL-4506 HCPL-0466	f = 1 MHz		6
			0.5			HCNW4506			

*All typical values at 25°C, V_{CC} = 15 V.

†The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the VDE 0884 Insulation Related Characteristics Table (if applicable), your equipment level safety specification or HP Application Note 1074 entitled "Optocoupler Input-Output Endurance Voltage," publication number 5963-2203E.

Notes:

1. Derate linearly above 90°C free-air temperature at a rate of 0.8 mA/°C.
2. Derate linearly above 90°C free-air temperature at a rate of 1.6 mA/°C.
3. Derate linearly above 90°C free-air temperature at a rate of 3.0 mW/°C.
4. Derate linearly above 90°C free-air temperature at a rate of 4.2 mW/°C.
5. CURRENT TRANSFER RATIO in percent is defined as the ratio of output collector current (I_O) to the forward LED input current (I_F) times 100.
6. Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.
7. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 3000 V rms for 1 second (leakage detection current limit, $I_{I-O} \leq 5$ μA). This test is performed before the 100% Production test shown in the VDE 0884 Insulation Related Characteristics Table, if applicable.
8. For option 020, in accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 6000 V rms for 1 second (leakage detection current limit, $I_{I-O} \leq 5$ μA). This test is performed before the 100% Production test for partial discharge (method b) shown in the VDE 0884 Insulation Related Characteristics Table, if applicable.
9. Pulse: f = 20 kHz, Duty Cycle = 10%.
10. The internal 20 kΩ resistor can be used by shorting pins 6 and 7 together.
11. Due to tolerance of the internal resistor, and since propagation delay is dependent on the load resistor value, performance can be improved by using an external 20 kΩ 1% load resistor. For more information on how propagation delay varies with load resistance, see Figure 12.
12. The R_L = 20 kΩ, C_L = 100 pF load represents a typical IPM (Intelligent Power Module) load.
13. See Option 020 data sheet for more information.
14. Use of a 0.1 μF bypass capacitor connected between pins 5 and 8 can improve performance by filtering power supply line noise.
15. The difference between t_{PLH} and t_{PHL} between any two devices under the same test condition. (See IPM Dead Time and Propagation Delay Specifications section.)
16. Common mode transient immunity in a Logic High level is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (i.e., V_O > 3.0 V).
17. Common mode transient immunity in a Logic Low level is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., V_O < 1.0 V).
18. Pulse Width Distortion (PWD) is defined as $|t_{PHL} - t_{PLH}|$ for any given device.

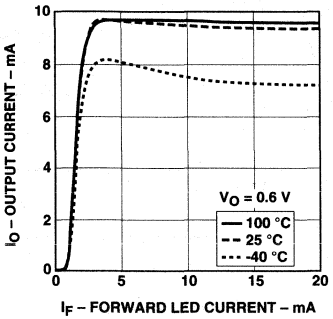


Figure 5. Typical Transfer Characteristics.

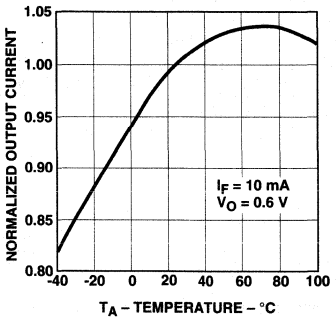


Figure 6. Normalized Output Current vs. Temperature.

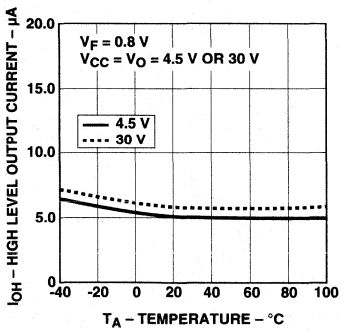


Figure 7. High Level Output Current vs. Temperature.

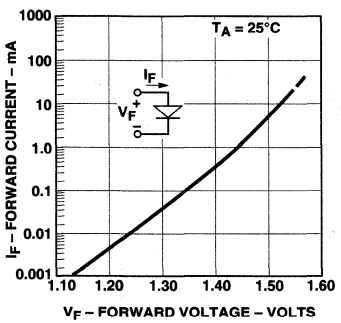


Figure 8. HCPL-4506 and HCPL-0466 Input Current vs. Forward Voltage.

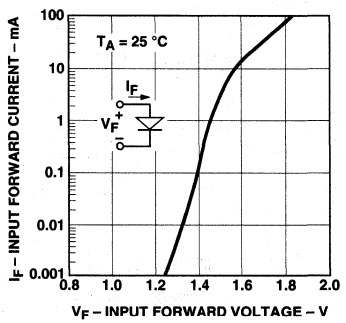
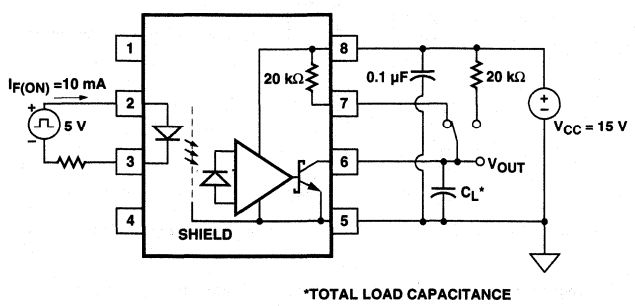


Figure 9. HCNW4506 Input Current vs. Forward Voltage.



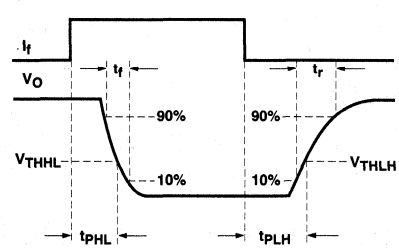


Figure 10. Propagation Delay Test Circuit.

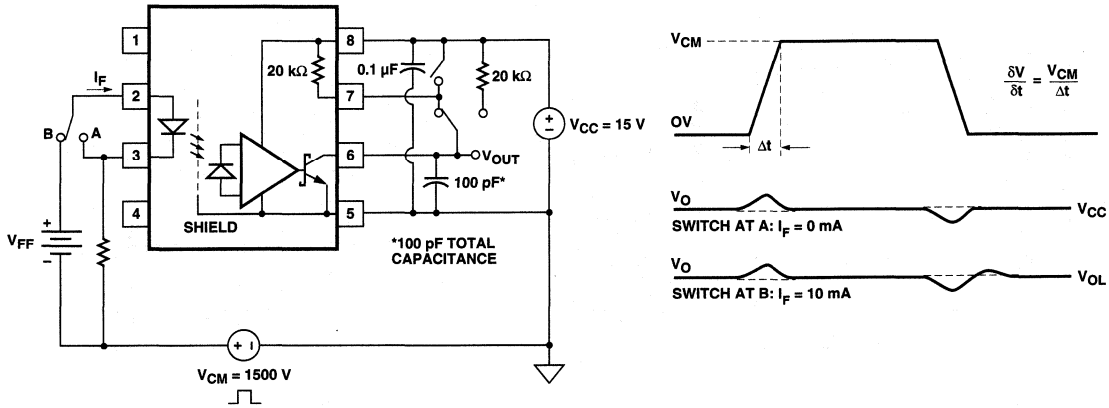


Figure 11. CMR Test Circuit. Typical CMR Waveform.

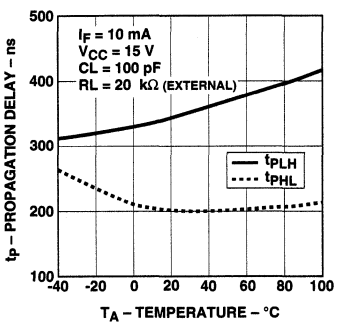


Figure 12. Propagation Delay with External 20 kΩ RL vs. Temperature.

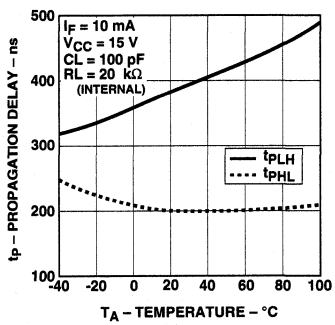


Figure 13. Propagation Delay with Internal 20 kΩ RL vs. Temperature.

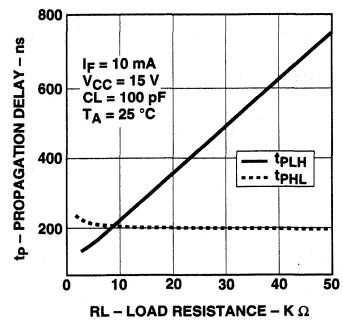


Figure 14. Propagation Delay vs. Load Resistance.

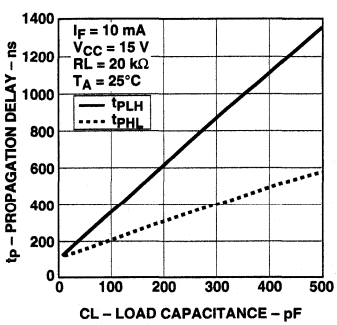


Figure 15. Propagation Delay vs. Load Capacitance.

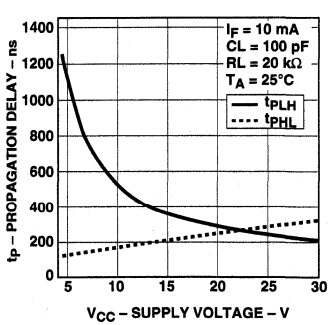


Figure 16. Propagation Delay vs. Supply Voltage.

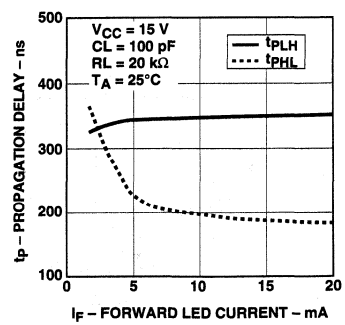
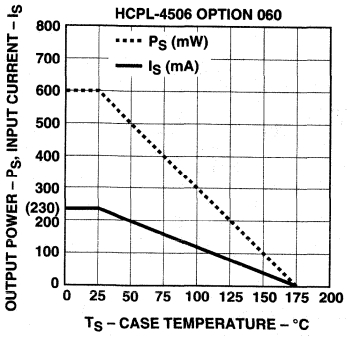


Figure 17. Propagation Delay vs. Input Current.



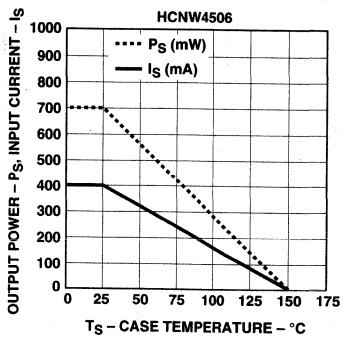


Figure 18. Thermal Derating Curve, Dependence of Safety Limiting Value with Case Temperature per VDE 0884.

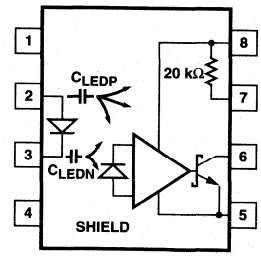


Figure 20. Optocoupler Input to Output Capacitance Model for Unshielded Optocouplers.

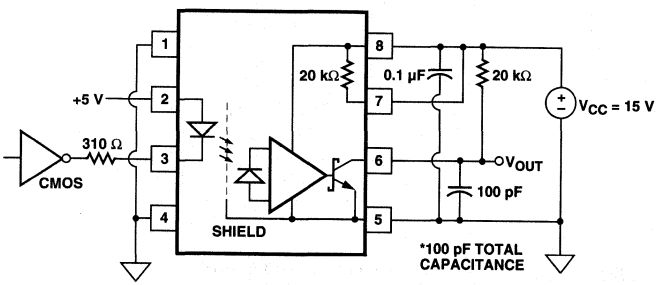


Figure 19. Recommended LED Drive Circuit.

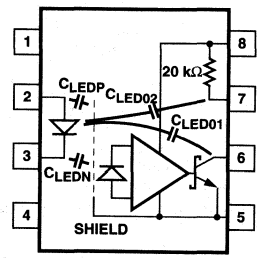


Figure 21. Optocoupler Input to Output Capacitance Model for Shielded Optocouplers.

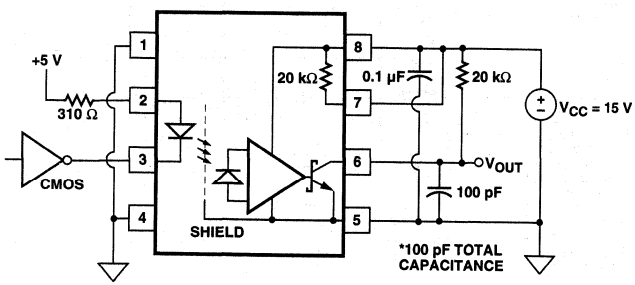


Figure 22. LED Drive Circuit with Resistor Connected to LED Anode (Not Recommended).

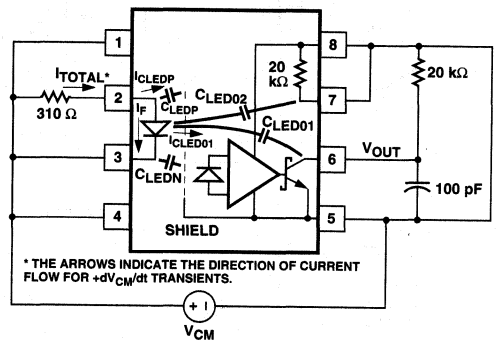


Figure 23. AC Equivalent Circuit for Figure 22 During Common Mode Transients.

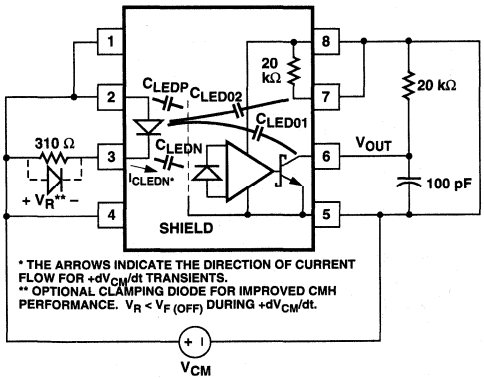


Figure 24. AC Equivalent Circuit for Figure 19 During Common Mode Transients.

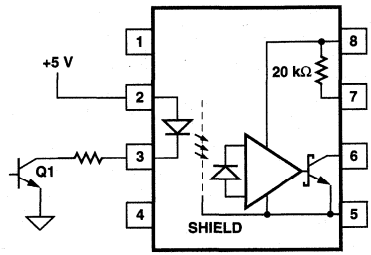


Figure 25. Not Recommended Open Collector LED Drive Circuit.

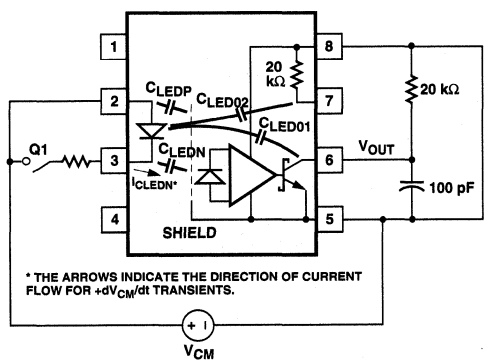


Figure 26. AC Equivalent Circuit for Figure 25 During Common Mode Transients.

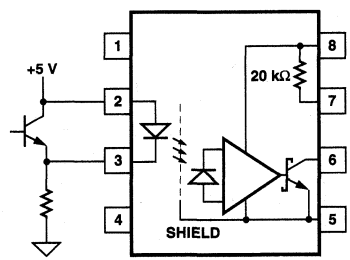


Figure 27. Recommended LED Drive Circuit for Ultra High CMR.

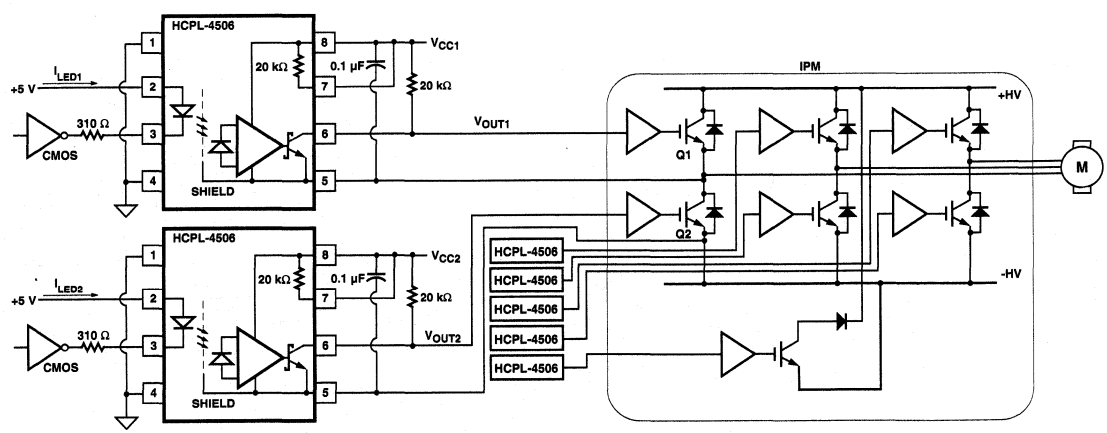


Figure 28. Typical Application Circuit.

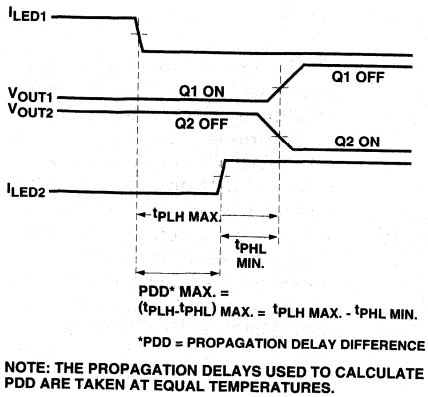


Figure 29. Minimum LED Skew for Zero Dead Time.

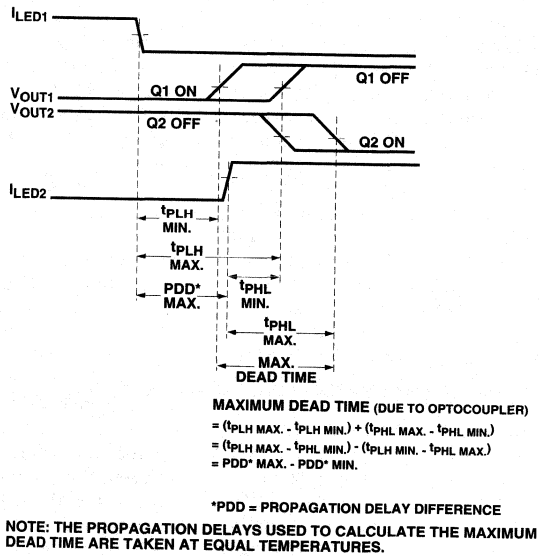


Figure 30. Waveforms for Dead Time Calculation.

LED Drive Circuit Considerations for Ultra High CMR Performance

Without a detector shield, the dominant cause of optocoupler CMR failure is capacitive coupling from the input side of the optocoupler, through the package, to the detector IC as shown in Figure 20. The HCPL-4506, HCPL-0466 and HCNW4506 improve CMR performance by using a detector IC with an optically transparent Faraday shield, which diverts the capacitively coupled current away from the sensitive IC circuitry. However, this shield does not eliminate the capacitive coupling between the LED and the optocoupler output pins and output ground as shown in Figure 21. This capacitive coupling causes perturbations in the LED current during common mode transients and becomes the major source of CMR failures for a shielded optocoupler. The main design objective of a high CMR LED drive circuit becomes keeping the LED in the proper state (on or off) during common mode transients. For example, the recommended application circuit (Figure 19), can achieve 15 kV/μs CMR while minimizing component complexity. Note that a CMOS gate is recommended in Figure 19 to keep the LED off when the gate is in the high state.

Another cause of CMR failure for a shielded optocoupler is direct coupling to the optocoupler output pins through C_{LEDO1} and C_{LEDO2} in Figure 21. Many factors influence the effect and magnitude of the direct coupling including: the use of an internal or external output pull-up resistor, the position of the LED current setting resistor, the connection of the unused input package pins, and the value of the capacitor at the optocoupler output (C_L).

Techniques to keep the LED in the proper state and minimize the effect of the direct coupling are discussed in the next two sections.

CMR with the LED On (CMR_L)

A high CMR LED drive circuit must keep the LED on during common mode transients. This is achieved by overdriving the LED current beyond the input threshold so that it is not pulled below the threshold during a transient. The recommended minimum LED current of 10 mA provides adequate margin over the maximum I_{TH} of 5.0 mA (see Figure 5) to achieve 15 kV/μs CMR. Capacitive coupling is higher when the internal load resistor is used (due to C_{LEDO2}) and an I_F = 16 mA is required to obtain 10 kV/μs CMR.

The placement of the LED current setting resistor effects the ability of the drive circuit to keep the LED on during transients and interacts with the direct coupling to the optocoupler output. For example, the LED resistor in Figure 22 is connected to the anode. Figure 23 shows the AC equivalent circuit for Figure 22 during common mode transients. During a +dVcm/dt in Figure 23, the current available at the LED anode (Itotal) is limited by the series resistor. The LED current (I_F) is reduced from its DC value by an amount equal to the current that flows through C_{LEDP} and C_{LEDO1}. The situation is made worse

because the current through C_{LEDO1} has the effect of trying to pull the output high (toward a CMR failure) at the same time the LED current is being reduced. For this reason, the recommended LED drive circuit (Figure 19) places the current setting resistor in series with the LED cathode. Figure 24 is the AC equivalent circuit for Figure 19 during common mode transients. In this case, the LED current is not reduced during a +dVcm/dt transient because the current flowing through the package capacitance is supplied by the power supply. During a -dVcm/dt transient, however, the LED current is reduced by the amount of current flowing through C_{LEDN}. But, better CMR performance is achieved since the current flowing in C_{LEDO1} during a negative transient acts to keep the output low.

Coupling to the LED and output pins is also affected by the connection of pins 1 and 4. If CMR is limited by perturbations in the LED on current, as it is for the recommended drive circuit (Figure 19), pins 1 and 4 should be connected to the input circuit common. However, if CMR performance is limited by direct coupling to the output when the LED is off, pins 1 and 4 should be left unconnected.

CMR with the LED Off (CMR_H)

A high CMR LED drive circuit must keep the LED off ($V_F \leq V_{F(OFF)}$) during common mode transients. For example, during a +dVcm/dt transient in Figure 24, the current flowing through C_{LEDN} is supplied by the parallel combination of the LED and series resistor. As long as the voltage developed across the resistor is less than $V_{F(OFF)}$ the LED will remain off and no common mode failure will occur. Even if the LED momentarily turns on, the 100 pF capacitor from pins 6-5 will keep the output from dipping below the threshold. The recommended LED drive circuit (Figure 19) provides about 10 V of margin between the lowest optocoupler output voltage and a 3 V IPM threshold during a 15 kV/μs transient with V_{CM} = 1500 V. Additional margin can be obtained by adding a diode in parallel with the resistor, as shown by the dashed line connection in Figure 24, to clamp the voltage across the LED below $V_{F(OFF)}$.

Since the open collector drive circuit, shown in Figure 25, cannot keep the LED off during a +dVcm/dt transient, it is not desirable for applications requiring ultra high CMR_H performance. Figure 26 is the AC equivalent circuit for Figure 25 during common mode transients. Essentially all the current flowing through C_{LEDN} during a +dVcm/dt transient must be supplied by the LED. CMR_H failures can occur at dV/dt rates where the current through the LED and C_{LEDN} exceeds the input threshold. Figure 27 is an alternative drive circuit which does achieve ultra high CMR performance by shunting the LED in the off state.

IPM Dead Time and Propagation Delay Specifications

The HCPL-4506, HCPL-0466 and HCNW4506 include a Propagation Delay Difference specification intended to help designers minimize "dead time" in their power inverter designs. Dead time is the time period during which both the high and low side power transistors (Q1 and Q2 in Figure 28) are off. Any overlap in Q1 and Q2 conduction will result in large currents flowing through the power devices between the high and low voltage motor rails.

To minimize dead time the designer must consider the propagation delay characteristics of the optocoupler as well as the characteristics of the IPM IGBT gate drive circuit. Considering only the delay characteristics of the optocoupler (the characteristics of the IPM IGBT gate drive circuit can be analyzed in the same way) it is important to know the minimum and maximum turn-on (t_{PHL}) and turn-off (t_{PLH}) propagation delay specifications, preferably over the desired operating temperature range.

The limiting case of zero dead time occurs when the input to Q1 turns off at the same time that the input to Q2 turns on. This case determines the minimum delay between LED1 turn-off and LED2 turn-on, which is related to the worst case optocoupler propagation delay waveforms, as shown in Figure 29. A minimum dead time of zero is achieved in Figure 29 when the signal to turn on LED2 is delayed by ($t_{PLH\ max}$ - $t_{PHL\ min}$) from the LED1 turn off. Note that the propagation delays used to calculate PDD are taken at equal temperatures since the optocouplers under consideration are typically mounted in close proximity to each other. (Specifically, $t_{PLH\ max}$ and $t_{PHL\ min}$ in the previous equation are not the same as the $t_{PLH\ max}$ and $t_{PHL\ min}$, over the full operating temperature range, specified in the data sheet.) This delay is the maximum value for the propagation delay difference specification which is specified at 450 ns for the HCPL-4506, HCPL-0466 and HCNW4506 over an operating temperature range of -40°C to 100°C.

Delaying the LED signal by the maximum propagation delay difference ensures that the minimum dead time is zero, but it does not tell a designer what the maximum dead time will be. The maximum dead time occurs in the highly unlikely case where one optocoupler with the fastest t_{PLH} and another with the slowest t_{PHL} are in the same inverter leg. The maximum dead time in this case becomes the sum of the spread in the t_{PLH} and t_{PHL} propagation delays as shown in Figure 30. The maximum dead time is also equivalent to the difference between the maximum and minimum propagation delay difference specifications. The maximum dead time (due to the optocouplers) for the HCPL-4506, HCPL-0466 and HCNW4506 is 600 ns (= 450 ns - (-150 ns)) over an operating temperature range of -40°C to 100°C.

Dual Channel, High Speed Optocouplers

Technical Data

HCPL-2530 HCPL-0530
HCPL-2531 HCPL-0531
HCPL-4534 HCPL-0534

Features

- **15 kV/µs Minimum Common Mode Transient Immunity at V_{CM} = 1500 V (HCPL-4534/0534)**
- **High Speed: 1 Mb/s**
- **TTL Compatible**
- **Available in 8 Pin DIP, SO-8, and 8 Pin DIP – Gull Wing Surface Mount (Option 020) Packages**
- **High Density Packaging**
- **3 MHz Bandwidth**
- **Open Collector Outputs**
- **Guaranteed Performance from 0°C to 70°C**
- **Safety Approval**
  UL Recognized – 2500 V rms for 1 minute (5000 V rms for 1 minute for Option 020) per UL1577
  CSA Approved
- **Single Channel Version Available (4502/3, 0452/3)**
- **MIL-STD-1772 Version Available (55XX/65XX/4N55)**

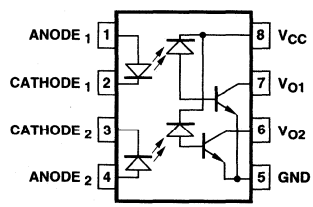
Applications

- **Line Receivers** – High Common Mode Transient Immunity (>1000 V/µs) and Low Input-Output Capacitance (0.6 pF)
- **High Speed Logic Ground Isolation** – TTL/TTL, TTL/LTTL, TTL/CMOS, TTL/LSTTL
- **Replace Pulse Transformers** – Save Board Space and Weight
- **Analog Signal Ground Isolation** – Integrated Photon Detector Provides Improved Linearity over Phototransistor Type
- **Polarity Sensing**
- **Isolated Analog Amplifier** – Dual Channel Packaging Enhances Thermal Tracking

Description

These dual channel optocouplers contain a pair of light emitting diodes and integrated photodetectors with electrical insulation between input and output. Separate connection for the photodiode bias and output transistor collectors increase the speed up to a hundred times that of a conventional phototransistor coupler by reducing the base-collector capacitance.

Functional Diagram



TRUTH TABLE (POSITIVE LOGIC)

LED	V_O
ON	LOW
OFF	HIGH

A 0.1 µF bypass capacitor between pins 5 and 8 is recommended.

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

These dual channel optocouplers are available in an 8 Pin DIP and in an industry standard SO-8 package. The following is a cross reference table listing the 8 Pin DIP part number and the electrically equivalent SO-8 part number.

8 Pin DIP	SO-8 Package
HCPL-2530	HCPL-0530
HCPL-2531	HCPL-0531
HCPL-4534	HCPL-0534

The SO-8 does not require "through holes" in a PCB. This package occupies approximately one-third the footprint area of the standard dual-in-line package. The lead profile is designed to be compatible with standard surface mount processes.

The HCPL-2530/0530 is for use in TTL/CMOS, TTL/LSTTL or wide bandwidth analog applications. Current transfer ratio (CTR) for the HCPL-2530/0530 is 7% minimum at I_F = 16 mA.

The HCPL-2531/0531 is designed for high speed TTL/TTL applications. A standard 16 mA TTL sink current through the input LED will provide enough output current for 1 TTL load and a 5.6 kΩ pull-up resistor. CTR of the HCPL-2531/0531 is 19% minimum at I_F = 16 mA.

The HCPL-4534/0534 is an HCPL-2531/0531 with increased common mode transient immunity of 15,000 V/μs minimum at V_{CM} = 1500 V guaranteed.

Selection Guide

Minimum CMR			8-pin DIP (300 Mil)		Small-Outline SO-8		Widebody (400 Mil)	Hermetic
dV/dt (V/μs)	V_{CM} (V)	Current Transfer Ratio (%)	Dual Channel Package	Single Channel Package*	Dual Channel Package	Single Channel Package*	Single Channel Package*	Single and Dual Channel Packages*
1,000	10	7	HCPL-2530	6N135	HCPL-0530	HCPL-0500	HCNW135	
		19	HCPL-2531	6N136 HCPL-4502	HCPL-0531	HCPL-0501 HCPL-0452	HCNW136 HCNW4502	
15,000	1500	19	HCPL-4534	HCPL-4503	HCPL-0534	HCPL-0453	HCNW4503	
1,000	10	9						HCPL-55XX HCPL-65XX 4N55

*Technical data for these products are on separate HP publications.

Ordering Information

Specify Part Number followed by Option Number (if desired).

Example:

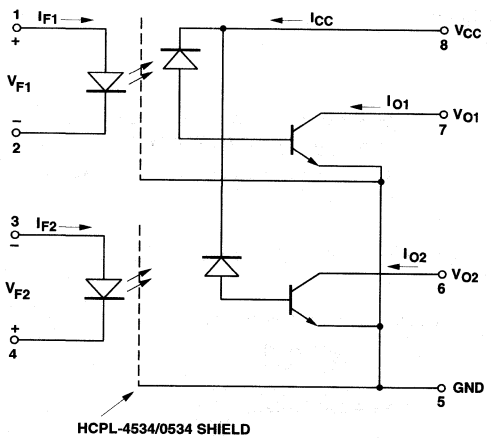
HCPL-2531#XXX

- 020 = UL 5000 V rms/1 Minute Option*
- 300 = Gull Wing Surface Mount Option†
- 500 = Tape and Reel Packaging Option

Option data sheets available. Contact your Hewlett-Packard sales representative or authorized distributor for information.

*For HCPL-2530/1 and HCPL-4534 only.
†Gull wing surface mount option applies to through hole parts only.

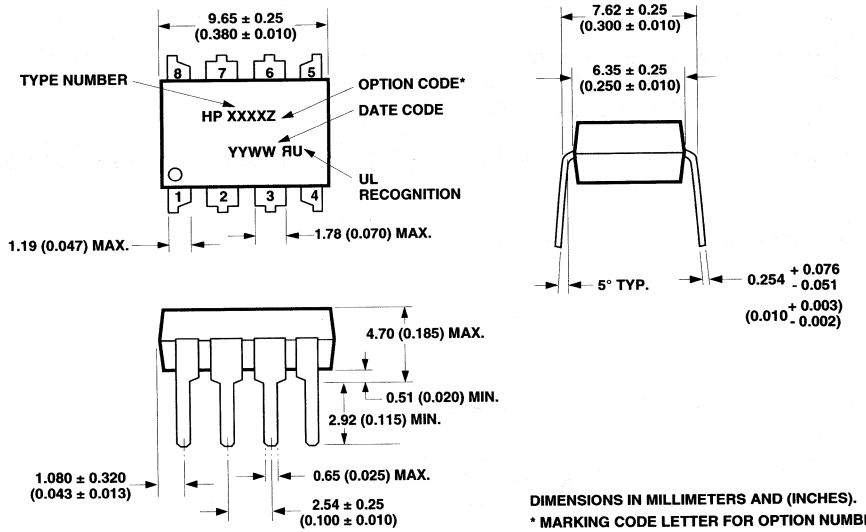
Schematic



USE OF A 0.1 µF BYPASS CAPACITOR CONNECTED BETWEEN PINS 5 AND 8 IS RECOMMENDED.

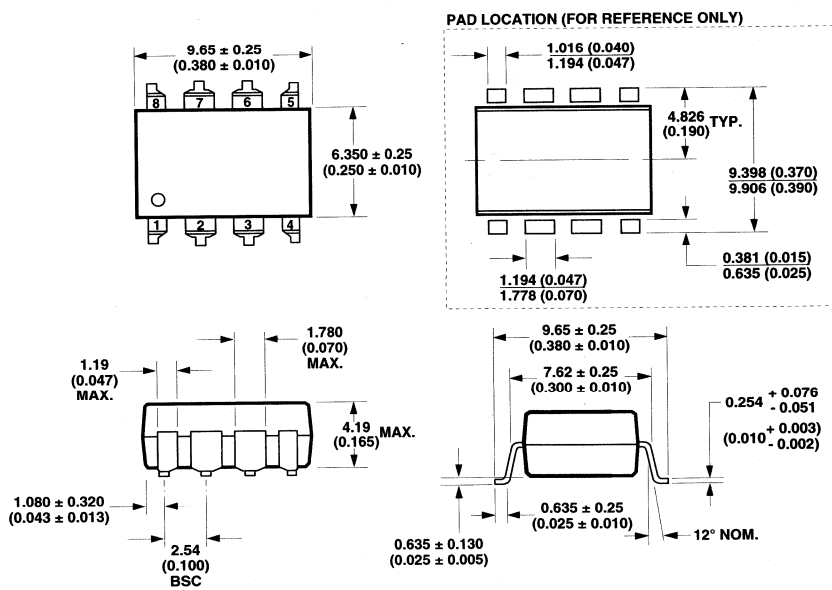
Package Outline Drawings

8-Pin DIP Package (HCPL-2530/2531/4534)



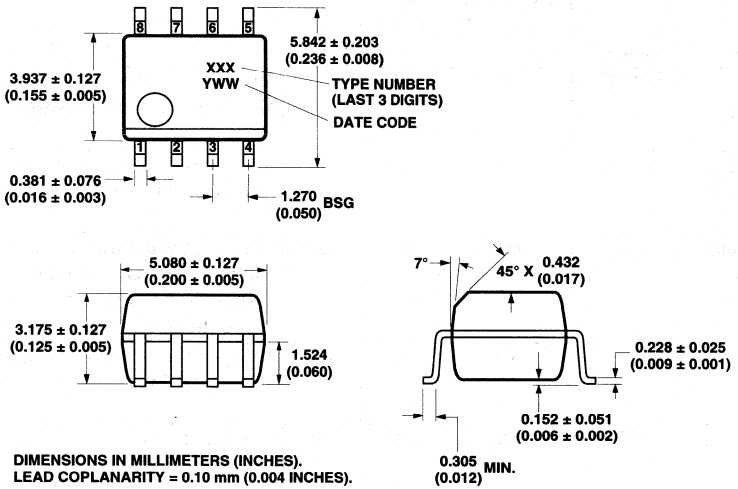
DIMENSIONS IN MILLIMETERS AND (INCHES).
* MARKING CODE LETTER FOR OPTION NUMBERS.
"L" = OPTION 020
OPTION NUMBERS 300 AND 500 NOT MARKED.

8-Pin DIP Package with Gull Wing Surface Mount Option 300 (HCPL-2530/2531/4534)

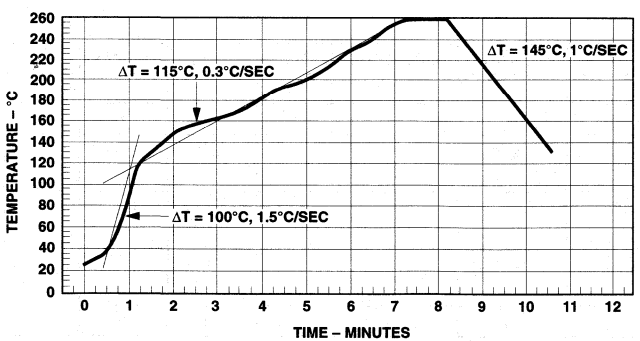


DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES).

Small Outline SO-8 Package (HCPL-0530/0531/0534)



Solder Reflow Temperature Profile (HCPL-0530/0531/0534 and Gull Wing Surface Mount Option Parts)



Note: Use of nonchlorine activiated fluxes is highly recommended.

Regulatory Information

The devices contained in this data sheet have been approved by the following organizations:

UL

Recognized under UL 1577, Component Recognition Program, File E55361.

CSA

Approved under CSA Component Acceptance Notice #5, File CA 88324.

Insulation and Safety Related Specifications

Parameter	Symbol	8-Pin DIP (300 Mil) Value	SO-8 Value	Units	Conditions
Minimum External Air Gap (External Clearance)	L(101)	7.1	4.9	mm	Measured from input terminals to output to to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L(102)	7.4	4.8	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	0.08	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity.
Minimum Internal Tracking (Internal Creepage)		NA	NA	mm	Measured from input terminals to output terminals, along internal cavity.
Tracking Resistance (Comparative Tracking Index)	CTI	200	200	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa	IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Option 300 - surface mount classification is Class A in accordance with CECC 00802.

Absolute Maximum Ratings

Parameter	Symbol	Device	Min.	Max.	Units	Note
Storage Temperature	T_S		-55	125	°C	
Operating Temperature	T_A		-55	100	°C	
Average Forward Input Current (each channel)	$I_{F(AVG)}$			25	mA	
Peak Forward Input Current (each channel) (50% duty cycle, 1 ms pulse width)	$I_{F(PEAK)}$			50	mA	
Peak Transient Input Current (each channel) (≤ 1 µs pulse width, 300 pps)	$I_{F(TRANS)}$			1	A	
Reverse LED Input Voltage (each channel)	V_R			5	V	
Input Power Dissipation (each channel)	P_{IN}			45	mW	
Average Output Current (each channel)	$I_{O(AVG)}$			8	mA	
Peak Output Current	$I_{O(PEAK)}$			16	mA	
Supply Voltage (Pin 8-5)	V_{CC}		-0.5	30	V	
Output Voltage (Pins 7-5, 6-5)	V_O		-0.5	20	V	
Output Power Dissipation (each channel)	P_O			35	mW	13
Lead Solder Temperature (Through-Hole Parts Only) 1.6 mm below seating plane, 10 seconds	T_{LS}	8 Pin DIP		260	°C	
Reflow Temperature Profile	T_{RP}	SO-8 and Option 300	See **Package Outline Drawings** section			

Electrical Specifications (DC)

Over recommended temperature (T_A = 0°C to 70°C) unless otherwise specified. See note 9.

Parameter	Sym.	Device	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR	HCPL-2530/ 0530	7	18	50	%	T_A = 25°C; I_F = 16 mA, V_{CC} = 4.5 V, V_O = 0.5 V	1, 2 4	1, 2
			5						
		HCPL-2531/ 0531 HCPL-4534/ 0534	19	24	50	%	T_A = 25°C		
			15						
Logic Low Output Voltage	V_{OL}	HCPL-2530/ 0530		0.1	0.5	V	T_A = 25°C; I_O = 1.1 mA; I_F = 16 mA, V_{CC} = 4.5 V	1	1
					0.5		I_O = 0.8 mA		
		HCPL-2531/ 0531 HCPL-4534/ 0534		0.1	0.5	V	T_A = 25°C; I_O = 3.0 mA		
					0.5		I_O = 2.4 mA		
Logic High Output Current	I_{OH}			0.003	0.5	µA	T_A = 25°C; V_O = Open, V_{CC} = 5.5 V; I_F = 0 mA	6	1
					50		V_O = Open, V_{CC} = 15.0 V		
Logic Low Supply Current	I_{CCL}			100	400	µA	I_F = 16 mA, V_O = Open, V_{CC} = 15 V		
Logic High Supply Current	I_{CCH}			0.05	4	µA	I_F = 0 mA, V_O = Open, V_{CC} = 15 V		
Input Forward Voltage	V_F			1.5	1.7	V	T_A = 25°C; I_F = 16 mA	3	1
					1.8				
Input Reverse Breakdown Voltage	BV_R		5			V	I_R = 10 µA		1
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			-1.6		mV/ °C	I_F = 16 mA		
Input Capacitance	C_{IN}			60		pF	f = 1 MHz, V_F = 0 V	1	

*All typicals at T_A = 25°C.

Switching Specifications (AC)

Over recommended temperature (T_A = 0°C to 70°C), V_{CC} = 5 V, I_F = 16 mA unless otherwise specified.

Parameter	Sym.	Device HCPL-	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to Logic Low at Output	t_{PHL}	2530/0530		0.2	1.5	µs	T_A = 25°C, R_L = 4.1 kΩ	5, 9, 11	6, 7
					2.0				
		2531/0531/ 4534/0534		0.2	0.8		T_A = 25°C, R_L = 1.9 kΩ		
					1.0				
Propagation Delay Time High to Logic at Output	t_{PLH}	2530/0530		1.3	1.5	µs	T_A = 25°C, R_L = 4.1 kΩ	5, 9, 11	6, 7
					2.0				
		2531/0531/ 4534/0534		0.6	0.8		T_A = 25°C, R_L = 1.9 kΩ		
					1.0				
Common Mode Transient Immunity at Logic High Level Output	$\|CM_H\|$	2530/0530	1	10		kV/µs	R_L = 4.1 kΩ, I_F = 0 mA,	10	5, 6, 7
		2531/0531	1	10			R_L = 1.9 kΩ, T_A = 25°C,		
		4534/0534	15	30			R_L = 1.9 kΩ, V_{CM} = 10 V_{p-p}		
Common Mode Transient Immunity at Logic Low Level Output	$\|CM_L\|$	2530/0530	1	10		kV/µs	R_L = 4.1 kΩ, I_F = 0 mA,	10	5, 6, 7
		2531/0531	1	10			R_L = 1.9 kΩ, T_A = 25°C,		
		4534/0534	15	30			R_L = 1.9 kΩ, V_{CM} = 10 V_{p-p}		
Bandwidth	BW			3		MHz	R_L = 100 kΩ	7, 8	

*All typicals at T_A = 25°C.

Package Characteristics

Parameter	Sym.	Device	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage**	V_{ISO}		2500			V rms	RH < 50%, t = 1 min.,		3, 10
		HCPL-2530/ 2531/4534 Option 020	5000						3, 11
Resistance (Input-Output)	R_{I-O}			10^{12}		Ω	RH ≤ 45% V_{I-O} = 500 Vdc, t = 5 s		3
Capacitance (Input-Output)	C_{I-O}			0.6		pF	f = 1 MHz, T_A = 25°C		12
Input-Input Insulation Leakage Current	I_{I-I}			0.005		µA	RH ≤ 45%, t = 5 s, V_{I-I} = 500 Vdc		4
Resistance (Input-Input)	R_{I-I}			10^{11}		Ω			4
Capacitance (Input-Input)	C_{I-I}	HCPL-2530/ 2531/4534		0.03		pF	f = 1 MHz		4
		HCPL-0530/ 0531/0534		0.25					

*All typicals at T_A = 25°C.

**The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the VDE 0884 Insulation Characteristics Table (if applicable), your equipment level safety specification or HP Application Note 1074 entitled "Optocoupler Input-Output Endurance Voltage," publication number 5963-2203E.

Notes:

1. Each channel.
2. CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
3. Device considered a two-terminal device: pins 1, 2, 3, and 4 shorted together and pins 5, 6, 7, and 8 shorted together.
4. Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.
5. Common mode transient immunity in a Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the rising edge of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (i.e., $V_O > 2.0$ V). Common mode transient immunity in a Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the falling edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., $V_O < 0.8$ V).
6. The 1.9 kΩ load represents 1 TTL unit load of 1.6 mA and the 5.6 kΩ pull-up resistor.
7. The 4.1 kΩ load represents 1 LSTTL unit load of 0.36 mA and the 6.1 kΩ pull-up resistor.
8. The frequency at which the ac output voltage is 3 dB below the low frequency asymptote.
9. Use of a 0.1 μF bypass capacitor connected between pins 5 and 8 is recommended.
10. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 3000 V rms for 1 second (leakage detection current limit, $I_{I-O} \leq 5$ μA).
11. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 6000 V rms for 1 second (leakage detection current limit, $I_{I-O} \leq 5$ μA).
12. Measured between the LED anode and cathode shorted together and pins 5 through 8 shorted together.
13. Derate linearly above 90°C free-air temperature at a rate of 3.0 mW/°C for the SOIC-8 package.

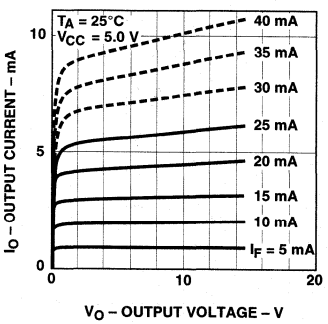


Figure 1. DC and Pulsed Transfer Characteristics.

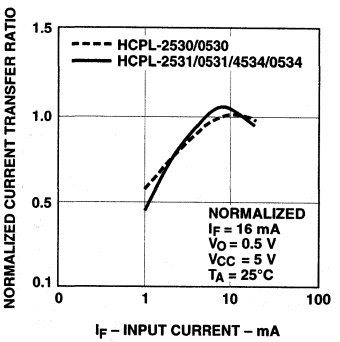


Figure 2. Current Transfer Ratio vs. Input Current.

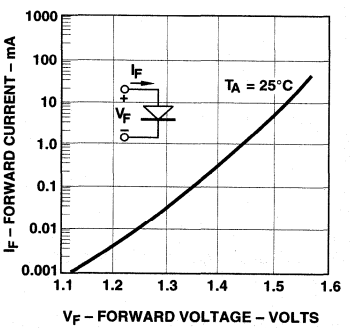


Figure 3. Input Current vs. Forward Voltage.

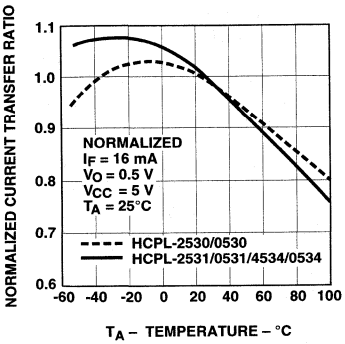


Figure 4. Current Transfer Ratio vs. Temperature.

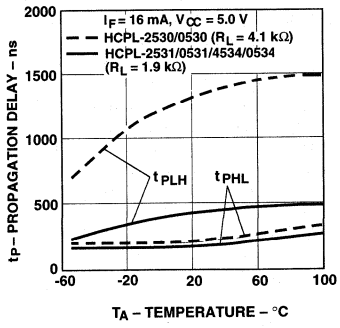


Figure 5. Propagation Delay vs. Temperature.

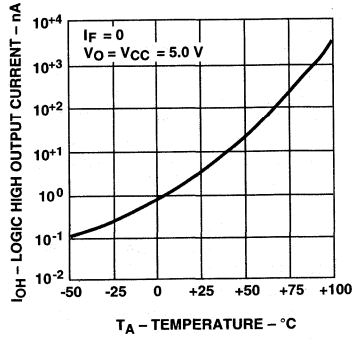


Figure 6. Logic High Output Current vs. Temperature.

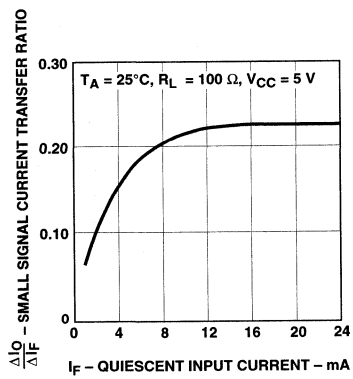


Figure 7. Small-Signal Current Transfer Ratio vs. Quiescent Input Current.

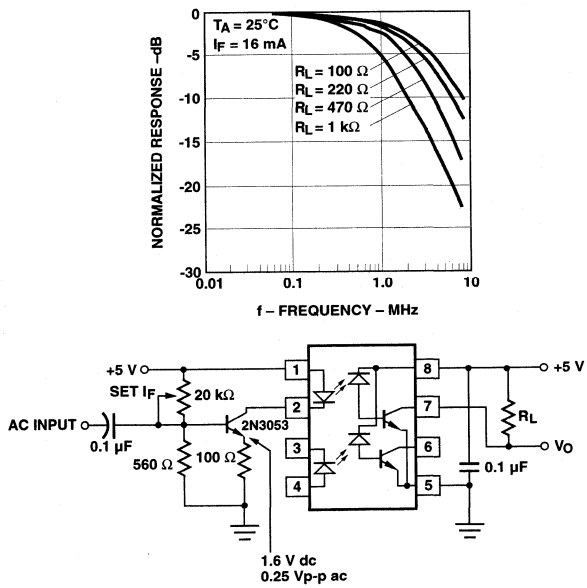


Figure 8. Frequency Response.

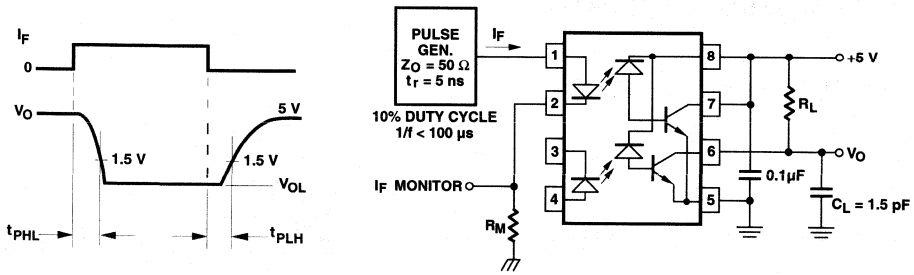


Figure 9. Switching Test Circuit.

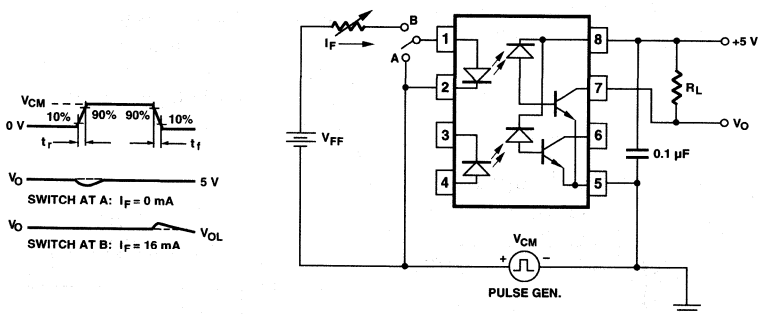


Figure 10. Test Circuit for Transient Immunity and Typical Waveforms.

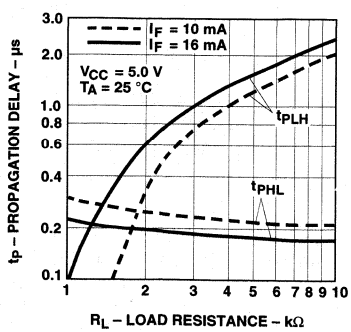


Figure 11. Propagation Delay Time vs. Load Resistance.

HEWLETT® PACKARD

Bi-Directional High Speed Optocouplers

Preliminary Technical Data

HCPL-0560
HCPL-0561

Features

- **SOIC-8 Package**
- **Available in**
  V_{CC} Common: HCPL-0560
  GND Common: HCPL-0561
- **High Speed: 1 Mbd**
- **TTL Compatible**
- **Open Collector Output**
- **0°C to 70°C Performance Guaranteed**
- **Safety Approval**
  UL Recognized per UL 1577 for 2500 Vrms/1min.
  CSA Approved

Applications

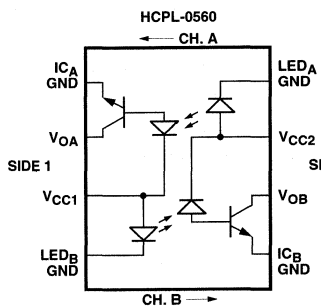
- **Full Duplex Communication**
- **Data Communication Transmit/Receive**
- **Bi-directional Communication**
- **PLC I/O Interface**
- **Industrial Standard Data Interface: RS232C**
- **Industrial Controls**
- **Remote/Isolation Sensing**

Description

These bidirectional dual channel optocouplers, packaged in the industry standard SOIC-8 package, provide full bidirectional isolated communication in a compact, surface mount footprint.

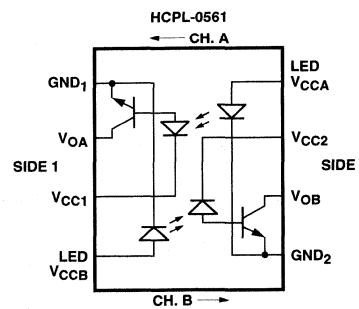
Each device contains two pairs of light emitting diodes and integrated photodetectors with electrical insulation. Separate photodiode bias and collector output transistor connections reduce the base-collector capacitance and increase speed by a hundred times over that of a conventional photo-transistor coupler.

Functional Diagram



TRUTH TABLE

LED	V_O
ON	LOW
OFF	HIGH



TRUTH TABLE

LED	V_O
ON	LOW
OFF	HIGH

A 0.1 µF bypass capacitor must be connected between pins 5 and 8.

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

This data sheet represents the latest information at the time of publication of this catalog. All specifications subject to change. Samples available Fall 1996.

The HCPL-0560 is in a V_{CC} common configuration, with the anodes of the LEDs connected to V_{CC}.

The HCPL-0561 is a GND common configuration where the two isolated grounds are common on each side of the optocoupler.

All AC and DC electrical parameters are identical for both configurations. Each has a minimum CTR of 15% over temperature (0-70°C), and a maximum propagation delay of 1 µsec. Minimum common mode transient immunity of 1kV/µs is also guaranteed at a V_{CM} of 10 Vp-p at room temperature.

Selection Guide

Common Type	Small-Outline SO-8 Bi-Directional Channel	Data Rate (baud)	Recommended I_F On-Current (mA)	Minimum CTR (%)	Electrical Equivalent 8-pin DIP Single Channel
V_{cc} Common	HCPL-0560	1M	16	15	HCPL-4502
GND Common	HCPL-0561				

Ordering Information

Specify Part Number followed by Option Number (if desired)

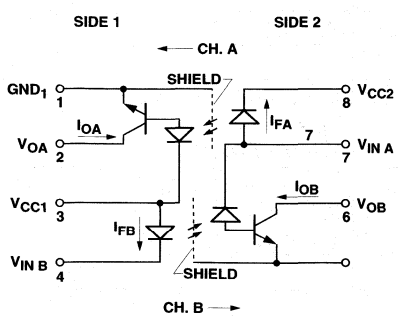
Example

HCPL-0560#XXX

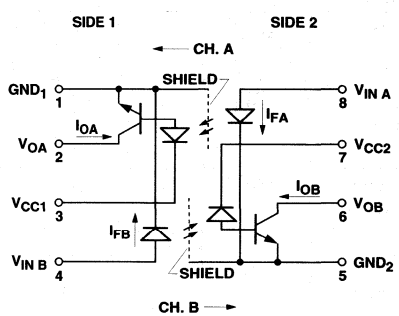
- No Option = 100 per tube.
- 500 = Tape and Reel Packaging Option, 1000 per reel.

Option data sheets available. Contact Hewlett-Packard sales representative or authorized distributor for information.

Schematic



HCPL-0560 V_{CC} COMMON



HCPL-0561 GND COMMON

Preliminary Electrical Specifications

Over recommended temperature (T_A = 0°C to 70°C) unless otherwise specified. All typical values at T_A = 25°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Current Transfer Ratio	CTR	19	24	55	%	T_A = 25°C, I_F = 16 mA, V_{CC} = 4.5 V, V_O = 0.5 V
		15				
Logic Low Output Voltage	V_{OL}		0.1	0.5	V	T_A = 25°C, I_O = 3 mA, I_F = 16 mA
				0.5		I_O = 2.4 mA, V_{CC} = 4.5 V
Logic High Output Current	I_{OH}		0.003	0.5	µA	T_A = 25°C, V_{CC} = 5.5 V, I_F = 0 mA
				50		V_{CC} = 15 V, V_O = Open
Logic Low Supply Current	I_{CCL}		100	400	µA	I_F = 16 mA, V_O = Open, V_{CC} = 15 V
Logic High Supply Current	I_{CCH}		0.05	4	µA	I_F = 0 mA, V_O = Open, V_{CC} = 15 V
Input Forward Voltage	V_F		1.5	1.7	V	T_A = 25°C, I_F = 16 mA
				1.8		
Input Reverse Breakdown Voltage	BV_R	5			V	I_R = 10 µA
Temperature Coefficient of Forward Voltage	$\Delta V_F / \Delta T_A$		-1.6		mV/°C	I_F = 16 mA
Input Capacitance	C_{IN}		60		pF	f = 1 MHz, V_F = 0 V

Preliminary Switching Specifications (AC)

Over recommended operating conditions (T_A = 0 to 70°C), V_{CC} = 5 V, I_F = 16 mA unless otherwise specified. All typical values at T_A = 25°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Propagation Delay Time to Logic Low at Output	t_{PHL}		0.2	0.85	µs	T_A = 25°C, R_L = 1.9 kΩ
				1		
Propagation Delay Time to Logic High at Output	t_{PLH}		0.6	0.85	µs	T_A = 25°C, R_L = 1.9 kΩ
				1.0		
Common Mode Transient Immunity at Logic High Output	$\|CM_H\|$	1	10		kV/µs	I_F = 0 mA, T_A = 25°C, R_L = 1.9 kΩ, V_{CM} = 10 Vp-p
Common Mode Transient Immunity at Logic Low Output	$\|CM_L\|$	1	10		kV/µs	I_F = 16 mA, T_A = 25°C, R_L = 1.9 kΩ, V_{CM} = 10 Vp-p
Bandwidth	BW			3	MHz	

Low Input Current, High Gain Optocouplers

Technical Data

6N139 6N138
HCPL-0701 HCPL-0700
HCNW139 HCNW138

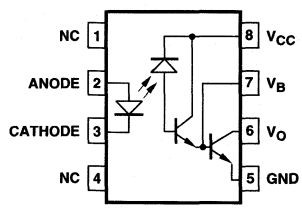
Features

- **High Current Transfer Ratio – 2000% Typical (4500% Typical for HCNW139/138)**
- **Low Input Current Requirements – 0.5 mA**
- **TTL Compatible Output – 0.1 V V_{OL} Typical**
- **Performance Guaranteed over Temperature 0°C to 70°C**
- **Base Access Allows Gain Bandwidth Adjustment**
- **High Output Current – 60 mA**
- **Safety Approval**
  UL Recognized – 2500 V rms for 1 Minute and 5000 V rms* for 1 Minute per UL 1577
  CSA Approved
  VDE 0884 Approved with V_{IORM} = 1414 V peak for HCNW139 and HCNW138
  BSI Certified (HCNW139 and HCNW138)
- **Available in 8-Pin DIP or SOIC-8 Footprint or Widebody Package**
- **MIL-STD-1772 Version Available (HCPL-5700/1)**

Applications

- **Ground Isolate Most Logic Families – TTL/TTL, CMOS/TTL, CMOS/CMOS, LSTTL/TTL, CMOS/LSTTL**
- **Low Input Current Line Receiver**
- **High Voltage Insulation (HCNW139/138)**
- **EIA RS-232C Line Receiver**
- **Telephone Ring Detector**
- **117 V ac Line Voltage Status Indicator – Low Input Power Dissipation**
- **Low Power Systems – Ground Isolation**

Functional Diagram



TRUTH TABLE

LED	V_O
ON	LOW
OFF	HIGH

Description

These high gain series couplers use a Light Emitting Diode and an integrated high gain photodetector to provide extremely high current transfer ratio between input and output. Separate pins for the photodiode and output stage result in TTL compatible saturation voltages and high speed operation. Where desired the V_{CC} and V_O terminals may be tied together to achieve conventional photodarlington operation. A base access terminal allows a gain bandwidth adjustment to be made.

*5000 V rms/1 minute rating is for HCNW139/138 and Option 020 (6N139/138) products only.
A 0.1 µF bypass capacitor connected between pins 8 and 5 is recommended.

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

The 6N139, HCPL-0701, and CNW139 are for use in CMOS, LSTTL or other low power applications. A 400% minimum current transfer ratio is guaranteed over 0 to 70°C operating range for only 0.5 mA of LED current.

The 6N138, HCPL-0700, and HCNW138 are designed for use mainly in TTL applications. Current Transfer Ratio (CTR) is 300% minimum over 0 to 70°C for an LED current of 1.6 mA (1 TTL Unit load). A 300% minimum CTR enables operation with 1 TTL Load using a 2.2 kΩ pull-up resistor.

Selection for lower input current down to 250 μA is available upon request.

The HCPL-0701 and HCPL-0700 are surface mount devices packaged in an industry standard SOIC-8 footprint.

The SOIC-8 does not require "through holes" in a PCB. This package occupies approximately one-third the footprint area of the standard dual-in-line package. The lead profile is designed to be compatible with standard surface mount processes.

The HCNW139 and HCNW138 are packaged in a widebody encapsulation that provides creepage and clearance dimensions suitable for safety approval by regulatory agencies worldwide.

Selection Guide

8-Pin DIP (300 Mil)		Small Outline SO-8		Widebody Package (400 mil)				Hermetic
Single Channel Package	Dual Channel Package HCPL-	Single Channel Package HCPL-	Dual Channel Package HCPL-	Single Channel Package	Minimum Input ON Current (I_F)	Minimum CTR	Absolute Maximum V_{CC}	Single and Dual Channel Packages HCPL-
6N139	2731[1]	0701	0731	HCNW139	0.5 mA	400%	18 V	
6N138	2730[1]	0700	0730	HCNW138	1.6 mA	300%	7 V	
HCPL-4701[1]	4731[1]	070A[1]	073A[1]		40 μA	800%	18 V	
					0.5 mA	300%	20 V	5701[1] 5700[1] 5731[1] 5730[1]

Note:
1. Technical data are on separate HP publications.

Ordering Information

Specify Part Number followed by Option Number (if desired).

Example:

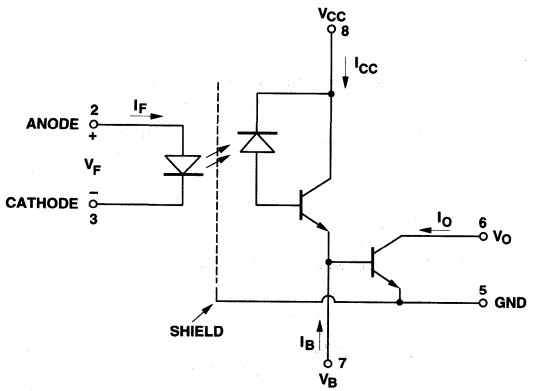
6N139#XXX

- 020 = 5000 V rms/1 Minute UL Rating Option*
- 300 = Gull Wing Surface Mount Option†
- 500 = Tape and Reel Packaging Option

Option data sheets available. Contact your Hewlett-Packard sales representative or authorized distributor for information.

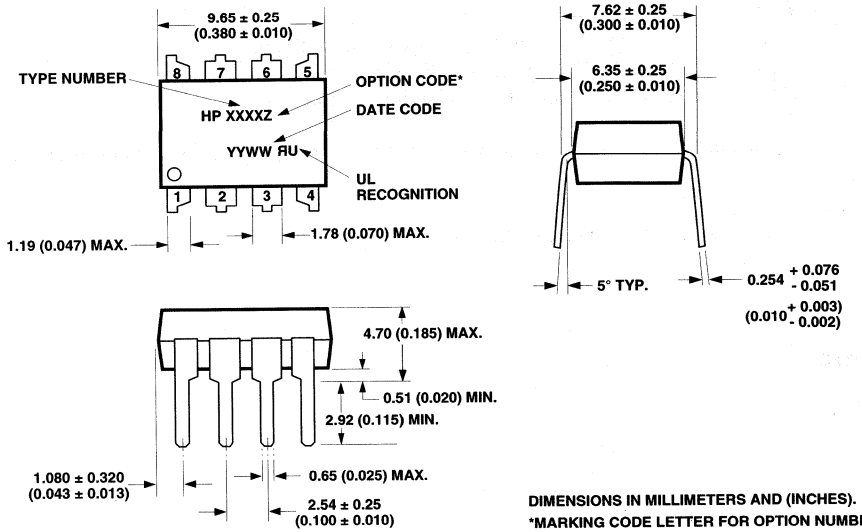
*For 6N139 and 6N138 only.
†Gull wing surface mount option applies to through hole parts only.

Schematic



Package Outline Drawings

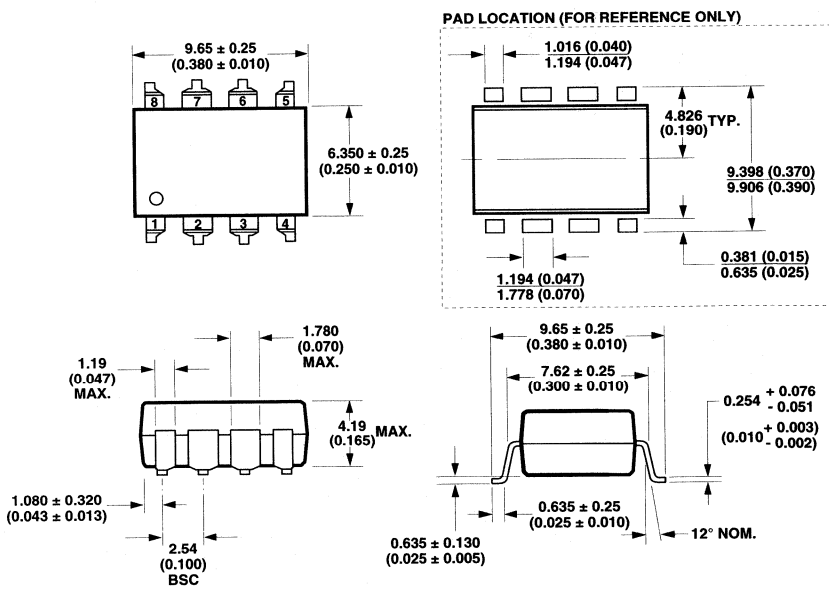
8-Pin DIP Package (6N139/6N138)**



DIMENSIONS IN MILLIMETERS AND (INCHES).
*MARKING CODE LETTER FOR OPTION NUMBERS
"L" = OPTION 020
OPTION NUMBERS 300 AND 500 NOT MARKED.

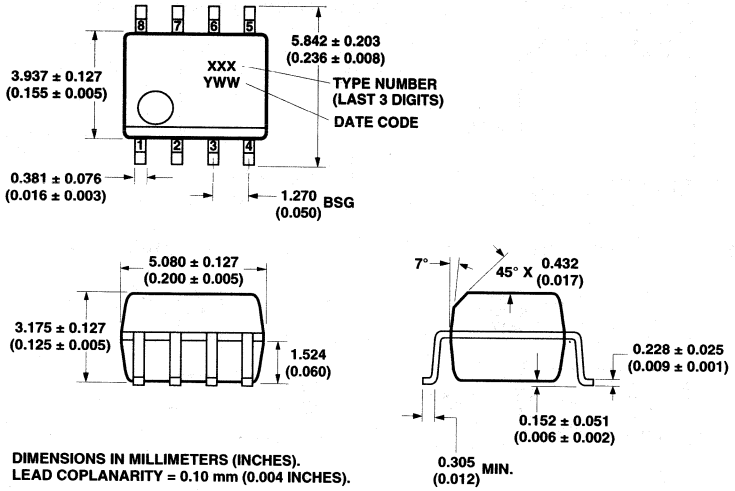
**JEDEC Registered Data.

8-Pin DIP Package with Gull Wing Surface Mount Option 300 (6N139/6N138)



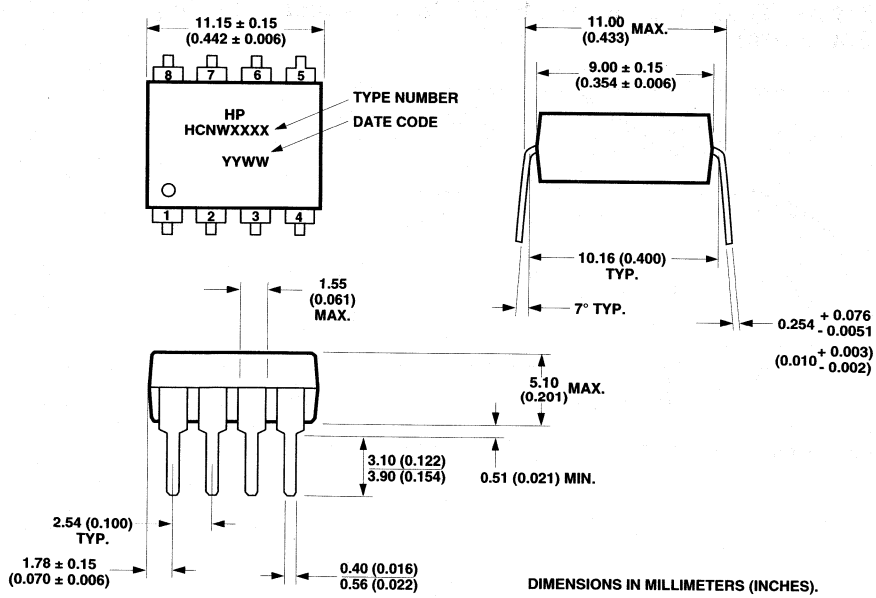
DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES).

Small Outline SO-8 Package (HCPL-0701/HCPL-0700)



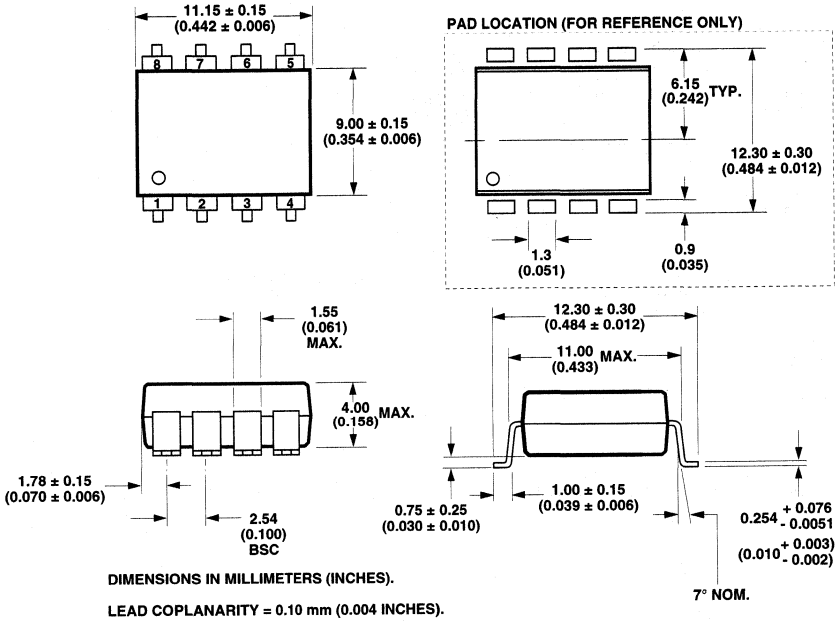
DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES).

8-Pin Widebody DIP Package (HCNW139/HCNW138)

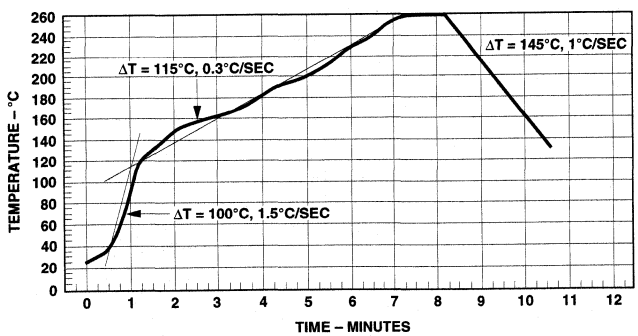


DIMENSIONS IN MILLIMETERS (INCHES).

8-Pin Widebody DIP Package with Gull Wing Surface Mount Option 300 (HCNW139/HCNW138)



Solder Reflow Temperature Profile (HCPL-07XX and Gull Wing Surface Mount Option 300 Parts)



Note: Use of nonchlorine activated fluxes is highly recommended.

Regulatory Information

The 6N139/138, HCNW139/138, and HCPL-0701/0700 have been approved by the following organizations:

UL

Recognized under UL 1577, Component Recognition Program, File E55361.

CSA

Approved under CSA Component Acceptance Notice #5, File CA 88324.

VDE

Approved according to VDE 0884/ 06.92 (HCNW139/138 only).

BSI

Certification according to BS415:1994, (BS EN60065:1994); BS EN60950:1992 (BS7002:1992) and EN41003:1993 for Class II applications (HCNW139/ HCNW138 only.)

Insulation and Safety Related Specifications

Parameter	Symbol	8-Pin DIP (300 Mil) Value	SO-8 Value	Widebody (400 Mil) Value	Units	Conditions
Minimum External Air Gap (External Clearance)	L(101)	7.1	4.9	9.6	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L(102)	7.4	4.8	10.0	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	0.08	1.0	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity.
Minimum Internal Tracking (Internal Creepage)		NA	NA	4.0	mm	Measured from input terminals to output terminals, along internal cavity.
Tracking Resistance (Comparative Tracking Index)	CTI	200	200	200	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa	IIIa	IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Option 300 - surface mount classification is Class A in accordance with CECC 00802.

VDE 0884 Insulation Related Characteristics (HCNW139 and HCNW138)

Description	Symbol	Characteristic	Units
Installation Classification per DIN VDE 0110/1.89, Table 1 for rated mains voltage ≤ 600 V rms		I-IV	
for rated mains voltage ≤ 1000 V rms		I-III	
Climatic Classification		55/100/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	1414	V peak
Input to Output Test Voltage, Method b* V_{PR} = 1.875 x V_{IORM}, 100% Production Test with t_P = 1 sec, Partial Discharge < 5 pC	V_{PR}	2652	V peak
Input to Output Test Voltage, Method a* V_{PR} = 1.5 x V_{IORM}, Type and Sample Test, t_P = 60 sec, Partial Discharge < 5 pC	V_{PR}	2121	V peak
Highest Allowable Overvoltage* (Transient Overvoltage, t_{ini} = 10 sec)	V_{IOTM}	8000	V peak
Safety Limiting Values (Maximum values allowed in the event of a failure, also see Figure 11, Thermal Derating curve.)			
Case Temperature	T_S	175	°C
Current (Input Current I_F, P_S = 0)	$I_{S,INPUT}$	400	mA
Output Power	$P_{S,OUTPUT}$	700	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	> 10^9	Ω

*Refer to the front of the optocoupler section of the current catalog, under Product Safety Regulations section, (VDE 0884) for a detailed description.

Note: Isolation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuits in application.

Absolute Maximum Ratings* (No Derating Required up to 85°C)

Parameter	Symbol	Min.	Max.	Units
Storage Temperature	T_S	-55	125	°C
Operating Temperature**	T_A	-40	85	°C
Average Forward Input Current	$I_{F(AVG)}$		20	mA
Peak Forward Input Current (50% Duty Cycle, 1 ms Pulse Width)	I_{FPK}		40	mA
Peak Transient Input Current (<1 µs Pulse Width, 300 pps)	$I_{F(TRAN)}$		1.0	A
Reverse Input Voltage	V_R		5	V
HCNW139/138			3	V
Input Power Dissipation	P_I		35	mW
Output Current (Pin 6)	I_O		60	mA
Emitter Base Reverse Voltage (Pin 5-7)	V_{EB}		0.5	V
Supply Voltage and Output Voltage (6N139, HCPL-0701, HCNW139)	V_{CC}	-0.5	18	V
Supply Voltage and Output Voltage (6N138, HCPL-0700, HCNW138)	V_{CC}	-0.5	7	V
Output Power Dissipation	P_O		100	mW
Total Power Dissipation	P_T		135	mW
Lead Solder Temperature (for Through Hole Devices)	260°C for 10 sec., 1.6 mm below seating plane			
HCNW139/138	260°C for 10 sec., up to seating plane			
Reflow Temperature Profile (for SOIC-8 and Option #300)	See Package Outline Drawings section			

*JEDEC Registered Data for 6N139 and 6N138.
**0°C to 70°C on JEDEC Registration.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage	V_{CC}	4.5	18	V
Forward Input Current (ON)	$I_{F(ON)}$	0.5	12.0	mA
Forward Input Voltage (OFF)	$V_{F(OFF)}$	0	0.8	V
Operating Temperature	T_A	0	70	°C

Electrical Specifications

$0°C \le T_A \le 70°C$, $4.5\ V \le V_{CC} \le 18\ V$, $0.5\ mA \le I_{F(ON)} \le 12\ mA$, $0\ V \le V_{F(OFF)} \le 0.8\ V$, unless otherwise specified. All Typicals at $T_A = 25°C$. See Note 7.

Parameter	Sym.	Device	Min.	Typ.**	Max.	Units	Test Conditions		Fig.	Note
Current Transfer Ratio	CTR	6N139 HCPL-0701	400*	2000	5000	%	$I_F = 0.5\ mA$	$V_{CC} = 4.5$ $V_O = 0.4\ V$	2, 3	1, 2, 4
		HCNW139	400	4500						
		6N139 HCPL-0701	500*	1600	2600		$I_F = 1.6\ mA$			
		HCNW139	500	3000						
			300	1600			$I_F = 5.0\ mA$			
			200	850			$I_F = 12\ mA$			
		6N138 HCPL-0700	300*	1600	2600		$I_F = 1.6\ mA$			
		HCNW138		1500						
Logic Low Output Voltage	V_{OL}	6N139 HCPL-0701 HCNW139		0.1	0.4	V	$I_F = 0.5\ mA$, $I_O = 2\ mA$	$V_{CC} = 4.5$	1	2
							$I_F = 1.6\ mA$, $I_O = 8\ mA$			
							$I_F = 5.0\ mA$, $I_O = 15\ mA$			
				0.2			$I_F = 12\ mA$, $I_O = 24\ mA$			
		6N138 HCPL-0700 HCNW138		0.1			$I_F = 1.6\ mA$, $I_O = 4.8\ mA$			
Logic High Output Current	I_{OH}	6N139 HCPL-0701 HCNW139		0.05	100	µA	$V_O = V_{CC} = 18\ V$	$I_F = 0\ mA$		2
		6N138 HCPL-0700 HCNW138		0.1	250		$V_O = V_{CC} = 7\ V$			
Logic Low Supply Current	I_{CCL}	6N138/139 HCPL-0701/ 0700		0.4	1.5	mA	$I_F = 1.6\ mA$, V_O = Open, $V_{CC} = 18\ V$		10	2
		HCNW139 HCNW138		0.5	2					
Logic High Supply Current	I_{CCH}	6N138/139 HCPL-0701/ 0700		0.01	10	µA	$I_F = 0\ mA$, V_O = Open, $V_{CC} = 18\ V$			2
		HCNW139 HCNW138			1					
Input Forward Voltage	V_F	6N138 6N139	1.25	1.40	1.7*	V	$T_A = 25°C$	$I_F = 1.6\ mA$	4, 8	
		HCPL-0701 HCPL-0700			1.75					
		HCNW139 HCNW138	1.0	1.45	1.85		$T_A = 25°C$			
			0.95		1.95					
Input Reverse Breakdown Voltage	BVR		5.0*			V	$I_R = 10\ µA$, $T_A = 25°C$			
		HCNW139 HCNW138	3.0				$I_R = 100\ µA$, $T_A = 25°C$			
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			-1.8		mV/°C	$I_F = 1.6\ mA$		8	
Input Capacitance	C_{IN}			60		pF	f = 1 MHz, $V_F = 0\ V$			
		HCNW139 HCNW138		90						

*JEDEC Registered Data for 6N139 and 6N138.

**All typical values at $T_A = 25°C$ and $V_{CC} = 5\ V$, unless otherwise noted.

Switching Specifications (AC)

Over recommended operating conditions (T_A = 0 to 70°C), V_{CC} = 5 V, unless otherwise specified.

Parameter	Sym.	Device	Min.	Typ.**	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to Logic Low at Output	t_{PHL}	6N139 HCPL-0701 HCNW139		5	25* 30	µs	T_A = 25°C I_F = 0.5 mA, Rl = 4.7 kΩ	5, 6, 7, 9, 12	2, 4
		6N139 HCPL-0701 HCNW139		0.2	1* 2 1.1	µs	T_A = 25°C I_F = 12 mA, Rl = 270 Ω		
		6N138 HCPL-0700 HCNW138		1.6	10* 15 11	µs	T_A = 25°C I_F = 1.6 mA, Rl = 2.2 kΩ		
Propagation Delay Time to Logic High at Output	t_{PLH}	6N139 HCPL-0701 HCNW139		18	60* 90 115	µs	T_A = 25°C I_F = 0.5 mA, Rl = 4.7 kΩ	5, 6, 7, 9, 12	2, 4
		6N139 HCPL-0701 HCNW139		2	7* 10 1.1	µs	T_A = 25°C I_F = 12 mA, Rl = 270 Ω		
		6N138 HCPL-0700 HCNW138 6N138 HCPL-0700 HCNW139		10	35* 50 70	µs	T_A = 25°C I_F = 1.6 mA, Rl = 2.2 kΩ		
Common Mode Transient Immunity at Logic High Output	$\|CM_H\|$		1000	10000		V/µs	I_F = 0 mA, T_A = 25°C Rl = 2.2 kΩ $\|V_{CM}\|$ = 10 Vp-p	13	5, 6
Common Mode Transient Immunity at Logic Low Output	$\|CM_L\|$		1000	10000		V/µs	I_F = 1.6 mA, T_A = 25°C Rl = 2.2 kΩ $\|V_{CM}\|$ = 10 Vp-p	13	5, 6

*JEDEC Registered Data for 6N139 and 6N138.

**All typical values at T_A = 25°C and V_{CC} = 5 V, unless otherwise noted.

Package Characteristics

Parameter	Sym.	Min.	Typ.**	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage†	V_{ISO}	2500			V rms	RH < 50%, t = 1 min., T_A = 25°C		3, 8
Option 020 HCNW139 HCNW138		5000						3, 9
Resistance (Input-Output)	R_{I-O}		10^{12}		Ω	V_{I-O} = 500 Vdc RH < 45%		3
Capacitance (Input-Output)	C_{I-O}		0.6		pF	f = 1 MHz		3

**All typicals at T_A = 25°C, unless otherwise noted.
†The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the VDE 0884 Insulation Characteristics Table (if applicable), your equipment level safety specification or HP Application Note 1074 entitled "Optocoupler Input-Output Endurance Voltage."

Notes:

1. DC CURRENT TRANSFER RATIO (CTR) is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
2. Pin 7 Open.
3. Device considered a two-terminal device. Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.
4. Use of a resistor between pin 5 and 7 will decrease gain and delay time. Significant reduction in overall gain can occur when using resistor values below 47 kΩ. For more information, please contact your local HP Components representative.
5. Common mode transient immunity in a Logic High level is the maximum tolerable (positive) dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (i.e., V_O > 2.0 V). Common mode transient immunity in a Logic Low level is the maximum tolerable (negative) dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., V_O < 0.8 V).
6. In applications where dV/dt may exceed 50,000 V/μs (such as static discharge) a series resistor, R_{CC}, should be included to protect the detector IC from destructively high surge currents. The recommended value is R_{CC} = 220 Ω.
7. Use of a 0.1 μF bypass capacitor connected between pins 8 and 5 adjacent to the device is recommended.
8. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage 3000 V rms for 1 second (leakage detection current limit, I_{I-O} < 5 μA). This test is performed before the 100% production test shown in the VDE 0884 Insulation Related Characteristics Table, if applicable.
9. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage > 6000 V rms for 1 second (leakage detection current limit, I_{I-O} < 5 μA). This test is performed before the 100% production test for partial discharge (method b) shown in the VDE 0884 Insulation Related Characteristics Table, if applicable.

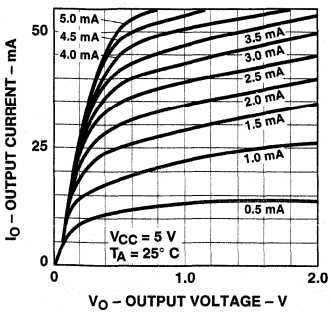


Figure 1. 6N138/6N139 DC Transfer Characteristics.

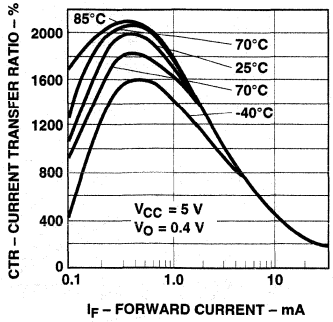


Figure 2. Current Transfer Ratio vs. Forward Current 6N138/6N139.

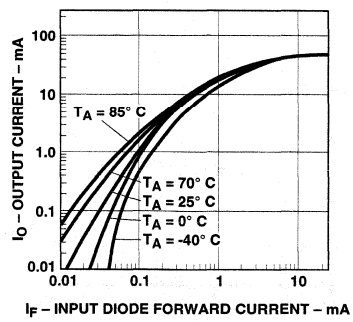


Figure 3. 6N138/6N139 Output Current vs. Input Diode Forward Current.

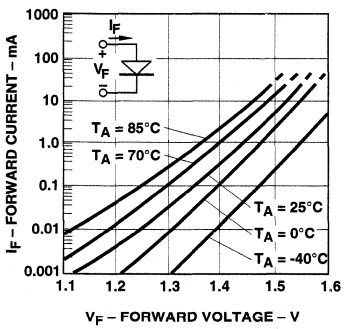


Figure 4. Input Diode Forward Current vs. Forward Voltage.

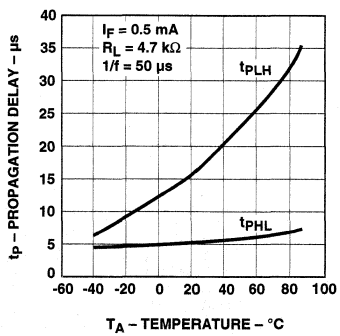


Figure 5. Propagation Delay vs. Temperature.

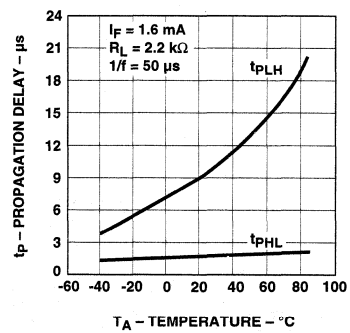


Figure 6. Propagation Delay vs. Temperature.

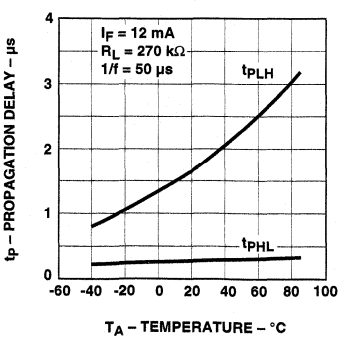


Figure 7. Propagation Delay vs. Temperature.

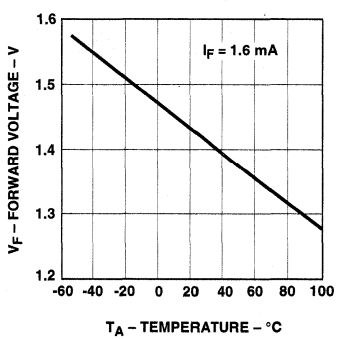


Figure 8. Forward Voltage vs. Temperature.

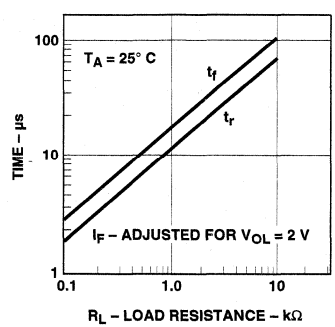


Figure 9. Nonsaturated Rise and Fall Times vs. Load Resistance.

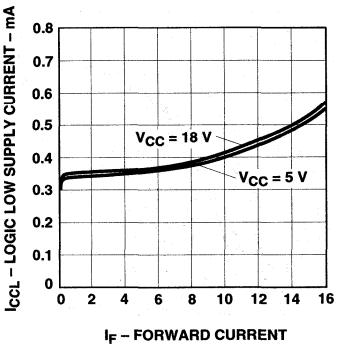


Figure 10. Logic Low Supply Current vs. Forward Current.

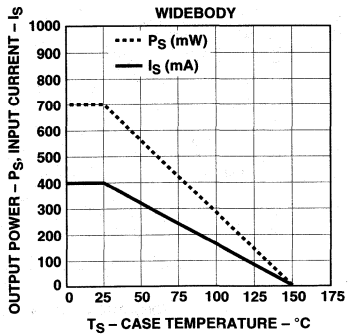


Figure 11. Thermal Derating Curve, Dependence of Safety Limiting Value with Case Temperature per VDE 0884.

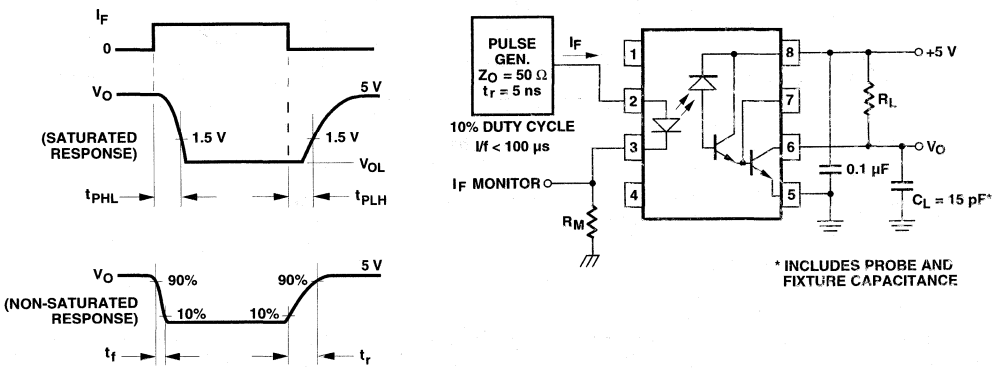


Figure 12. Switching Test Circuit.

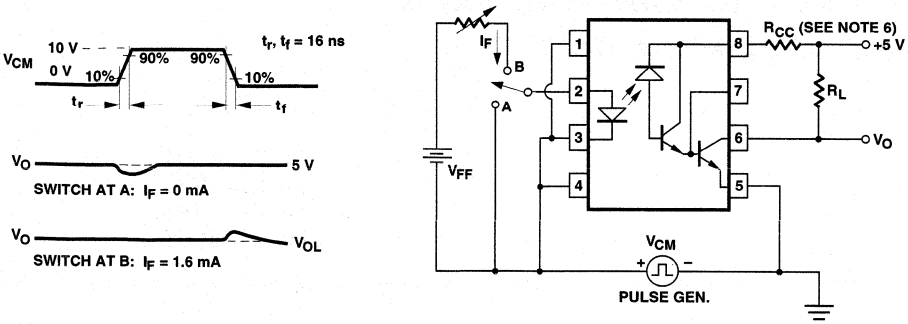


Figure 13. Test Circuit for Transient Immunity and Typical Waveforms.

HEWLETT® PACKARD

Very Low Power Consumption High Gain Optocouplers

Technical Data

HCPL-4701
HCPL-4731
HCPL-070A
HCPL-073A

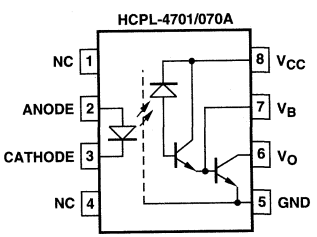
Features

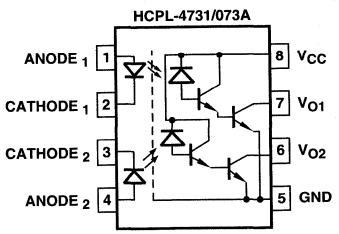
- **Ultra Low Input Current Capability - 40 μA**
- **Specified for 3 V Operation**
  Typical Power Consumption: <1 mW
  Input Power: <50 μW
  Output Power: <500 μW
- **Will Operate with V_{CC} as Low as 1.6 V**
- **High Current Transfer Ratio – 3500% at I_F = 40 μA**
- **TTL and CMOS Compatible Output**
- **Specified AC and DC Performance over Temperature: 0°C to 70°C**
- **Safety Approval**
  UL Recognized - 2500 V rms for 1 Minute and 5000 V rms* for 1 minute per UL1577
  CSA Approved
  VDE 0884 Approved with V_{IORM} = 630 V peak (Option 060) for HCPL-4701
- **8-Pin Product Compatible with 6N138/6N139 and HCPL-2730/HCPL-2731**
- **Available in 8-Pin DIP and SOIC-8 Footprint**
- **Through Hole and Surface Mount Assembly Available**

Applications

- **Battery Operated Applications**
- **ISDN Telephone Interface**
- **Ground Isolation between Logic Families – TTL, LSTTL, CMOS, HCMOS, HL-CMOS, LV-HCMOS**
- **Low Input Current Line Receiver**
- **EIA RS-232C Line Receiver**
- **Telephone Ring Detector**
- **AC Line Voltage Status Indicator - Low Input Power Dissipation**
- **Low Power Systems – Ground Isolation**
- **Portable System I/O Interface**

Functional Diagram





TRUTH TABLE

LED	V_O
ON	LOW
OFF	HIGH

*5000 V rms/1 Minute rating is for Option 020 (HCPL-4701 and HCPL-4731) products only.
A 0.1 μF bypass capacitor connected between pins 8 and 5 is recommended.

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

5965-6116E

Description

These devices are very low power consumption, high gain single and dual channel optocouplers. The HCPL-4701 represents the single channel 8-Pin DIP configuration and is pin compatible with the industry standard 6N139. The HCPL-4731 represents the dual channel 8-Pin DIP configuration and is pin compatible with the popular standard HCPL-2731. The HCPL-070A and HCPL-073A are the equivalent single and dual channel products in an SO-8 footprint. Each channel can be driven with an input current as low as 40 μA and has a typical current transfer ratio of 3500%.

These high gain couplers use an AlGaAs LED and an integrated high gain photodetector to provide an extremely high current transfer ratio between input and output. Separate pins for the photodiode and output stage results in TTL compatible saturation voltages and high speed operation. Where desired, the V_{CC} and V_O terminals may be tied together to achieve conventional Darlington operation (single channel package only).

These devices are designed for use in CMOS, LSTTL or other low power applications. They are especially well suited for ISDN telephone interface and battery operated applications due to the low power consumption. A 700% minimum current transfer ratio is guaranteed from 0°C to 70°C operating temperature range at 40 μA of LED current and $V_{CC} \geq 3$ V.

The SO-8 does not require "through holes" in a PCB. This package occupies approximately one-third the footprint area of the standard dual-in-line package. The lead profile is designed to be compatible with standard surface mount processes.

Selection Guide

8-Pin DIP (300 Mil)		Small Outline SO-8		Widebody Package (400 mil)				Hermetic
Single Channel Package	Dual Channel Package HCPL-	Single Channel Package HCPL-	Dual Channel Package HCPL-	Single Channel Package	Minimum Input ON Current (I_F)	Minimum CTR	Absolute Maximum V_{CC}	Single and Dual Channel Packages HCPL-
6N139[1]	2731[1]	0701[1]	0731[1]	HCNW139[1]	0.5 mA	400%	18 V	
6N138[1]	2730[1]	0700[1]	0730[1]	HCNW138[1]	1.6 mA	300%	7 V	
HCPL-4701	4731	070A	0730A		40 μA	800%	18 V	
					0.5 mA	300%	20 V	5701[1] 5700[1] 5731[1] 5730[1]

Notes:
1. Technical data are on separate HP publication.

Ordering Information

Specify Part Number followed by Option Number (if desired).

Example:

HCPL-4701#XXX

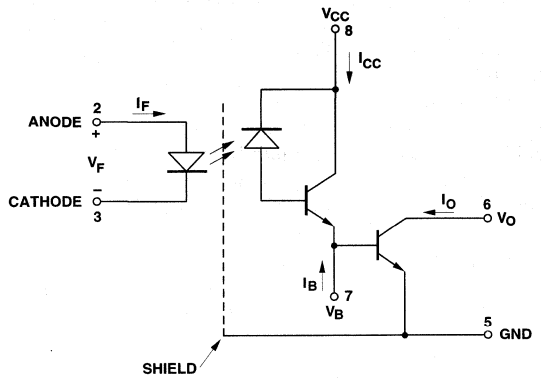
- 020 = 5000 V rms/1 minute UL Rating Option.**
- 060 = VDE 0884 V_{IORM} = 630 V peak Option†
- 300 = Gull Wing Surface Mount Option.*
- 500 = Tape and Reel Packaging Option.

*Gull wing surface mount option applies to through hole parts only.
**For HCPL-4701 and HCPL-4731 (8-Pin DIP products) only.
†For HCPL-4701 only. Combination of Option 020 and Option 060 is not available.

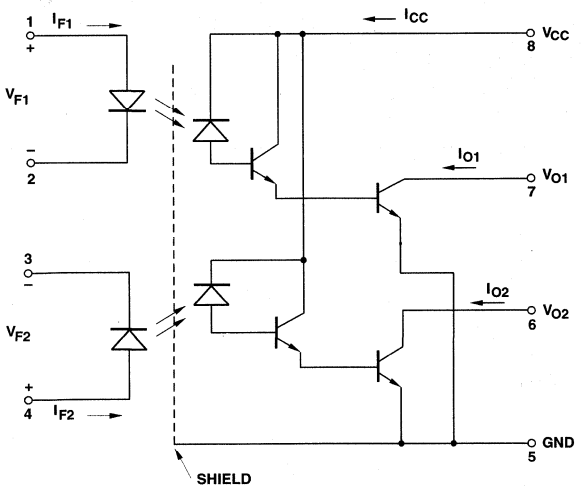
Option data sheets available. Contact your Hewlett-Packard sales representative or authorized distributor for information.

Schematic

HCPL-4701 and HCPL-070A



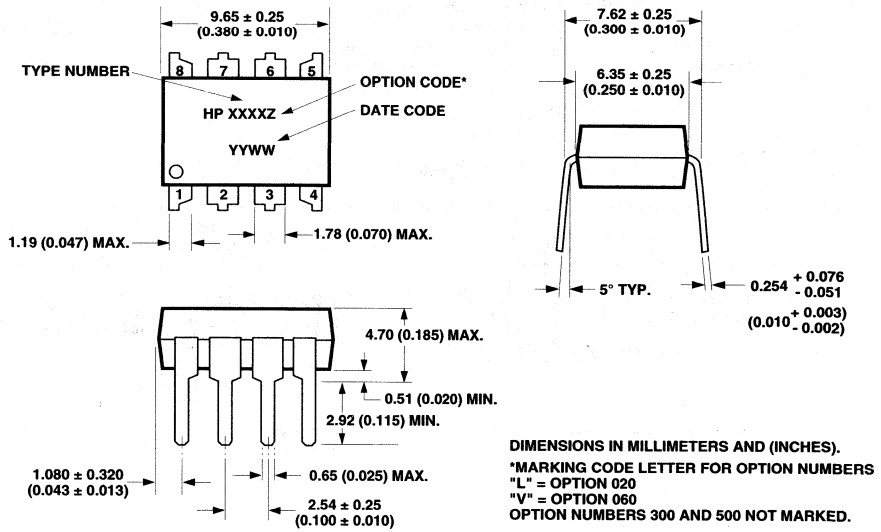
HCPL-4731 and HCPL-073A



USE OF A 0.1 µF BYPASS CAPACITOR CONNECTED BETWEEN PINS 5 AND 8 IS RECOMMENDED (SEE NOTE 8)

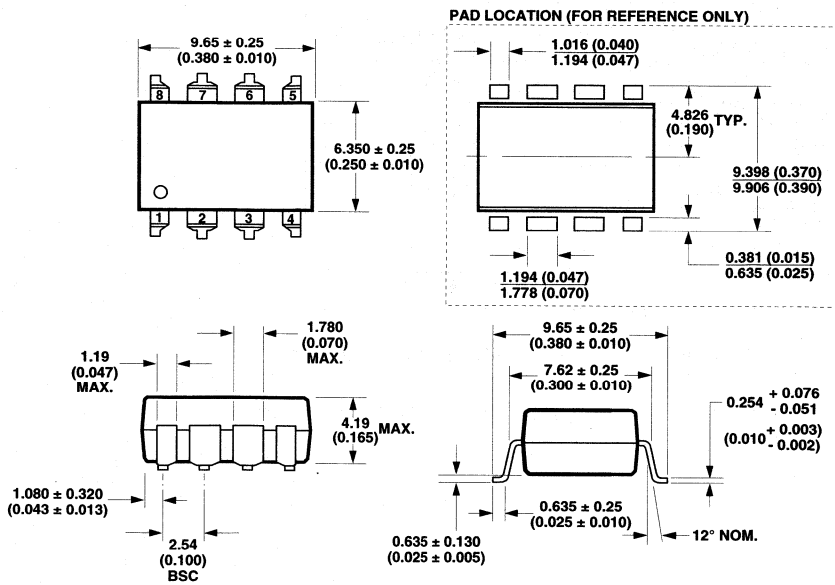
Package Outline Drawings

8-Pin DIP Package (HCPL-4701, HCPL-4731)



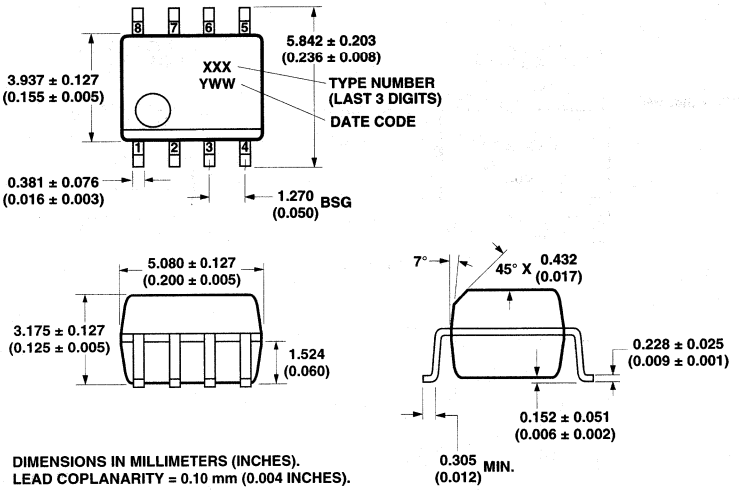
DIMENSIONS IN MILLIMETERS AND (INCHES).
*MARKING CODE LETTER FOR OPTION NUMBERS
"L" = OPTION 020
"V" = OPTION 060
OPTION NUMBERS 300 AND 500 NOT MARKED.

8-Pin DIP Package with Gull Wing Surface Mount Option 300 (HCPL-4701, HCPL-4731)

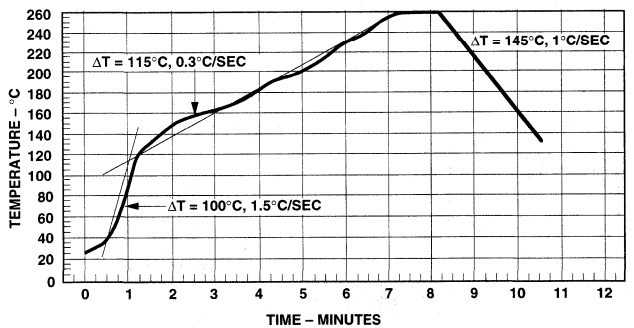


DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES).

Small-Outline SO-8 Package (HCPL-070A, HCPL-073A)



Solder Reflow Temperature Profile



Note: Use of nonchlorine activated fluxes is highly recommended.

Figure 1. Solder Reflow Thermal Profile (HCPL-070A, HCPL-073A, and Gull Wing Surface Mount Option 300 Parts).

Regulatory Information

The HCPL-4701/4731 and HCPL-070A/073A have been approved by the following organizations:

UL

Recognized under UL 1577, Component Recognition Program, File E55361.

CSA

Approved under CSA Component Acceptance Notice #5, File CA 88324.

VDE

Approved according to VDE 0884/06.92 (Option 060 only).

Insulation Related Specifications

Parameter	Symbol	8-Pin DIP (300 Mil) Value	SO-8 Value	Units	Conditions
Minimum External Air Gap (External Clearance)	L(101)	7.1	4.9	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L(102)	7.4	4.8	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	0.08	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity.
Tracking Resistance (Comparative Tracking Index)	CTI	200	200	Volts	DIN IEC 112/ VDE 0303 Part 1
Isolation Group		IIIa	IIIa		Material Group DIN VDE 0110, 1/89, Table 1)

Option 300 – surface mount classification is Class A in accordance with CECC 00802.

VDE 0884 Insulation Related Characteristics (HCPL-4701 OPTION 060 ONLY)

Description	Symbol	Characteristic	Units
Installation classification per DIN VDE 0110/1.89, Table 1 for rated mains voltage ≤ 300 V rms		I-IV	
for rated mains voltage ≤ 450 V rms		I-III	
Climatic Classification		55/85/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	630	V peak
Input to Output Test Voltage, Method b* V_{IORM} x 1.87 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial Discharge < 5 pC	V_{PR}	1181	V peak
Input to Output Test Voltage, Method a* V_{IORM} x 1.5 = V_{PR}, Type and sample test, t_m = 60 sec, Partial Discharge < 5 pC	V_{PR}	945	V peak
Highest Allowable Overvoltage* (Transient Overvoltage, t_{ini} = 10 sec)	V_{IOTM}	6000	V peak
Safety Limiting Values (Maximum values allowed in the event of a failure, also see Figure 16, Thermal Derating curve.)			
Case Temperature	T_S	175	°C
Input Current	$I_{S,INPUT}$	230	mA
Output Power	$P_{S,OUTPUT}$	600	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	$>10^9$	Ω

*Refer to the front of the optocoupler section of the current catalog, under Product Safety Regulations section, (VDE 0884) for a detailed description.
Note: Isolation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuits in application.

Absolute Maximum Ratings

(No Derating Required up to 70°C)

Parameter	Symbol	Minimum	Maximum	Units
Storage Temperature	T_S	-55	125	°C
Operating Temperature	T_A	-40	85	°C
Average Forward Input Current (HCPL-4701/4731)	$I_{F(AVG)}$		10	mA
Average Forward Input Current (HCPL-070A/073A)	$I_{F(AVG)}$		5	mA
Peak Transient Input Current (HCPL-4701/4731) (50% Duty Cycle, 1 ms Pulse Width)	I_{FPK}		20	mA
Peak Transient Input Current (HCPL-070A/073A) (50% Duty Cycle, 1 ms Pulse Width)	I_{FPK}		10	mA
Reverse Input Voltage	V_R		2.5	V
Input Power Dissipation (Each Channel)	P_I		15	mW
Output Current (Each Channel)	I_O		60	mA
Emitter Base Reverse Voltage (HCPL-4701/070A)	V_{EB}		0.5	V
Output Transistor Base Current (HCPL-4701/070A)	I_B		5	mA
Supply Voltage	V_{CC}	-0.5	18	V
Output Voltage	V_O	-0.5	18	V
Output Power Dissipation (Each Channel)	P_O		100	mW
Total Power Dissipation (Each Channel)	P_T		115	mW
Lead Solder Temperature (for Through Hole Devices)	260°C for 10 sec., 1.6 mm below seating plane			
Reflow Temperature Profile (for SOIC-8 and Option #300)	See **Package Outline Drawings** section			

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage	V_{CC}*	1.6	18	V
Forward Input Current (ON)	$I_{F(ON)}$	40	5000	μA
Forward Input Voltage (OFF)	$V_{F(OFF)}$	0	0.8	V
Operating Temperature	T_A	0	70	°C

*See Note 1.

Electrical Specifications

$0°C \le T_A \le 70°C$, $4.5\ V \le V_{CC} \le 20\ V$, $1.6\ mA \le I_{F(ON)} \le 5\ mA$, $0\ V \le V_{F(OFF)} \le 0.8\ V$, unless otherwise specified. All Typicals at $T_A = 25°C$. See note 8.

Parameter	Symbol	Device HCPL-	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR		800	3500	25k	%	$I_F = 40\ \mu A$, $V_O = 0.4\ V$, $V_{CC} = 4.5\ V$	4, 5	2
			600	3000	8k		$I_F = 0.5\ mA$, $V_{CC} = 4.5\ V$		
			700	3200	25k		$I_F = 40\ \mu A$		
			500	2700	8k		$I_F = 0.5\ mA$		
Logic Low Output Voltage	V_{OL}			0.06	0.4	V	$I_F = 40\ \mu A$, $I_O = 280\ \mu A$	2, 3	
				0.04	0.4		$I_F = 0.5\ mA$, $I_O = 2.5\ mA$		
Logic High Output Current	I_{OH}			0.01	5	µA	$V_O = V_{CC} = 3$ to $7\ V$, $I_F = 0\ mA$		
				0.02	80		$V_O = V_{CC} = 18\ V$, $I_F = 0\ mA$		
Logic Low Supply Current	I_{CCL}	4701/070A		0.02	0.2	mA	$I_F = 40\ \mu A$, V_O = Open		
				0.1	1		$I_F = 0.5\ mA$		
		4731/073A		0.04	0.4		$I_F = 40\ \mu A$		
				0.2	2.0		$I_F = 0.5\ mA$		
Logic High Supply Current	I_{CCH}	4701/070A		<0.01	10	µA	$I_F = 0\ mA$, V_O = Open		
		4731/073A		<0.01	20				
Input Forward Voltage	V_F		1.1	1.25	1.4	V	$I_F = 40$ to $500\ \mu A$, $T_A = 25°C$	6	
			0.95		1.5		$I_F = 40$ to $500\ \mu A$		
Input Reverse Breakdown Voltage	BV_R		3.0	5.0		V	$I_R = 100\ \mu A$, $T_A = 25°C$		
			2.5				$I_R = 100\ \mu A$		
Temperature Coefficient of Forward Voltage	$\Delta V_F/\Delta T_A$			-2.0		mV/°C	$I_F = 40\ \mu A$		
				-1.6			$I_F = 0.5\ mA$		
Input Capacitance	C_{IN}			18		pF	$f = 1\ MHz$, $V_F = 0\ V$		

*All typical values at $T_A = 25°C$ and $V_{CC} = 5\ V$, unless otherwise noted.

Switching Specifications (AC)

Over Recommended Operating Conditions T_A = 0°C to 70°C, V_{CC} = 3 V to 18 V, unless otherwise specified.

Parameter	Symbol	Device HCPL-	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to Logic Low at Output	t_{PHL}			65	500	µs	I_F = 40 µA, R_L = 11 to 16 kΩ, V_{CC} = 3.3 to 5 V	7, 9	9, 10
				3	25		T_A = 25°C, I_F = 0.5 mA, R_L = 4.7 kΩ		
					30				
Propagation Delay Time to Logic High Output	t_{PLH}			70	500	µs	I_F = 40 µA, R_L = 11 to 16 kΩ, V_{CC} = 3.3 to 5 V	7, 9	9, 10
				34	60		T_A = 25°C, I_F = 0.5 mA, R_L = 4.7 kΩ		
		4701/4731			90				
		070A/073A			130				
Common Mode Transient Immunity at Logic High Output	$\|CM_H\|$		1,000	10,000		V/µs	I_F = 0 mA, R_L = 4.7 to 11 kΩ, V_{CM} = 10 V_{p-p}, T_A = 25°C,	8	6, 7
Common Mode Transient Immunity at Logic Low Output	$\|CM_L\|$		1,000	10,000		V/µs	I_F = 0.5 mA, R_L = 4.7 to 11 kΩ, $\|V_{CM}\|$ = 10 V_{p-p}, T_A = 25°C	8	6, 7
				2,000			I_F = 40 µA, R_L = 11 to 16 kΩ, $\|V_{CM}\|$ = 10 V_{p-p} V_{CC} = 3.3 to 5 V, T_A = 25°C		

*All typical values at T_A = 25°C and V_{CC} = 5 V, unless otherwise noted.

Package Characteristics

Parameter	Symbol	Device HCPL-	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage**	V_{ISO}		2500			V rms	RH ≤ 50%, t = 1 min., T_A = 25°C		3, 4
Option 020		4701 4731	5000						3, 4a
Resistance (Input-Output)	R_{I-O}			10^{12}		Ω	V_{I-O} = 500 VDC RH ≤ 45%		3
Capacitance (Input-Output)	C_{I-O}			0.6		pF	f = 1 MHz		3
Insulation Leakage Current (Input-Input)	I_{I-I}	4731 073A		0.005		µA	RH ≤ 45%, t = 5 s, V_{I-I} = 500 VDC		5
Resistance (Input-Input)	R_{I-I}			10^{11}		Ω			
Capacitance (Input-Input)	C_{I-I}	4731		0.03		pF	f = 1 MHz		5
		073A		0.25					

*All typical values at T_A = 25°C and V_{CC} = 5 V.
**The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the VDE 0884 Insulation Characteristics Table (if applicable), your equipment level safety specification or HP Application Note 1074 entitled "Optocoupler Input-Output Endurance Voltage."

Notes:

1. Specification information is available form the factory for 1.6 V operation. Call your local field sales office for further information.
2. DC CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
3. Device considered a two terminal device: pins 1, 2, 3, and 4 shorted together, and pins 5, 6, 7, and 8 shorted together.
4. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 3000 V_{RMS} for 1 second (leakage detection current limit, $I_{I-O} \leq 5$ μA.

4a. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 6000 V_{RMS} for 1 second (leakage detection current limit, $I_{I-O} \leq 5$ μA. This test is performed before the 100% production test for partial discharge (Method b) shown in the VDE 0884 Insulation Characteristics Table.

5. Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.
6. Common transient immunity in a Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (i.e., $V_O > 2.0$ V). Common transient immunity in a Logic Low level is he maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., $V_O < 0.8$ V).
7. In applications where dV/dt may exceed 50,000 V/μs (such as static discharge) a series resistor, R_{CC}, should be included to protect the detector IC form destructively high surge currents. The recommended value is $R_{CC} = 220\ \Omega$.
8. Use of a 0.1 μF bypass capacitor connected between pins 8 and 5 adjacent to the device is recommended.
9. Pin 7 open for single channel product.
10. Use of resistor between pins 5 and 7 will decrease gain and delay time. Significant reduction in overall gain can occur when using resistor values below 47 kΩ for single channel product.
11. The Applications Information section of this data sheet references the HCPL-47XX part family, but applies equally to the HCPL-070A and HCPL-073A parts.

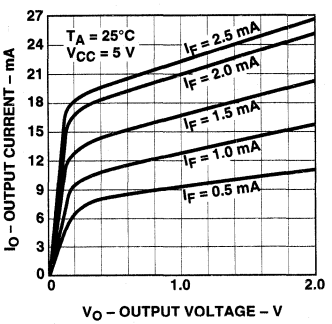


Figure 2. DC Transfer Characteristics (I_F = 0.5 mA to 2.5 mA).

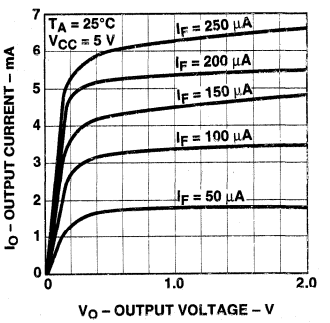


Figure 3. DC Transfer Characteristics (I_F = 50 μA to 250 μA).

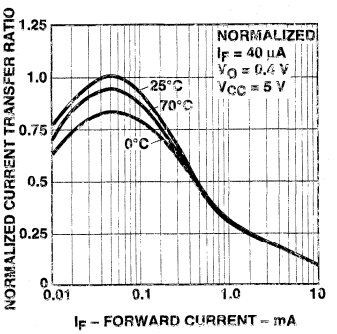


Figure 4. Current Transfer Ratio vs. Forward Current.

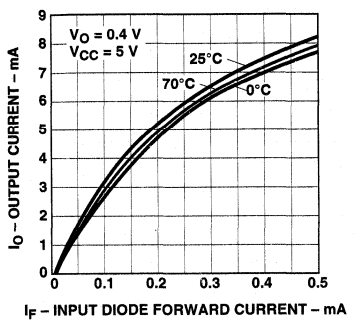


Figure 5. Output Current vs. Input Diode Forward Current.

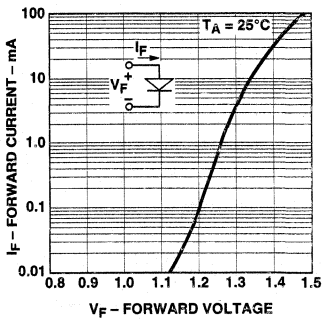


Figure 6. Input Diode Forward Current vs. Forward Voltage.

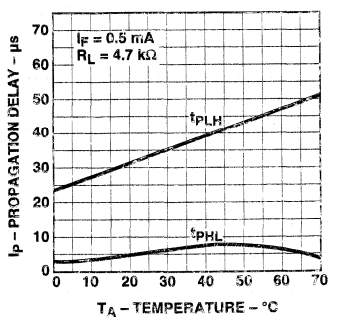


Figure 7. Propagation Delay vs. Temperature.

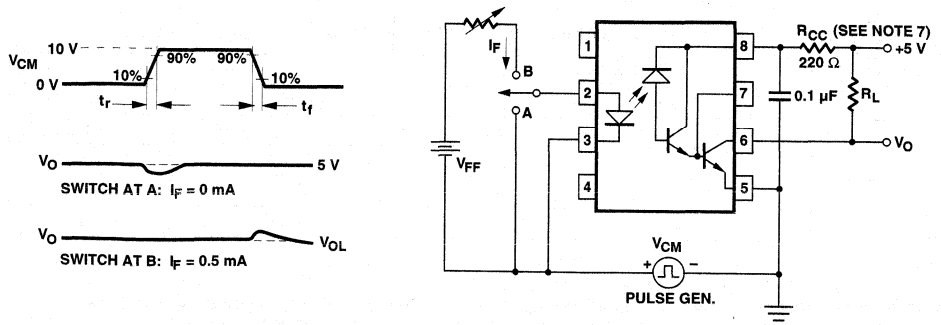


Figure 8. Test Circuit for Transient Immunity and Typical Waveforms.

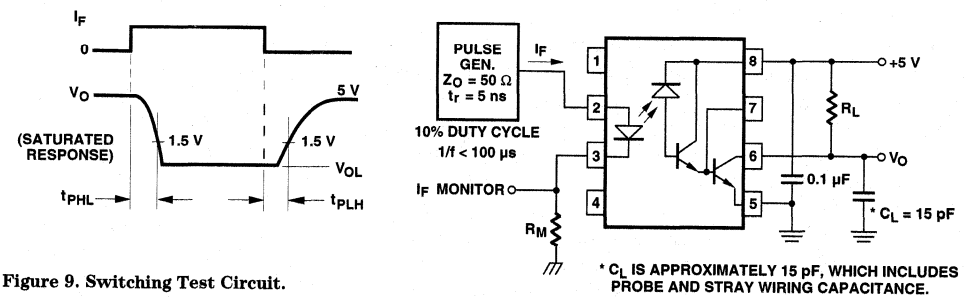


Figure 9. Switching Test Circuit.

Applications Information

Low-Power Operation

Current Gain

There are many applications where low-power isolation is needed and can be provided by the single-channel HCPL-4701, or the dual-channel HCPL-4731 low-power optocouplers. Either or both of these two devices are referred to in this text as HCPL-47XX product(s). These optocouplers are Hewlett-Packard's lowest input current, low-power optocouplers. Low-power isolation can be defined as less than a milliwatt of input power needed to operate the LED of an optocoupler (generally less than 500 μA). This level of input forward current conducting through the LED can control a worst-case total output (I_{ol}) and power supply current (I_{ccl}) of two and a half milliamperes. Typically, the HCPL-47XX can control a total output and supply current of 15 mA. The output current, I_O is determined by the LED forward current multiplied by the current gain of the optocoupler, $I_O = I_F(CTR)/100\%$. In particular with the HCPL-47XX optocouplers, the LED can be driven with a very small I_F of 40 μA to control a maximum I_O of 320 μA with a worst case design Current Transfer Ratio (CTR) of 800%. Typically, the CTR and the corresponding I_{ol}, are 4 times larger. For low-power operation, Table 1 lists the typical power dissipations that occur for both the 3.3 Vdc and 5 Vdc HCPL-47XX optocoupler applications. These approximate power dissipation values are listed respectively for the LED, for the output V_{CC} and for the open-collector output transistor. Those values are summed together for a comparison of total power dissipation consumed in either the 3.3 Vdc or 5 Vdc applications.

Table 1. Typical HCPL-4701 Power Dissipation for 3 V and 5 V Applications

Power Dissipation (μW)	V_{CC} = 3.3 Vdc		V_{CC} = 5 Vdc	
	I_F = 40 μA	I_F = 500 μA	I_F = 40 μA	I_F = 500 μA
P_{LED}	50	625	50	625
P_{Vcc}	65	330	100	500
P_{O-C}[1]	20	10	25	20
P_{TOTAL}[2]	135 μW	965 μW	175 μW	1,145 μW

Notes:

1. R_L of 11 kΩ open-collector (o-c) pull-up resistor was used for both 3.3 Vdc and 5 Vdc calculations.
2. For typical total interface circuit power consumption in 3.3 Vdc application, add to P_{TOTAL} approximately 80 μW for 40 μA (1,025 μW for 500 μA) LED current-limiting resistor, and 960 μW for the 11 kΩ pull-up resistor power dissipations. Similarly, for 5 Vdc applications, add to P_{TOTAL} approximately 150 μW for 40 μA (1,875 μW for 500 μA) LED current-limiting resistor and 2,230 μW for the 11 kΩ pull-up resistor power dissipations.

Propagation Delay

When the HCPL-47XX optocoupler is operated under very low input and output current conditions, the propagation delay times will lengthen. When lower input drive current level is used to switch the high-efficiency AlGaAs LED, the slower the charge and discharge time will be for the LED. Correspondingly, the propagation delay times will become longer as a result. In addition, the split-Darlington (open-collector) output amplifier needs a larger, pull-up load resistance to ensure the output current is within a controllable range. Applications that are not sensitive to longer propagation delay times and that are easily served by this HCPL-47XX optocoupler, typically 65 μs or greater, are those of status monitoring of a telephone line, power line, battery condition of a portable unit, etc. For faster HCPL-47XX propagation delay times, approximately 30 μs, this optocoupler needs to operate at higher I_F (≥ 500 μA) and I_o (≥ 1 mA) levels.

Applications

Battery-Operated Equipment

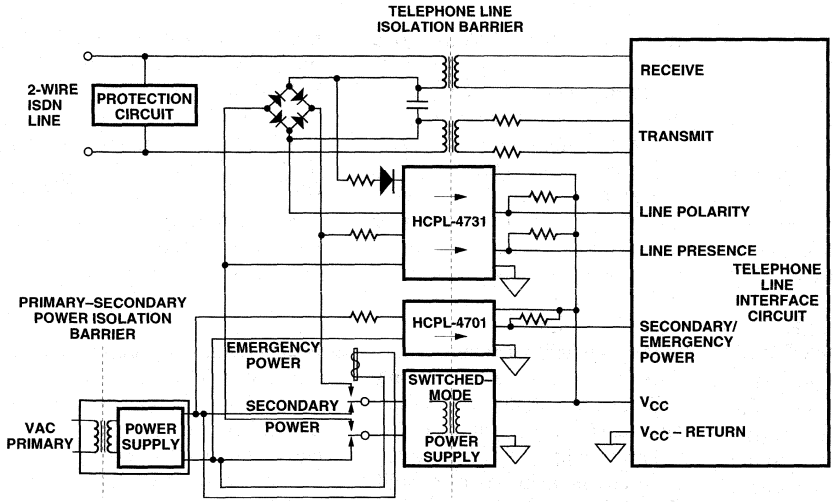
Common applications for the HCPL-47XX optocoupler are within battery-operated, portable equipment, such as test or medical instruments, computer peripherals and accessories where energy conservation is required to maximize battery life. In these applications, the optocoupler would monitor the battery voltage and provide an isolated output to another electrical system to indicate battery status or the need to switch to a backup supply or begin a safe shutdown of the equipment via a communication port. In addition, the HCPL-47XX optocouplers are specified to operate with 3 Vdc CMOS logic family of devices to provide logic-signal isolation between similar or different logic circuit families.

Telephone Line Interfaces

Applications where the HCPL-47XX optocoupler would be best used are in telephone line interface circuitry for functions of ring detection, on-off hook detection, line polarity, line presence and supplied-power sensing. In particular, Integrated Services Digital Network (ISDN) applications, as illustrated in Figure 10, can severely restrict the input power that an optocoupler interface circuit can use (approximately 3 mW). Figure 10 shows three isolated signals that can be served by the small input LED current of the HCPL-47XX dual- and single-channel optocouplers. Very low, total power dissipation occurs with these series of devices.

Switched-Mode Power Supplies

Within Switched-Mode Power Supplies (SMPS) the less power consumed the better. Isolation for monitoring line power, regulation status, for use within a feedback path between primary and secondary circuits or to external circuits are common applications for optocouplers. Low-power HCPL-47XX optocoupler can help keep higher energy conversion efficiency for the SMPS. The block diagram of Figure 11 shows where low-power isolation can be used.



NOTE: THE CIRCUITS SHOWN IN THIS FIGURE REPRESENT POSSIBLE, FUNCTIONAL APPLICATION OF THE HCPL-47XX OPTOCOUPLER TO AN ISDN LINE INTERFACE. THIS CIRCUIT ARRANGEMENT DOES NOT GUARANTEE COMPLIANCE, CONFORMITY, OR ACCEPTANCE TO AN ISDN, OR OTHER TELECOMMUNICATION STANDARD, OR TO FCC OR TO OTHER GOVERNMENTAL REGULATORY AGENCY REQUIREMENTS. THESE CIRCUITS ARE RECOMMENDATIONS THAT MAY MEET THE NEEDS OF THESE APPLICATIONS. HEWLETT-PACKARD DOES NOT IMPLY, REPRESENT, NOR GUARANTEE THAT THESE CIRCUIT ARRANGEMENTS ARE FREE FROM PATENT INFRINGEMENT.

Figure 10. HCPL-47XX Isolated Monitoring Circuits for 2-Wire ISDN Telephone Line.

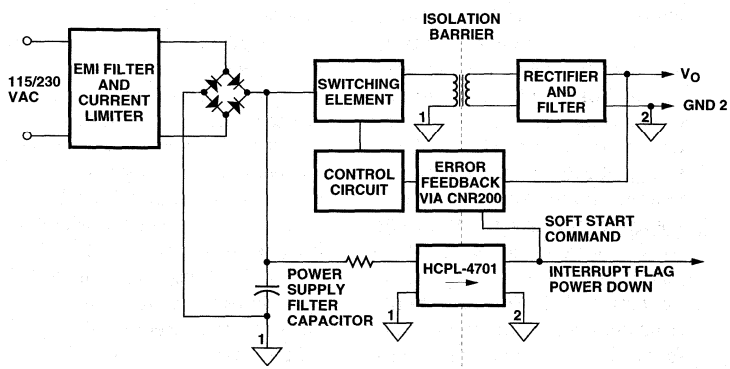


Figure 11. Typical Optical Isolation Used for Power-Loss Indication and Regulation Signal Feedback.

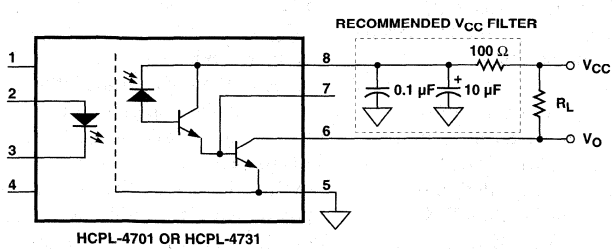


Figure 12. Recommended Power Supply Filter for HCPL-47XX Optocouplers.

Data Communication and Input/Output Interfaces

In data communication, the HCPL-47XX can be used as a line receiver on a RS-232-C line or this optocoupler can be part of a proprietary data link with low input current, multi-drop stations along the data path. Also, this low-power optocoupler can be used within equipment that monitors the presence of high-voltage. For example, a benefit of the low input LED current (40 μA) helps the input sections of a Programmable Logic Controller (PLC) monitor proximity and limit switches. The PLC I/O sections can benefit from low input current optocouplers because the total input power dissipation when monitoring the high voltage (120 Vac - 220 Vac) inputs is minimized at the I/O connections. This is especially important when many input channels are stacked together.

Circuit Design Issues

Power Supply Filtering

Since the HCPL-47XX is a high-gain, split-Darlington amplifier, any conducted electrical noise on the V_{CC} power supply to this optocoupler should be minimized. A recommended V_{CC} filter circuit is shown in Figure 12 to improve the power supply rejection (psr) of the optocoupler. The filter should be located near the combination of pin 8 and pin 5 to provide best filtering action. This filter will drastically limit any sudden rate of change of V_{CC} with time to a slower rate that cannot interfere with the optocoupler.

Common-Mode Rejection & LED Driver Circuits

With the combination of a high-efficiency AlGaAs LED and a high-gain amplifier in the HCPL-47XX optocoupler, a few circuit techniques can enhance the common-mode rejection (CMR) of this optocoupler. First, use good high-frequency circuit layout practices to minimize coupling of common-mode signals between input and output circuits. Keep input traces away from output traces to minimize capacitive coupling of interference between input and output sections. If possible, parallel, or shunt switch the LED current as shown in Figure 13, rather than series switch the LED current as illustrated in Figure 15. Not only will CMR be enhanced with these circuits (Figures 13 and 14), but the switching speed of the optocoupler will be improved as well. This is because in the parallel switched case the LED current is current-steered into or away from the LED, rather than being fully turned off as in the series switched case. Figure 13 illustrates this type of circuit. The Schottky diode helps quickly to discharge and pre-bias the LED in the off state. If a common-mode voltage across the optocoupler suddenly attempts to inject a current into the off LED anode, the Schottky diode would divert the interfering current to ground. The combination of the Schottky diode forward voltage and the Vol saturation voltage of the driver output stage (on-condition) will keep the LED voltage at or below 0.8 V. This will prevent the LED (off-condition) from conducting any significant forward current that might cause the HCPL-47XX to turn on. Also, if the driver stage is an active totem-pole output, the Schottky diode allows the active output pull-up section to disconnect from the LED and pull high.

As shown in Figure 14, most active output driver integrated circuits can source directly the forward current needed to operate the LED of the HCPL-47XX optocoupler. The advantage of using the silicon diode in this circuit is to conduct charge out of the LED quickly when the LED is turned off. Upon turn-on of the LED, the silicon diode capacitance will provide a rapid charging path (peaking current) for the LED. In addition, this silicon diode prevents common-mode current from entering the LED anode when the driver IC is on and no operating LED current exists.

In general, series switching the low input current of the HCPL-47XX LED is not recommended. This is particularly valid when in a high common-mode interference environment. However, if series switching of the LED current must be done, use an additional pull-up resistor from the cathode of the LED to the input V_{CC} as shown in Figure 15. This helps minimize any differential-mode current from conducting in the LED while the LED is off, due to a common-mode signal occurring on the input V_{CC} (anode) of the LED. The common-mode signal coupling to the anode and cathode could be slightly different. This could potentially create a LED current to flow that would rival the normal, low input current needed to operate the optocoupler. This additional parallel resistor can help shunt any leakage current around the LED should the drive circuit, in the off state, have any significant leakage current on the order of 40 μA. With the use of this parallel resistor, the total drive current conducted when the LED is on is the sum of the parallel resistor and LED currents. In the series circuit of Figure 15 with the LED off, if a common-mode voltage were to couple to the LED cathode, there can be enough imbalance of common-mode voltage across the LED to cause a LED current to flow and, inadvertently, turn on the optocoupler. This series, switching circuit has no protection against a negative-transition, input common-mode signal.

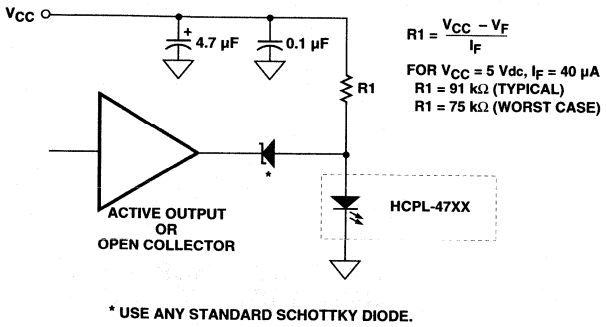


Figure 13. Recommended Parallel LED Driver Circuit for HCPL-4701/-4731.

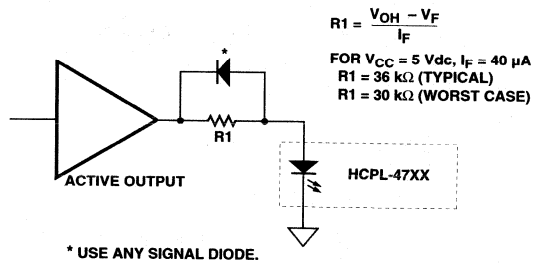


Figure 14. Recommended Alternative LED Driver Circuit for HCPL-4701/-4731 .

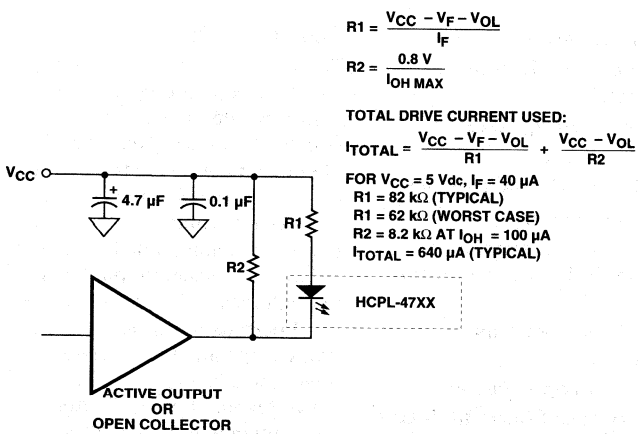


Figure 15. Series LED Driver Circuit for HCPL-4701/-4731.

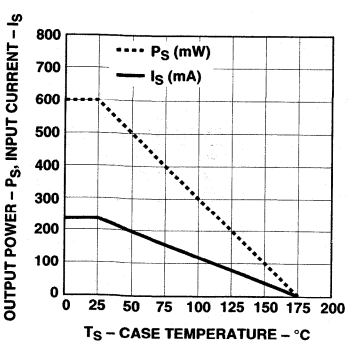


Figure 16. Thermal Derating Curve, Dependence of Safety Limiting Value with Case Temperature per VDE 0884.

HEWLETT® PACKARD

Dual Channel Low Input Current, High Gain Optocouplers

Technical Data

HCPL-2730 HCPL-0730
HCPL-2731 HCPL-0731

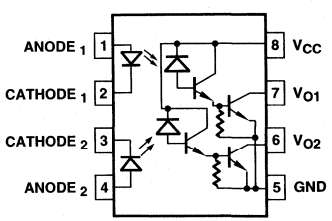
Features

- **High Current Transfer Ratio – 1800% Typical**
- **Low Input Current Requirements – 0.5 mA**
- **Low Output Saturation Voltage – 0.1 V**
- **High Density Packaging**
- **Performance Guaranteed over Temperature 0°C to 70°C**
- **LSTTL Compatible**
- **High Output Current – 60 mA**
- **Safety Approval**
  UL Recognized - 2500 V rms for 1 Minute and 5000 V rms* for 1 minute
  CSA Approved
- **Available in 8 Pin DIP and SO-8 Footprint**
- **MIL-STD-1772 Version Available (HCPL-5730/5731)**
- **Surface Mount Gull Wing Option Available for 8-Pin DIP (Option 300)**

Applications

- **Digital Logic Ground Isolation**
- **Telephone Ring Detector**
- **Level Shifting**
- **EIA RS-232C Line Receiver**
- **Polarity Sensing**
- **Low Input Current Line Receiver - Long Line or Party Line**
- **Microprocessor Bus Isolation**
- **Current Loop Receiver**
- **Line Voltage Status Indicator -Low Input Power Dissipation**

Functional Diagram



TRUTH TABLE

LED	V_O
ON	LOW
OFF	HIGH

Description

These dual channel optocouplers contain a separated pair of GaAsP light emitting diodes optically coupled to a pair of integrated high gain photo detectors. They provide extremely high current transfer ratio and excellent input-output common mode transient immunity. A separate pin for the photodiodes and first gain stages (V_{CC}) permits lower output saturation voltage and higher speed operation than possible with conventional photodarlington type optocouplers. In addition, V_{CC} may be as low as 1.6 V

*5000 V rms/1 minute withstand voltage rating is for Option 020 (HCPL-2730, HCLP-2731) products only.
A 0.1 µF bypass capacitor connected between pins 5 and 8 is recommended.

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

5965-3597E

without adversely affecting the parametric performance.

These dual channel optocouplers are available in an 8-Pin DIP and in an industry standard SO-8 package. The following is a cross reference table listing the 8-Pin DIP part number and the electrically equivalent SOIC-8 part number.

8-Pin DIP	SO-8
HCPL-2730	HCPL-0730
HCPL-2731	HCPL-0731

The SO-8 does not require "through holes" in a PCB. This package occupies approximately one-third the footprint area of the standard dual-in-line package. The lead profile is designed to be compatible with standard surface mount processes.

Guaranteed operation at low input currents and the high current transfer ratio (CTR) reduce the magnitude and effects of CTR degradation.

The outstanding high temperature performance of this split Darlington type output amplifier results from the inclusion of an integrated emitter-base bypass resistor which shunts photodiode and first stage leakage currents to ground.

The HCPL-2731/0731 have a 400% minimum CTR at an input current of only 0.5 mA making it ideal for use in low input current applications such as MOS, CMOS, and low power logic interfacing or RS232C data transmission systems. In addition, the high CTR and high output current capability make this device extremely useful in applications where a high fanout is required. Compatibility with high voltage CMOS logic systems is guaranteed by the 18 V V_{CC} and V_O specifications and by testing output high leakage (I_{OH}) at 18 V.

The HCPL-2730/0730 are specified at an input current of 1.6 mA and have a 7 V V_{CC} and V_O rating. The 300% minimum CTR allows TTL to TTL interfacing at this input current.

Important specifications such as CTR, leakage current, and output saturation voltage are guaranteed over the 0°C to 70°C temperature range to allow trouble-free system operation. Selection for lower input currents down to 250 μA is available upon request.

Selection Guide

8-Pin DIP (300 Mil)		Small Outline SO-8		Widebody Package (400 mil)				Hermetic
Single Channel Package	Dual Channel Package HCPL-	Single Channel Package HCPL-	Dual Channel Package HCPL-	Single Channel Package	Minimum Input ON Current (I_F)	Minimum CTR	Absolute Maximum V_{CC}	Single and Dual Channel Packages HCPL-
6N139[1]	2731	0701[1]	0731	HCNW139[1]	0.5 mA	400%	18 V	
6N138[1]	2730	0700[1]	0730	HCNW138[1]	1.6 mA	300%	7 V	
HCPL-4701[1]	4731[1]	070A[1]	073A[1]		40 μA	800%	18 V	
					0.5 mA	300%	20 V	5701[1] 5700[1] 5731[1] 5730[1]

Note:
1. Technical data are on separate HP publications.

Ordering Information

Specify Part Number followed by Option Number (if desired).

Example:

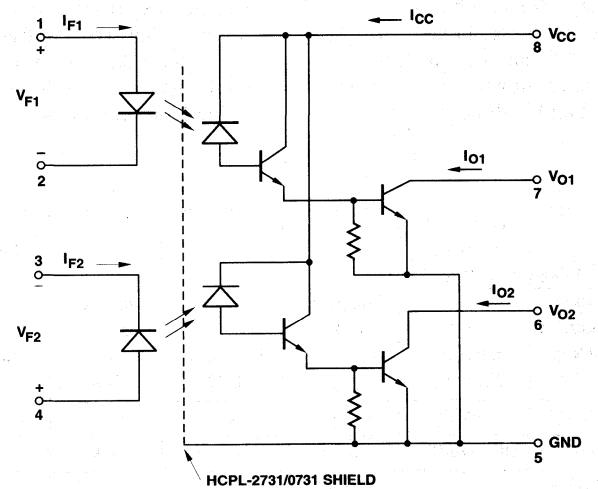
HCPL-2731#XXX

- 020 = 5000 V rms/1 Minute UL Rating Option.*
- 300 = Gull Wing Surface Mount Option, 50 per tube.**
- 500 = Tape and Reel Packaging Option, 1000 per reel.

Option data sheets available. Contact your Hewlett-Packard sales representative or authorized distributor for information.

*For HCPL-2731 and HCPL-2730 only.
**Gull wing surface mount option applies to through hole parts only.

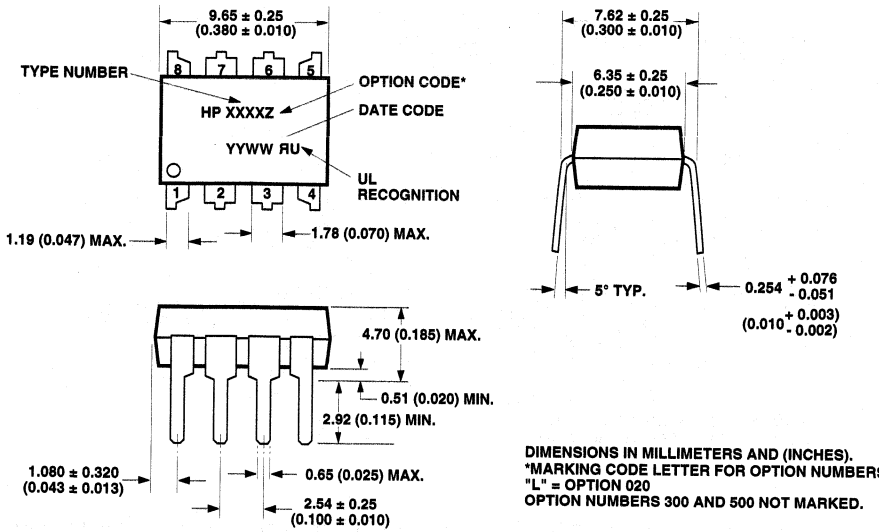
Schematic



USE OF A 0.1 µF BYPASS CAPACITOR CONNECTED BETWEEN PINS 5 AND 8 IS RECOMMENDED (SEE NOTE 8)

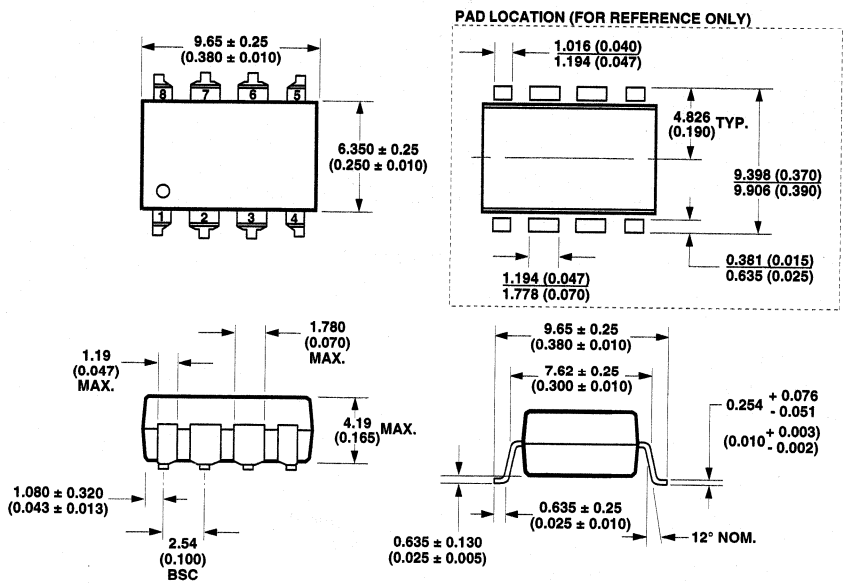
Package Outline Drawings

8-Pin DIP Package (HCPL-2731/HCPL-2730)



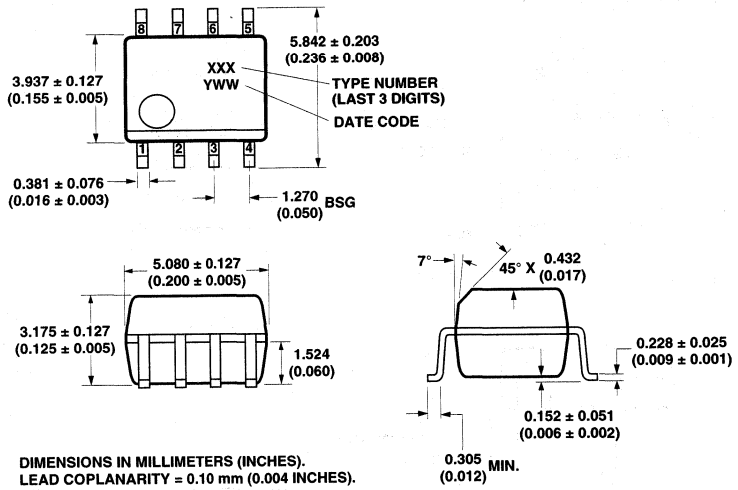
DIMENSIONS IN MILLIMETERS AND (INCHES).
*MARKING CODE LETTER FOR OPTION NUMBERS
"L" = OPTION 020
OPTION NUMBERS 300 AND 500 NOT MARKED.

8-Pin DIP Package with Gull Wing Surface Mount Option 300 (HCPL-2731/HCPL-2730)

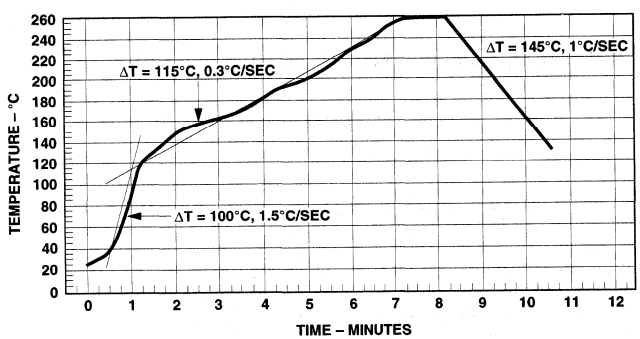


DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES).

Small Outline SO-8 Package (HCPL-0731/HCPL-0730)



Solder Reflow Temperature Profile (HCPL-073X and Gull Wing Surface Mount Option 300 Parts).



Note: Use of nonchlorine activated fluxes is highly recommended.

Regulatory Information

The HCPL-2731/2730 have been approved by the following organizations:

UL

Recognized under UL 1577, Component Recognition Program, File E55361.

CSA

Approved under CSA Component Acceptance Notice #5, File CA 88324.

Insulation Related Specifications (HCPL-2731/2730/0731/0730)

Parameter	Symbol	8-Pin DIP (300 Mil) Value	SO-8 Value	Units	Conditions
Minimum External Air Gap (External Clearance)	L(101)	7.1	4.9	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L(102)	7.4	4.8	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	0.08	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity.
Tracking Resistance (Comparative Tracking Index)	CTI	200	200	Volts	DIN IEC 112/ VDE 0303 Part 1
Isolation Group		IIIa	IIIa		Material Group DIN VDE 0110

Option 300 – surface mount classification is Class A in accordance with CECC 00802.

Absolute Maximum Ratings (No Derating Required up to 85°C)

Parameter	Symbol	Min.	Max.	Units
Storage Temperature	T_S	-55	125	°C
Operating Temperature	T_A	-40	85	°C
Average Forward Input Current	$I_{F(AVG)}$		20	mA
Peak Forward Input Current (50% Duty Cycle, 1 ms Pulse Width)	I_{FPK}		40	mA
Reverse Input Voltage (Each Channel)	V_R		5	V
Input Power Dissipation (Each Channel)	P_I		35	mW
Output Current (Each Channel)	I_O		60	mA
Supply Voltage and Output Voltage (HCPL-2731, HCPL-0731) (V_{CC} - Pin 8-5, V_O - Pin 7,6-5) -Note 1	V_{CC}	-0.5	18	V
Supply Voltage and Output Voltage (HCPL-2730, HCPL-0730) (V_{CC} - Pin 8-5, V_O - Pin 7,6-5) -Note 1	V_{CC}	-0.5	7	V
Output Power Dissipation (Each Channel) -Note 12	P_O		100	mW
Total Power Dissipation (Each Channel)	P_T		135	mW
Lead Solder Temperature (for Through Hole Devices)	260°C for 10 sec., 1.6 mm below seating plane			
Reflow Temperature Profile (for SOIC-8 and Option #300)	See Package Outline Drawings section			

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage (HCPL-2731/HCPL-0731)	V_{CC}	4.5	18	V
Power Supply Voltage (HCPL-2730/HCPL-0730)	V_{CC}	4.5	7	V
Forward Input Current (ON)	$I_{F(ON)}$	0.5	12	mA
Forward Input Voltage (OFF)	$V_{F(OFF)}$	0	0.8	V
Operating Temperature	T_A	0	70	°C

Electrical Specifications

$0°C \le T_A \le 70°C$, $4.5\ V \le V_{CC} \le 18\ V$, $0.5\ mA \le I_{F(ON)} \le 12\ mA$, $0\ V \le V_{F(OFF)} \le 0.8\ V$, unless otherwise specified. All Typicals at $T_A = 25°C$. (See note 8.)

Parameter	Sym.	Device HCPL-	Min.	Typ.*	Max.	Units	Test Conditions		Fig.	Note
Current Transfer Ratio	CTR	2731 0731	400	1800	5000	%	$I_F = 0.5\ mA$	$V_{CC} = 4.5$ $V_O = 0.4\ V$	2, 3	2
			500	1600	2600		$I_F = 1.6\ mA$			
		2730/0730	300	1600	2600		$I_F = 1.6\ mA$			
Logic Low Output Voltage	V_{OL}	2731 0731		0.1	0.4	V	$I_F = 1.6\ mA$, $I_O = 8\ mA$	$V_{CC} = 4.5\ V$	1	
				0.1	0.4		$I_F = 5.0\ mA$, $I_O = 15\ mA$			
				0.2	0.4		$I_F = 12\ mA$, $I_O = 24\ mA$			
		2730/0730		0.1	0.4		$I_F = 1.6\ mA$, $I_O = 4.8\ mA$			
Logic High Output Current	I_{OH}	2731/0731		0.05	100	μA	$V_O = V_{CC} = 18\ V$	$I_F = 0\ mA$		2
		2730/0731		0.1	250		$V_O = V_{CC} = 7\ V$			
Logic Low Supply Current	I_{CCL}	2731/0731		1.2	3	mA	$V_{CC} = 18\ V$	$I_{F1} = I_{F2} = 1.6\ mA$, $V_{O1} = V_{O2} = Open$	5	
		2730/0730		0.9			$V_{CC} = 7\ V$			
Logic High Supply Current	I_{CCH}	2731/0731		0.005	20	μA	$V_{CC} = 18\ V$	$I_{F1} = I_{F2} = 0\ mA$, $V_{O1} = V_{O2} = Open$	5	
		2730/0730		0.004			$V_{CC} = 7\ V$			
Input Forward Voltage	V_F			1.4	1.7	V	$T_A = 25°C$		4	
					1.75		$I_F = 1.6\ mA$			
Input Reverse Breakdown Voltage	BV_R		5.0			V	$I_R = 10\ \mu A$, $T_A = 25°C$			2
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			-1.8		mV/°C	$I_F = 1.6\ mA$			
Input Capacitance	C_{IN}			60		pF	f = 1 MHz, $V_F = 0$			2

*All typical values at $T_A = 25°C$ and $V_{CC} = 5\ V$, unless otherwise noted.

Switching Specifications (AC)

Over recommended operating conditions (T_A = 0°C to 70°C), V_{CC} = 5 V, unless otherwise specified. (See note 8.)

Parameter	Sym.	Device HCPL-	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to Logic Low at Output	t_{PHL}	2731 0731		25	100	µs	T_A = 25°C	6, 7, 8, 9	2
					120		I_F = 0.5 mA Rl = 4.7 kΩ		
		2730 2731 0730 0731		5	20		T_A = 25°C		
					25		I_F = 1.6 mA, Rl = 2.2 kΩ		
				0.5	2		T_A = 25°C		
					3		I_F = 12 mA, Rl = 270 Ω		
Propagation Delay Time to Logic High at Output	t_{PLH}	2731 0731		10	60	µs	T_A = 25°C	7, 8, 9	2
					90		I_F = 0.5 mA, Rl = 4.7 kΩ		
		2730 2731 0730 0731		10	35		T_A = 25°C		
					50		I_F = 1.6 mA, Rl = 2.2 kΩ		
				1	10		T_A = 25°C		
					15		I_F = 12 mA, Rl = 270 Ω		
Common Mode Transient Immunity at Logic High Output	$\|CM_H\|$		1000	10000		V/µs	I_F = 0 mA, T_A = 25°C, Rl = 2.2 kΩ $\|V_{CM}\|$ = 10 V_{p-p}	10	2, 6, 7
Common Mode Transient Immunity at Logic Low Level Output	$\|CM_L$		1000	10000		V/µs	I_F = 1.6 mA, T_A = 25°C, Rl = 2.2 kΩ $\|V_{CM}\|$ = 10 V_{p-p}		

*All typical values at T_A = 25°C and V_{CC} = 5 V, unless otherwise noted.

Package Characteristics

Parameter	Symbol	Device HCPL-	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage**	V_{ISO}		2500			V rms	RH ≤ 50%, t = 1 min., T_A = 25°C		4, 9
Option 020		2730 2731	5000						4, 10
Resistance (Input-Output)	R_{I-O}			10^{12}		Ω	V_{I-O} = 500 VDC RH ≤ 45%		4
Capacitance (Input-Output)	C_{I-O}			0.6		pF	f = 1 MHz		11
Input-Input Insulation Leakage Current	I_{I-I}		0.005			μA	RH ≤ 45% V_{I-I} = 500 VDC		5
Input-Input Insulation Leakage Current	R_{I-I}			10^{11}		Ω			5
Capacitance (Input-Input)	C_{I-I}	2730 2731		0.03		pF			5
		0730 0731		0.25					

*All Typical values at T_A = 25°C unless otherwise noted.
**The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the VDE 0884 Insulation Characteristics Table (if applicable), your equipment level safety specification or HP Application Note 1074 entitled "Optocoupler Input-Output Endurance Voltage."

Notes:
1. Pin 5 should be the most negative voltage at the detector side.
2. Each channel.
3. DC CURRENT TRANSFER RATIO (CTR) is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
4. Device considered a two-terminal device: pins 1, 2, 3, and 4 shorted together, and pins 5, 6, 7, and 8 shorted together.
5. Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.
6. Common mode transient immunity in a Logic High level is the maximum tolerable (positive) dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (i.e., V_O > 2.0 V). Common mode transient immunity in a Logic Low level is the maximum tolerable (negative) dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., V_O < 0.8 V).
7. In applications where dV/dt may exceed 50,000 V/μs (such as static discharge) a series resistor, R_{CC}, should be included to protect the detector IC from destructively high surge currents. The recommended value is R_{CC} = 110 Ω.
8. Use of a 0.1 μF bypass capacitor connected between pins 5 and 8 adjacent to the device is recommended.
9. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage > 3000 V rms for 1 second (leakage detection current limit, I_{I-O} < 5 μA).
10. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage > 6000 V rms for 1 second (leakage detection current limit, I_{I-O} < 5 μA).
11. Measured between the LED anode and cathode shorted together and pins 5 through 8 shorted together.
12. Derate linearly above 65°C free-air temperature at a rate of 2.3 mW/°C for the SO-8 package.

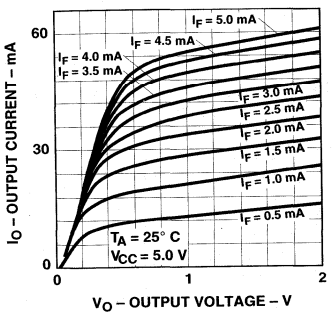


Figure 1. DC Transfer Characteristics.

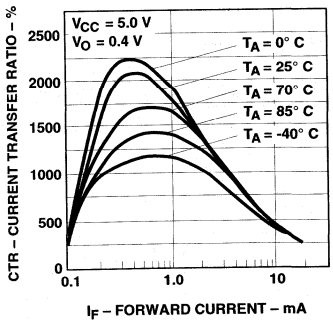


Figure 2. Current Transfer Ratio vs. Forward Current.

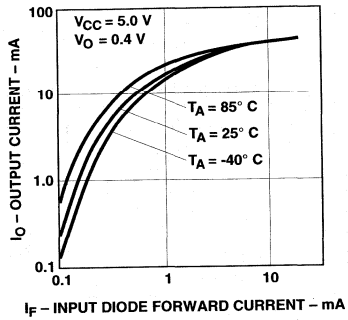


Figure 3. Output Current vs. Input Diode Forward Current.

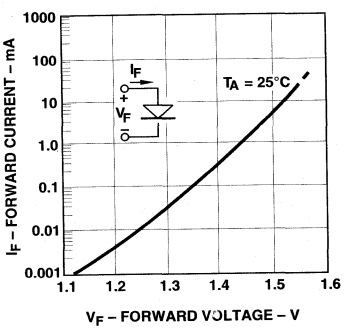


Figure 4. Input Diode Forward Current vs. Forward Voltage.

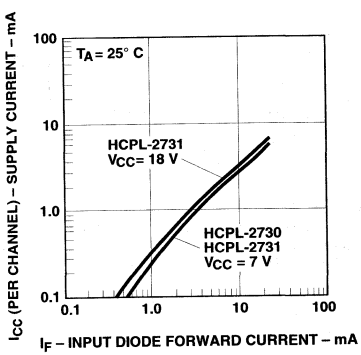


Figure 5. Supply Current per Channel vs. Input Diode Forward Current.

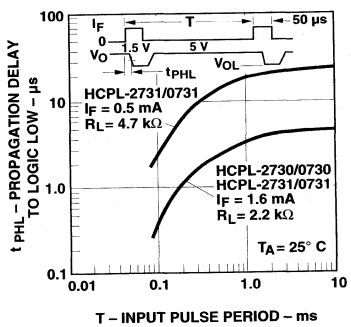


Figure 6. Propagation Delay to Logic Low vs. Pulse Period.

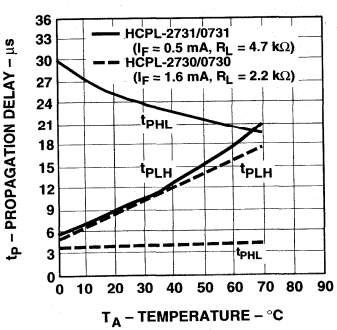


Figure 7. Propagation Delay vs. Temperature.

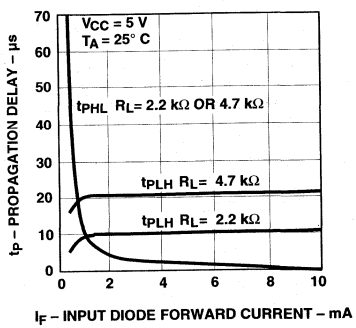


Figure 8. Propagation Delay vs. Input Diode Forward Current.

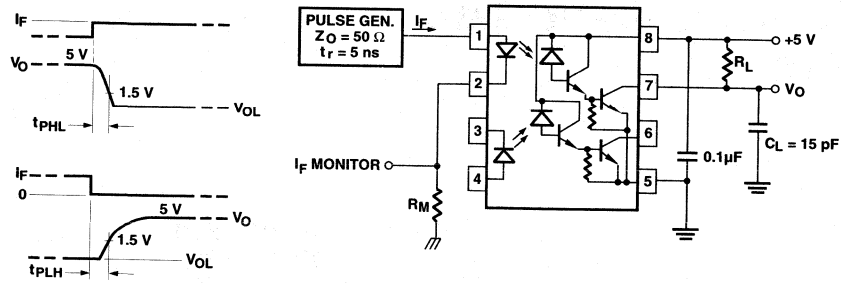


Figure 9. Switching Test Circuit.

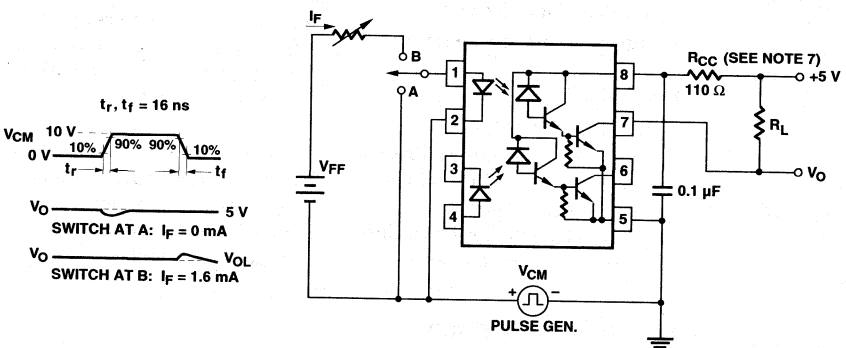


Figure 10. Test Circuit for Transient Immunity and Typical Waveforms.

HEWLETT® PACKARD

Low Input Current Logic Gate Optocouplers

Technical Data

HCPL-2200
HCPL-2219

Features

- **2.5 kV/µs Minimum Common Mode Rejection (CMR) at V_{CM} = 400 V (HCPL-2219)**
- **Compatible with LSTTL, TTL, and CMOS Logic**
- **Wide V_{CC} Range (4.5 to 20 V)**
- **2.5 Mbd Guaranteed over Temperature**
- **Low Input Current (1.6 mA)**
- **Three State Output (No Pullup Resistor Required)**
- **Guaranteed Performance from 0°C to 85°C**
- **Hysteresis**
- **Safety Approval**
  UL Recognized -2500 V rms for 1 minute
  CSA Approved
  VDE 0884 Approved with V_{IORM} = 630 V_{peak} (HCPL-2219 Option 060 Only)
- **MIL-STD-1772 Version Available (HCPL-5200/1)**

Applications

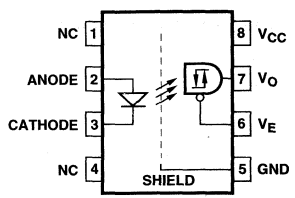
- **Isolation of High Speed Logic Systems**
- **Computer-Peripheral Interfaces**
- **Microprocessor System Interfaces**
- **Ground Loop Elimination**
- **Pulse Transformer Replacement**
- **Isolated Buss Driver**
- **High Speed Line Receiver**

Description

The HCPL-2200/2219 are optically coupled logic gates that combine a GaAsP LED and an integrated high gain photo detector. The detector has a three state output stage and has a detector threshold with hysteresis. The three state output eliminates the need for a pullup resistor and allows for direct drive of data busses. The hysteresis provides differential mode noise immunity and eliminates the potential for output signal chatter.

A superior internal shield on the HCPL-2219 guarantees common mode transient immunity of 2.5 kV/µs at a common mode voltage of 400 volts.

Functional Diagram



TRUTH TABLE (POSITIVE LOGIC)

LED	ENABLE	OUTPUT
ON	H	Z
OFF	H	Z
ON	L	H
OFF	L	L

A 0.1 µF bypass capacitor must be connected between pins 5 and 8.

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

The Electrical and Switching Characteristics of the HCPL-2200/2219 are guaranteed over the temperature range of 0°C to 85°C and a V_{CC} range of 4.5 volts to 20 volts. Low I_F and wide V_{CC} range allow compatibility with TTL, LSTTL, and CMOS logic and result in lower power consumption compared to other high speed optocouplers. Logic signals are transmitted with a typical propagation delay of 160 nsec. The HCPL-2200/2219 are useful for isolating high speed logic interfaces, buffering of input and output lines, and implementing isolated line receivers in high noise environments.

Selection Guide

Minimum CMR			8-Pin DIP (300 Mil)		Small-Outline SO-8	Widebody (400 Mil)	Hermetic
dV/dt (V/μs)	V_{CM} (V)	Input On-Current (mA)	Single Channel Package	Dual Channel Package	Single Channel Package	Single Channel Package	Single and Dual Channel Packages
1,000	50	1.6	HCPL-2200[1] HCPL-2201 HCPL-2202		HCPL-0201	HCNW2201	
		1.8		HCPL-2231			
2,500	400	1.6	HCPL-2219[1]				
5,000[2]	300[2]	1.6	HCPL-2211 HCPL-2212		HCPL-0211	HCNW2211	
		1.8		HCPL-2232			
1,000	50	2.0					HCPL-52XX HCPL-62XX

Notes:
1. HCPL-2200/2219 devices include output enable/disable functionality.
2. Minimum CMR of 10 kV/μs with V_{CM} = 1000 V can be achieved with input current, I_F, of 5 mA.

Ordering Information

Specify Part Number followed by Option Number (if desired).

Example:

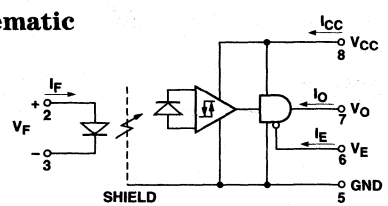
HCPL-2219#XXX

- 060 = VDE 0884 V_{IORM} = 630 Vpeak Option*
- 300 = Gull Wing Surface Mount Option
- 500 = Tape and Reel Packaging Option

Option data sheets available. Contact your Hewlett-Packard sales representative or authorized distributor for information.

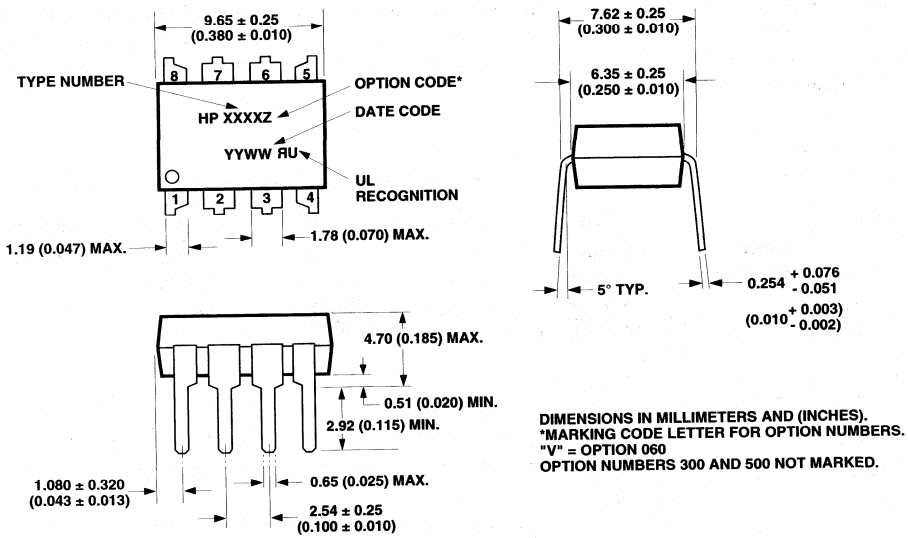
*For HCPL-2219 only.

Schematic



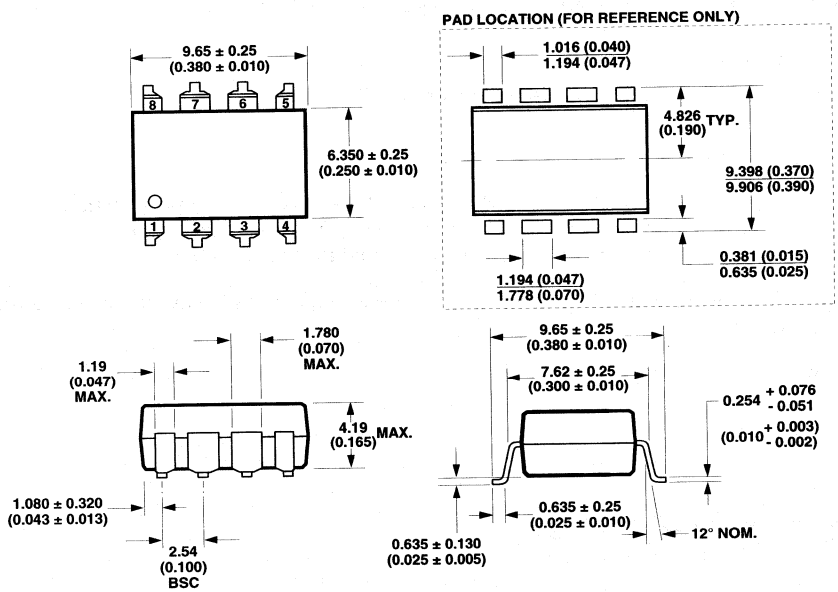
Package Outline Drawings

8-Pin DIP Package



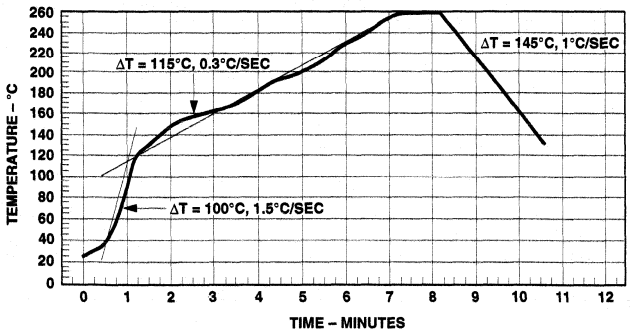
DIMENSIONS IN MILLIMETERS AND (INCHES).
*MARKING CODE LETTER FOR OPTION NUMBERS.
"V" = OPTION 060
OPTION NUMBERS 300 AND 500 NOT MARKED.

8-Pin DIP Package with Gull Wing Surface Mount Option 300



DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES).

Maximum Solder Reflow Thermal Profile



Note: Use of nonchlorine activated fluxes is highly recommended.

Regulatory Information

The HCPL-2200/2219 have been approved by the following organizations:

UL

Recognized under UL 1577, Component Recognition Program, File E55361.

CSA

Approved under CSA Component Acceptance Notice #5, File CA 88324.

VDE

Approved according to VDE 0884/06.92. (HCPL-2219 Option 060 Only)

Insulation and Safety Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min. External Air Gap (External Clearance)	L(IO1)	7.1	mm	Measured from input terminals to output terminals, shortest distance through air.
Min. External Tracking Path (External Creepage)	L(IO2)	7.4	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity.
Tracking Resistance (Comparative Tracking Index)	CTI	200	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Option 300 - surface mount classification is Class A in accordance with CECC 00802.

VDE 0884 Insulation Related Characteristics (HCPL-2219 OPTION 060 ONLY)

Description	Symbol	Characteristic	Units
Installation classification per DIN VDE 0110/1.89, Table 1 for rated mains voltage ≤ 300 V rms		I-IV	
for rated mains voltage ≤ 450 V rms		I-III	
Climatic Classification		55/85/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	630	V peak
Input to Output Test Voltage, Method b* V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial Discharge < 5 pC	V_{PR}	1181	V peak
Input to Output Test Voltage, Method a* V_{IORM} x 1.5 = V_{PR}, Type and sample test, t_m = 60 sec, Partial Discharge < 5 pC	V_{PR}	945	V peak
Highest Allowable Overvoltage* (Transient Overvoltage, t_{ini} = 10 sec)	V_{IOTM}	6000	V peak
Safety Limiting Values (Maximum values allowed in the event of a failure, also see Figure 12, Thermal Derating curve.)			
Case Temperature	T_S	175	°C
Input Current	$I_{S,INPUT}$	230	mA
Output Power	$P_{S,OUTPUT}$	600	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	$\geq 10^9$	Ω

*Refer to the front of the optocoupler section of the current catalog, under Product Safety Regulations section, (VDE 0884), for a detailed description.

Note: Isolation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuits in application.

Absolute Maximum Ratings

(No Derating Required up to 70°C)

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	T_S	-55	125	°C	
Operating Temperature	T_A	-40	85	°C	1
Average Forward Input Current	$I_{F(AVG)}$		10	mA	
Peak Transient Input Current (≤ 1 μs Pulse Width, 300 pps)	$I_{F(TRAN)}$		1.0	A	
Reverse Input Voltage	V_R		5	V	
Average Output Current	I_O		25	mA	
Supply Voltage	V_{CC}	0	20	V	
Three State Enable Voltage	V_E	-0.5	20	V	
Output Voltage	V_O	-0.5	20	V	
Total Package Power Dissipation	P_T		210	mW	1
Lead Solder Temperature	260°C for 10 sec., 1.6 mm below seating plane				
Solder Reflow Temperature Profile	See Package Outline Drawings section				

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage	V_{CC}	4.5	20	V
Enable Voltage High	V_{EH}	2.0	20	V
Enable Voltage Low	V_{EL}	0	0.8	V
Forward Input Current	$I_{F(ON)}$	1.6*	5	mA
Forward Input Current	$I_{F(OFF)}$	–	0.1	mA
Operating Temperature	T_A	0	85[1]	°C
Fan Out	N		4	TTL Loads

*The initial switching threshold is 1.6 mA or less. It is recommended that 2.2 mA be used to permit at least a 20% CTR degradation guardband.

Electrical Specifications

For $0°C \le T_A$[1] $\le 85°C$, $4.5\ V \le V_{CC} \le 20\ V$, $1.6\ mA \le I_{F(ON)} \le 5\ mA$, $2.0\ V \le V_{EH} \le 20\ V$, $0.0\ V \le V_{EL} \le 0.8\ V$, $0\ mA \le I_{F(OFF)} \le 0.1\ mA$. All Typicals at $T_A = 25°C$, $V_{CC} = 5\ V$, $I_{F(ON)} = 3\ mA$ unless otherwise specified. See Note 7.

Parameter	Sym.	Min.	Typ.	Max.	Units	Test Conditions		Fig.	Note
Logic Low Output Voltage	V_{OL}			0.5	V	$I_{OL} = 6.4\ mA$ (4 TTL Loads)		1	
Logic High Output Voltage	V_{OH}	2.4	*		V	$I_{OH} = -2.6\ mA$ *$V_{OH} = V_{CC} - 2.1\ V$		2	
Output Leakage Current ($V_{OUT} > V_{CC}$)	I_{OHH}			100	µA	$V_O = 5.5\ V$	$I_F = 5\ mA$, $V_{CC} = 4.5\ V$		
				500	µA	$V_O = 20\ V$			
Logic High Enable Voltage	V_{EH}	2.0			V				
Logic Low Enable Voltage	V_{EL}			0.8	V				
Logic High Enable Current	I_{EH}			20	µA	$V_{EN} = 2.7\ V$			
				100	µA	$V_{EN} = 5.5\ V$			
			0.004	250	µA	$V_{EN} = 20\ V$			
Logic Low Enable Current	I_{EL}			-0.32	mA	$V_{EN} = 0.4\ V$			
Logic Low Supply Current	I_{CCL}		4.5	6.0	mA	$V_{CC} = 5.5\ V$	$I_F = 0\ mA$, I_O = Open, V_E = Don't Care		
			5.25	7.5	mA	$V_{CC} = 20\ V$			
Logic High Supply Current	I_{CCH}		2.7	4.5	mA	$V_{CC} = 5.5\ V$	$I_F = 5\ mA$, I_O = Open, V_E = Don't Care		
			3.1	6.0	mA	$V_{CC} = 20\ V$			
High Impedance State Output Current	I_{OZL}			-20	µA	$V_O = 0.4\ V$	$V_{EN} = 2\ V$, $I_F = 5\ mA$		
	I_{OZH}			20	µA	$V_O = 2.4\ V$	$V_{EN} = 2\ V$, $I_F = 5\ mA$		
				100	µA	$V_O = 5.5\ V$			
				500	µA	$V_O = 20\ V$			
Logic Low Short Circuit Output Current	I_{OSL}	25			mA	$V_O = V_{CC} = 5.5\ V$	$I_F = 0\ mA$		2
		40			mA	$V_O = V_{CC} = 20\ V$			
Logic High Short Circuit Output Current	I_{OSH}	-10			mA	$V_{CC} = 5.5\ V$	$I_F = 5\ mA$, V_O = GND		2
		-25			mA	$V_{CC} = 20\ V$			
Input Current Hysteresis	I_{HYS}		0.12		mA	$V_{CC} = 5\ V$		3	
Input Forward Voltage	V_F		1.5	1.7	V	$T_A = 25°C$	$I_F = 5\ mA$	4	
				1.75					
Input Reverse Breakdown Voltage	BV_R	5			V	$I_R = 10\ µA$			
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$		-1.7		mV/°C	$I_F = 5\ mA$			
Input Capacitance	C_{IN}		60		pF	f = 1 MHz, $V_F = 0\ V$, Pins 2 and 3			

Switching Specifications (AC)

For 0°C ≤ T_A[1] ≤ 85°C, 4.5 V ≤ V_{CC} ≤ 20 V, 1.6 mA ≤ $I_{F(ON)}$ ≤ 5 mA, 0.0 mA ≤ $I_{F(OFF)}$ ≤ 0.1 mA.
All Typicals at T_A = 25°C, V_{CC} = 5 V, $I_{F(ON)}$ = 3 mA unless otherwise specified.

Parameter	Sym.	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to Logic Low Output Level	t_{PHL}		210		ns	Without Peaking Capacitor	5, 6	4, 5
			160	300		With Peaking Capacitor		
Propagation Delay Time to Logic High Output Level	t_{PLH}		170		ns	Without Peaking Capacitor	5. 6	4. 5
			115	300		With Peaking Capacitor		
Output Enable Time to Logic High	t_{PZH}		25		ns		7, 9	
Output Enable Time to Logic Low	t_{PZL}		28		ns		7, 8	
Output Disable Time from Logic High	t_{PHZ}		105		ns		7, 9	
Output Disable Time from Logic Low	t_{PLZ}		60		ns		7, 8	
Output Rise Time (10-90%)	t_r		55		ns		5, 10	
Output Fall Time (90-10%)	t_f		15		ns		5, 10	

Parameter	Sym.	Device	Min.	Units	Test Conditions		Fig.	Note
Logic High Common Mode Transient Immunity	$\|CM_H\|$	HCPL-2200	1,000	V/μs	$\|V_{CM}\|$ = 50 V	I_F = 1.6 mA, V_{CC} = 5 V, T_A = 25°C	11	6
		HCPL-2219	2,500	V/μs	$\|V_{CM}\|$ = 400 V			
Logic Low Common Mode Transient Immunity	$\|CM_L\|$	HCPL-2200	1,000	V/μs	$\|V_{CM}\|$ = 50 V	V_F = 0 V, V_{CC} = 5 V, T_A = 25°C	11	6
		HCPL-2219	2,500	V/μs	$\|V_{CM}\|$ = 400 V			

Package Characteristics

Parameter	Sym.	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage*	V_{ISO}	2500			V rms	RH ≤ 50%, t = 1 min., T_A = 25°C		3, 8
Input-Output Resistance	R_{I-O}		10^{12}		Ω	V_{I-O} = 500 VDC		3
Input-Output Capacitance	C_{I-O}		0.6		pF	f = 1 MHz, V_{I-O} = 0 VDC		3

*The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the VDE 0884 Insulation Characteristics Table (if applicable), your equipment level safety specification or HP Application Note 1074 entitled "Optocoupler Input-Output Endurance Voltage," publication number 5963-2203E.

Notes:

1. Derate total package power dissipation, P_T, linearly above 70°C free air temperature at a rate of 4.5 mW/°C.
2. Duration of output short circuit time should not exceed 10 ms.
3. Device considered a two-terminal device: pins 1, 2, 3, and 4 shorted together and pins 5, 6, 7, and 8 shorted together.
4. The t_{PLH} propagation delay is measured from the 50% point on the leading edge of the input pulse to the 1.3 V point on the leading edge of the output pulse. The t_{PHL} propagation delay is measured from the 50% point on the trailing edge of the input pulse to the 1.3 V point on the trailing edge of the output pulse.
5. When the peaking capacitor is omitted, propagation delay times may increase by 100 ns.
6. CM_L is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic low state (V_O < 0.8 V). CM_H is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic high state (V_O > 2.0 V).
7. Use of a 0.1 μF bypass capacitor connected between pins 5 and 8 is recommended.
8. In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 3000 V rms for one second (leakage detection current limit, I_{I-O} ≤ 5 μA). This test is performed before the 100% production test for partial discharge (Method b) shown in the VDE 0884 Insulation Characteristics Table, if applicable.

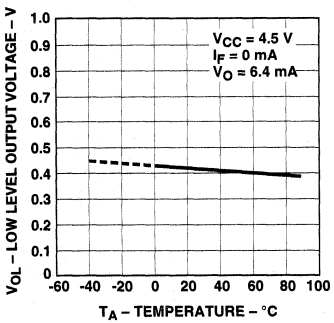


Figure 1. Typical Logic Low Output Voltage vs. Temperature.

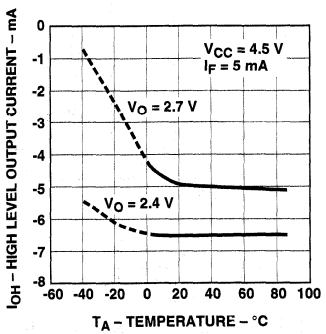


Figure 2. Typical Logic High Output Current vs. Temperature.

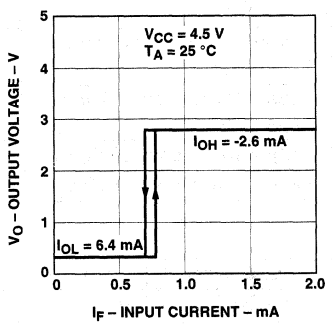


Figure 3. Output Voltage vs. Forward Input Current.

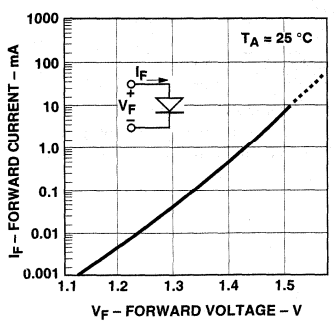


Figure 4. Typical Input Diode Forward Characteristic.

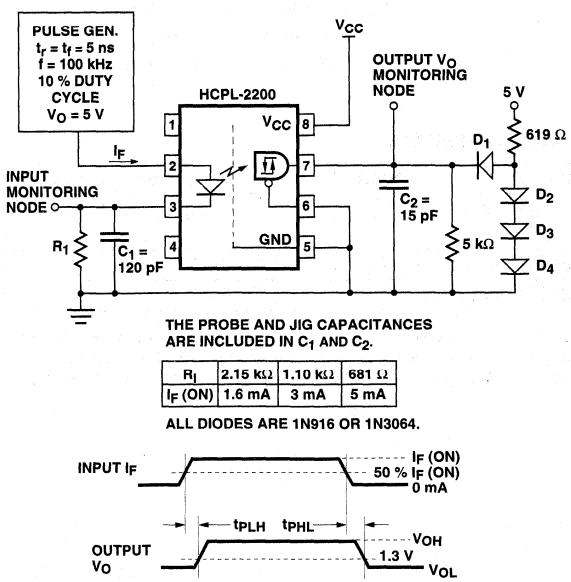


Figure 5. Test Circuit for t_{PLH}, t_{PHL}, t_r, and t_f.

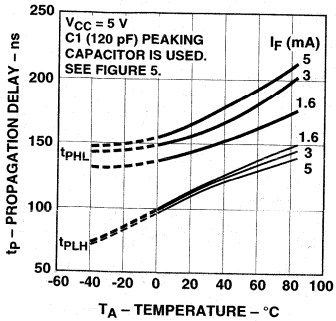


Figure 6. Typical Propagation Delays vs. Temperature.

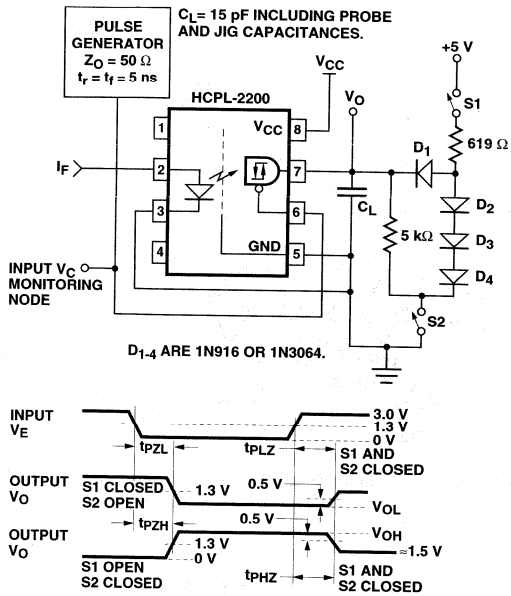


Figure 7. Test Circuit for t_{PHZ}, t_{PZH}, t_{PLZ}, and t_{PZL}.

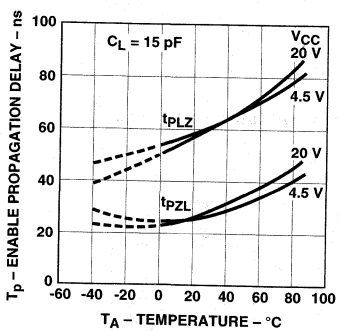


Figure 8. Typical Logic Low Enable Propagation Delay vs. Temperature.

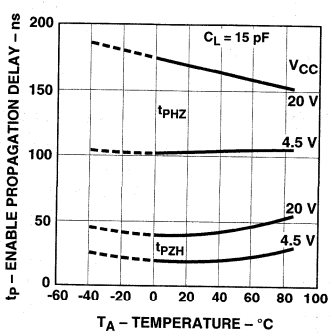


Figure 9. Typical Logic High Enable Propagation Delay vs. Temperature.

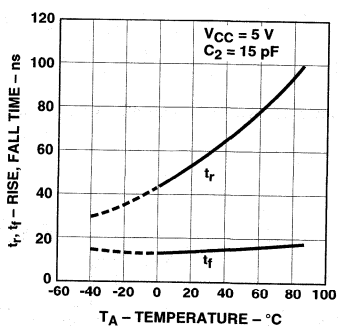


Figure 10. Typical Rise, Fall Time vs. Temperature.

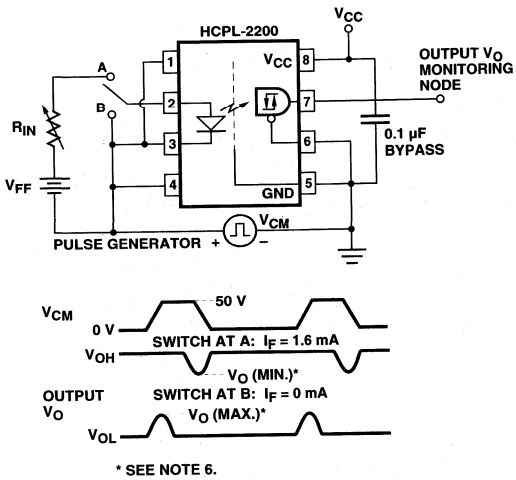


Figure 11. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

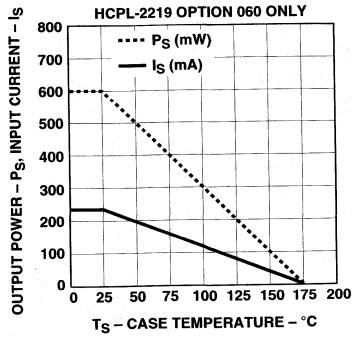


Figure 12. Thermal Derating Curve, Dependence of Safety Limiting Value with Case Temperature per VDE 0884.

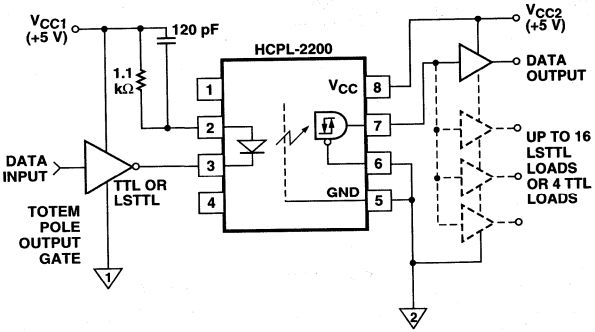


Figure 13. Recommended LSTTL to LSTTL Circuit.

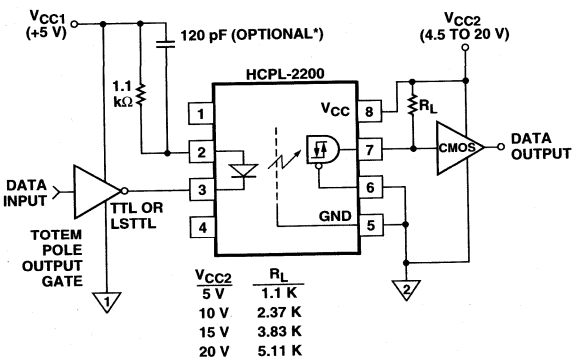


Figure 14. LSTTL to CMOS Interface Circuit.

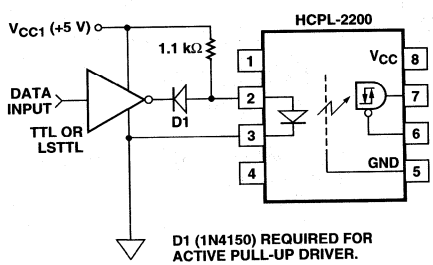


Figure 15. Recommended LED Drive Circuit.

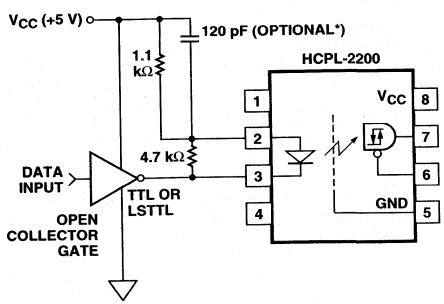


Figure 16. Series LED Drive with Open Collector Gate (4.7 kΩ Resistor Shunts I_{OH} from the LED).

*The 120 pF capacitor may be omitted in applications where 500 ns propagation delay is sufficient.

Very High CMR, Wide V_{CC} Logic Gate Optocouplers

Technical Data

HCPL-2201 HCPL-2202
HCPL-2211 HCPL-2212
HCPL-2231 HCPL-2232
HCPL-0201 HCPL-0211
HCNW2201 HCNW2211

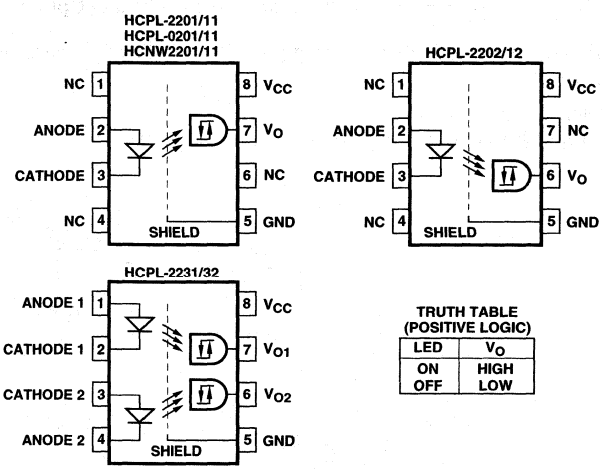
Features

- **10 kV/µs Minimum Common Mode Rejection (CMR) at V_{CM} = 1000 V (HCPL-2211/2212/0211/2232, HCNW2211)**
- **Wide Operating V_{CC} Range: 4.5 to 20 Volts**
- **300 ns Propagation Delay Guaranteed over the Full Temperature Range**
- **5 Mbd Typical Signal Rate**
- **Low Input Current (1.6 mA to 1.8 mA)**
- **Hysteresis**
- **Totem Pole Output (No Pullup Resistor Required)**
- **Available in 8-Pin DIP, SOIC-8, Widebody Packages**
- **Guaranteed Performance from -40°C to 85°C**
- **Safety Approval**
  UL Recognized -2500 V rms for 1 minute (5000 V rms for 1 minute for HCNW22XX) per UL1577
  CSA Approved
  VDE 0884 Approved with V_{IORM} = 630 V peak (HCPL-2211/2212 Option 060 only) and V_{IORM} = 1414 V peak (HCNW22XX only)
  BSI Certified (HCNW22XX only)
- **MIL-STD-1772 Version Available (HCPL-52XX/62XX)**

Applications

- **Isolation of High Speed Logic Systems**
- **Computer-Peripheral Interfaces**
- **Microprocessor System Interfaces**
- **Ground Loop Elimination**
- **Pulse Transformer Replacement**
- **High Speed Line Receiver**
- **Power Control Systems**

Functional Diagram



TRUTH TABLE (POSITIVE LOGIC)

LED	V_O
ON	HIGH
OFF	LOW

Description

The HCPL-22XX, HCPL-02XX, and HCNW22XX are optically-coupled logic gates. The HCPL-22XX, and HCPL-02XX contain a GaAsP LED while the HCNW22XX contains an AlGaAs LED. The detectors have totem pole output stages and optical receiver input stages with built-in Schmitt triggers to provide logic-compatible waveforms, eliminating the need for additional waveshaping.

A superior internal shield on the HCPL-2211/12, HCPL-0211,

A 0.1 µF bypass capacitor must be connected between pins 5 and 8.

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

HCPL-2232 and HCNW2211 guarantees common mode transient immunity of 10 kV/μs at a common mode voltage of 1000 volts.

The electrical and switching characteristics of the HCPL-22XX, HCPL-02XX and HCNW22XX are guaranteed from -40°C to +85°C and a V_{CC} from 4.5 volts to 20 volts. Low I_F and wide V_{CC} range allow compatibility with TTL, LSTTL, and CMOS logic and result in lower power consumption compared to other high speed couplers. Logic signals are transmitted with a typical propagation delay of 150 ns.

Selection Guide

Minimum CMR		Input	8-Pin DIP (300 Mil)		Small-Outline SO-8	Widebody (400 Mil)	Hermetic
dV/dt (V/μs)	V_{CM} (V)	On-Current (mA)	Single Channel Package	Dual Channel Package	Single Channel Package	Single Channel Package	Single and Dual Channel Packages
1,000	50	1.6	HCPL-2200[1,2] HCPL-2201 HCPL-2202		HCPL-0201	HCNW2201	
		1.8		HCPL-2231			
2,500	400	1.6	HCPL-2219[1,2]				
5,000[3]	300[3]	1.6	HCPL-2211 HCPL-2212		HCPL-0211	HCNW2211	
		1.8		HCPL-2232			
1,000	50	2.0					HCPL-52XX[2] HCPL-62XX[2]

Notes:
1. HCPL-2200/2219 devices include output enable/disable function.
2. Technical data for the HCPL-2200/2219, HCPL-52XX and HCPL-62XX are on separate HP publications.
3. Minimum CMR of 10 kV/μs with V_{CM} = 1000 V can be achieved with input current, I_F, of 5 mA.

Ordering Information

Specify Part Number followed by Option Number (if desired).

Example:

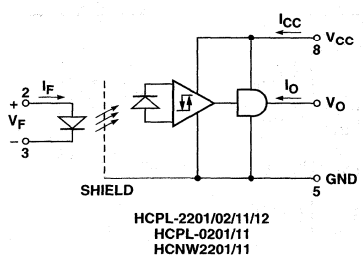
HCPL-2211#XXX

- 060 = VDE 0884 V_{IORM} = 630 V peak Option*
- 300 = Gull Wing Surface Mount Option**
- 500 = Tape and Reel Packaging Option

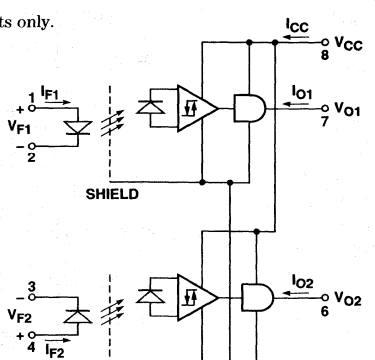
Option data sheets available. Contact your Hewlett-Packard sales representative or authorized distributor for information.

*For HCPL-2211/2212 only.
**Gull wing surface mount option applies to through hole parts only.

Schematic



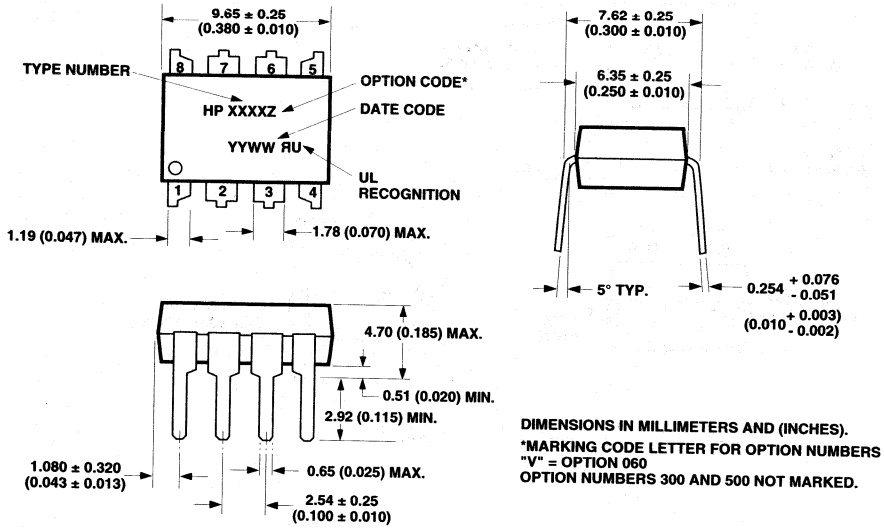
HCPL-2201/02/11/12
HCPL-0201/11
HCNW2201/11



HCPL-2231/32

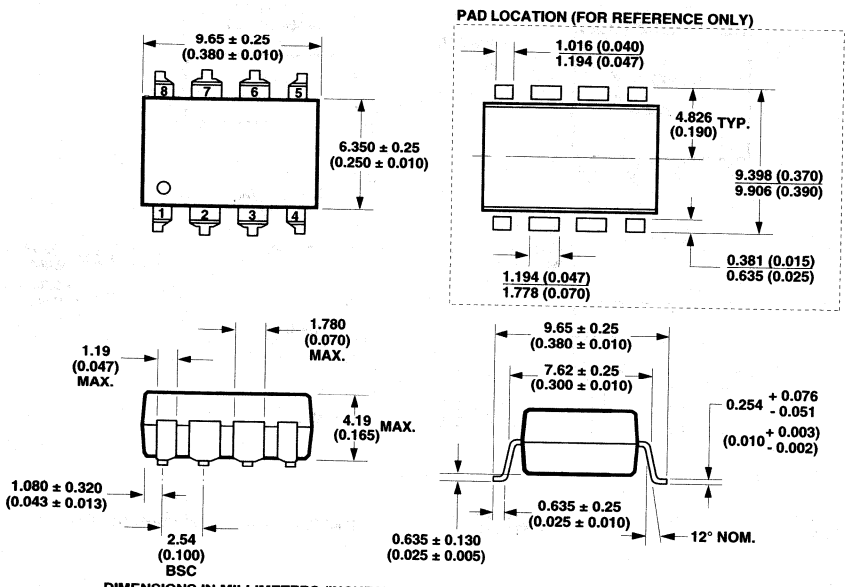
Package Outline Drawings

8-Pin DIP Package (HCPL-2201/02/11/12/31/32)



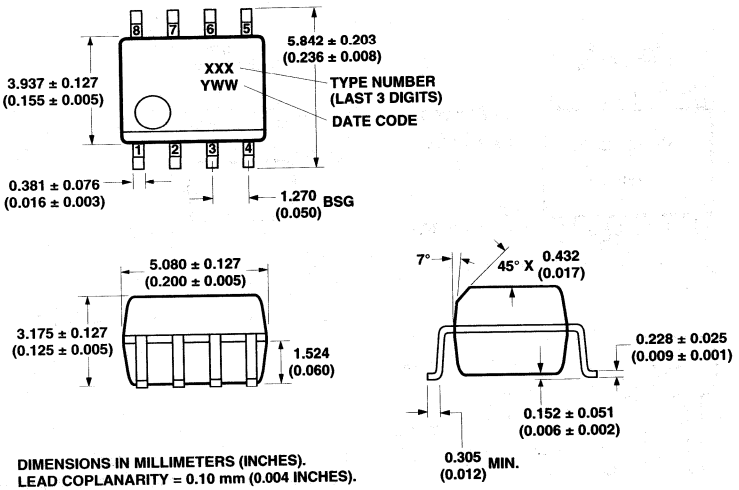
DIMENSIONS IN MILLIMETERS AND (INCHES).
*MARKING CODE LETTER FOR OPTION NUMBERS
"V" = OPTION 060
OPTION NUMBERS 300 AND 500 NOT MARKED.

8-Pin DIP Package with Gull Wing Surface Mount Option 300 (HCPL-2201/02/11/12/31/32)



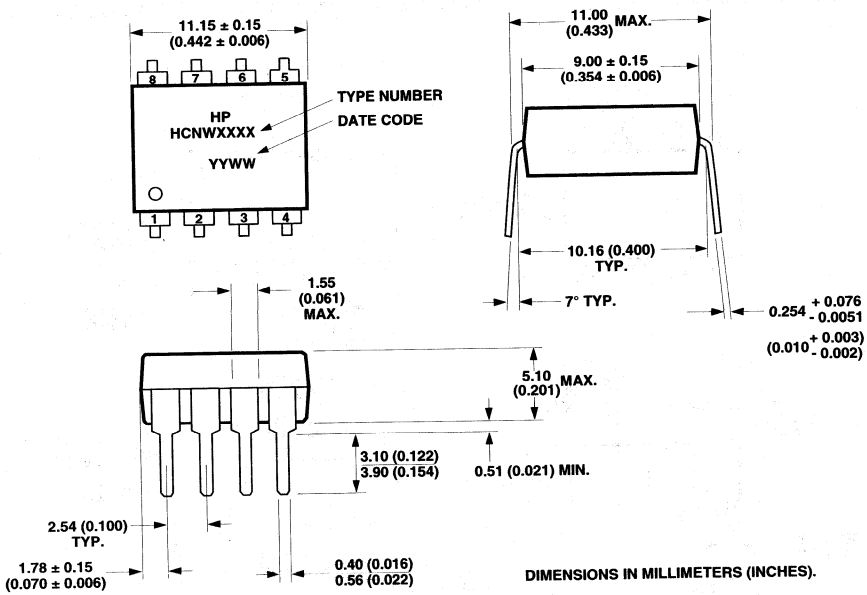
DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES).

Small-Outline SO-8 Package (HCPL-0201/11)



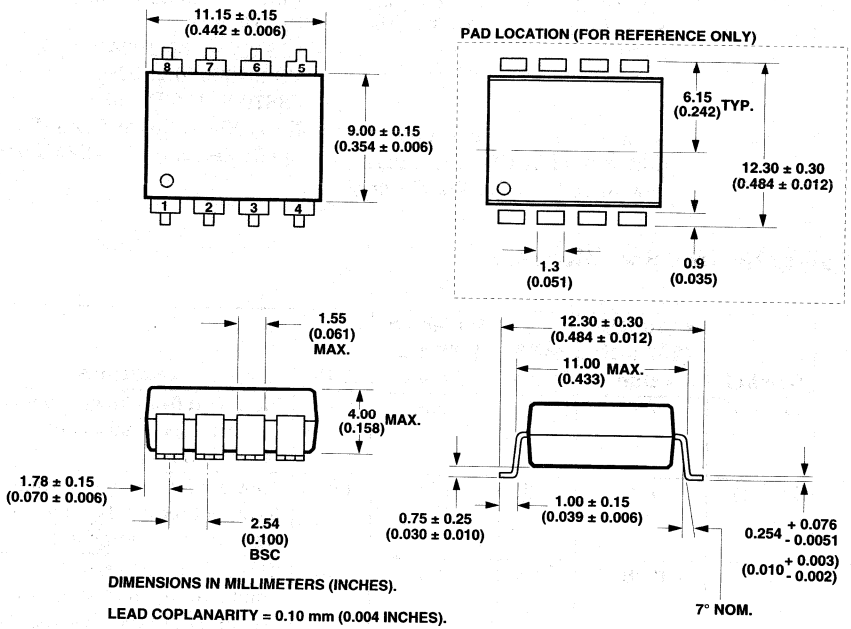
DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES).

8-Pin Widebody DIP Package (HCNW2201/11)

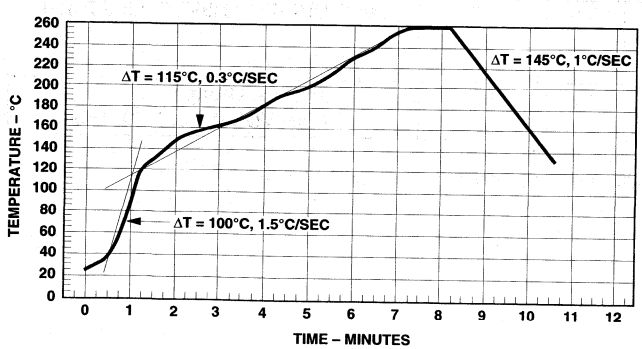


DIMENSIONS IN MILLIMETERS (INCHES).

8-Pin Widebody DIP Package with Gull Wing Surface Mount Option 300 (HCNW2201/11)



Solder Reflow Temperature Profile (HCPL-02XX and Gull Wing Surface Mount Option 300 Parts)



Note: Use of nonchlorine activated fluxes is highly recommended.

Regulatory Information

The HCPL-22XX/02XX and HCNW22XX have been approved by the following organizations:

UL

Recognized under UL 1577, Component Recognition Program, File E55361.

CSA

Approved under CSA Component Acceptance Notice #5, File CA 88324.

VDE

Approved according to VDE 0884/06.92. (HCPL-2211/2212 Option 060 and HCNW22XX only)

BSI

Certification according to BS415:1994, (BS EN60065:1994); BS EN60950:1992 (BS7002:1992) and EN41003:1993 for Class II applications. (HCNW22XX only)

Insulation and Safety Related Specifications

8-pin DIP Package

Parameter	Symbol	8-Pin DIP (300 Mil) Value	SO-8 Value	Widebody (400 Mil) Value	Units	Conditions
Minimum External Air Gap (External Clearance)	L(101)	7.1	4.9	9.6	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L(102)	7.4	4.8	10.0	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	0.08	1.0	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity.
Minimum Internal Tracking (Internal Creepage)		NA	NA	4.0	mm	Measured from input terminals to output terminals, along internal cavity.
Tracking Resistance (Comparative Tracking Index)	CTI	200	200	200	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa	IIIa	IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Option 300 - surface mount classification is Class A in accordance with CECC 00802.

VDE 0884 Insulation Related Characteristics (HCPL-2211/2212 Option 060 ONLY)

Description	Symbol	Characteristic	Units
Installation classification per DIN VDE 0110/1.89, Table 1 for rated mains voltage ≤ 300 V rms		I-IV	
for rated mains voltage ≤ 450 V rms		I-III	
Climatic Classification		55/85/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	630	V peak
Input to Output Test Voltage, Method b* V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial Discharge < 5 pC	V_{PR}	1181	V peak
Input to Output Test Voltage, Method a* V_{IORM} x 1.5 = V_{PR}, Type and sample test, t_m = 60 sec, Partial Discharge < 5 pC	V_{PR}	945	V peak
Highest Allowable Overvoltage* (Transient Overvoltage, t_{ini} = 10 sec)	V_{IOTM}	6000	V peak
Safety Limiting Values (Maximum values allowed in the event of a failure, also see Figure 12, Thermal Derating curve.)			
Case Temperature	T_S	175	°C
Input Current	$I_{S,OUTPUT}$	230	mA
Output Power	$P_{S,OUTPUT}$	600	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	$\geq 10^9$	Ω

*Refer to the front of the optocoupler section of the current catalog, under Product Safety Regulations section (VDE 0884), for a detailed description.

Note: Isolation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuits in application.

VDE 0884 Insulation Related Characteristics (HCNW22XX ONLY)

Description	Symbol	Characteristic	Units
Installation classification per DIN VDE 0110/1.89, Table 1			
for rated mains voltage ≤ 600 V rms		I-IV	
for rated mains voltage ≤ 1000 V rms		I-III	
Climatic Classification		55/100/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	1414	V peak
Input to Output Test Voltage, Method b* V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial Discharge < 5 pC	V_{PR}	2652	V peak
Input to Output Test Voltage, Method a* V_{IORM} x 1.5 = V_{PR}, Type and sample test, t_m = 60 sec, Partial Discharge < 5 pC	V_{PR}	2121	V peak
Highest Allowable Overvoltage* (Transient Overvoltage, t_{ini} = 10 sec)	V_{IOTM}	8000	V peak
Safety Limiting Values (Maximum values allowed in the event of a failure, also see Figure 12, Thermal Derating curve.)			
Case Temperature	T_S	150	°C
Current (Input Current I_F, P_S = 0)	$I_{S,INPUT}$	400	mA
Output Power	$P_{S,OUTPUT}$	700	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	≥ 10^9	Ω

*Refer to the front of the optocoupler section of the current catalog, under Product Safety Regulations section (VDE 0884), for a detailed description.

Note: Isolation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuits in application.

Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Units	Note
Storage Temperature		T_S	-55	125	°C	
Operating Temperature		T_A	-40	85	°C	
Average Forward Input Current		$I_{F(AVG)}$		10	mA	1
Peak Transient Input Current (≤ 1 µs Pulse Width, 300 pps)		$I_{F(TRAN)}$		1.0	A	1
(≤ 200 µs Pulse Width, < 1% Duty Cycle)	HCNW22XX			40	mA	
Reverse Input Voltage		V_R		5	V	1
	HCNW22XX			3		
Average Output Current		I_O		25	mA	1
Supply Voltage		V_{CC}	0	20	V	
Output Voltage		V_O	-0.5	20	V	1
Total Package Power Dissipation		P_T		210	mW	2
	HCPL-223X			294		
Output Power Dissipation		P_O	See Figure 7			1
Lead Solder Temperature (Through Hole Parts Only)		260°C for 10 sec., 1.6 mm below seating plane				
	HCNW22XX	260°C for 10 sec., up to seating plane				
Solder Reflow Temperature Profile (Surface Mount Parts Only)		See Package Outline Drawings section				

Recommended Operating Conditions

Parameter		Symbol	Min.	Max.	Units
Power Supply Voltage		V_{CC}	4.5	20	V
Forward Input Current (ON)		$I_{F(ON)}$	1.6*	5	mA
	HCPL-223X		1.8†		
Forward Input Voltage (OFF)		$V_{F(OFF)}$	-	0.8	V
Operating Temperature		T_A	-40	85	°C
Junction Temperature		T_J	-40	125	°C
Fan Out		N		4	TTL Loads

*The initial switching threshold is 1.6 mA or less. It is recommended that 2.2 mA be used to permit at least a 20% LED degradation guardband.
†The initial switching threshold is 1.8 mA or less. It is recommended that 2.5 mA be used to permit at least a 20% LED degradation guardband.

Electrical Specifications

-40°C ≤ T_A ≤ 85°C, 4.5 V ≤ V_{CC} ≤ 20 V, 1.6 mA ≤ $I_{F(ON)}$* ≤ 5 mA, 0 V ≤ $V_{F(OFF)}$ ≤ 0.8 V, unless otherwise specified. All Typicals at T_A = 25°C. See Note 7.

Parameter	Sym.	Min.	Typ.	Max.	Units	Test Conditions		Fig.	Note
Logic Low Output Voltage	V_{OL}			0.5	V	I_{OL} = 6.4 mA (4 TTL Loads)		1, 3	1
Logic High Output Voltage	V_{OH}	2.4	**		V	I_{OH} = -2.6 mA		2, 3, 8	1
		2.7				I_{OH} = -0.4 mA			
Output Leakage Current (V_{OUT} > V_{CC})	I_{OHH}			100	µA	V_O = 5.5 V	I_F = 5 mA		1
				500		V_O = 20 V			
Logic Low Supply Current	I_{CCL}		3.7	6.0	mA	V_{CC} = 5.5 V	V_F = 0 V		
			4.3	7.0		V_{CC} = 20 V	I_O = Open		
HCPL-223X			7.4	12.0		V_{CC} = 5.5 V			
			8.6	14.0		V_{CC} = 20 V			
Logic High Supply Current	I_{CCH}		2.4	4.0	mA	V_{CC} = 5.5 V	I_F = 5 mA		
			2.7	5.0		V_{CC} = 20 V	I_O = Open		
HCPL-223X			4.8	8.0		V_{CC} = 5.5 V			
			5.4	10.0		V_{CC} = 20 V			
Logic Low Short Circuit Output Current	I_{OSL}	15			mA	V_O = V_{CC} = 5.5 V	V_F = 0 V		1, 3
		20				V_O = V_{CC} = 20 V			
Logic High Short Circuit Output Current	I_{OSH}			-10	mA	V_{CC} = 5.5 V	I_F = 5 mA		1, 3
				-20		V_{CC} = 20 V	V_O = GND		
Input Forward Voltage	V_F		1.5	1.7	V	T_A = 25°C	I_F = 5 mA	4	1
				1.85					
HCNW22XX			1.5	1.82		T_A = 25°C			
				1.95					
Input Reverse Breakdown Voltage	BV_R	5			V	I_R = 10 µA			1
HCNW22XX		3				I_R = 100 µA			
Input Diode Temperature Coefficient	$\Delta V_F / \Delta T_A$		-1.7		mV/°C	I_F = 5 mA			
HCNW22XX			-1.4						
Input Capacitance	C_{IN}		60		pF	f = 1 MHz, V_F = 0 V			1, 4
HCNW22XX			70						

*For HCPL-223X, 1.8 mA ≤ $I_{F(ON)}$ ≤ 5 mA.
**Typical V_{OH} = V_{CC} - 2.1 V.

Switching Specifications (AC)

-40°C ≤ T_A ≤ 85°C, 4.5 V ≤ V_{CC} ≤ 20 V, 1.6 mA ≤ $I_{F(ON)}$* ≤ 5 mA, 0 V ≤ $V_{F(OFF)}$ ≤ 0.8 V.
All Typicals at T_A = 25°C, V_{CC} = 5 V, $I_{F(ON)}$ = 3 mA unless otherwise specified.

Parameter	Sym.	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to Logic Low Output Level	t_{PHL}		150		ns	Without Peaking Capacitor	5, 6	1, 6
			160			HCNW22XX		
			150	300		With Peaking Capacitor		
Propagation Delay Time to Logic High Output Level	t_{PLH}		110		ns	Without Peaking Capacitor	5, 6	1, 6
			180			HCNW22XX		
			90	300		With Peaking Capacitor		
Output Rise Time (10-90%)	t_r		30		ns		5, 9	1
Output Fall Time (90-10%)	t_f		7		ns		5, 9	1

Parameter	Sym.	Device	Min.	Units	Test Conditions		Fig.	Note
Logic High Common Mode Transient Immunity	$\|CM_H\|$	HCPL-2201/02 HCPL-0201 HCPL-2231 HCNW2201	1,000	V/µs	$\|V_{CM}\|$ = 50 V I_F = 1.6 mA†	V_{CC} = 5 V T_A = 25°C	10	1, 7
		HCPL-2211/12 HCPL-0211 HCPL-2232 HCNW2211	5,000	V/µs	$\|V_{CM}\|$ = 300 V I_F = 1.6 mA‡			
			10,000	V/µs	$\|V_{CM}\|$ = 1 kV I_F = 5.0 mA			
Logic Low Common Mode Transient Immunity	$\|CM_L\|$	HCPL-2201/02 HCPL-0201 HCPL-2231 HCNW2201	1,000	V/µs	$\|V_{CM}\|$ = 50 V	V_F = 0 V V_{CC} = 5 V T_A = 25°C	10	1, 7
		HCPL-2211/12 HCPL-0211 HCPL-2232 HCNW2211	10,000	V/µs	$\|V_{CM}\|$ = 1 kV			

*For HCPL-223X, 1.8 mA ≤ $I_{F(ON)}$ ≤ 5 mA.
†I_F = 1.8 mA for HCPL-2231.
‡I_F = 1.8 mA for HCPL-2232.

Package Characteristics

Parameter		Sym.	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage*		V_{ISO}	2500			V rms	RH < 50%, t = 1 min.		5, 10
	HCNW22XX		5000				T_A = 25°C		5, 11
Input-Output Resistance		R_{I-O}		10^{12}		Ω	V_{I-O} = 500 Vdc		5
	HCNW22XX		10^{12}	10^{13}			T_A = 25°C		
			10^{11}				T_A = 100°C		
Input-Output Capacitance		C_{I-O}		0.6		pF	f = 1 MHz,		5
	HCNW22XX			0.5	0.6		T_A = 25°C, V_{I-O} = 0 Vdc		
Input-Input Insulation Leakage Current		I_{I-I}		0.005		μA	Relative Humidity = 45%, t = 5 s, V_{I-I} = 500 V		12
Resistance (Input-Input)		R_{I-I}		10^{11}		Ω	V_{I-I} = 500 V		12
Capacitance (Input-Input)		C_{I-I}		0.25		pF	f = 1 MHz		12

*The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the VDE 0884 Insulation Characteristics Table (if applicable), your equipment level safety specification or HP Application Note 1074 entitled "Optocoupler Input-Output Endurance Voltage," publication number 5963-2203E.

Notes:

1. Each channel.
2. Derate total package power dissipation, P_T, linearly above 70°C free-air temperature at a rate of 4.5 mW/°C.
3. Duration of output short circuit time should not exceed 10 ms.
4. For single devices, input capacitance is measured between pin 2 and pin 3.
5. Device considered a two-terminal device: pins 1, 2, 3, and 4 shorted together and pins 5, 6, 7, and 8 shorted together.
6. The t_{PLH} propagation delay is measured from the 50% point on the leading edge of the input pulse to the 1.3 V point on the leading edge of the output pulse. The t_{PHL} propagation delay is measured from the 50% point on the trailing edge of the input pulse to the 1.3 V point on the trailing edge of the output pulse.
7. CM_H is the maximum slew rate of the common mode voltage that can be sustained with the output voltage in the logic high state, V_O > 2.0 V. CM_L is the maximum slew rate of the common mode voltage that can be sustained with the output voltage in the logic low state, V_O < 0.8 V.
8. For HCPL-2202/12, V_O is on pin 6.
9. Use of a 0.1 μF bypass capacitor connected between pins 5 and 8 is recommended.
10. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 3000 V rms for one second (leakage detection current limit, I_{I-O} ≤ 5 μA). This test is performed before the 100% production test for partial discharge (Method b) shown in the VDE 0884 Insulation Characteristics Table, if applicable.
11. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 6000 V rms for one second (leakage detection current limit, I_{I-O} ≤ 5 μA). This test is performed before the 100% production test for partial discharge (Method b) shown in the VDE 0884 Insulation Characteristics Table.
12. For HCPL-2231/32 only. Measured between pins 1 and 2, shorted together, and pins 3 and 4, shorted together.

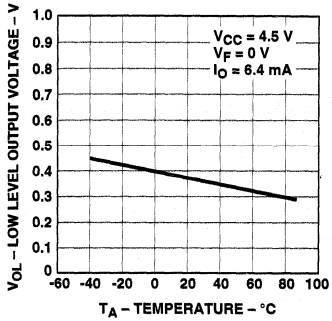


Figure 1. Typical Logic Low Output Voltage vs. Temperature.

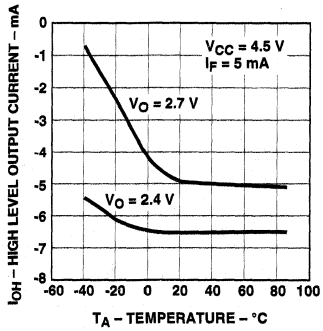


Figure 2. Typical Logic High Output Current vs. Temperature.

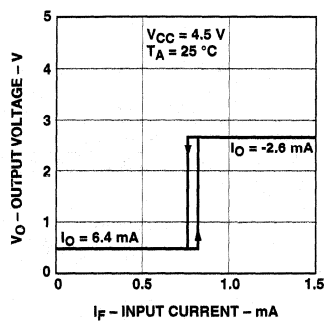


Figure 3. Typical Output Voltage vs. Forward Input Current.

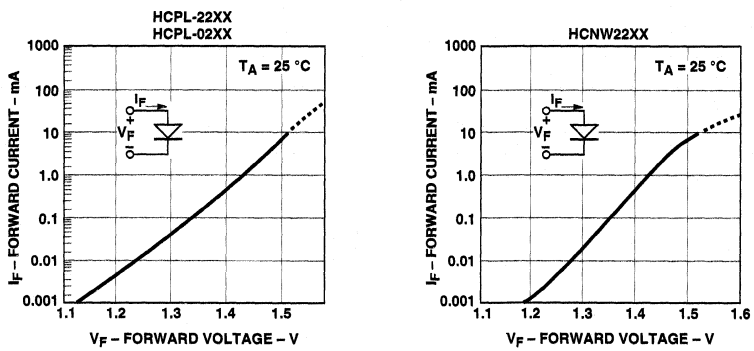
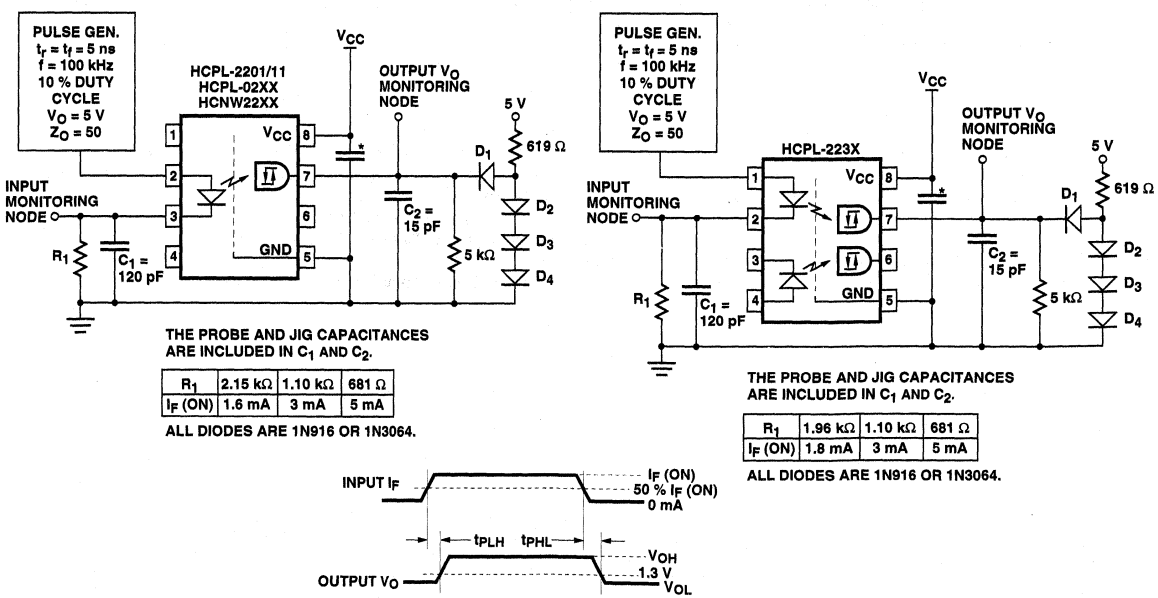


Figure 4. Typical Input Diode Forward Characteristic.



R_1	2.15 kΩ	1.10 kΩ	681 Ω
I_F (ON)	1.6 mA	3 mA	5 mA

R_1	1.96 kΩ	1.10 kΩ	681 Ω
I_F (ON)	1.8 mA	3 mA	5 mA

Figure 5. Circuit for t_{PLH}, t_{PHL}, t_r, t_f.

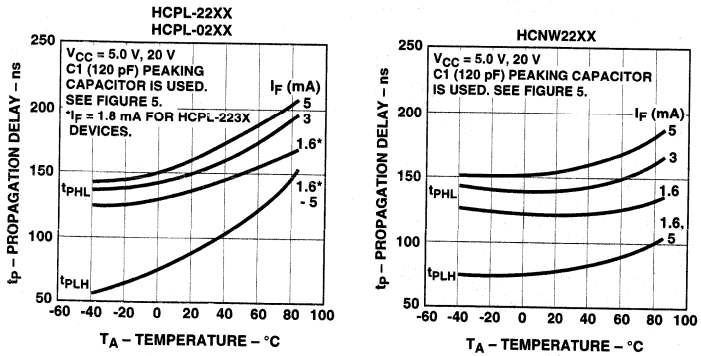


Figure 6. Typical Propagation Delays vs. Temperature.

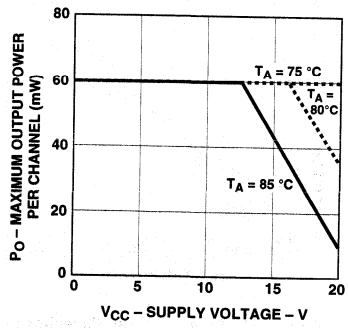


Figure 7. Maximum Output Power per Channel vs. Supply Voltage.

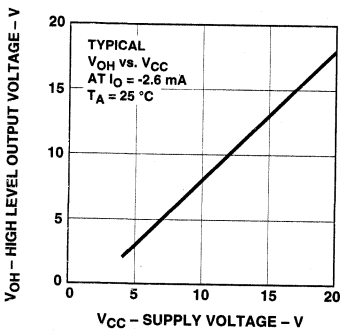


Figure 8. Typical Logic High Output Voltage vs. Supply Voltage.

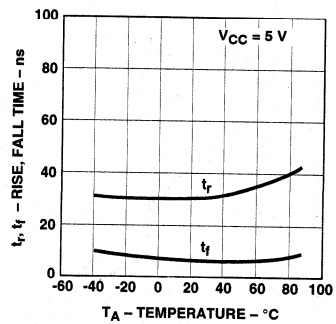


Figure 9. Typical Rise, Fall Time vs. Temperature.

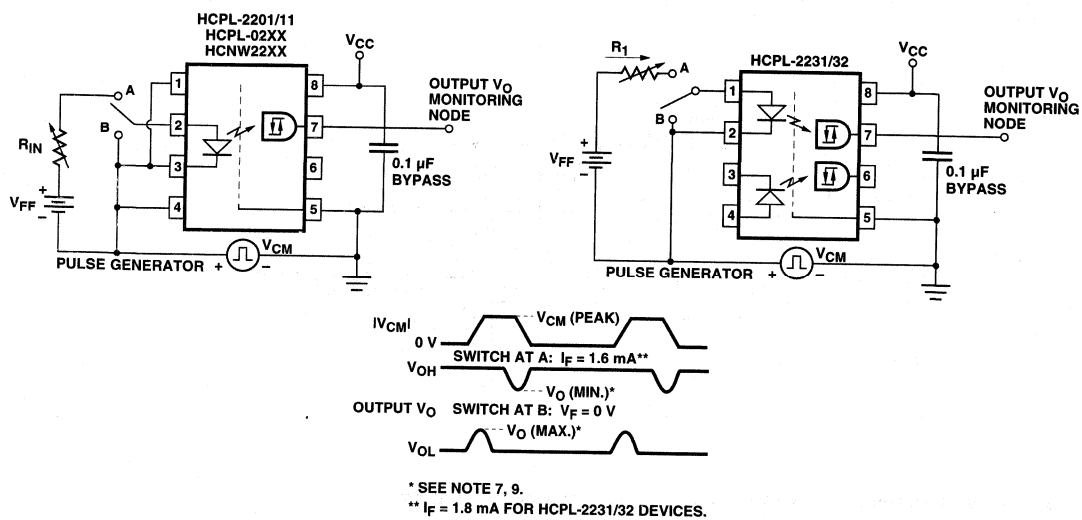


Figure 10. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

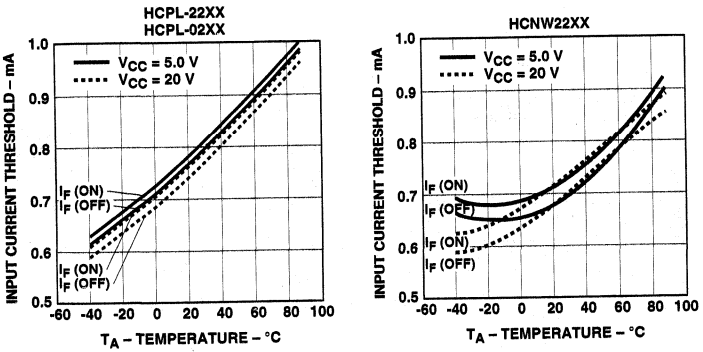


Figure 11. Typical Input Threshold Current vs. Temperature.

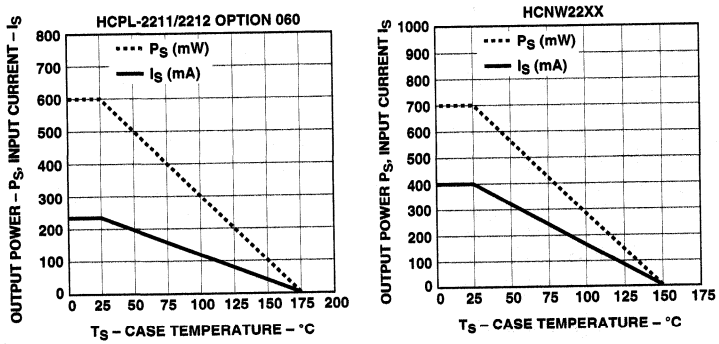


Figure 12. Thermal Derating Curve, Dependence of Safety Limiting Value with Case Temperature per VDE 0884.

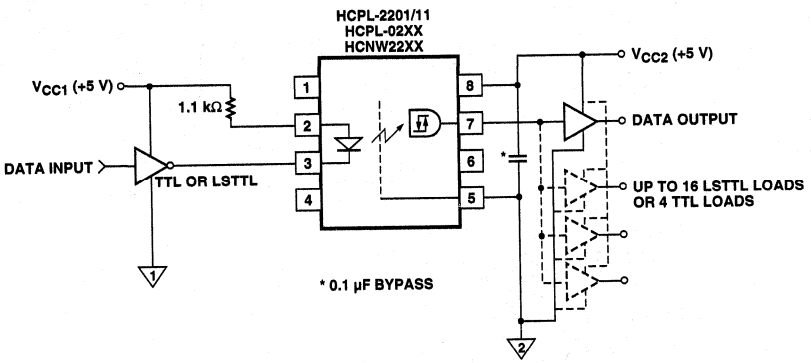


Figure 13a. Recommended LSTTL to LSTTL Circuit where 500 ns Propagation Delay is Sufficient.

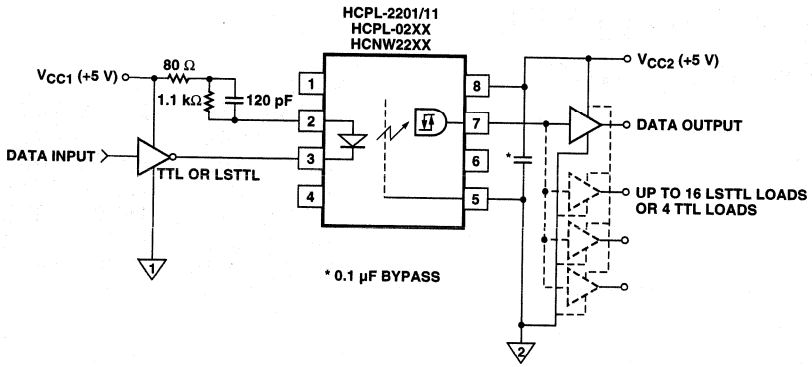


Figure 13b. Recommended LSTTL to LSTTL Circuit for Applications Requiring a Maximum Allowable Propagation Delay of 300 ns.

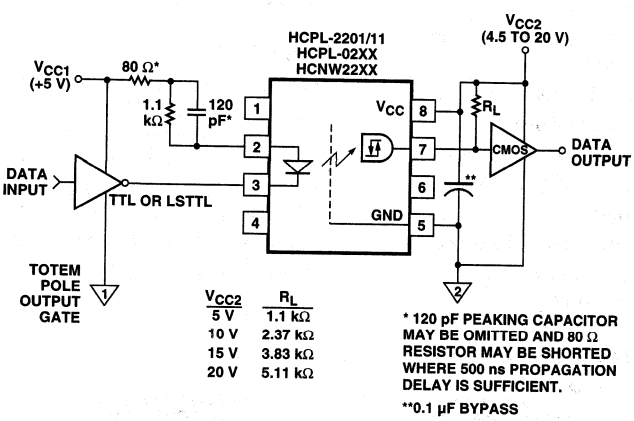


Figure 14. LSTTL to CMOS Interface Circuit.

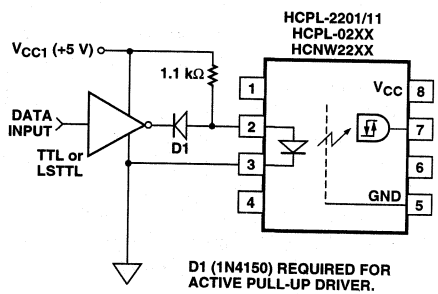


Figure 15. Alternative LED Drive Circuit.

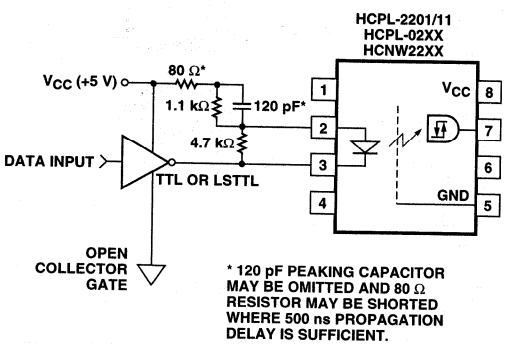


Figure 16. Series LED Drive with Open Collector Gate (4.7 k Resistor Shunts I_{OH} from the LED).

HEWLETT® PACKARD

High CMR, High Speed TTL Compatible Optocouplers

Technical Data

6N137
HCNW137 **HCPL-0631**
HCNW2601 **HCPL-0661**
HCNW2611 **HCPL-2601**
HCPL-0600 **HCPL-2611**
HCPL-0601 **HCPL-2630**
HCPL-0611 **HCPL-2631**
HCPL-0630 **HCPL-4661**

Features

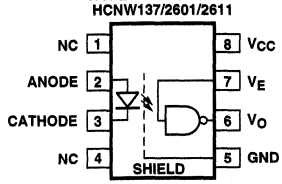
- **5 kV/µs Minimum Common Mode Rejection (CMR) at V_{CM} = 50 V for HCPL-X601/X631, HCNW2601 and 10 kV/µs Minimum CMR at V_{CM} = 1000 V for HCPL-X611/X661, HCNW2611**
- **High Speed:** 10 MBd Typical
- **LSTTL/TTL Compatible**
- **Low Input Current Capability: 5 mA**
- **Guaranteed ac and dc Performance over Temperature:** -40°C to +85°C
- **Available in 8-Pin DIP, SOIC-8, Widebody Packages**
- **Strobable Output (Single Channel Products Only)**
- **Safety Approval**
  UL Recognized - 2500 V rms for 1 minute and 5000 V rms* for 1 minute per UL1577
  CSA Approved
  VDE 0884 Approved with V_{IORM} = 630 V peak for HCPL-2611 Option 060 and V_{IORM} = 1414 V peak for HCNW137/26X1
  BSI Certified (HCNW137/26X1 Only)
- **MIL-STD-1772 Version Available (HCPL-56XX/66XX)**

Applications

- **Isolated Line Receiver**
- **Computer-Peripheral Interfaces**
- **Microprocessor System Interfaces**
- **Digital Isolation for A/D, D/A Conversion**
- **Switching Power Supply**
- **Instrument Input/Output Isolation**
- **Ground Loop Elimination**
- **Pulse Transformer Replacement**
- **Power Transistor Isolation in Motor Drives**
- **Isolation of High Speed Logic Systems**

Functional Diagram

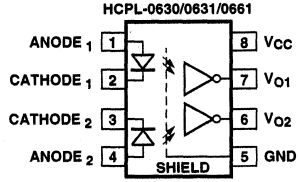
6N137, HCPL-2601/2611
HCPL-0600/0601/0611
HCNW137/2601/2611



TRUTH TABLE
(POSITIVE LOGIC)

LED	ENABLE	OUTPUT
ON	H	L
OFF	H	H
ON	L	H
OFF	L	H
ON	NC	L
OFF	NC	H

HCPL-2630/2631/4661
HCPL-0630/0631/0661



TRUTH TABLE
(POSITIVE LOGIC)

LED	OUTPUT
ON	L
OFF	H

Description

The 6N137, HCPL-26XX/06XX/4661, HCNW137/26X1 are optically coupled gates that combine a GaAsP light emitting diode and an integrated high gain photo detector. An enable input allows the detector to be strobed. The output of the detector IC is

*5000 V rms/1 Minute rating is for HCNW137/26X1 and Option 020 (6N137, HCPL-2601/11/30/31, HCPL-4661) products only.

A 0.1 µF bypass capacitor must be connected between pins 5 and 8.

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

5965-3594E

an open collector Schottky-clamped transistor. The internal shield provides a guaranteed common mode transient immunity specification of 5,000 V/μs for the HCPL-X601/X631 and HCNW2601, and 10,000 V/μs for the HCPL-X611/X661 and HCNW2611.

This unique design provides maximum ac and dc circuit isolation while achieving TTL compatibility. The optocoupler ac and dc operational parameters are guaranteed from -40°C to +85°C allowing troublefree system performance.

The 6N137, HCPL-26XX, HCPL-06XX, HCPL-4661, HCNW137, and HCNW26X1 are suitable for high speed logic interfacing, input/output buffering, as line receivers in environments that conventional line receivers cannot tolerate and are recommended for use in extremely high ground or induced noise environments.

Selection Guide

Minimum CMR		Input On-Current (mA)	Output Enable	8-Pin DIP (300 Mil)		Small-Outline SO-8		Widebody (400 Mil)	Hermetic
dV/dt (V/μs)	V_{CM} (V)			Single Channel Package	Dual Channel Package	Single Channel Package	Dual Channel Package	Single Channel Package	Single and Dual Channel Packages
NA	NA	5	YES	6N137		HCPL-0600		HCNW137	
			NO		HCPL-2630		HCPL-0630		
5,000	50		YES	HCPL-2601		HCPL-0601		HCNW2601	
			NO		HCPL-2631		HCPL-0631		
10,000	1,000		YES	HCPL-2611		HCPL-0611		HCNW2611	
			NO		HCPL-4661		HCPL-0661		
1,000	50		YES	HCPL-2602[1]					
3, 500	300		YES	HCPL-2612[1]					
1,000	50	3	YES	HCPL-261A[1]		HCPL-061A[1]			
			NO		HCPL-263A[1]		HCPL-063A[1]		
1,000[2]	1,000		YES	HCPL-261N[1]		HCPL-061N[1]			
			NO		HCPL-263N[1]		HCPL-063N[1]		
1,000	50	12.5	[3]						HCPL-193X[1] HCPL-56XX[1] HCPL-66XX[1]

Notes:
1. Technical data are on separate HP publications.
2. 15 kV/μs with V_{CM} = 1 kV can be achieved using HP application circuit.
3. Enable is available for single channel products only, except for HCPL-193X devices.

Ordering Information

Specify Part Number followed by Option Number (if desired).

Example:

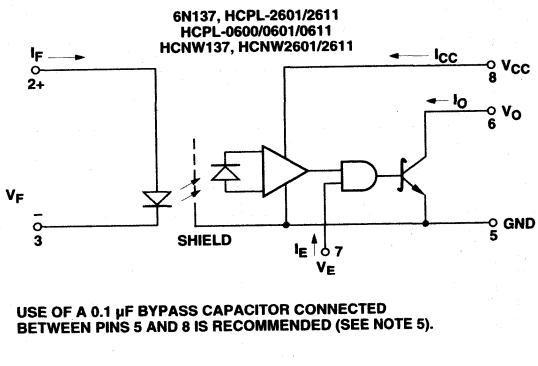
HCPL-2611#XXX

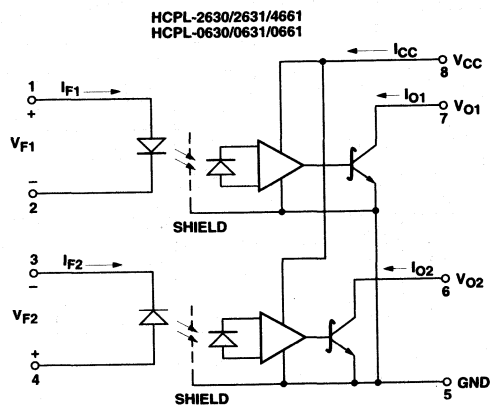
- 020 = 5000 V rms/1 minute UL Rating Option*
- 060 = VDE 0884 V_{IORM} = 630 Vpeak Option**
- 300 = Gull Wing Surface Mount Option†
- 500 = Tape and Reel Packaging Option

Option data sheets available. Contact Hewlett-Packard sales representative or authorized distributor for information.

*For 6N137, HCPL-2601/11/30/31 and HCPL-4661 (8-pin DIP products) only.
**For HCPL-2611 only. Combination of Option 020 and Option 060 is not available.
†Gull wing surface mount option applies to through hole parts only.

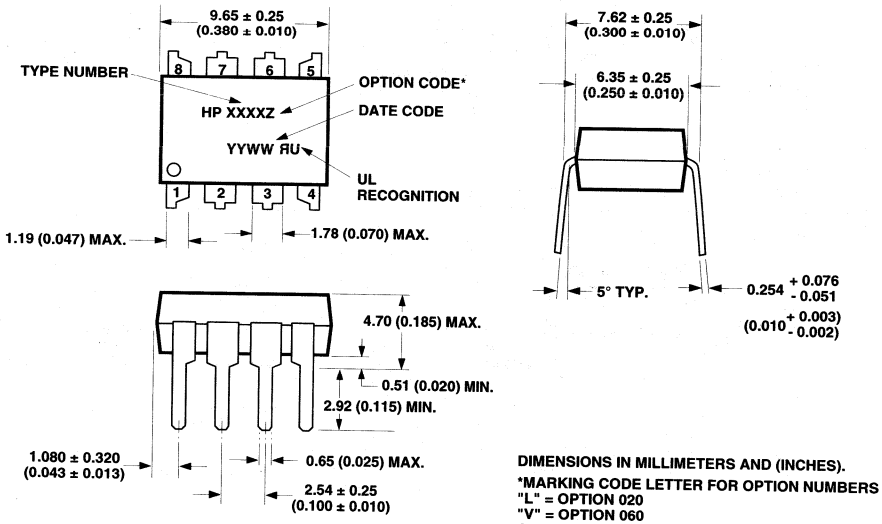
Schematic





Package Outline Drawings

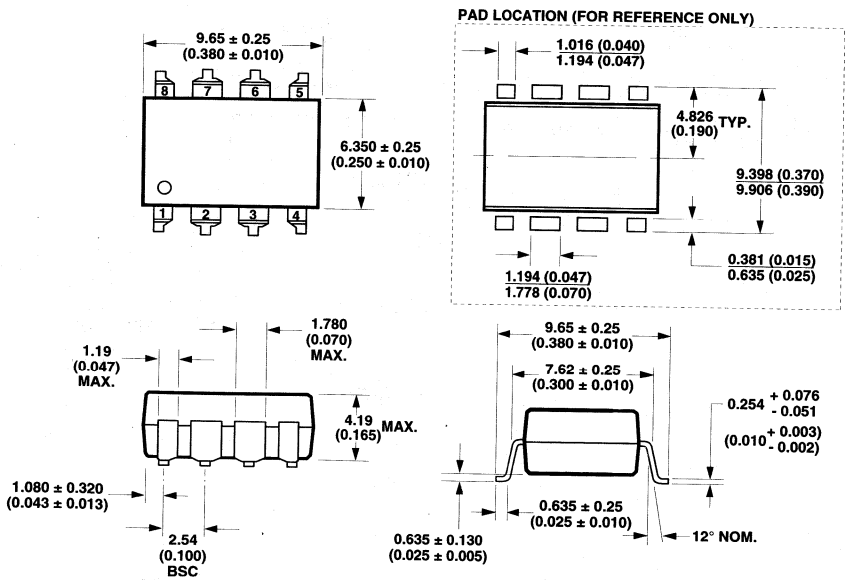
8-pin DIP Package** (6N137, HCPL-2601/11/30/31, HCPL-4661)



DIMENSIONS IN MILLIMETERS AND (INCHES).
*MARKING CODE LETTER FOR OPTION NUMBERS
"L" = OPTION 020
"V" = OPTION 060
OPTION NUMBERS 300 AND 500 NOT MARKED.

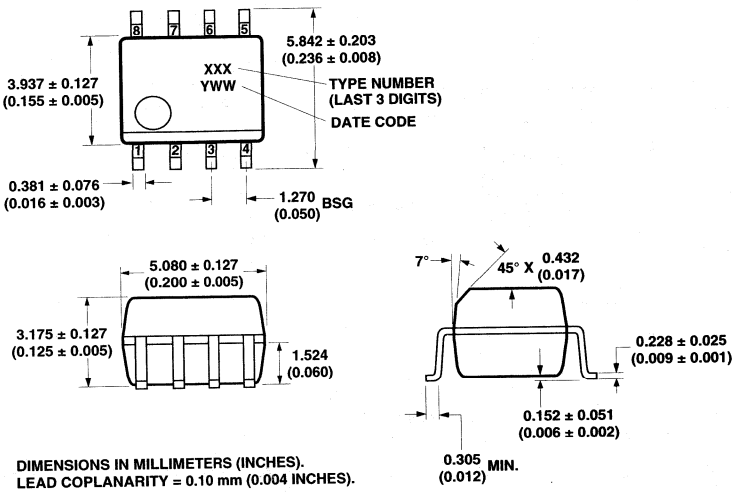
**JEDEC Registered Data (for 6N137 only).

8-pin DIP Package with Gull Wing Surface Mount Option 300 (6N137, HCPL-2601/11/30/31, HCPL-4661)



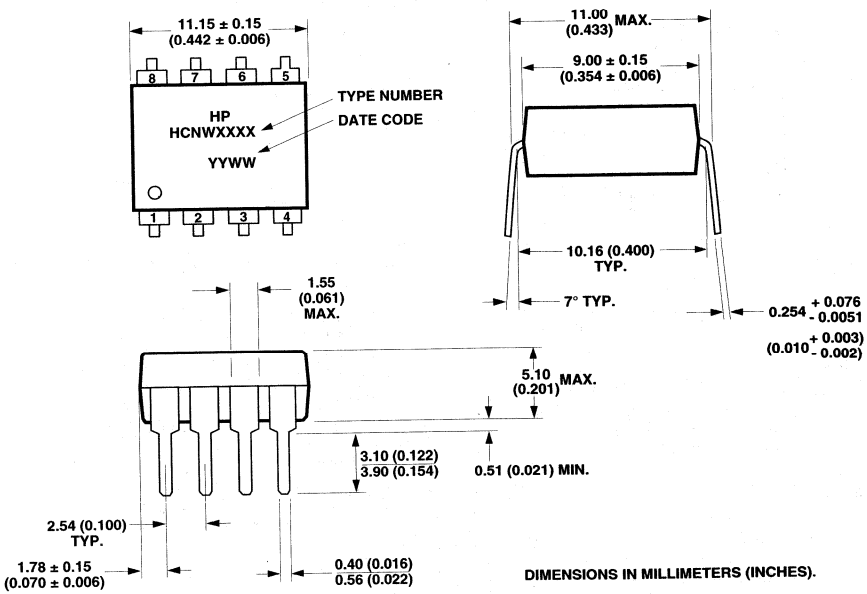
DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES).

Small-Outline SO-8 Package (HCPL-0600/01/11/30/31/61)



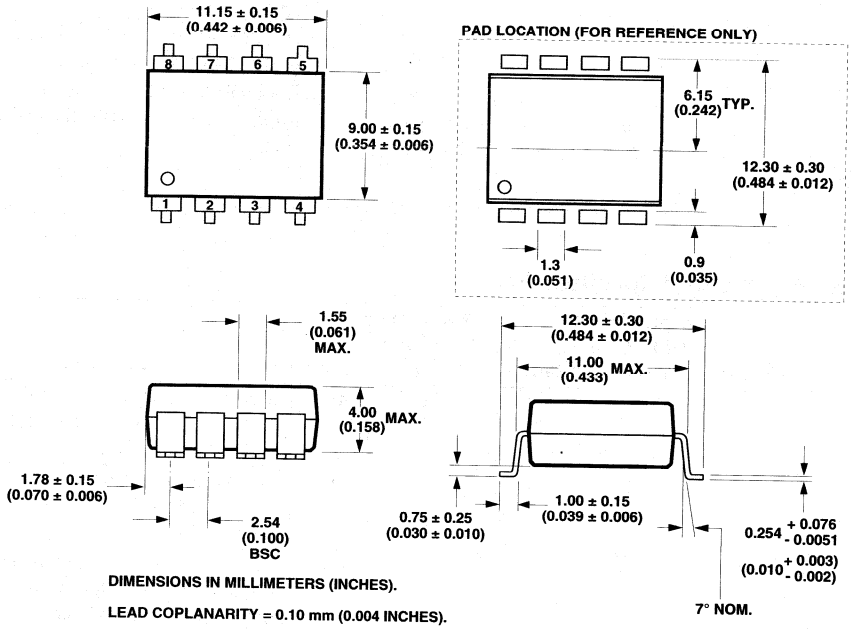
DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES).

8-Pin Widebody DIP Package (HCNW137, HCNW2601/11)

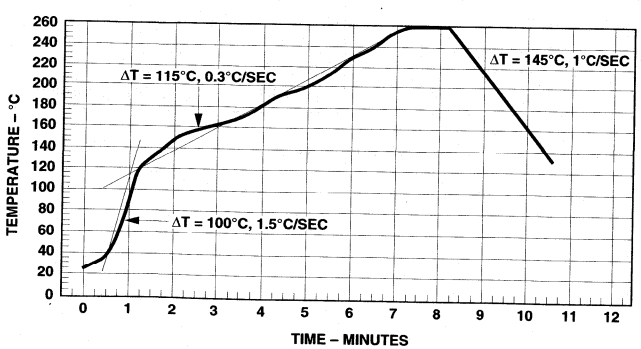


DIMENSIONS IN MILLIMETERS (INCHES).

8-Pin Widebody DIP Package with Gull Wing Surface Mount Option 300 (HCNW137, HCNW2601/11)



Solder Reflow Temperature Profile (HCPL-06XX and Gull Wing Surface Mount Option 300 Parts)



Note: Use of nonchlorine activated fluxes is highly recommended.

Regulatory Information

The 6N137, HCPL-26XX/06XX/46XX, and HCNW137/26XX have been approved by the following organizations:

UL

Recognized under UL 1577, Component Recognition Program, File E55361.

CSA

Approved under CSA Component Acceptance Notice #5, File CA 88324.

VDE

Approved according to VDE 0884/06.92. (HCPL-2611 Option 060 and HCNW137/26X1 only)

BSI

Certification according to BS415:1994 (BS EN60065:1994), BS7002:1992 (BS EN60950:1992) and EN41003:1993 for Class II applications. (HCNW137/26X1 only)

Insulation and Safety Related Specifications

Parameter	Symbol	8-pin DIP (300 Mil) Value	SO-8 Value	Widebody (400 Mil) Value	Units	Conditions
Minimum External Air Gap (External Clearance)	L(101)	7.1	4.9	9.6	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L(102)	7.4	4.8	10.0	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	0.08	1.0	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity.
Minimum Internal Tracking (Internal Creepage)		NA	NA	4.0	mm	Measured from input terminals to output terminals, along internal cavity.
Tracking Resistance (Comparative Tracking Index)	CTI	200	200	200	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa	IIIa	IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Option 300 - surface mount classification is Class A in accordance with CECC 00802.

VDE 0884 Insulation Related Characteristics (HCPL-2611 Option 060 Only)

Description	Symbol	Characteristic	Units
Installation classification per DIN VDE 0110/1.89, Table 1			
for rated mains voltage ≤ 300 V rms		I-IV	
for rated mains voltage ≤ 450 V rms		I-III	
Climatic Classification		55/85/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	630	V_{peak}
Input to Output Test Voltage, Method b* V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial Discharge < 5 pC	V_{PR}	1181	V_{peak}
Input to Output Test Voltage, Method a* V_{IORM} x 1.5 = V_{PR}, Type and sample test, t_m = 60 sec, Partial Discharge < 5 pC	V_{PR}	945	V_{peak}
Highest Allowable Overvoltage* (Transient Overvoltage, t_{ini} = 10 sec)	V_{IOTM}	6000	V_{peak}
Safety Limiting Values (Maximum values allowed in the event of a failure, also see Figure 16, Thermal Derating curve.)			
Case Temperature	T_S	175	°C
Input Current	$I_{S,INPUT}$	230	mA
Output Power	$P_{S,OUTPUT}$	600	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	$\geq 10^9$	Ω

*Refer to the front of the optocoupler section of the current catalog, under Product Safety Regulations section (VDE 0884), for a detailed description.

Note: Isolation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuits in application.

VDE 0884 Insulation Related Characteristics (HCNW137/2601/2611 Only)

Description	Symbol	Characteristic	Units
Installation classification per DIN VDE 0110/1.89, Table 1			
for rated mains voltage ≤ 600 V rms		I-IV	
for rated mains voltage ≤ 1000 V rms		I-III	
Climatic Classification (DIN IEC 68 part 1)		55/100/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	1414	V_{peak}
Input to Output Test Voltage, Method b* V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial Discharge < 5 pC	V_{PR}	2651	V_{peak}
Input to Output Test Voltage, Method a* V_{IORM} x 1.5 = V_{PR}, Type and sample test, t_m = 60 sec, Partial Discharge < 5 pC	V_{PR}	2121	V_{peak}
Highest Allowable Overvoltage* (Transient Overvoltage, t_{ini} = 10 sec)	V_{IOTM}	8000	V_{peak}
Safety Limiting Values (Maximum values allowed in the event of a failure, also see Figure 16, Thermal Derating curve.)			
Case Temperature	T_S	150	°C
Input Current	$I_{S,INPUT}$	400	mA
Output Power	$P_{S,OUTPUT}$	700	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	$\geq 10^9$	Ω

*Refer to the front of the optocoupler section of the current catalog, under Product Safety Regulations section (VDE 0884), for a detailed description.

Note: Isolation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuits in application.

Absolute Maximum Ratings* (No Derating Required up to 85°C)

Parameter	Symbol	Package**	Min.	Max.	Units	Note
Storage Temperature	T_S		-55	125	°C	
Operating Temperature†	T_A		-40	85	°C	
Average Forward Input Current	I_F	Single 8-Pin DIP Single SO-8 Widebody		20	mA	2
		Dual 8-Pin DIP Dual SO-8		15		1, 3
Reverse Input Voltage	V_R	8-Pin DIP, SO-8		5	V	1
		Widebody		3		
Input Power Dissipation	P_I	Widebody		40	mW	
Supply Voltage (1 Minute Maximum)	V_{CC}			7	V	
Enable Input Voltage (Not to Exceed V_{CC} by more than 500 mV)	V_E	Single 8-Pin DIP Single SO-8 Widebody		V_{CC} + 0.5	V	
Enable Input Current	I_E			5	mA	
Output Collector Current	I_O			50	mA	1
Output Collector Voltage (Selection for Higher Output Voltages up to 20 V is Available.)	V_O			7	V	1
Output Collector Power Dissipation	P_O	Single 8-Pin DIP Single SO-8 Widebody		85	mW	
		Dual 8-Pin DIP Dual SO-8		60		1, 4
Lead Solder Temperature (Through Hole Parts Only)	T_{LS}	8-Pin DIP	260°C for 10 sec., 1.6 mm below seating plane			
		Widebody	260°C for 10 sec., up to seating plane			
Solder Reflow Temperature Profile (Surface Mount Parts Only)		SO-8 and Option 300	See Package Outline Drawings section			

*JEDEC Registered Data (for 6N137 only).
Ratings apply to all devices except otherwise noted in the **Package column.
†0°C to 70°C on JEDEC Registration.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Input Current, Low Level	I_{FL}*	0	250	μA
Input Current, High Level[1]	I_{FH}**	5	15	mA
Power Supply Voltage	V_{CC}	4.5	5.5	V
Low Level Enable Voltage†	V_{EL}	0	0.8	V
High Level Enable Voltage†	V_{EH}	2.0	V_{CC}	V
Operating Temperature	T_A	-40	85	°C
Fan Out (at R_L = 1 kΩ)[1]	N		5	TTL Loads
Output Pull-up Resistor	R_L	330	4 k	Ω

*The off condition can also be guaranteed by ensuring that $V_{FL} \leq 0.8$ volts.
**The initial switching threshold is 5 mA or less. It is recommended that 6.3 mA to 10 mA be used for best performance and to permit at least a 20% LED degradation guardband.
†For single channel products only.

Electrical Specifications

Over recommended temperature (T_A = -40°C to +85°C) unless otherwise specified. All Typicals at V_{CC} = 5 V, T_A = 25°C. All enable test conditions apply to single channel products only. See note 5.

Parameter	Sym.	Package	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
High Level Output Current	I_{OH}*	All		5.5	100	µA	V_{CC} = 5.5 V, V_E = 2.0 V, V_O = 5.5 V, I_F = 250 µA	1	1, 6, 19
Input Threshold Current	I_{TH}	Single Channel Widebody		2.0	5.0	mA	V_{CC} = 5.5 V, V_E = 2.0 V, V_O = 0.6 V, I_{OL} (Sinking) = 13 mA	2, 3	19
		Dual Channel		2.5					
Low Level Output Voltage	V_{OL}*	8-Pin DIP SO-8		0.35	0.6	V	V_{CC} = 5.5 V, V_E = 2.0 V, I_F = 5 mA, I_{OL} (Sinking) = 13 mA	2, 3, 4, 5	1, 19
		Widebody		0.4					
High Level Supply Current	I_{CCH}	Single Channel		7.0	10.0*	mA	V_E = 0.5 V; V_{CC} = 5.5 V; I_F = 0 mA		7
				6.5			V_E = V_{CC}		
		Dual Channel		10	15		Both Channels		
Low Level Supply Current	I_{CCL}	Single Channel		9.0	13.0*	mA	V_E = 0.5 V; V_{CC} = 5.5 V; I_F = 10 mA		8
				8.5			V_E = V_{CC}		
		Dual Channel		13	21		Both Channels		
High Level Enable Current	I_{EH}	Single Channel		-0.7	-1.6	mA	V_{CC} = 5.5 V, V_E = 2.0 V		
Low Level Enable Current	I_{EL}*			-0.9	-1.6	mA	V_{CC} = 5.5 V, V_E = 0.5 V		9
High Level Enable Voltage	V_{EH}		2.0			V			19
Low Level Enable Voltage	V_{EL}				0.8	V			
Input Forward Voltage	V_F	8-Pin DIP	1.4	1.5	1.75*	V	T_A = 25°C; I_F = 10 mA	6, 7	1
		SO-8	1.3		1.80				
		Widebody	1.25	1.64	1.85		T_A = 25°C		
			1.2		2.05				
Input Reverse Breakdown Voltage	BV_R*	8-Pin DIP SO-8	5			V	I_R = 10 µA		1
		Widebody	3				I_R = 100 µA, T_A = 25°C		
Input Diode Temperature Coefficient	$\Delta V_F/\Delta T_A$	8-Pin DIP SO-8		-1.6		mV/°C	I_F = 10 mA	7	1
		Widebody		-1.9					
Input Capacitance	C_{IN}	8-Pin DIP SO-8		60		pF	f = 1 MHz, V_F = 0 V		1
		Widebody		70					

*JEDEC registered data for the 6N137. The JEDEC Registration specifies 0°C to +70°C. HP specifies -40°C to +85°C.

Switching Specifications (AC)

Over Recommended Temperature (T_A = -40°C to +85°C), V_{CC} = 5 V, I_F = 7.5 mA unless otherwise specified. All Typicals at T_A = 25°C, V_{CC} = 5 V.

Parameter	Sym.	Package**	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to High Output Level	t_{PLH}		20	48	75* 100	ns	T_A = 25°C | R_L = 350 Ω C_L = 15 pF	8, 9, 10	1, 10, 19
Propagation Delay Time to Low Output Level	t_{PHL}		25	50	75* 100	ns	T_A = 25°C		1, 11, 19
Pulse Width Distortion	$\|t_{PHL} - t_{PLH}\|$	8-Pin DIP SO-8 Widebody		3.5	35 40	ns		8, 9, 10, 11	13, 19
Propagation Delay Skew	t_{PSK}				40	ns			12, 13, 19
Output Rise Time (10-90%)	t_r			24		ns		12	1, 19
Output Fall Time (90-10%)	t_f			10		ns		12	1, 19
Propagation Delay Time of Enable from V_{EH} to V_{EL}	t_{ELH}	Single Channel		30		ns	R_L = 350 Ω, C_L = 15 pF, V_{EL} = 0 V, V_{EH} = 3 V	13, 14	14
Propagation Delay Time of Enable from V_{EL} to V_{EH}	t_{EHL}	Single Channel		20		ns			15

*JEDEC registered data for the 6N137.

Ratings apply to all devices except otherwise noted in the **Package column.

Parameter	Sym.	Device	Min.	Typ.	Units	Test Conditions		Fig.	Note
Logic High Common Mode Transient Immunity	$\|CM_H\|$	6N137 HCPL-2630 HCPL-0600/0630 HCNW137		10,000	V/µs	$\|V_{CM}\|$ = 10 V	V_{CC} = 5 V, I_F = 0 mA, $V_{O(MIN)}$ = 2 V, R_L = 350 Ω, T_A = 25°C	15	1, 16, 18, 19
		HCPL-2601/2631 HCPL-0601/0631 HCNW2601	5,000	10,000		$\|V_{CM}\|$ = 50 V			
		HCPL-2611/4661 HCPL-0611/0661 HCNW2611	10,000	15,000		$\|V_{CM}\|$ = 1 kV			
Logic Low Common Mode Transient Immunity	$\|CM_L\|$	6N137 HCPL-2630 HCPL-0600/0630 HCNW137		10,000	V/µs	$\|V_{CM}\|$ = 10 V	V_{CC} = 5 V, I_F = 7.5 mA, $V_{O(MAX)}$ = 0.8 V, R_L = 350 Ω, T_A = 25°C	15	1, 17, 18, 19
		HCPL-2601/2631 HCPL-0601/0631 HCNW2601	5,000	10,000		$\|V_{CM}\|$ = 50 V			
		HCPL-2611/4661 HCPL-0611/0661 HCNW2611	10,000	15,000		$\|V_{CM}\|$ = 1 kV			

Package Characteristics

All Typicals at T_A = 25°C.

Parameter	Sym.	Package	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Input-Output Insulation	I_{I-O}*	Single 8-Pin DIP Single SO-8			1	μA	45% RH, t = 5 s, V_{I-O} = 3 kV dc, T_A = 25°C		20, 21
Input-Output Momentary Withstand Voltage**	V_{ISO}	8-Pin DIP, SO-8	2500			V rms	RH ≤ 50%, t = 1 min, T_A = 25°C		20, 21
		Widebody	5000						20, 22
		OPT 020†	5000						
Input-Output Resistance	R_{I-O}	8-Pin DIP, SO-8		10^{12}		Ω	V_{I-O} = 500 V dc		1, 20, 23
		Widebody	10^{12}	10^{13}			T_A = 25°C		
			10^{11}				T_A = 100°C		
Input-Output Capacitance	C_{I-O}	8-Pin DIP, SO-8		0.6		pF	f = 1 MHz, T_A = 25°C		1, 20, 23
		Widebody		0.5	0.6				
Input-Input Insulation Leakage Current	I_{I-I}	Dual Channel		0.005		μA	RH ≤ 45%, t = 5 s, V_{I-I} = 500 V		24
Resistance (Input-Input)	R_{I-I}	Dual Channel		10^{11}		Ω			24
Capacitance (Input-Input)	C_{I-I}	Dual 8-Pin DIP		0.03		pF	f = 1 MHz		24
		Dual SO-8		0.25					

*JEDEC registered data for the 6N137. The JEDEC Registration specifies 0°C to 70°C. HP specifies -40°C to 85°C.
**The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the VDE 0884 Insulation Characteristics Table (if applicable), your equipment level safety specification or HP Application Note 1074 entitled "Optocoupler Input-Output Endurance Voltage."
†For 6N137, HCPL-2601/2611/2630/2631/4661 only.

Notes:

1. Each channel.
2. Peaking circuits may produce transient input currents up to 50 mA, 50 ns maximum pulse width, provided average current does not exceed 20 mA.
3. Peaking circuits may produce transient input currents up to 50 mA, 50 ns maximum pulse width, provided average current does not exceed 15 mA.
4. Derate linearly above 80°C free-air temperature at a rate of 2.7 mW/°C for the SOIC-8 package.
5. Bypassing of the power supply line is required, with a 0.1 μF ceramic disc capacitor adjacent to each optocoupler as illustrated in Figure 17. Total lead length between both ends of the capacitor and the isolator pins should not exceed 20 mm.
6. The JEDEC registration for the 6N137 specifies a maximum I_{OH} of 250 μA. HP guarantees a maximum I_{OH} of 100 μA.
7. The JEDEC registration for the 6N137 specifies a maximum I_{CCH} of 15 mA. HP guarantees a maximum I_{CCH} of 10 mA.
8. The JEDEC registration for the 6N137 specifies a maximum I_{CCL} of 18 mA. HP guarantees a maximum I_{CCL} of 13 mA.
9. The JEDEC registration for the 6N137 specifies a maximum I_{EL} of –2.0 mA. HP guarantees a maximum I_{EL} of -1.6 mA.
10. The t_{PLH} propagation delay is measured from the 3.75 mA point on the falling edge of the input pulse to the 1.5 V point on the rising edge of the output pulse.
11. The t_{PHL} propagation delay is measured from the 3.75 mA point on the rising edge of the input pulse to the 1.5 V point on the falling edge of the output pulse.
12. t_{PSK} is equal to the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between units at any given temperature and specified test conditions.
13. See application section titled "Propagation Delay, Pulse-Width Distortion and Propagation Delay Skew" for more information.
14. The t_{ELH} enable propagation delay is measured from the 1.5 V point on the falling edge of the enable input pulse to the 1.5 V point on the rising edge of the output pulse.
15. The t_{EHL} enable propagation delay is measured from the 1.5 V point on the rising edge of the enable input pulse to the 1.5 V point on the falling edge of the output pulse.
16. CM_H is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state (i.e., V_O > 2.0 V).
17. CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state (i.e., V_O < 0.8 V).
18. For sinusoidal voltages, $(|dV_{CM}| / dt)_{max} = \pi f_{CM} V_{CM}(p\text{-}p)$.

19. No external pull up is required for a high logic state on the enable input. If the V_E pin is not used, tying V_E to V_{CC} will result in improved CMR performance. For single channel products only.
20. Device considered a two-terminal device: pins 1, 2, 3, and 4 shorted together, and pins 5, 6, 7, and 8 shorted together.
21. In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 3000 V rms for one second (leakage detection current limit, $I_{I-O} \leq 5\ \mu A$). This test is performed before the 100% production test for partial discharge (Method b) shown in the VDE 0884 Insulation Characteristics Table, if applicable.
22. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 6000 V rms for one second (leakage detection current limit, $I_{I-O} \leq 5\ \mu A$). This test is performed before the 100% production test for partial discharge (Method b) shown in the VDE 0884 Insulation Characteristics Table, if applicable.
23. Measured between the LED anode and cathode shorted together and pins 5 through 8 shorted together. For dual channel products only.
24. Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together. For dual channel products only.

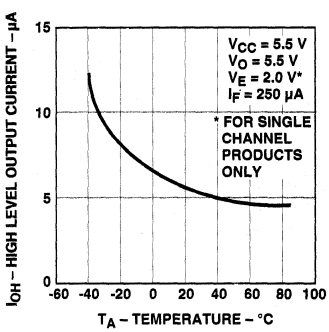


Figure 1. Typical High Level Output Current vs. Temperature.

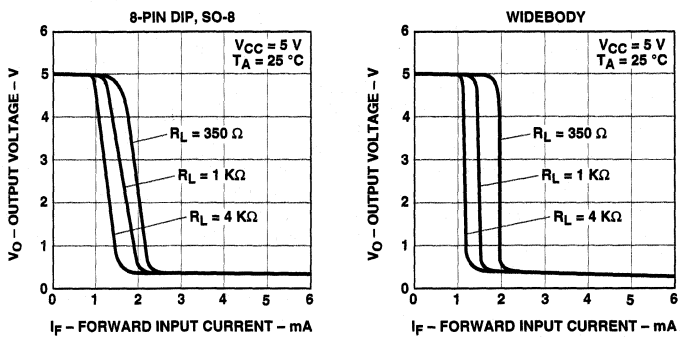


Figure 2. Typical Output Voltage vs. Forward Input Current.

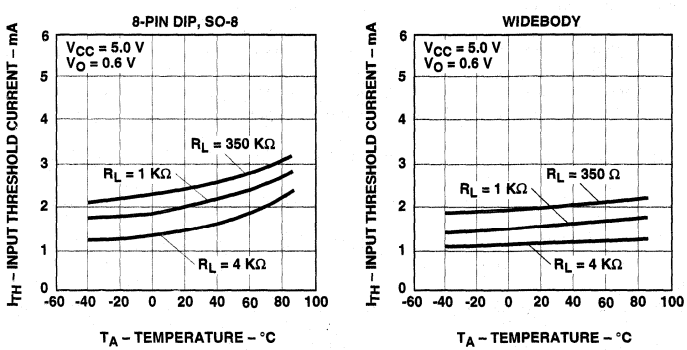


Figure 3. Typical Input Threshold Current vs. Temperature.

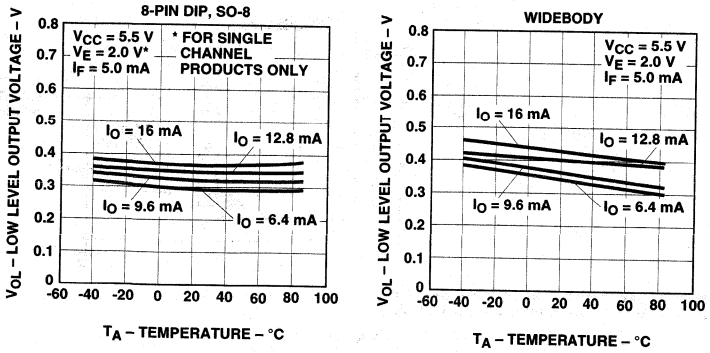


Figure 4. Typical Low Level Output Voltage vs. Temperature.

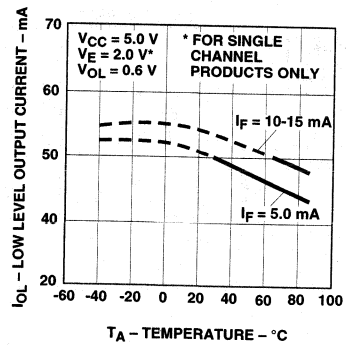


Figure 5. Typical Low Level Output Current vs. Temperature.

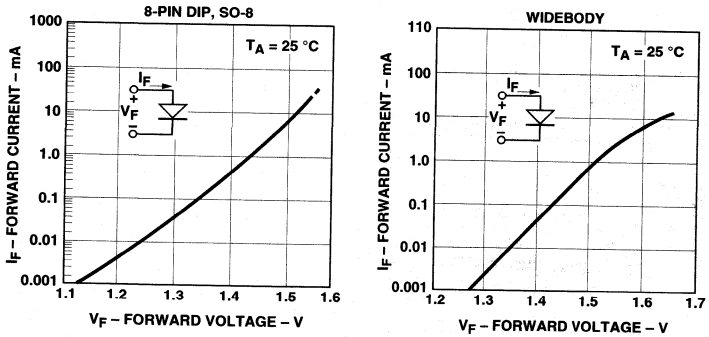


Figure 6. Typical Input Diode Forward Characteristic.

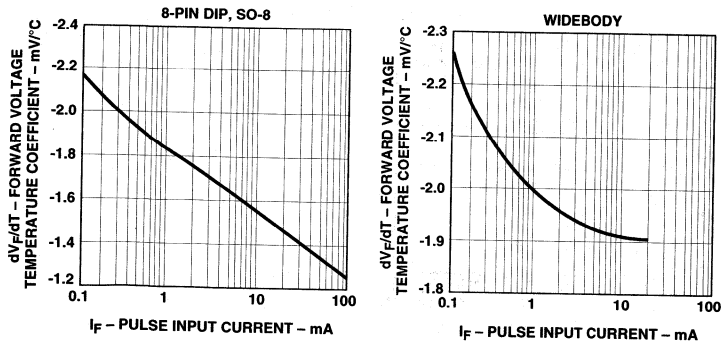


Figure 7. Typical Temperature Coefficient of Forward Voltage vs. Input Current.

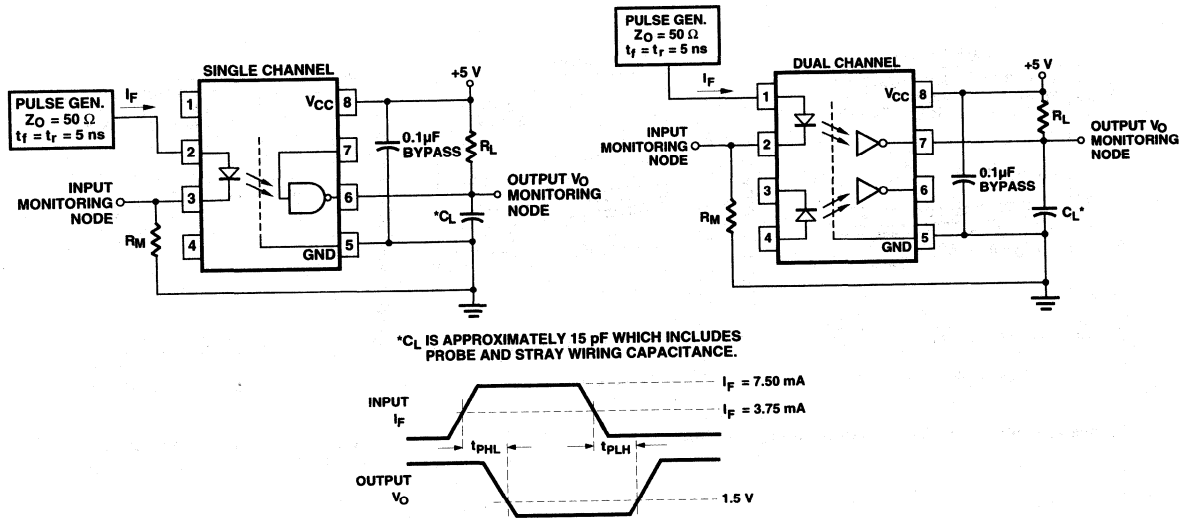


Figure 8. Test Circuit for t_{PHL} and t_{PLH}.

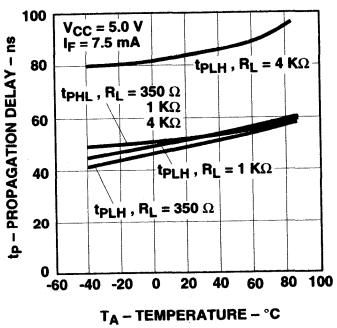


Figure 9. Typical Propagation Delay vs. Temperature.

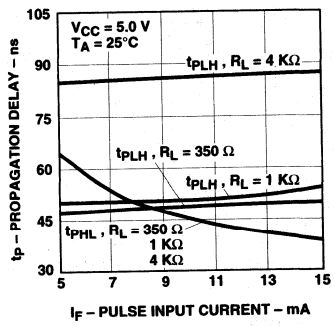


Figure 10. Typical Propagation Delay vs. Pulse Input Current.

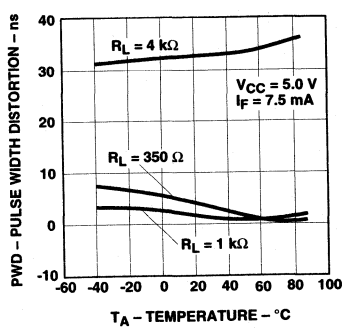


Figure 11. Typical Pulse Width Distortion vs. Temperature.

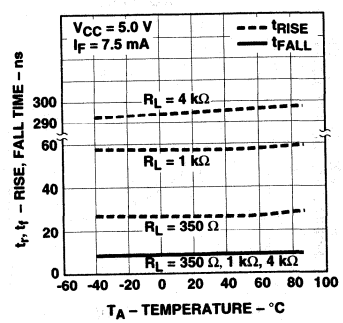


Figure 12. Typical Rise and Fall Time vs. Temperature.

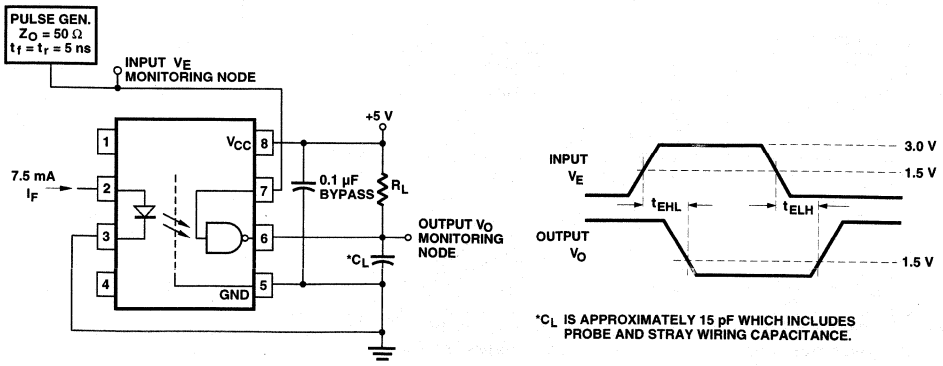


Figure 13. Test Circuit for t_{EHL} and t_{ELH}.

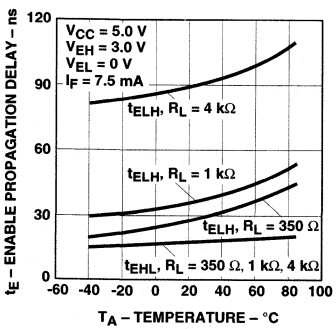


Figure 14. Typical Enable Propagation Delay vs. Temperature.

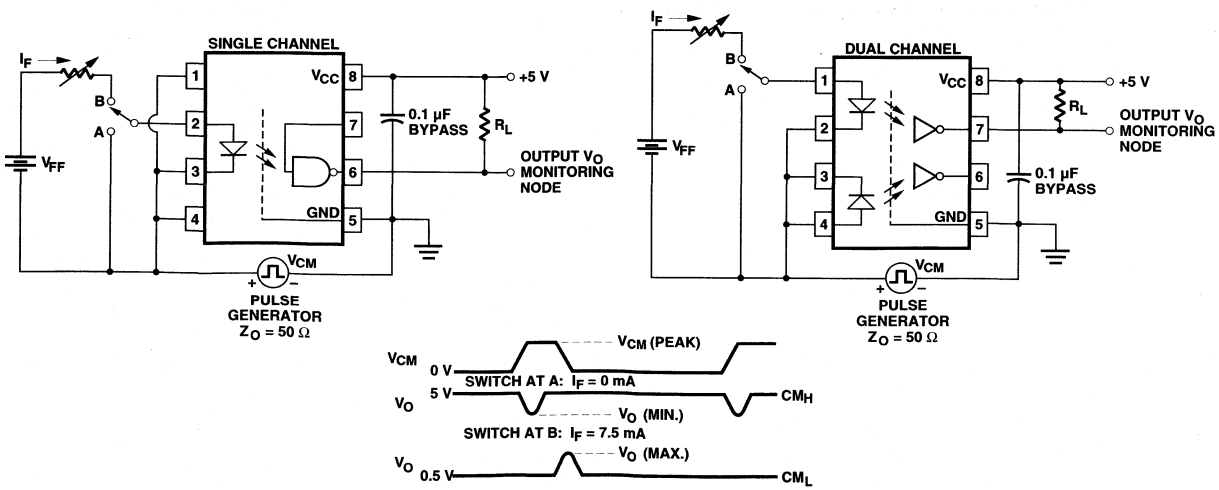


Figure 15. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

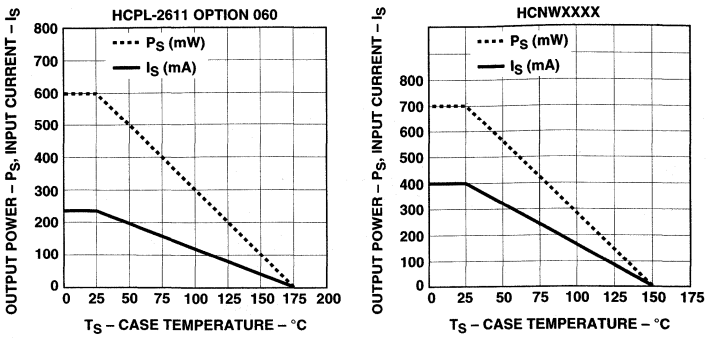


Figure 16. Thermal Derating Curve, Dependence of Safety Limiting Value with Case Temperature per VDE 0884.

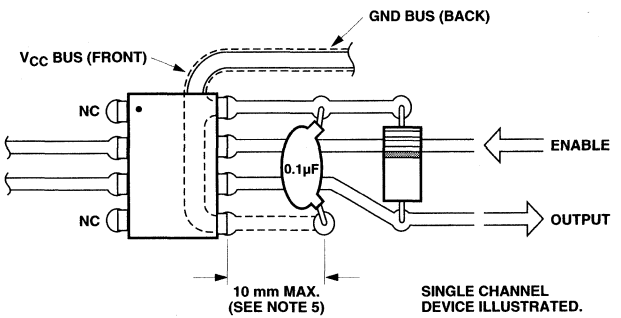
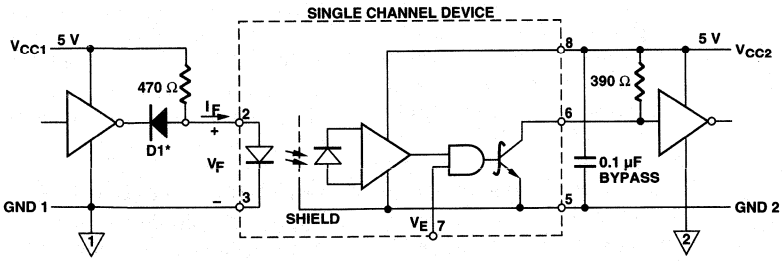


Figure 17. Recommended Printed Circuit Board Layout.



*DIODE D1 (1N916 OR EQUIVALENT) IS NOT REQUIRED FOR UNITS WITH OPEN COLLECTOR OUTPUT.

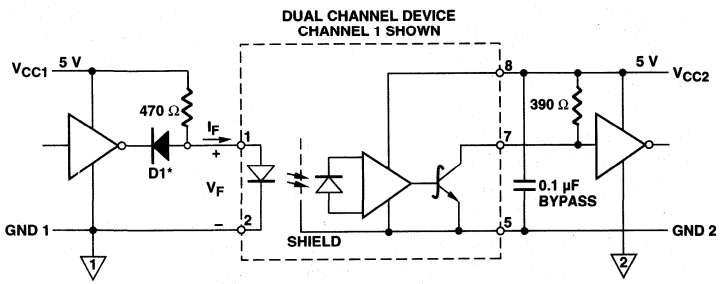


Figure 18. Recommended TTL/LSTTL to TTL/LSTTL Interface Circuit.

Propagation Delay, Pulse-Width Distortion and Propagation Delay Skew

Propagation delay is a figure of merit which describes how quickly a logic signal propagates through a system. The propagation delay from low to high (t_{PLH}) is the amount of time required for an input signal to propagate to the output, causing the output to change from low to high. Similarly, the propagation delay from high to low (t_{PHL}) is the amount of time required for the input signal to propagate to the output causing the output to change from high to low (see Figure 8).

Pulse-width distortion (PWD) results when t_{PLH} and t_{PHL} differ in value. PWD is defined as the difference between t_{PLH} and t_{PHL} and often determines the maximum data rate capability of a transmission system. PWD can be expressed in percent by dividing the PWD (in ns) by the minimum pulse width (in ns) being transmitted. Typically, PWD on the order of 20-30% of the minimum pulse width is tolerable; the exact figure depends on the particular application (RS232, RS422, T-l, etc.).

Propagation delay skew, t_{PSK}, is an important parameter to consider in parallel data applications where synchronization of signals on parallel data lines is a concern. If the parallel data is being sent through a group of optocouplers, differences in propagation delays will cause the data to arrive at the outputs of the optocouplers at different times. If this difference in propagation delays is large enough, it will determine the maximum rate at which parallel data can be sent through the optocouplers.

Propagation delay skew is defined as the difference between the minimum and maximum propagation delays, either t_{PLH} or t_{PHL}, for any given group of optocouplers which are operating under the same conditions (i.e., the same drive current, supply voltage, output load, and operating temperature). As illustrated in Figure 19, if the inputs of a group of optocouplers are switched either ON or OFF at the same time, t_{PSK} is the difference between the shortest propagation delay, either t_{PLH} or t_{PHL}, and the longest propagation delay, either t_{PLH} or t_{PHL}.

As mentioned earlier, t_{PSK} can determine the maximum parallel data transmission rate. Figure 20 is the timing diagram of a typical parallel data application with both the clock and the data lines being sent through optocouplers. The figure shows data and clock signals at the inputs and outputs of the optocouplers. To obtain the maximum data transmission rate, both edges of the clock signal are being used to clock the data; if only one edge were used, the clock signal would need to be twice as fast.

Propagation delay skew represents the uncertainty of where an edge might be after being sent through an optocoupler. Figure 20 shows that there will be uncertainty in both the data and the clock lines. It is important that these two areas of uncertainty not overlap, otherwise the clock signal might arrive before all of the data outputs have settled, or some of the data outputs may start to change before the clock signal has arrived. From these considerations, the absolute minimum pulse width that can be sent through optocouplers in a parallel application is twice t_{PSK}. A cautious design should use a slightly longer pulse width to ensure that any additional uncertainty in the rest of the circuit does not cause a problem.

The t_{PSK} specified optocouplers offer the advantages of guaranteed specifications for propagation delays, pulsewidth distortion and propagation delay skew over the recommended temperature, input current, and power supply ranges.

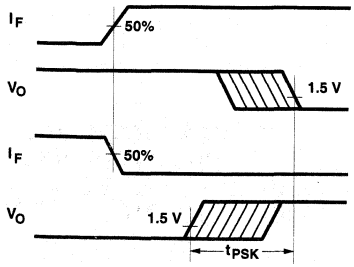


Figure 19. Illustration of Propagation Delay Skew - t_{PSK}.

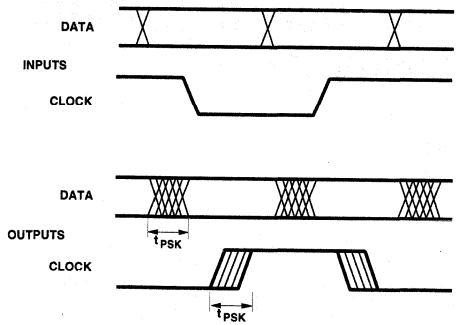


Figure 20. Parallel Data Transmission Example.

HEWLETT® PACKARD

HCMOS Compatible, High CMR, 10 MBd Optocouplers

Technical Data

HCPL-261A HCPL-061A
HCPL-263A HCPL-063A
HCPL-261N HCPL-061N
HCPL-263N HCPL-063N

Features

- **HCMOS/LSTTL/TTL Performance Compatible**
- **1000 V/μs Minimum Common Mode Rejection (CMR) at V_{CM} = 50 V (HCPL-261A Family) and 15 kV/μs Minimum CMR at V_{CM} = 1000 V (HCPL-261N Family)**
- **High Speed: 10 MBd Typical**
- **AC and DC Performance Specified over Industrial Temperature Range -40°C to +85°C**
- **Available in 8 Pin DIP, SOIC-8 Packages**
- **Safety Approval**
  UL Recognized per UL1577
  2500 V rms for 1 minute and
  5000 V rms for 1 minute
  (Option 020)
  CSA Approved
  VDE 0884 Approved with
  V_{IORM} = 630 V peak for
  HCPL-261A/261N
  Option 060

Applications

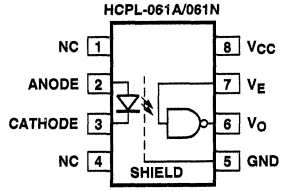
- **Low Input Current (3.0 mA) HCMOS Compatible Version of 6N137 Optocoupler**
- **Isolated Line Receiver**
- **Simplex/Multiplex Data Transmission**
- **Computer-Peripheral Interface**
- **Digital Isolation for A/D, D/A Conversion**
- **Switching Power Supplies**
- **Instrumentation Input/Output Isolation**
- **Ground Loop Elimination**
- **Pulse Transformer Replacement**

Description

The HCPL-261A family of optically coupled gates shown on this data sheet provide all the benefits of the industry standard 6N137 family with the added benefit of HCMOS compatible input current. This allows direct interface to all common circuit topologies without additional LED buffer or drive components. The AlGaAs LED used allows lower drive currents and reduces degradation by using the latest LED technology. On the single channel parts, an enable output allows the detector to be strobed. The output of the detector IC is an open collector schottky-clamped transistor. The internal shield provides a minimum common mode transient immunity of 1000 V/μs for the HCPL-261A family and 15000 V/μs for the HCPL-261N family.

Functional Diagram

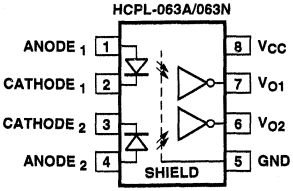
HCPL-261A/261N
HCPL-061A/061N



TRUTH TABLE
(POSITIVE LOGIC)

LED	ENABLE	OUTPUT
ON	H	L
OFF	H	H
ON	L	H
OFF	L	H
ON	NC	L
OFF	NC	H

HCPL-263A/263N
HCPL-063A/063N



TRUTH TABLE
(POSITIVE LOGIC)

LED	OUTPUT
ON	L
OFF	H

The connection of a 0.1 μF bypass capacitor between pins 5 and 8 is required.

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Selection Guide

Minimum CMR		Input On-Current (mA)	Output Enable	8-Pin DIP (300 Mil)		Small-Outline SO-8		Widebody (400 Mil)	Hermetic
dV/dt (V/µs)	V_{CM} (V)			Single Channel Package	Dual Channel Package	Single Channel Package	Dual Channel Package	Single Channel Package	Single and Dual Channel Packages
NA	NA	5	YES	6N137[1]		HCPL-0600[1]		HCNW137[1]	
			NO		HCPL-2630[1]		HCPL-0630[1]		
5,000	50		YES	HCPL-2601[1]		HCPL-0601[1]		HCNW2601[1]	
			NO		HCPL-2631[1]		HCPL-0631[1]		
10,000	1,000		YES	HCPL-2611[1]		HCPL-0611[1]		HCNW2611[1]	
			NO		HCPL-4661[1]		HCPL-0661[1]		
1,000	50		YES	HCPL-2602[1]					
3,500	300		YES	HCPL-2612[1]					
1,000	50	3	YES	HCPL-261A		HCPL-061A			
			NO		HCPL-263A		HCPL-063A		
1,000[2]	1,000		YES	HCPL-261N		HCPL-061N			
			NO		HCPL-263N		HCPL-063N		
1,000	50	12.5	[3]						HCPL-193X[1] HCPL-56XX[1] HCPL-66XX[1]

Notes:
1. Technical data are on separate HP publications.
2. 15 kV/µs with V_{CM} = 1 kV can be achieved using HP application circuit.
3. Enable is available for single channel products only, except for HCPL-193X devices.

Ordering Information

Specify Part Number followed by Option Number (if desired).

Example:

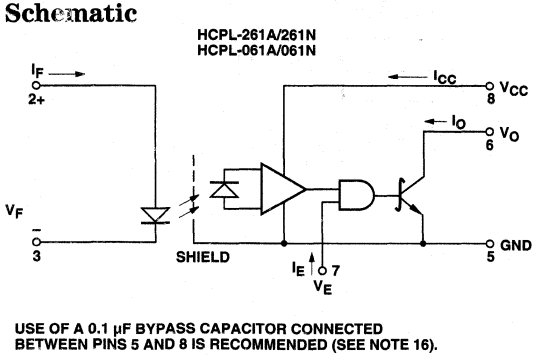
HCPL-261A#XXX

- 020 = 5000 V rms/1 minute UL Rating Option*
- 060 = VDE 0884 V_{IORM} = 630 Vpeak Option**
- 300 = Gull Wing Surface Mount Option***
- 500 = Tape and Reel Packaging Option

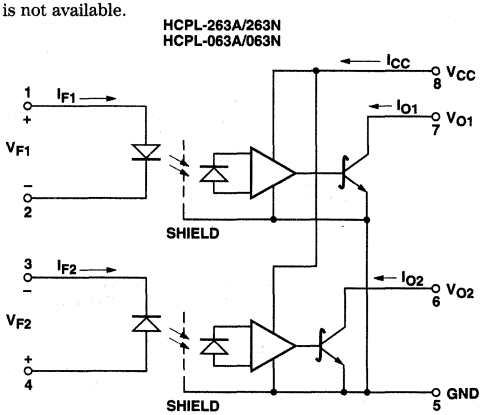
Option data sheets available. Contact your Hewlett-Packard sales representative or authorized distributor for information.

*For HCPL-261A/261N/263A/263N (8-pin DIP products) only.
**For HCPL-261A/261N only. Combination of Option 020 and Option 060 is not available.
***Gull wing surface mount option applies to through hole parts only.

Schematic



USE OF A 0.1 µF BYPASS CAPACITOR CONNECTED BETWEEN PINS 5 AND 8 IS RECOMMENDED (SEE NOTE 16).



HCPL-261A/261N/263A/263N Outline Drawing

Pin Location (for reference only)

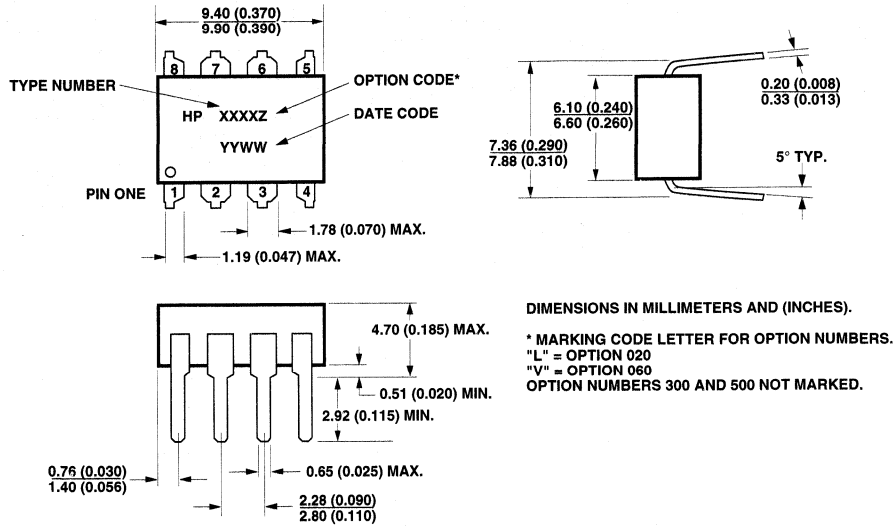


Figure 1. 8-Pin Dual In-Line Package Device Outline Drawing.

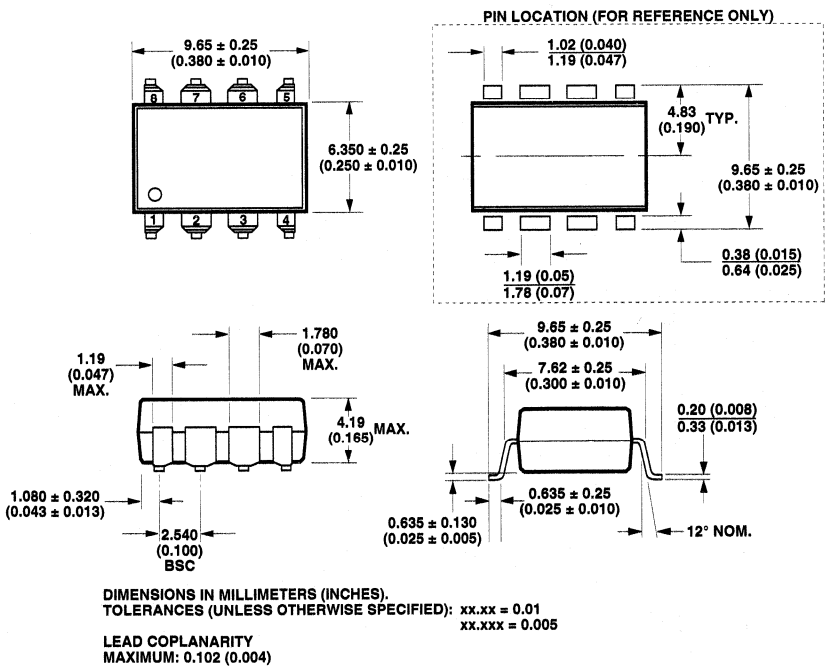


Figure 2. Gull Wing Surface Mount Option #300.

HCPL-061A/061N/063A/063N Outline Drawing

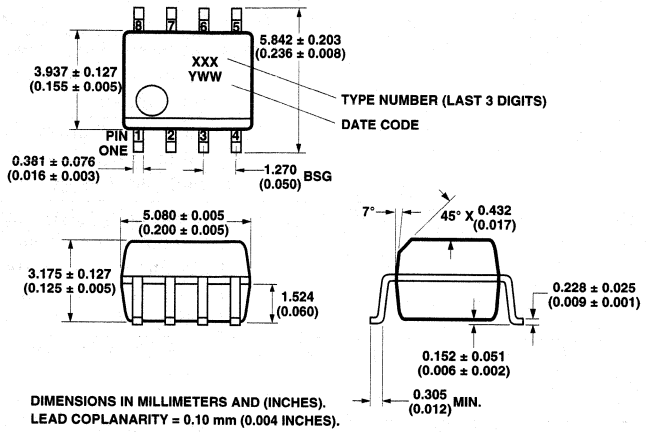
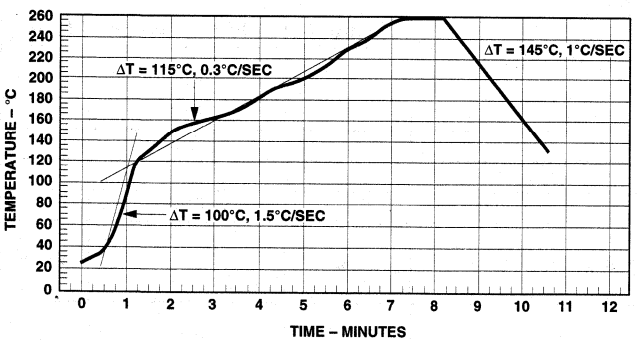


Figure 3. 8-Pin Small Outline Package Device Drawing.

Solder Reflow Temperature Profile (HCPL-06XX and Gull Wing Surface Mount Option 300 Parts)



Note: Use of Nonchlorine Activated Fluxes is Recommended.

Regulatory Information

The HCPL-261A and HCPL-261N families have been approved by the following organizations:

UL

Recognized under UL 1577, Component Recognition Program, File E55361.

CSA

Approved under CSA Component Acceptance Notice #5, File CA 88324.

VDE

Approved according to VDE 0884/06.92. (HCPL-261A/261N Option 060 only)

Insulation and Safety Related Specifications

Parameter	Symbol	8-Pin DIP (300 Mil) Value	SO-8 Value	Units	Conditions
Minimum External Air Gap (External Clearance)	L(101)	7.1	4.9	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L(102)	7.4	4.8	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	0.08	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity.
Tracking Resistance (Comparative Tracking Index)	CTI	200	200	Volts	DIN IEC 112/ VDE 0303 Part 1
Isolation Group		IIIa	IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Option 300 – surface mount classification is Class A in accordance with CECC 00802.

VDE 0884 Insulation Related Characteristics (HCPL-261A/261N Option 060 ONLY)

Description	Symbol	Characteristic	Units
Installation classification per DIN VDE 0110/1.89, Table 1			
for rated mains voltage ≤ 300 V rms		I-IV	
for rated mains voltage ≤ 450 V rms		I-III	
Climatic Classification		55/85/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	630	V_{peak}
Input to Output Test Voltage, Method b* V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial Discharge < 5 pC	V_{PR}	1181	V_{peak}
Input to Output Test Voltage, Method a* V_{IORM} x 1.5 = V_{PR}, Type and sample test, t_m = 60 sec, Partial Discharge < 5 pC	V_{PR}	945	V_{peak}
Highest Allowable Overvoltage* (Transient Overvoltage, t_{ini} = 10 sec)	V_{IOTM}	6000	V_{peak}
Safety Limiting Values (Maximum values allowed in the event of a failure, also see Figure 18, Thermal Derating curve.)			
Case Temperature	T_S	175	°C
Input Current	$I_{S,INPUT}$	230	mA
Output Power	$P_{S,OUTPUT}$	600	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	≥ 10^9	Ω

*Refer to the front of the optocoupler section of the current catalog, under Product Safety Regulations section (VDE 0884), for a detailed description.

Note: Isolation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuits in application.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	T_S	-55	125	°C	
Operating Temperature	T_A	-40	+85	°C	
Average Input Current	$I_{F(AVG)}$		10	mA	1
Reverse Input Voltage	V_R		3	Volts	
Supply Voltage	V_{CC}	-0.5	7	Volts	2
Enable Input Voltage	V_E	-0.5	5.5	Volts	
Output Collector Current (Each Channel)	I_O		50	mA	
Output Power Dissipation (Each Channel)	P_O		60	mW	3
Output Voltage (Each channel)	V_O	-0.5	7	Volts	
Lead Solder Temperature (Through Hole Parts Only)	260°C for 10 s, 1.6 mm Below Seating Plane				
Solder Reflow Temperature Profile (Surface Mount Parts Only)	See Package Outline Drawings section				

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Input Voltage, Low Level	V_{FL}	-3	0.8	V
Input Current, High Level	I_{FH}	3.0	10	mA
Power Supply Voltage	V_{CC}	4.5	5.5	Volts
High Level Enable Voltage	V_{EH}	2.0	V_{CC}	Volts
Low Level Enable Voltage	V_{EL}	0	0.8	Volts
Fan Out (at R_L = 1 kΩ)	N		5	TTL Loads
Output Pull-up Resistor	R_L	330	4k	Ω
Operating Temperature	T_A	-40	85	°C

Electrical Specifications

Over recommended operating temperature (T_A = -40°C to +85°C) unless otherwise specified.

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions		Fig.	Note
High Level Output Current	I_{OH}		3.1	100	µA	V_{CC} = 5.5 V, V_O = 5.5 V, V_F = 0.8 V, V_E = 2.0 V		4	18
Low Level Output Voltage	V_{OL}		0.4	0.6	V	V_{CC} = 5.5 V, I_{OL} = 13 mA (sinking), I_F = 3.0 mA, V_E = 2.0 V		5, 8	4, 18
High Level Supply Current	I_{CCH}		7	10	mA	V_E = 0.5 V**	V_{CC} = 5.5 V, I_F = 0 mA		4
			9	15		Dual Channel Products***			
Low Level Supply Current	I_{CCL}		8	13	mA	V_E = 0.5 V**	V_{CC} = 5.5 V, I_F = 3.0 mA		
			12	21		Dual Channel Products***			
High Level Enable Current**	I_{EH}		-0.6	-1.6	mA	V_{CC} = 5.5 V, V_E = 2.0 V			
Low Level Enable Current**	I_{EL}		-0.9	-1.6	mA	V_{CC} = 5.5 V, V_E = 0.5 V			
Input Forward Voltage	V_F	1.0	1.3	1.6	V	I_F = 4 mA		6	4
Temperature Co-efficient of Forward Voltage	$\Delta V_F/\Delta T_A$		-1.25		mV/°C	I_F = 4 mA			4
Input Reverse Breakdown Voltage	BV_R	3	5		V	I_R = 100 µA			4
Input Capacitance	C_{IN}		60		pF	f = 1 MHz, V_F = 0 V			

*All typical values at T_A = 25°C, V_{CC} = 5 V
**Single Channel Products only (HCPL-261A/261N/061A/061N)
***Dual Channel Products only (HCPL-263A/263N/063A/063N)

Switching Specifications

Over recommended operating temperature (T_A = -40°C to +85°C) unless otherwise specified

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Input Current Threshold High to Low	I_{THL}		1.5	3.0	mA	V_{CC} = 5.5 V, V_O = 0.6 V, I_O >13 mA (Sinking)	7, 10	18
Propagation Delay Time to High Output Level	t_{PLH}		52	100	ns	I_F = 3.5 mA, V_{CC} = 5.0 V, V_E = Open, C_L = 15 pF, R_L = 350 Ω	9, 11, 12	4, 9, 18
Propagation Delay Time to Low Output Level	t_{PHL}		53	100	ns		9, 11, 12	4, 10, 18
Pulse Width Distortion	PWD $\lvert t_{PHL} - t_{PLH} \rvert$		11	45	ns		9, 13	17, 18
Propagation Delay Skew	t_{PSK}			60	ns		24	11, 18
Output Rise Time	t_R		42		ns		9, 14	4, 18
Output Fall Time	t_F		12		ns		9, 14	4, 18
Propagation Delay Time of Enable from V_{EH} to V_{EL}	t_{EHL}		19		ns	I_F = 3.5 mA, V_{CC} = 5.0 V, V_{EL} = 0 V, V_{EH} = 3 V, C_L = 15 pF, R_L = 350 Ω	15, 16	12
Propagation Delay Time of Enable from V_{EL} to V_{EH}	t_{ELH}		30		ns		15, 16	12

*All typical values at T_A = 25°C, V_{CC} = 5 V.

Common Mode Transient Immunity Specifications, All values at T_A = 25°C

Parameter	Device	Symbol	Min.	Typ.	Max.	Units	Test Conditions		Fig.	Note
Output High Level Common Mode Transient Immunity	HCPL-261A HCPL-061A HCPL-263A HCPL-063A	$\lvert CM_H \rvert$	1	5		kV/µs	V_{CM} = 50 V	V_{CC} = 5.0 V, R_L = 350 Ω, I_F = 0 mA, T_A = 25°C $V_{O(MIN)}$ = 2 V	17	4, 13, 15, 18
	HCPL-261N HCPL-061N		1	5		kV/µs	V_{CM} = 1000 V			
	HCPL-263N HCPL-063N		15	25		kV/µs		Using HP App Circuit	20	4, 13, 15
Output Low Level Common Mode Transient Immunity	HCPL-261A HCPL-061A HCPL-263A HCPL-063A	$\lvert CM_L \rvert$	1	5		kV/µs	V_{CM} = 50 V	V_{CC} = 5.0 V, R_L = 350 Ω, I_F = 3.5 mA, $V_{O(MAX)}$ = 0.8 V T_A = 25°C	17	4, 14, 15, 18
	HCPL-261N HCPL-061N		1	5		kV/µs	V_{CM} = 1000 V			
	HCPL-263N HCPL-063N		15	25		kV/µs		Using HP App Circuit	20	4, 14, 15

Package Characteristics

All Typicals at $T_A = 25°C$

Parameter	Sym.	Package*	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage**	V_{ISO}		2500			V rms	RH ≤ 50%, t = 1 min., T_A = 25°C		5, 6
		OPT 020†	5000						5, 7
Input-Output Resistance	R_{I-O}			10^{12}		Ω	V_{I-O} = 500 Vdc		4, 8
Input-Output Capacitance	C_{I-O}			0.6		pF	f = 1 MHz, T_A = 25°C		4, 8
Input-Input Insulation Leakage Current	I_{I-I}	Dual Channel		0.005		μA	RH ≤ 45%, t = 5 s, V_{I-I} = 500 V		19
Resistance (Input-Input)	R_{I-I}	Dual Channel		10^{11}		Ω			19
Capacitance (Input-Input)	C_{I-I}	Dual 8-pin DIP		0.03		pF	f = 1 MHz		19
		Dual SO-8		0.25					

*Ratings apply to all devices except otherwise noted in the **Package** column.

**The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the VDE 0884 Insulation Characteristics Table (if applicable), your equipment level safety specification or HP Application Note 1074 entitled "Optocoupler Input-Output Endurance Voltage."

†For 8-pin DIP package devices (HCPL-261A/261N/263A/263N) only.

Notes:

1. Peaking circuits may be used which produce transient input currents up to 30 mA, 50 ns maximum pulse width, provided the average current does not exceed 10 mA.
2. 1 minute maximum.
3. Derate linearly above 80°C free-air temperature at a rate of 2.7 mW/°C for the SOIC-8 package.
4. Each channel.
5. Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.
6. In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 3000 V_{RMS} for 1 second (leakage detection current limit, $I_{I-O} \leq 5$ μA). This test is performed before the 100% production test for partial discharge (method b) shown in the VDE 0884 Insulation Characteristics Table, if applicable.
7. In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 6000 V_{RMS} for 1 second (leakage detection current limit, $I_{I-O} \leq 5$ μA).
8. Measured between the LED anode and cathode shorted together and pins 5 through 8 shorted together.
9. The t_{PLH} propagation delay is measured from the 1.75 mA point on the falling edge of the input pulse to the 1.5 V point on the rising edge of the output pulse.
10. The t_{PHL} propagation delay is measured from the 1.75 mA point on the rising edge of the input pulse to the 1.5 V point on the falling edge of the output pulse.
11. Propagation delay skew (t_{PSK}) is equal to the worst case difference in t_{PLH} and/or t_{PHL} that will be seen between any two units under the same test conditions and operating temperature.
12. Single channel products only (HCPL-261A/261N/061A/061N).
13. Common mode transient immunity in a Logic High level is the maximum tolerable $|dV_{CM}/dt|$ of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (i.e., Vo > 2.0 V).
14. Common mode transient immunity in a Logic Low level is the maximum tolerable $|dV_{CM}/dt|$ of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., V_O < 0.8 V).
15. For sinusoidal voltages $(|dV_{CM}/dt|)max = \pi f_{CM} V_{CM(P-P)}$.
16. Bypassing of the power supply line is required with a 0.1 μF ceramic disc capacitor adjacent to each optocoupler as shown in Figure 19. Total lead length between both ends of the capacitor and the isolator pins should not exceed 10 mm.
17. Pulse Width Distortion (PWD) is defined as the difference between t_{PLH} and t_{PHL} for any given device.
18. No external pull up is required for a high logic state on the enable input of a single channel product. If the V_E pin is not used, tying V_E to V_{CC} will result in improved CMR performance.
19. Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together. For dual channel parts only.

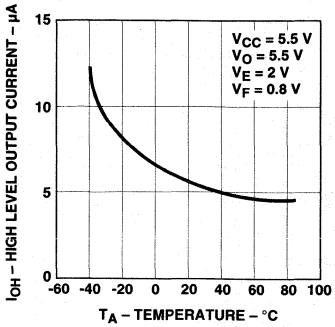


Figure 4. Typical High Level Output Current vs. Temperature.

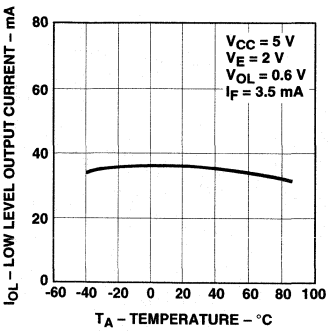


Figure 5. Low Level Output Current vs. Temperature.

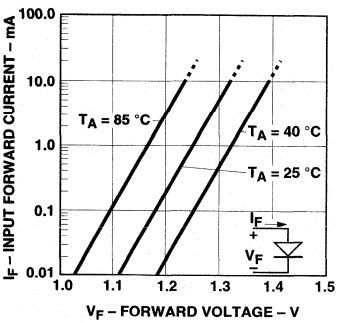


Figure 6. Typical Diode Input Forward Current Characteristic.

HCPL-261A fig 5

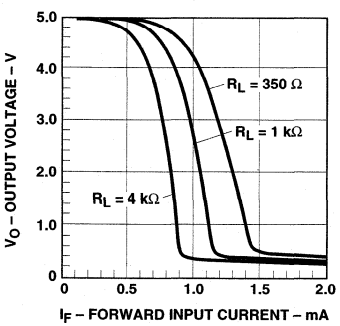


Figure 7. Typical Output Voltage vs. Forward Input Current.

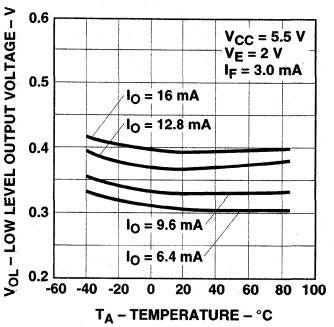


Figure 8. Typical Low Level Output Voltage vs. Temperature.

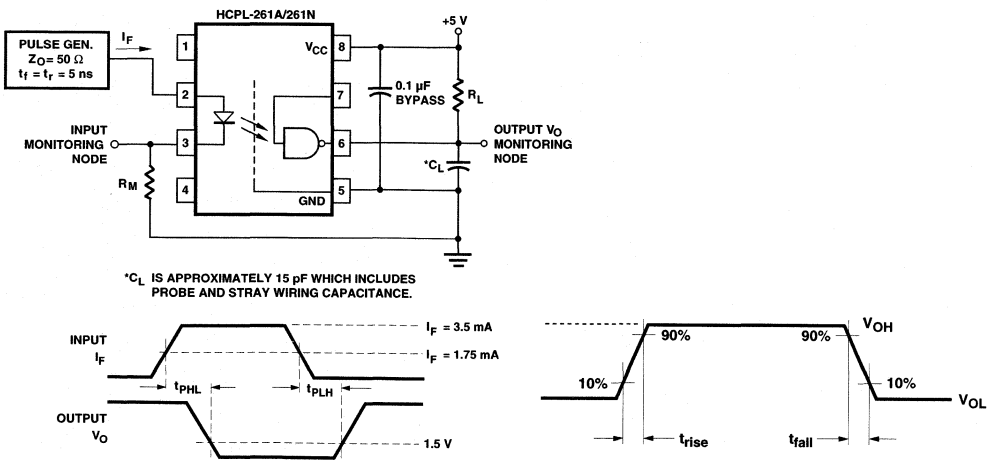


Figure 9. Test Circuit for t_{PHL} and t_{PLH}.

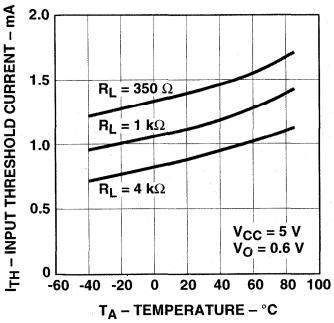


Figure 10. Typical Input Threshold Current vs. Temperature.

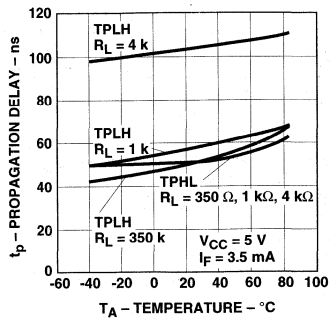


Figure 11. Typical Propagation Delay vs. Temperature.

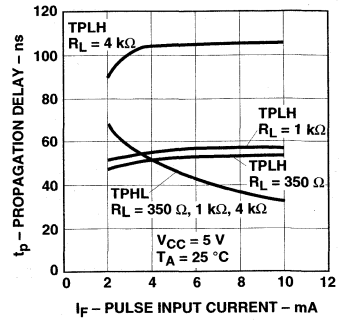


Figure 12. Typical Propagation Delay vs. Pulse Input Current.

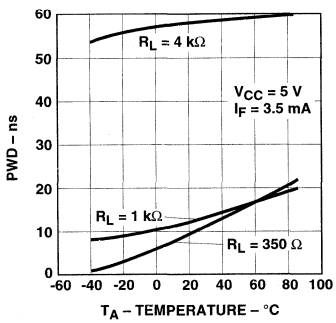


Figure 13. Typical Pulse Width Distortion vs. Temperature.

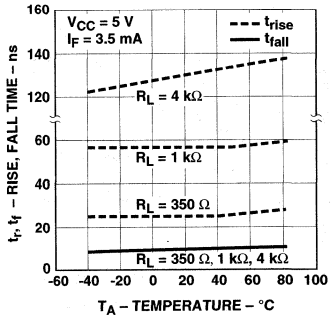


Figure 14. Typical Rise and Fall Time vs. Temperature.

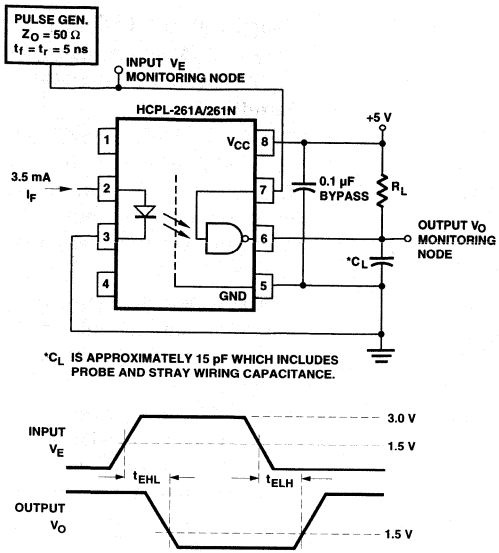


Figure 15. Test Circuit for t_{EHL} and t_{ELH}.

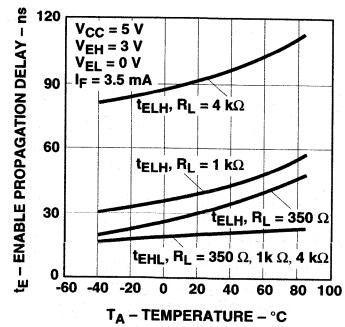


Figure 16. Typical Enable Propagation Delay vs. Temperature. HCPL-261A/-261N/-061A/-061N Only.

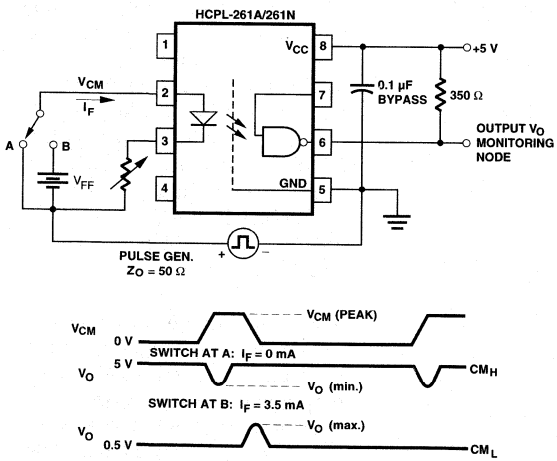


Figure 17. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

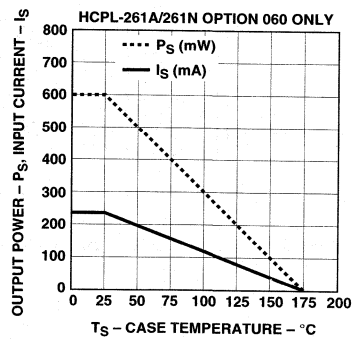


Figure 18. Thermal Derating Curve, Dependence of Safety Limiting Value with Case Temperature per VDE 0884.

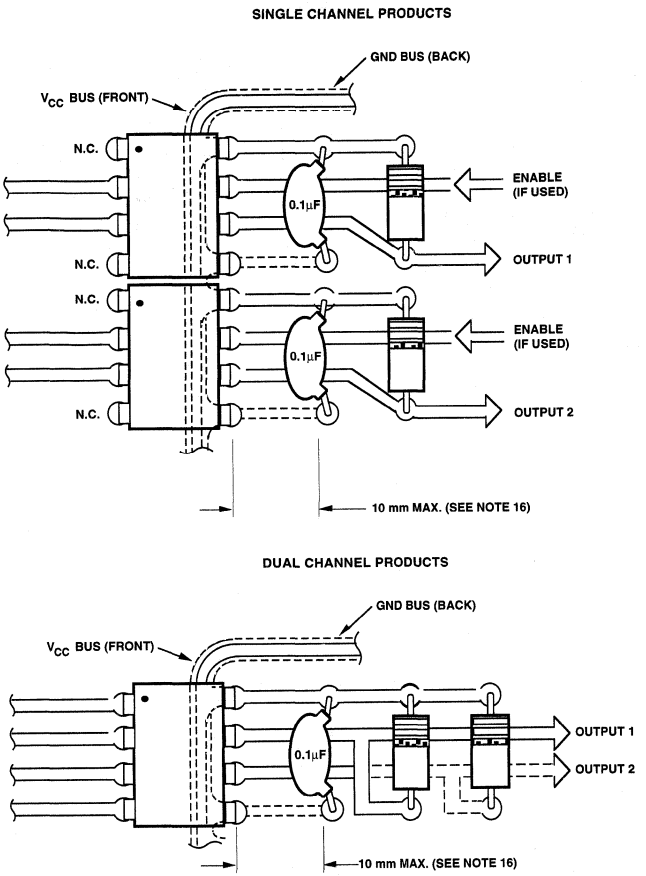
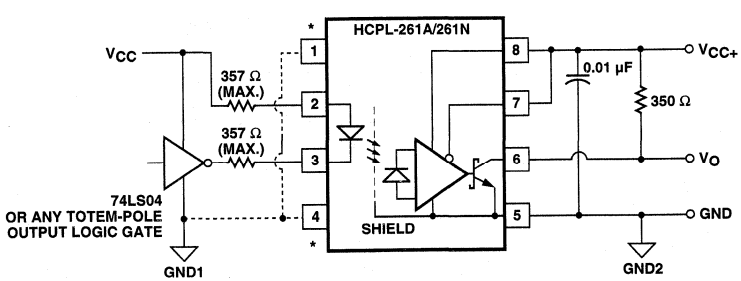


Figure 19. Recommended Printed Circuit Board Layout.



* HIGHER CMR MAY BE OBTAINABLE BY CONNECTING PINS 1, 4 TO INPUT GROUND (GND1).

Figure 20. Recommended Drive Circuit for HCPL-261A/-261N Families for High-CMR (Similar for HCPL-263A/-263N).

*Higher CMR May Be Obtainable by Connecting Pins 1, 4 to Input Ground (Gnd1).

Application Information

Common-Mode Rejection for HCPL-261A/HCPL-261N Families:

Figure 20 shows the recommended drive circuit for the HCPL-261N/-261A for optimal common-mode rejection performance. Two main points to note are:

1. The enable pin is tied to V_{CC} rather than floating (this applies to single-channel parts only).
2. Two LED-current setting resistors are used instead of one. This is to balance I_{LED} variation during common-mode transients.

If the enable pin is left floating, it is possible for common-mode transients to couple to the enable pin, resulting in common-mode failure. This failure mechanism only occurs when the LED is on and the output is in the Low State. It is identified as occurring when the transient output voltage rises above 0.8 V. Therefore, the enable pin should be connected to either V_{CC} or logic-level high for best common-mode performance with the output low (CMR_L). This failure mechanism is only present in single-channel parts (HCPL-261N, -261A, -061N, -061A) which have the enable function.

Also, common-mode transients can capacitively couple from the LED anode (or cathode) to the output-side ground causing current to be shunted away from the LED (which can be bad if the LED is on) or conversely cause current to be injected into the LED (bad if the LED is meant to be off). Figure 21 shows the parasitic capacitances which exists between LED

anode/cathode and output ground (C_{LA} and C_{LC}). Also shown in Figure 21 on the input side is an AC-equivalent circuit. Table 1 indicates the directions of I_{LP} and I_{LN} flow depending on the direction of the common-mode transient.

For transients occurring when the LED is on, common-mode rejection (CMR_L, since the output is in the "low" state) depends upon the amount of LED current drive (I_F). For conditions where I_F is close to the switching threshold (I_{TH}), CMR_L also depends on the extent which I_{LP} and I_{LN} balance each other. In other words, any condition where common-mode transients cause a momentary decrease in I_F (i.e. when $dV_{CM}/dt>0$ and $|I_{FP}| > |I_{FN}|$, referring to Table 1) will cause common-mode failure for transients which are fast enough.

Likewise for common-mode transients which occur when the LED is off (i.e. CMR_H, since the output is "high"), if an imbalance between I_{LP} and I_{LN} results in a transient I_F equal to or greater than the switching threshold of the optocoupler, the transient "signal" may cause the output to spike below 2 V (which constitutes a CMR_H failure).

By using the recommended circuit in Figure 20, good CMR can be achieved. (In the case of the -261N families, a minimum CMR of 15 kV/μs is guaranteed using this circuit.) The balanced I_{LED}-setting resistors help equalize I_{LP} and I_{LN} to reduce the amount by which I_{LED} is modulated from transient coupling through C_{LA} and C_{LC}.

CMR with Other Drive Circuits

CMR performance with drive circuits other than that shown in Figure 20 may be enhanced by following these guidelines:

1. Use of drive circuits where current is shunted from the LED in the LED "off" state (as shown in Figures 22 and 23). This is beneficial for good CMR_H.
2. Use of $I_{FH} > 3.5$ mA. This is good for high CMR_L.

Using any one of the drive circuits in Figures 22-24 with $I_F = 10$ mA will result in a typical CMR of 8 kV/μs for the HCPL-261N family, as long as the PC board layout practices are followed. Figure 22 shows a circuit which can be used with any totem-pole-output TTL/LSTTL/HCMOS logic gate. The buffer PNP transistor allows the circuit to be used with logic devices which have low current-sinking capability. It also helps maintain the driving-gate power-supply current at a constant level to minimize ground shifting for other devices connected to the input-supply ground.

When using an open-collector TTL or open-drain CMOS logic gate, the circuit in Figure 23 may be used. When using a CMOS gate to drive the optocoupler, the circuit shown in Figure 24 may be used. The diode in parallel with the R_{LED} speeds the turn-off of the optocoupler LED.

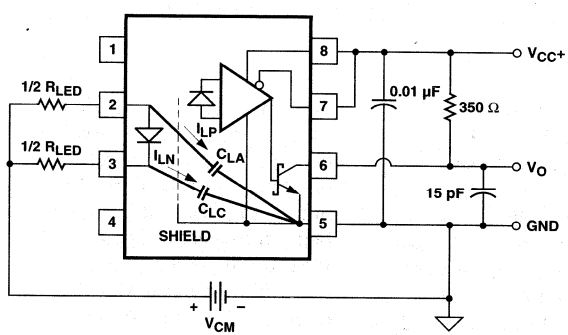


Figure 21. AC Equivalent Circuit for HCPL-261X.

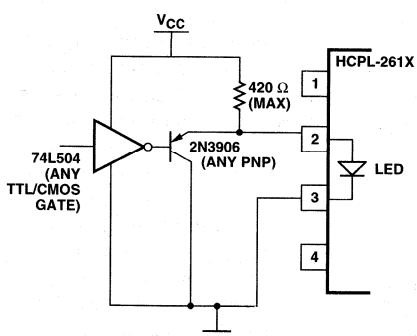


Figure 22. TTL Interface Circuit for the HCPL-261A/-261N Families.

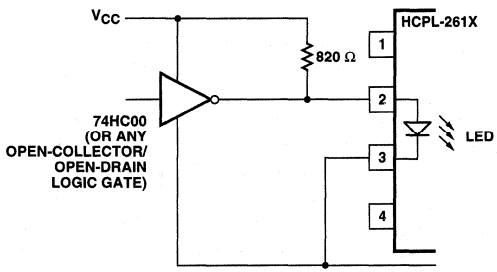


Figure 23. TTL Open-Collector/Open Drain Gate Drive Circuit for HCPL-261A/-261N Families.

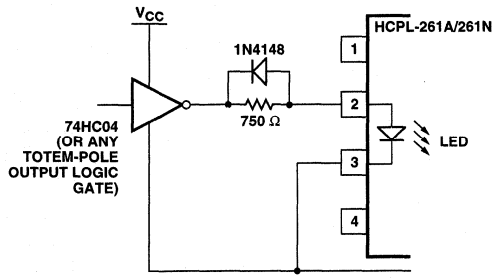


Figure 24. CMOS Gate Drive Circuit for HCPL-261A/-261N Families.

Table 1. Effects of Common Mode Pulse Direction on Transient I_{LED}

If dV_{CM}/dt Is:	then I_{LP} Flows:	and I_{LN} Flows:	If $\|I_{LP}\| < \|I_{LN}\|$, LED I_F Current Is Momentarily:	If $\|I_{LP}\| > \|I_{LN}\|$, LED I_F Current Is Momentarily:
positive (>0)	away from LED anode through C_{LA}	away from LED cathode through C_{LC}	increased	decreased
negative (<0)	toward LED anode through C_{LA}	toward LED cathode through C_{LC}	decreased	increased

Propagation Delay, Pulse-Width Distortion and Propagation Delay Skew

Propagation delay is a figure of merit which describes how quickly a logic signal propagates through a system. The propagation delay from low to high (t_{PLH}) is the amount of time required for an input signal to propagate to the output, causing the output to change from low to high. Similarly, the propagation delay from high to low (t_{PHL}) is the amount of time required for the input signal to propagate to the output, causing the output to change from high to low (see Figure 9).

Pulse-width distortion (PWD) results when t_{PLH} and t_{PHL} differ in value. PWD is defined as the difference between t_{PLH} and t_{PHL} and often determines the maximum data rate capability of a transmission system. PWD can be expressed in percent by dividing the PWD (in ns) by the minimum pulse width (in ns) being transmitted. Typically, PWD on the order of 20-30% of the minimum pulse width is tolerable; the exact figure depends on the particular application (RS232, RS422, T-1, etc.).

Propagation delay skew, t_{PSK}, is an important parameter to consider in parallel data applications where synchronization of signals on parallel data lines is a concern. If the parallel data is being sent through a group of optocouplers, differences in propagation delays will cause the data to arrive at the outputs of the optocouplers at different times. If this difference in propagation delay is large enough it will determine the maximum rate at which parallel data can be sent through the optocouplers.

Propagation delay skew is defined as the difference between the minimum and maximum propagation delays, either t_{PLH} or t_{PHL}, for any given group of optocouplers which are operating under the same conditions (i.e., the same drive current, supply voltage, output load, and operating temperature). As illustrated in Figure 25, if the inputs of a group of optocouplers are switched either ON or OFF at the same time, t_{PSK} is the difference between the shortest propagation delay, either t_{PLH} or t_{PHL}, and the longest propagation delay, either t_{PLH} or t_{PHL}.

As mentioned earlier, t_{PSK} can determine the maximum parallel

data transmission rate. Figure 26 is the timing diagram of a typical parallel data application with both the clock and the data lines being sent through optocouplers. The figure shows data and clock signals at the inputs and outputs of the optocouplers. To obtain the maximum data transmission rate, both edges of the clock signal are being used to clock the data; if only one edge were used, the clock signal would need to be twice as fast.

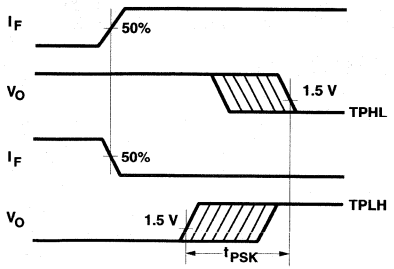


Figure 25. Illustration of Propagation Delay Skew – t_{PSK}.

Propagation delay skew represents the uncertainty of where an edge might be after being sent through an optocoupler. Figure 26 shows that there will be uncertainty in both the data and the clock lines. It is important that these two areas of uncertainty not overlap, otherwise the clock signal might arrive before all of the data outputs have settled, or some of the data outputs may start to change before the clock signal has arrived. From these considerations, the absolute minimum pulse width that can be sent through optocouplers in a parallel application is twice t_{PSK}. A cautious design should use a slightly longer pulse width to ensure that any additional uncertainty in the rest of the circuit does not cause a problem.

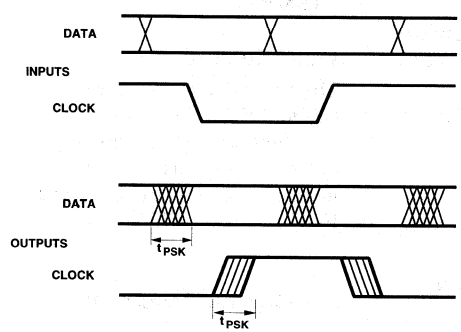


Figure 26. Parallel Data Transmission Example.

The t_{PSK} specified optocouplers offer the advantages of guaranteed specifications for propagation delays, pulse-width distortion, and propagation delay skew over the recommended temperature, input current, and power supply ranges.

HEWLETT® PACKARD

2.0 Amp Output Current IGBT Gate Drive Optocoupler

Technical Data

HCPL-3120

Features

- **2.0 A Minimum Peak Output Current**
- **15 kV/μs Minimum Common Mode Rejection (CMR) at V_{CM} = 1500 V**
- **0.5 V Maximum Low Level Output Voltage (V_{OL}) Eliminates Need for Negative Gate Drive**
- **I_{CC} = 5 mA Maximum Supply Current**
- **Under Voltage Lock-Out Protection (UVLO) with Hysteresis**
- **Wide Operating V_{CC} Range:** 15 to 30 Volts
- **500 ns Maximum Switching Speeds**
- **Industrial Temperature Range:** -40°C to 100°C
- **Safety Approval**
  UL Recognized - 2500 V rms for 1 minute per UL1577
  CSA Approval
  VDE 0884 Approved with V_{IORM} = 630 V peak (Option 060 only)

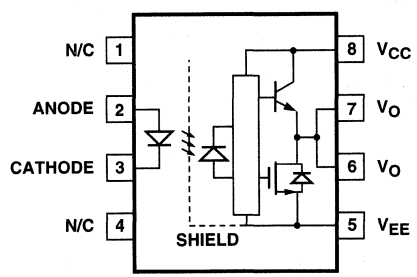
Applications

- **Isolated IGBT/MOSFET Gate Drive**
- **AC and Brushless DC Motor Drives**
- **Industrial Inverters**
- **Switch Mode Power Supplies (SMPS)**

Description

The HCPL-3120 consists of a GaAsP LED optically coupled to an integrated circuit with a power output stage. This optocoupler is ideally suited for driving power IGBTs and MOSFETs used in motor control inverter applications. The high operating voltage range of the output stage provides the drive voltages required by gate controlled devices. The voltage and current supplied by this optocoupler makes it ideally suited for directly driving IGBTs with ratings up to 1200 V/100 A. For IGBTs with higher ratings, the HCPL-3120 can be used to drive a discrete power stage which drives the IGBT gate.

Functional Diagram



TRUTH TABLE

LED	V_{CC} - V_{EE} "POSITIVE GOING" (i.e., TURN-ON)	V_{CC} - V_{EE} "NEGATIVE GOING" (i.e., TURN-OFF)	V_O
OFF	0 - 30 V	0 - 30 V	LOW
ON	0 - 11 V	0 - 9.5 V	LOW
ON	11 - 13.5 V	9.5 - 12 V	TRANSITION
ON	13.5 - 30 V	12 - 30 V	HIGH

A 0.1 μF bypass capacitor must be connected between pins 5 and 8.

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

5965-4779E

Ordering Information

Specify Part Number followed by Option Number (if desired)

Example

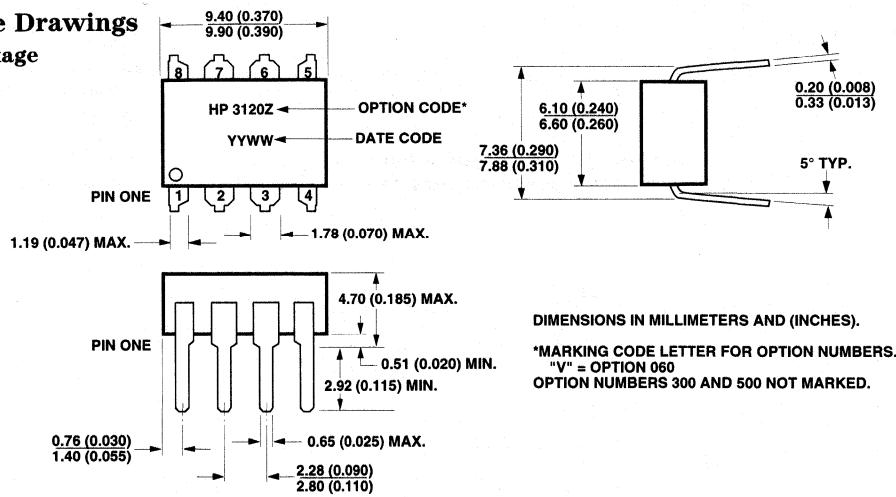
HCPL-3120#XXX

- No Option = Standard DIP Package, 50 per tube.
- 060 = VDE 0884 V_{IORM} = 630 V_{peak} Option, 50 per tube.
- 300 = Gull Wing Surface Mount Option, 50 per tube.
- 500 = Tape and Reel Packaging Option, 1000 per reel.

Option data sheets available. Contact Hewlett-Packard sales representative or authorized distributor.

Package Outline Drawings

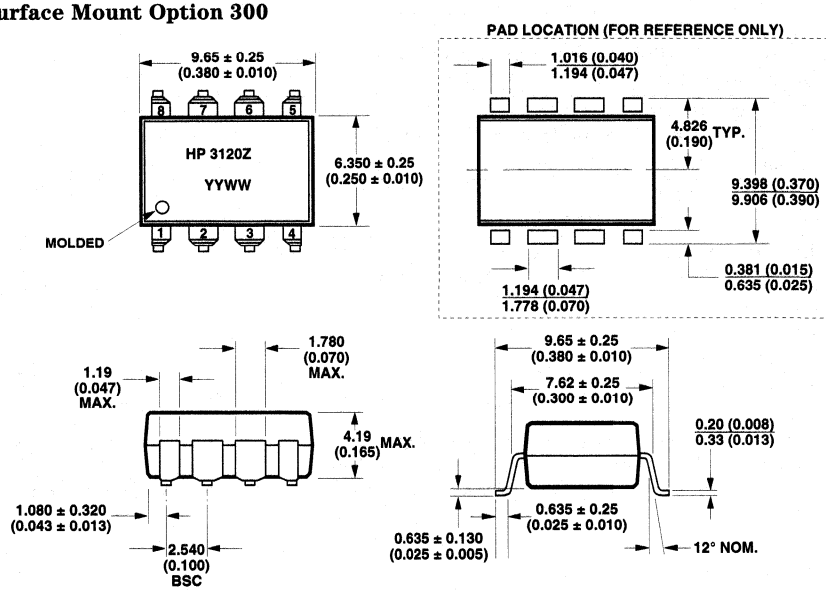
Standard DIP Package



DIMENSIONS IN MILLIMETERS AND (INCHES).

*MARKING CODE LETTER FOR OPTION NUMBERS.
"V" = OPTION 060
OPTION NUMBERS 300 AND 500 NOT MARKED.

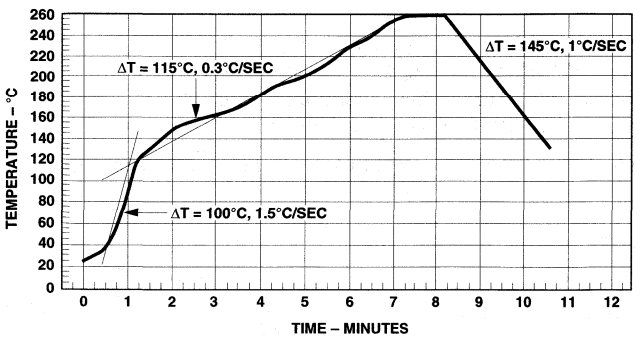
Gull Wing Surface Mount Option 300



DIMENSIONS IN MILLIMETERS (INCHES).
TOLERANCES (UNLESS OTHERWISE SPECIFIED): xx.xx = 0.01
xx.xxx = 0.005

LEAD COPLANARITY
MAXIMUM: 0.102 (0.004)

Reflow Temperature Profile



MAXIMUM SOLDER REFLOW THERMAL PROFILE
(NOTE: USE OF NON-CHLORINE ACTIVATED FLUXES IS RECOMMENDED.)

Regulatory Information

The HCPL-3120 has been approved by the following organizations:

UL

Recognized under UL 1577, Component Recognition Program, File E55361.

CSA

Approved under CSA Component Acceptance Notice #5, File CA 88324.

VDE (Option 060 Only)

Approved under VDE 0884/06.92 with V_{IORM} = 630 V peak.

VDE 0884 Insulation Characteristics (Option 060 Only)

Description	Symbol	Characteristic	Unit
Installation classification per DIN VDE 0110/1.89, Table 1			
for rated mains voltage ≤ 300 V rms		I-IV	
for rated mains voltage ≤ 450 V rms		I-III	
Climatic Classification		55/100/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	630	Vpeak
Input to Output Test Voltage, Method b* V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial discharge <5 pC	V_{PR}	1181	Vpeak
Input to Output Test Voltage, Method a* V_{IORM} x 1.5 = V_{PR}, Type and Sample Test, t_m = 60 sec, Partial discharge <5 pC	V_{PR}	945	Vpeak
Highest Allowable Overvoltage* (Transient Overvoltage t_{ini} = 10 sec)	V_{IOTM}	6000	Vpeak
Safety Limiting Values–Maximum Values Allowed in the Event of a Failure, Also See Figure 37, Thermal Derating Curve.			
Case Temperature	T_S	175	°C
Input Current	$I_{S, INPUT}$	230	mA
Output Power	$P_{S, OUTPUT}$	600	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	$\geq 10^9$	Ω

*Refer to the front of the optocoupler section of the current catalog, under Product Safety Regulations section, (VDE 0884) for a detailed description of Method a and Method b partial discharge test profiles.

Note: Isolation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuits in application.

Insulation and Safety Related Specifications

Parameter	Symbol	Value	Units	Conditions
Minimum External Air Gap (External Clearance)	L(101)	7.1	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L(102)	7.4	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	mm	Insulation thickness between emitter and detector; also known as distance through insulation.
Tracking Resistance (Comparative Tracking Index)	CTI	200	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Option 300 - surface mount classification is Class A in accordance with CECC 00802.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	T_S	-55.	125	°C	
Operating Temperature	T_A	-40	100	°C	
Average Input Current	$I_{F(AVG)}$		25	mA	1
Peak Transient Input Current (<1 µs pulse width, 300 pps)	$I_{F(TRAN)}$		1.0	A	
Reverse Input Voltage	V_R		5	Volts	
"High" Peak Output Current	$I_{OH(PEAK)}$		2.5	A	2
"Low" Peak Output Current	$I_{OL(PEAK)}$		2.5	A	2
Supply Voltage	$(V_{CC} - V_{EE})$	0	35	Volts	
Output Voltage	V_O	0	V_{CC}	Volts	
Output Power Dissipation	P_O		250	mW	3
Total Power Dissipation	P_T		295	mW	4
Lead Solder Temperature	260°C for 10 sec., 1.6 mm below seating plane				
Solder Reflow Temperature Profile	See Package Outline Drawings section				

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage	$(V_{CC} - V_{EE})$	15	30	Volts
Input Current (ON)	$I_{F(ON)}$	7	16	mA
Input Voltage (OFF)	$V_{F(OFF)}$	-3.0	0.8	V
Operating Temperature	T_A	-40	100	°C

Electrical Specifications (DC)

Over recommended operating conditions (T_A = -40 to 100°C, $I_{F(ON)}$ = 7 to 16 mA, $V_{F(OFF)}$ = -3.0 to 0.8 V, V_{CC} = 15 to 30 V, V_{EE} = Ground) unless otherwise specified.

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
High Level Output Current	I_{OH}	0.5	1.5		A	V_O = (V_{CC} - 4 V)	2, 3,	5
		2.0			A	V_O = (V_{CC} - 15 V)	17	2
Low Level Output Current	I_{OL}	0.5	2.0		A	V_O = (V_{EE} + 2.5 V)	5, 6,	5
		2.0			A	V_O = (V_{EE} + 15V)	18	2
High Level Output Voltage	V_{OH}	(V_{CC} - 4)	(V_{CC} - 3)		V	I_O = -100 mA	1, 3, 19	6, 7
Low Level Output Voltage	V_{OL}		0.1	0.5	V	I_O = 100 mA	4, 6, 20	
High Level Supply Current	I_{CCH}		2.0	5.0	mA	Output Open, I_F = 7 to 16 mA	7, 8	
Low Level Supply Current	I_{CCL}		2.0	5.0	mA	Output Open, V_F = -3.0 to +0.8 V		
Threshold Input Current Low to High	I_{FLH}		2.3	5.0	mA	I_O = 0 mA, V_O > 5 V	9, 15, 21	
Threshold Input Voltage High to Low	V_{FHL}	0.8			V			
Input Forward Voltage	V_F	1.2	1.5	1.8	V	I_F = 10 mA	16	
Temperature Coefficient of Forward Voltage	$\Delta V_F/\Delta T_A$		-1.6		mV/°C	I_F = 10 mA		
Input Reverse Breakdown Voltage	BV_R	5			V	Ir = 10 µA		
Input Capacitance	C_{IN}		60		pF	f = 1 MHz, V_F = 0 V		
UVLO Threshold	V_{UVLO+}	11.0	12.3	13.5	V	V_O > 5 V, I_F = 10 mA	22, 36	
	V_{UVLO-}	9.5	10.7	12.0				
UVLO Hysteresis	$UVLO_{HYS}$		1.6					

* All typical values at T_A = 25°C and V_{CC} - V_{EE} = 30 V, unless otherwise noted.

Switching Specifications (AC)

Over recommended operating conditions (T_A = -40 to 100°C, $I_{F(ON)}$ = 7 to 16 mA, $V_{F(OFF)}$ = -3.0 to 0.8 V, V_{CC} = 15 to 30 V, V_{EE} = Ground) unless otherwise specified.

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to High Output Level	t_{PLH}	0.10	0.30	0.50	µs	Rg = 10 Ω, Cg = 10 nF, f = 10 kHz, Duty Cycle = 50%	10, 11, 12, 13 14, 23	14
Propagation Delay Time to Low Output Level	t_{PHL}	0.10	0.27	0.50	µs			
Pulse Width Distortion	PWD			0.3	µs			15
Propagation Delay Difference Between Any Two Parts	(t_{PHL} - t_{PLH}) PDD	-0.35		0.35	µs		34,35	10
Rise Time	t_r		0.1		µs		23	
Fall Time	t_f		0.1		µs			
UVLO Turn On Delay	$t_{UVLO\ ON}$		0.8		µs	V_O > 5 V, I_F = 10 mA	22	
UVLO Turn Off Delay	$t_{UVLO\ OFF}$		0.6			V_O < 5 V, I_F = 10 mA		
Output High Level Common Mode Transient Immunity	$\|CM_H\|$	15	30		kV/µs	T_A = 25°C, I_F = 10 to 16 mA, V_{CM} = 1500 V, V_{CC} = 30 V	24	11, 12
Output Low Level Common Mode Transient Immunity	$\|CM_L\|$	15	30		kV/µs	T_A = 25°C, V_{CM} = 1500 V, V_F = 0 V, V_{CC} = 30 V		11, 13

*All typical values at T_A = 25°C and V_{CC} - V_{EE} = 30 V, unless otherwise noted.

Package Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage**	V_{ISO}	2500			V_{RMS}	RH < 50%, t = 1 min., T_A = 25°C		8, 9
Resistance (Input - Output)	R_{I-O}		10^{12}		Ω	V_{I-O} = 500 V_{DC}		9
Capacitance (Input - Output)	C_{I-O}		0.6		pF	f = 1 MHz		
LED-to-Case Thermal Resistance	θ_{LC}		467		°C/W	Thermocoupler located at center underside of package	28	
LED-to-Detector Thermal Resistance	θ_{LD}		442		°C/W			
Detector-to-Case Thermal Resistance	θ_{DC}		126		°C/W			

**The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to your equipment level safety specification or HP Application Note 1074 entitled "Optocoupler Input-Output Endurance Voltage."

Notes:

1. Derate linearly above 70°C free-air temperature at a rate of 0.3 mA/°C.
2. Maximum pulse width = 10 µs, maximum duty cycle = 0.2%. This value is intended to allow for component tolerances for designs with I_O peak minimum = 2.0 A. See Applications section for additional details on limiting I_{OH} peak.
3. Derate linearly above 70°C free-air temperature at a rate of 4.8 mW/°C.
4. Derate linearly above 70°C free-air temperature at a rate of 5.4 mW/°C. The maximum LED junction temperature should not exceed 125°C.
5. Maximum pulse width = 50 µs, maximum duty cycle = 0.5%.
6. In this test V_{OH} is measured with a dc load current. When driving capacitive loads V_{OH} will approach V_{CC} as I_{OH} approaches zero amps.
7. Maximum pulse width = 1 ms, maximum duty cycle = 20%.
8. In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 3000 Vrms for 1 second (leakage detection current limit, $I_{I-O} \leq 5$ µA). This test is performed before the 100% production test for partial discharge (method b) shown in the VDE 0884 Insulation Characteristic Table, if applicable.
9. Device considered a two-terminal device: pins 1, 2, 3, and 4 shorted together and pins 5, 6, 7, and 8 shorted together.
10. The difference between t_{PHL} and t_{PLH} between any two HCPL-3120 parts under the same test condition.
11. Pins 1 and 4 need to be connected to LED common.
12. Common mode transient immunity in the high state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in the high state (i.e., $V_O > 15.0$ V).
13. Common mode transient immunity in a low state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in a low state (i.e., $V_O < 1.0$ V).
14. This load condition approximates the gate load of a 1200V/75A IGBT.
15. Pulse Width Distortion (PWD) is defined as $|t_{PHL}-t_{PLH}|$ for any given device.

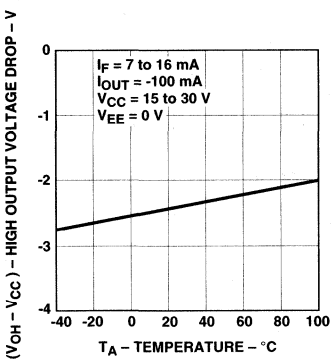


Figure 1. V_{OH} vs. Temperature.

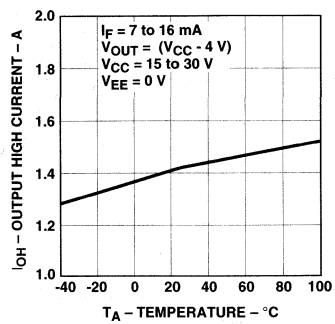


Figure 2. I_{OH} vs. Temperature.

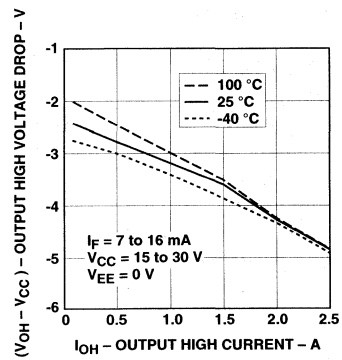


Figure 3. V_{OH} vs. I_{OH}.

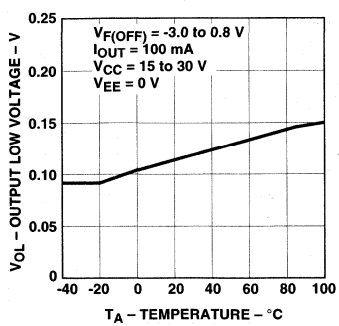


Figure 4. V_{OL} vs. Temperature.

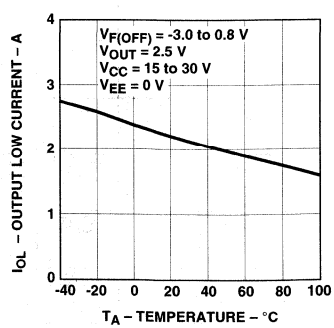


Figure 5. I_{OL} vs. Temperature.

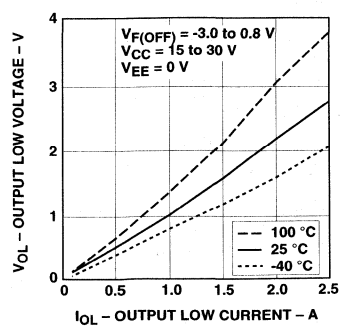


Figure 6. V_{OL} vs. I_{OL}.

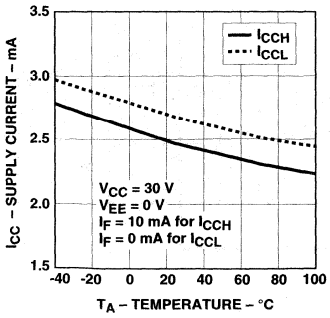


Figure 7. I_{CC} vs. Temperature.

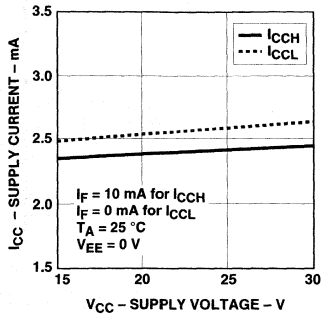


Figure 8. I_{CC} vs. V_{CC}.

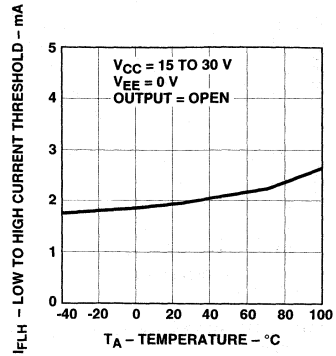


Figure 9. I_{FLH} vs. Temperature.

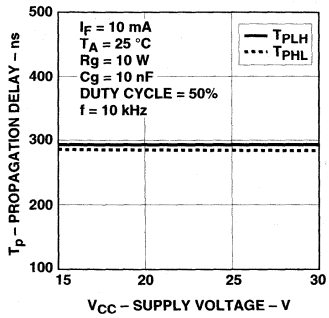


Figure 10. Propagation Delay vs. V_{CC}.

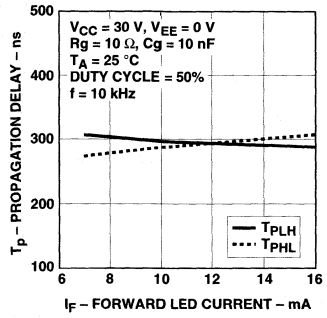


Figure 11. Propagation Delay vs. I_F.

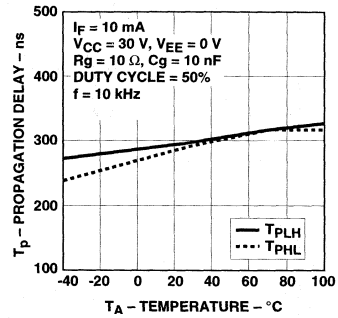


Figure 12. Propagation Delay vs. Temperature.

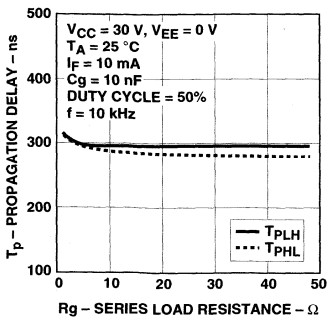


Figure 13. Propagation Delay vs. Rg.

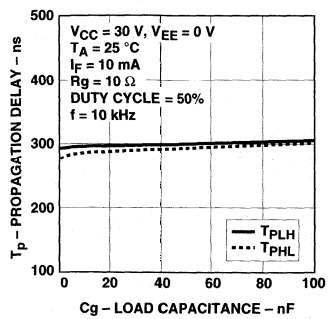


Figure 14. Propagation Delay vs. Cg.

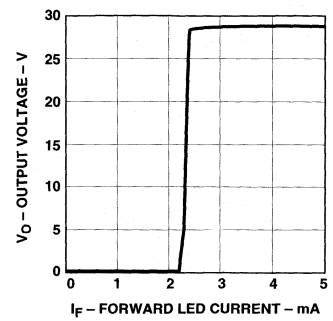


Figure 15. Transfer Characteristics.

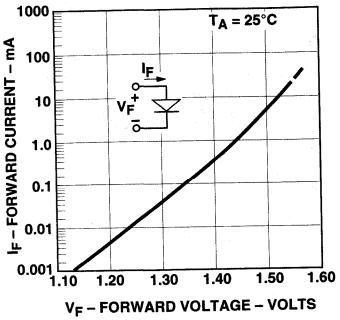


Figure 16. Input Current vs. Forward Voltage.

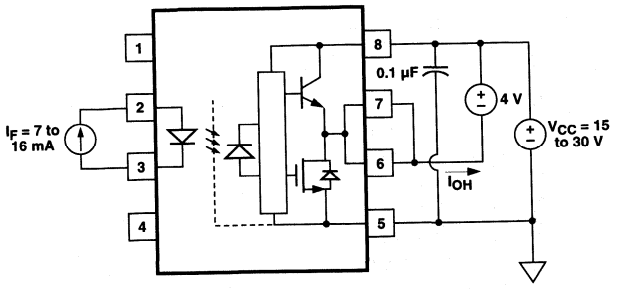


Figure 17. I_{OH} Test Circuit.

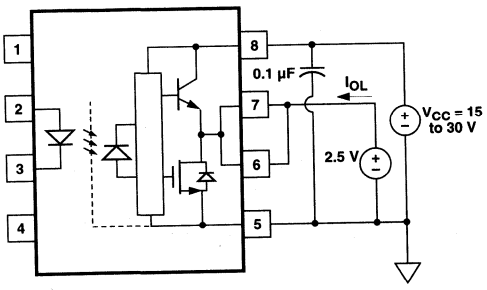


Figure 18. I_{OL} Test Circuit.

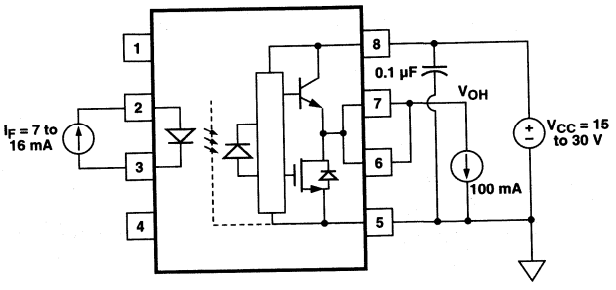


Figure 19. V_{OH} Test Circuit.

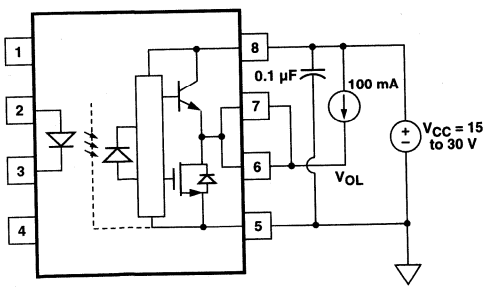


Figure 20. V_{OL} Test Circuit.

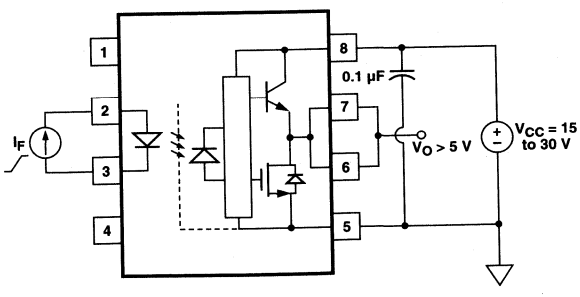


Figure 21. I_{FLH} Test Circuit.

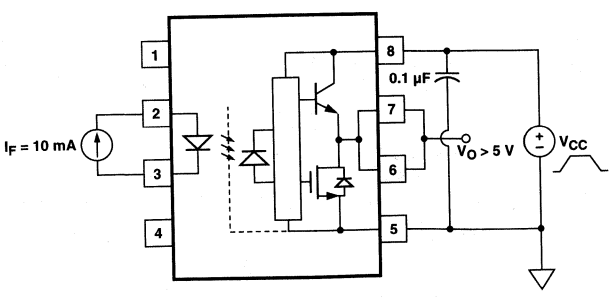


Figure 22. UVLO Test Circuit.

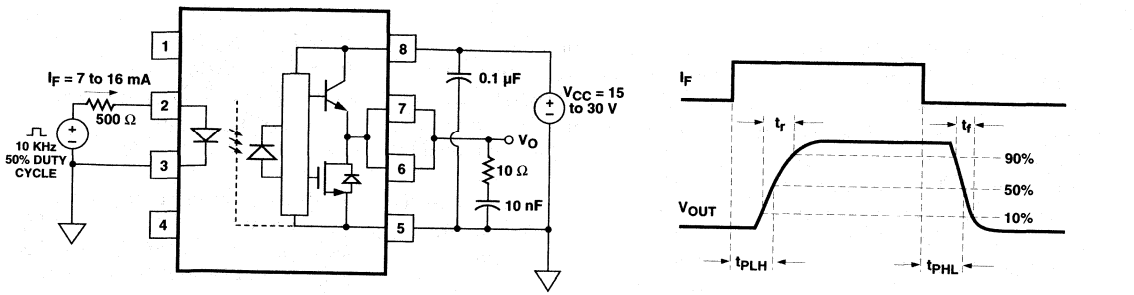


Figure 23. t_{PLH}, t_{PHL}, t_r, and t_f Test Circuit and Waveforms.

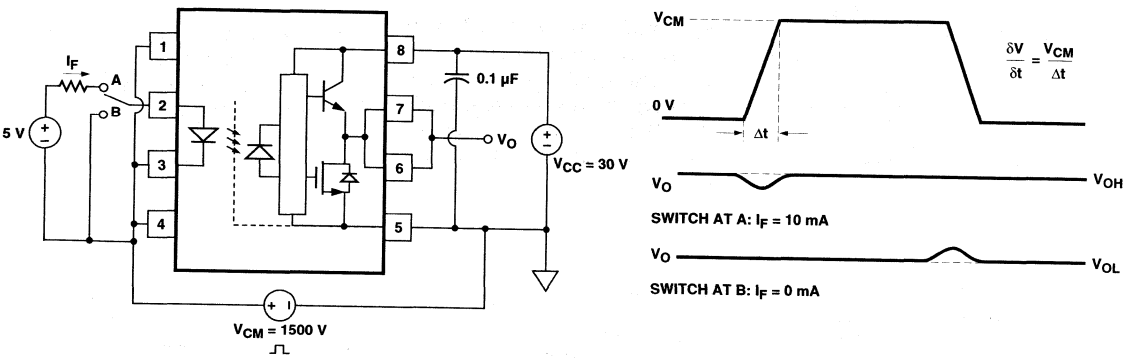


Figure 24. CMR Test Circuit and Waveforms.

Applications Information

Eliminating Negative IGBT Gate Drive

To keep the IGBT firmly off, the HCPL-3120 has a very low maximum V_{OL} specification of 0.5 V. The HCPL-3120 realizes this very low V_{OL} by using a DMOS transistor with 1 Ω (typical) on resistance in its pull down circuit. When the HCPL-3120 is in the low state, the IGBT gate is shorted to the emitter by Rg + 1 Ω. Minimizing Rg and the lead inductance from the HCPL-3120 to the IGBT gate and emitter (possibly by mounting the HCPL-3120 on a small PC board directly above the IGBT) can eliminate the need for negative IGBT gate drive in many applications as shown in Figure 25. Care should be taken with such a PC board design to avoid routing the IGBT collector or emitter traces close to the HCPL-3120 input as this can result in unwanted coupling of transient signals into the HCPL-3120 and degrade performance. (If the IGBT drain must be routed near the HCPL-3120 input, then the LED should be reverse-biased when in the off state, to prevent the transient signals coupled from the IGBT drain from turning on the HCPL-3120.)

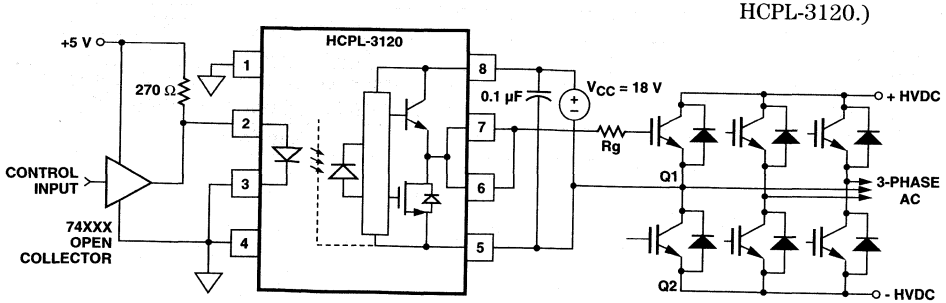


Figure 25. Recommended LED Drive and Application Circuit.

Selecting the Gate Resistor (Rg) to Minimize IGBT Switching Losses.

Step 1: Calculate Rg Minimum from the I_{OL} Peak Specification. The IGBT and Rg in Figure 26 can be analyzed as a simple RC circuit with a voltage supplied by the HCPL-3120.

$$Rg \geq \frac{(V_{CC} - V_{EE} - V_{OL})}{I_{OLPEAK}}$$

$$= \frac{(V_{CC} - V_{EE} - 2\ V)}{I_{OLPEAK}}$$

$$= \frac{(15\ V + 5\ V - 2\ V)}{2.5\ A}$$

$$= 7.2\ \Omega \cong 8\ \Omega$$

The V_{OL} value of 2 V in the previous equation is a conservative value of V_{OL} at the peak current of 2.5A (see Figure 6). At lower Rg values the voltage supplied by the HCPL-3120 is not an ideal voltage step. This results in lower peak currents (more margin) than predicted by this analysis. When negative gate drive is not used V_{EE} in the previous equation is equal to zero volts.

Step 2: Check the HCPL-3120 Power Dissipation and Increase Rg if Necessary. The HCPL-3120 total power dissipation (P_T) is equal to the sum of the emitter power (P_E) and the output power (P_O):

$$P_T = P_E + P_O$$

$$P_E = I_F \cdot V_F \cdot Duty\ Cycle$$

$$P_O = P_{O(BIAS)} + P_{O\ (SWITCHING)}$$

$$= I_{CC} \cdot (V_{CC} - V_{EE}) + E_{SW}(R_G, Q_G) \cdot f$$

For the circuit in Figure 26 with I_F (worst case) = 16 mA, Rg = 8 Ω, Max Duty Cycle = 80%, Qg = 500 nC, f = 20 kHz and T_A max = 85C:

$$P_E = 16\ mA \cdot 1.8\ V \cdot 0.8 = 23\ mW$$

$$P_O = 4.25\ mA \cdot 20\ V + 5.2\ \mu J \cdot 20\ kHz$$

$$= 85\ mW + 104\ mW$$

$$= 189\ mW$$

$$> 178\ mW\ (P_{O(MAX)}\ @\ 85C$$

$$= 250\ mW\text{–}15C * 4.8\ mW/C)$$

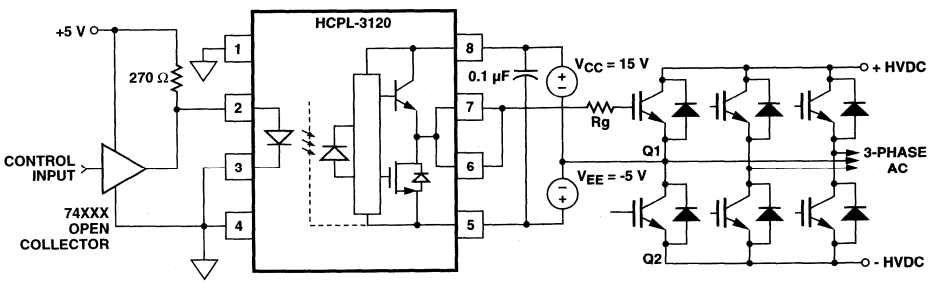


Figure 26. HCPL-3120 Typical Application Circuit with Negative IGBT Gate Drive.

P_E Parameter	Description
I_F	LED Current
V_F	LED On Voltage
Duty Cycle	Maximum LED Duty Cycle

P_O Parameter	Description
I_{CC}	Supply Current
V_{CC}	Positive Supply Voltage
V_{EE}	Negative Supply Voltage
E_{SW}(Rg,Qg)	Energy Dissipated in the HCPL-3120 for each IGBT Switching Cycle (See Figure 27)
f	Switching Frequency

The value of 4.25 mA for I_{CC} in the previous equation was obtained by derating the I_{CC} max of 5 mA (which occurs at -40°C) to I_{CC} max at 85C (see Figure 7).

Since P_O for this case is greater than $P_{O(MAX)}$, Rg must be increased to reduce the HCPL-3120 power dissipation.

$$P_{O(SWITCHING\ MAX)} = P_{O(MAX)} - P_{O(BIAS)} = 178\ mW - 85\ mW = 93\ mW$$

$$E_{SW(MAX)} = \frac{P_{O(SWITCHINGMAX)}}{f} = \frac{93\ mW}{20\ kHz} = 4.65\ \mu W$$

For Qg = 500 nC, from Figure 27, a value of E_{SW} = 4.65 µW gives a Rg = 10.3 Ω.

Thermal Model

The steady state thermal model for the HCPL-3120 is shown in Figure 28. The thermal resistance values given in this model can be used to calculate the temperatures at each node for a given operating condition. As shown by the model, all heat generated flows through θ_{CA} which raises the case temperature T_C accordingly. The value of θ_{CA} depends on the conditions of the board design and is, therefore, determined by the designer. The value of θ_{CA} = 83°C/W was obtained from thermal measurements using a 2.5 x 2.5 inch PC board, with small traces (no ground plane), a single HCPL-3120 soldered into the center of the board and still air. The absolute maximum power dissipation derating specifications assume a θ_{CA}value of 83°C/W.

From the thermal mode in Figure 28 the LED and detector IC junction temperatures can be expressed as:

$$T_{JE} = P_E \cdot (\theta_{LC} || (\theta_{LD} + \theta_{DC}) + \theta_{CA}) + P_D \cdot \left(\frac{\theta_{LC} * \theta_{DC}}{\theta_{LC} + \theta_{DC} + \theta_{LD}} + \theta_{CA} \right) + T_A$$

$$T_{JD} = P_E \left(\frac{\theta_{LC} \cdot \theta_{DC}}{\theta_{LC} + \theta_{DC} + \theta_{LD}} + \theta_{CA} \right) + P_D \cdot (\theta_{DC} || (\theta_{LD} + \theta_{LC}) + \theta_{CA}) + T_A$$

Inserting the values for θ_{LC} and θ_{DC} shown in Figure 28 gives:

$$T_{JE} = P_E \cdot (256°C/W + \theta_{CA}) + P_D \cdot (57°C/W + \theta_{CA}) + T_A$$
$$T_{JD} = P_E \cdot (57°C/W + \theta_{CA}) + P_D \cdot (111°C/W + \theta_{CA}) + T_A$$

For example, given P_E = 45 mW, P_O = 250 mW, T_A = 70°C and θ_{CA} = 83°C/W:

$$T_{JE} = P_E \cdot 339°C/W + P_D \cdot 140°C/W + T_A = 45\ mW \cdot 339°C/W + 250\ mW \cdot 140°C/W + 70°C = 120°C$$

$$T_{JD} = P_E \cdot 140°C/W + P_D \cdot 194°C/W + T_A = 45\ mW \cdot 140C/W + 250\ mW \cdot 194°C/W + 70°C = 125°C$$

T_{JE} and T_{JD} should be limited to 125C based on the board layout and part placement (θ_{CA}) specific to the application.

LED Drive Circuit Considerations for Ultra High CMR Performance.

Without a detector shield, the dominant cause of optocoupler CMR failure is capacitive coupling from the input side of the optocoupler, through the package, to the detector IC as shown in Figure 29. The HCPL-3120 improves CMR performance by using a detector IC with an optically transparent Faraday shield, which diverts the capacitively coupled current away from the sensitive IC circuitry. However, this shield does not eliminate the capacitive coupling between the LED and optocoupler pins 5-8 as shown in Figure 30. This capacitive coupling causes perturbations in the LED current during common mode transients and becomes the major source of CMR failures for a shielded optocoupler. The main design objective of a high CMR LED drive circuit becomes keeping the LED in the proper state (on or off) during common mode transients. For example, the recommended application circuit (Figure 25), can achieve 15 kV/µs CMR while minimizing component complexity.

Techniques to keep the LED in the proper state are discussed in the next two sections.

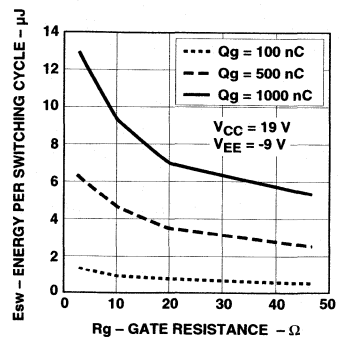
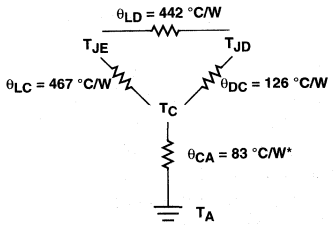


Figure 27. Energy Dissipated in the HCPL-3120 for Each IGBT Switching Cycle.



T_{JE} = LED junction temperature
T_{JD} = detector IC junction temperature
T_C = case temperature measured at the center of the package bottom
θ_{LC} = LED-to-case thermal resistance
θ_{LD} = LED-to-detector thermal resistance
θ_{DC} = detector-to-case thermal resistance
θ_{CA} = case-to-ambient thermal resistance
*θ_{CA} will depend on the board design and the placement of the part.

Figure 28. Thermal Model.

CMR with the LED On (CMR_H).

A high CMR LED drive circuit must keep the LED on during common mode transients. This is achieved by overdriving the LED current beyond the input threshold so that it is not pulled below the threshold during a transient. A minimum LED current of 10 mA provides adequate margin over the maximum I_{FLH} of 5 mA to achieve 15 kV/µs CMR.

CMR with the LED Off (CMR_L).

A high CMR LED drive circuit must keep the LED off ($V_F \leq V_{F(OFF)}$) during common mode transients. For example, during a $-dV_{cm}/dt$ transient in Figure 31, the current flowing through C_{LEDP} also flows through the R_{SAT} and V_{SAT} of the logic gate. As long as the low state voltage developed across the logic gate is less than $V_{F(OFF)}$, the LED will remain off and no common mode failure will occur.

The open collector drive circuit, shown in Figure 32, cannot keep the LED off during a +dVcm/dt transient, since all the current flowing through C_{LEDN} must be supplied by the LED, and it is not recommended for applications requiring ultra high CMR_L performance. Figure 33 is an alternative drive circuit which, like the recommended application circuit (Figure 25), does achieve ultra high CMR performance by shunting the LED in the off state.

Under Voltage Lockout Feature.

The HCPL-3120 contains an under voltage lockout (UVLO) feature that is designed to protect the IGBT under fault conditions which cause the HCPL-3120 supply voltage (equivalent to the fully-charged IGBT gate voltage) to drop below a level necessary to keep the IGBT in a low resistance state. When the HCPL-3120 output is in the high state and the supply voltage drops below the HCPL-3120 V_{UVLO-} threshold ($9.5 < V_{UVLO-} < 12.0$) the optocoupler output will go into the low state with a typical delay, UVLO Turn Off Delay, of 0.6 µs.

When the HCPL-3120 output is in the low state and the supply voltage rises above the HCPL-3120 V_{UVLO+} threshold ($11.0 < V_{UVLO+} < 13.5$) the optocoupler output will go into the high state (assumes LED is "ON") with a typical delay, UVLO Turn On Delay of 0.8 µs.

IPM Dead Time and Propagation Delay Specifications.

The HCPL-3120 includes a Propagation Delay Difference (PDD) specification intended to help designers minimize "dead time" in their power inverter designs. Dead time is the time period during which both the high and low side power transistors (Q1 and Q2 in Figure 25) are off. Any overlap in Q1 and Q2 conduction will result in large currents flowing through the power devices between the high and low voltage motor rails.

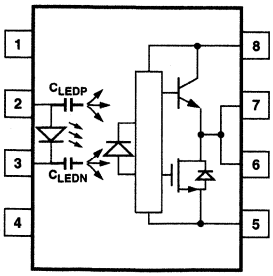


Figure 29. Optocoupler Input to Output Capacitance Model for Unshielded Optocouplers.

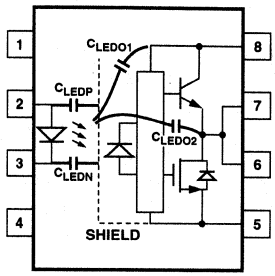


Figure 30. Optocoupler Input to Output Capacitance Model for Shielded Optocouplers.

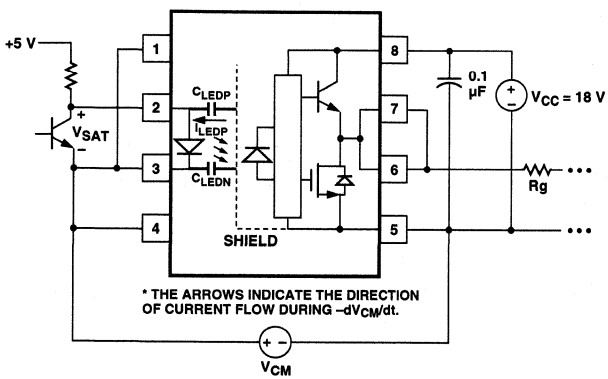


Figure 31. Equivalent Circuit for Figure 25 During Common Mode Transient.

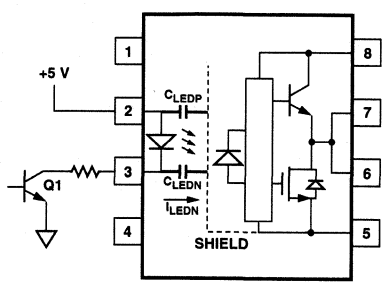


Figure 32. Not Recommended Open Collector Drive Circuit.

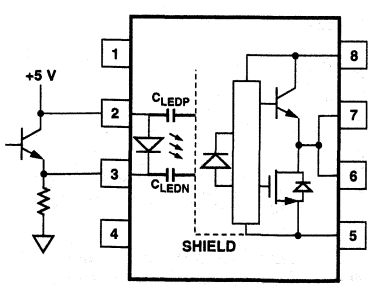


Figure 33. Recommended LED Drive Circuit for Ultra-High CMR.

To minimize dead time in a given design, the turn on of LED2 should be delayed (relative to the turn off of LED1) so that under worst-case conditions, transistor Q1 has just turned off when transistor Q2 turns on, as shown in Figure 34. The amount of delay necessary to achieve this conditions is equal to the maximum value of the propagation delay difference specification, PDD_{MAX}, which is specified to be 350 ns over the operating temperature range of -40°C to 100°C.

Delaying the LED signal by the maximum propagation delay difference ensures that the minimum dead time is zero, but it does not tell a designer what the maximum dead time will be. The maximum dead time is equivalent to the difference between the

maximum and minimum propagation delay difference specifications as shown in Figure 35. The maximum dead time for the HCPL-3120 is 700 ns (= 350 ns - (-350 ns)) over an operating temperature range of -40°C to 100°C.

Note that the propagation delays used to calculate PDD and dead time are taken at equal temperatures and test conditions since the optocouplers under consideration are typically mounted in close proximity to each other and are switching identical IGBTs.

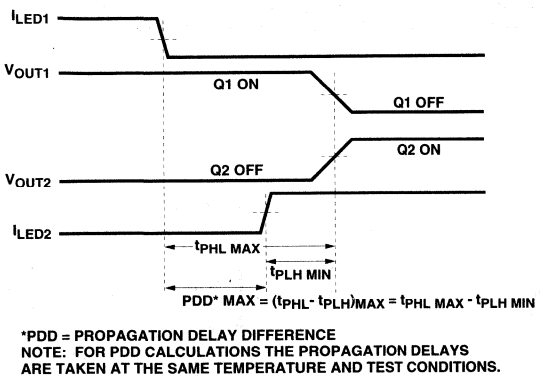


Figure 34. Minimum LED Skew for Zero Dead Time.

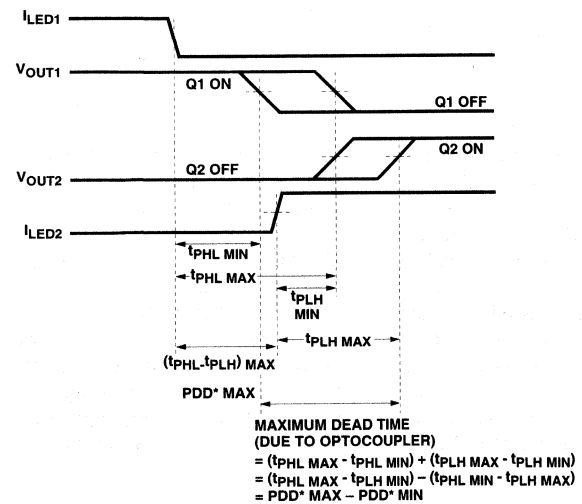


Figure 35. Waveforms for Dead Time.

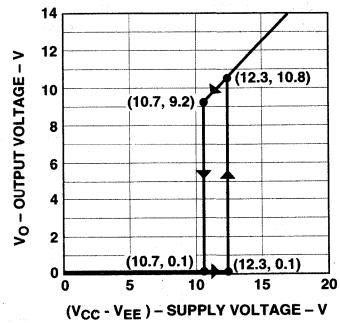


Figure 36. Under Voltage Lock Out.

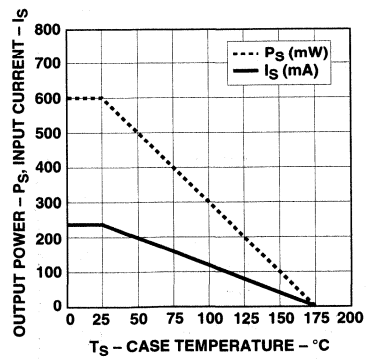


Figure 37. Thermal Derating Curve, Dependence of Safety Limiting Value with Case Temperature per VDE 0884.

0.5 Amp Output Current IGBT Gate Drive Optocoupler

Technical Data

HCPL-3150

Features

- **0.5 A Minimum Peak Output Current**
- **15 kV/μs Minimum Common Mode Rejection (CMR) at V_{CM} = 1500 V**
- **1.0 V Maximum Low Level Output Voltage (V_{OL}) Eliminates Need for Negative Gate Drive**
- **I_{CC} = 5 mA Maximum Supply Current**
- **Under Voltage Lock-Out Protection (UVLO) with Hysteresis**
- **Wide Operating V_{CC} Range:** 15 to 30 Volts
- **500 ns Maximum Switching Speeds**
- **Industrial Temperature Range:** -40°C to 100°C
- **Safety and Regulatory Approval:**
  UL Recognized
  2500 Vrms for 1 min. per UL1577
  VDE 0884 Approved with V_{IORM} = 630 Vpeak (Option 060 only)
  CSA Approved

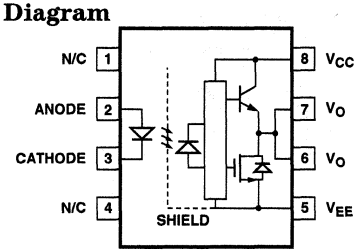
Applications

- **Isolated IGBT/MOSFET Gate Drive**
- **AC and Brushless DC Motor Drives**
- **Industrial Inverters**
- **Switch Mode Power Supplies (SMPS)**

Description

The HCPL-3150 consists of a GaAsP LED optically coupled to an integrated circuit with a power output stage. This optocoupler is ideally suited for driving power IGBTs and MOSFETs used in motor control inverter applications. The high operating voltage range of the output stage provides the drive voltages required by gate controlled devices. The voltage and current supplied by this optocoupler makes it ideally suited for directly driving IGBTs with ratings up to 1200 V/50 A. For IGBTs with higher ratings, the HCPL-3120 can be used to drive a discrete power stage which drives the IGBT gate.

Functional Diagram



Truth Table

LED	V_{CC} - V_{EE} "Positive Going" (i.e., Turn-On)	V_{CC} - V_{EE} "Negative-Going" (i.e., Turn-Off)	V_O
OFF	0 - 30 V	0 - 30 V	LOW
ON	0 - 11 V	0 - 9.5 V	LOW
ON	11 - 13.5 V	9.5 - 12 V	TRANSITION
ON	13.5 - 30 V	12 - 30 V	HIGH

A 0.1 μF bypass capacitor must be connected between pins 5 and 8.

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Ordering Information

Specify Part Number followed by Option Number (if desired)

Example

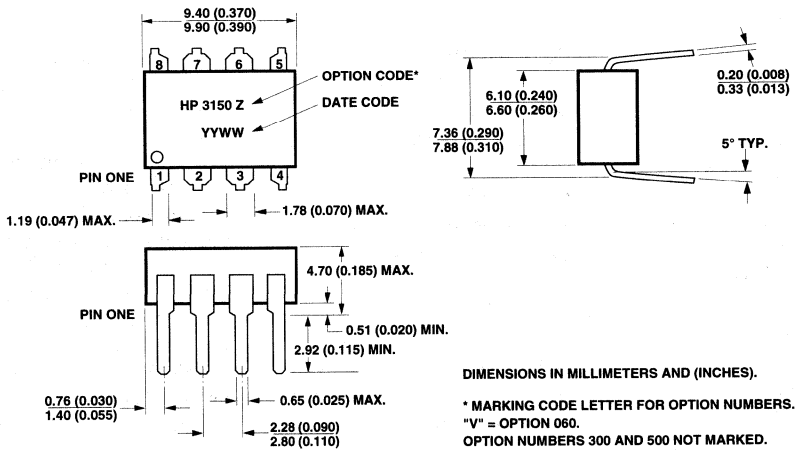
HCPL-3150#XXX

- No Option = Standard DIP package, 50 per tube.
- 060 = VDE 0884 V_{IORM} = 630 Vpeak Option, 50 per tube.
- 300 = Gull Wing Surface Mount Option, 50 per tube.
- 500 = Tape and Reel Packaging Option, 1000 per reel.

Option data sheets available. Contact Hewlett-Packard sales representative or authorized distributor.

Package Outline Drawings

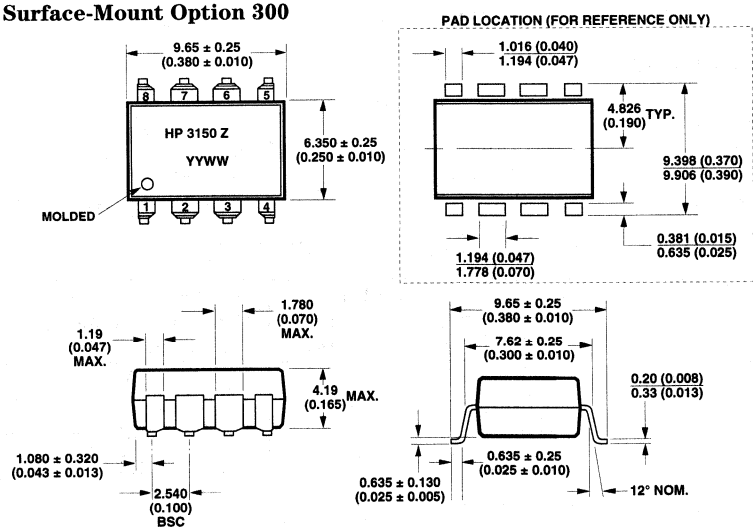
Standard DIP Package



DIMENSIONS IN MILLIMETERS AND (INCHES).

* MARKING CODE LETTER FOR OPTION NUMBERS.
"V" = OPTION 060.
OPTION NUMBERS 300 AND 500 NOT MARKED.

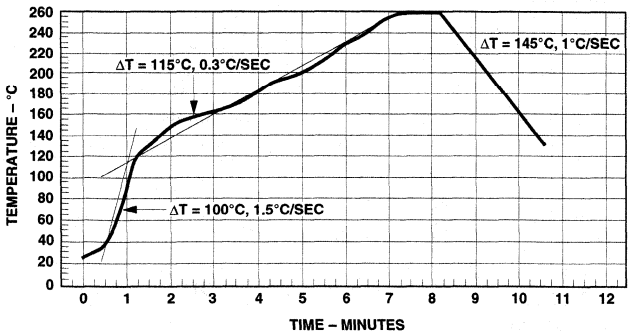
Gull-Wing Surface-Mount Option 300



DIMENSIONS IN MILLIMETERS (INCHES).
TOLERANCES (UNLESS OTHERWISE SPECIFIED): xx.xx = 0.01
xx.xxx = 0.005

LEAD COPLANARITY
MAXIMUM: 0.102 (0.004)

Reflow Temperature Profile



MAXIMUM SOLDER REFLOW THERMAL PROFILE
(NOTE: USE OF NON-CHLORINE ACTIVATED FLUXES IS RECOMMENDED.)

Regulatory Information

The HCPL-3150 has been approved by the following organizations:

UL

Recognized under UL 1577, Component Recognition Program, File E55361.

CSA

Approved under CSA Component Acceptance Notice #5, File CA 88324.

VDE (Option 060 only)

Approved under VDE 0884/06.92 with V_{IORM} = 630 Vpeak.

VDE 0884 Insulation Characteristics (Option 060 Only)

Description	Symbol	Characteristic	Unit
Installation classification per DIN VDE 0110/1.89, Table 1			
for rated mains voltage ≤ 300 Vrms		I-IV	
for rated mains voltage ≤ 600 Vrms		I-III	
Climatic Classification		55/100/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	630	Vpeak
Input to Output Test Voltage, Method b* V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial discharge < 5 pC	V_{PR}	1181	Vpeak
Input to Output Test Voltage, Method a* V_{IORM} x 1.5 = V_{PR}, Type and Sample Test, t_m = 60 sec, Partial discharge < 5 pC	V_{PR}	945	Vpeak
Highest Allowable Overvoltage* (Transient Overvoltage t_{ini} = 10 sec)	V_{IOTM}	6000	Vpeak
Safety-Limiting Values – Maximum Values Allowed in the Event of a Failure, Also See Figure 37, Thermal Derating Curve.			
Case Temperature	T_S	175	°C
Input Current	$I_{S, INPUT}$	230	mA
Output Power	$P_{S, OUTPUT}$	600	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	≥ 10^9	Ω

*Refer to the front of the optocoupler section of the current Catalog, under Product Safety Regulations section, (VDE 0884) for a detailed description of Method a and Method b partial discharge test profiles.

Note: Isolation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuits in application.

Insulation and Safety Related Specifications

Parameter	Symbol	Value	Units	Conditions
Minimum External Air Gap (External Clearance)	L(101)	7.1	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L(102)	7.4	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	mm	Through insulation distance conductor to conductor.
Tracking Resistance (Comparative Tracking Index)	CTI	200	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Option 300 - surface mount classification is Class A in accordance wtih CECC 00802.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	T_S	-55	125	°C	
Operating Temperature	T_A	-40	100	°C	
Average Input Current	$I_{F(AVG)}$		25	mA	1
Peak Transient Input Current (<1 µs pulse width, 300 pps)	$I_{F(TRAN)}$		1.0	A	
Reverse Input Voltage	V_R		5	Volts	
"High" Peak Output Current	$I_{OH(PEAK)}$		0.6	A	2
"Low" Peak Output Current	$I_{OL(PEAK)}$		0.6	A	2
Supply Voltage	$(V_{CC} - V_{EE})$	0	35	Volts	
Output Voltage	$V_{O(PEAK)}$	0	V_{CC}	Volts	
Output Power Dissipation	P_O		250	mW	3
Total Power Dissipation	P_T		295	mW	4
Lead Solder Temperature	260°C for 10 sec., 1.6 mm below seating plane				
Solder Reflow Temperature Profile	See Package Outline Drawings Section				

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage	$(V_{CC} - V_{EE})$	15	30	Volts
Input Current (ON)	$I_{F(ON)}$	7	16	mA
Input Voltage (OFF)	$V_{F(OFF)}$	-3.0	0.8	V
Operating Temperature	T_A	-40	100	°C

Electrical Specifications (DC)

Over recommended operating conditions (T_A = -40 to 100°C, $I_{F(ON)}$ = 7 to 16 mA, $V_{F(OFF)}$ = -3.0 to 0.8 V, V_{CC} = 15 to 30 V, V_{EE} = Ground) unless otherwise specified.

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
High Level Output Current	I_{OH}	0.1	0.4		A	V_O = (V_{CC} - 4 V)	2, 3, 17	5
		0.5				V_O = (V_{CC} - 15 V)		2
Low Level Output Current	I_{OL}	0.1	0.6		A	V_O = (V_{EE} + 2.5 V)	5, 6 18	5
		0.5				V_O = (V_{EE} + 15 V)		2
High Level Output Voltage	V_{OH}	(V_{CC} - 4)	(V_{CC} - 3)		V	I_O = -100 mA	1, 3 19	6, 7
Low Level Output Voltage	V_{OL}		0.4	1.0	V	I_O = 100 mA	4, 6 20	
High Level Supply Current	I_{CCH}		2.5	5.0	mA	Output Open, I_F = 7 to 16 mA	7, 8	
Low Level Supply Current	I_{CCL}		2.7	5.0	mA	Output Open, V_F = -3.0 to +0.8 V		
Threshold Input Current Low to High	I_{FLH}		2.2	5.0	mA	I_O = 0 mA, V_O > 5 V	9, 15, 21	
Threshold Input Voltage High to Low	V_{FHL}	0.8			V			
Input Forward Voltage	V_F	1.2	1.5	1.8	V	I_F = 10 mA	16	
Temperature Coefficient of Forward Voltage	$\Delta V_F/\Delta T_A$		-1.6		mV/°C	I_F = 10 mA		
Input Reverse Breakdown Voltage	BV_R	5			V	I_R = 10 µA		
Input Capacitance	C_{IN}		60		pF	f = 1 MHz, V_F = 0 V		
UVLO Threshold	V_{UVLO+}	11.0	12.3	13.5	V	V_O > 5 V, I_F = 10 mA	22, 36	
	V_{UVLO-}	9.5	10.7	12.0				
UVLO Hysteresis	$UVLO_{HYS}$		1.6		V			

*All typical values at T_A = 25°C and V_{CC} - V_{EE} = 30 V, unless otherwise noted.

Switching Specifications (AC)

Over recommended operating conditions (T_A = -40 to 100°C, $I_{F(ON)}$ = 7 to 16 mA, $V_{F(OFF)}$ = -3.0 to 0.8 V, V_{CC} = 15 to 30 V, V_{EE} = Ground) unless otherwise specified.

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to High Output Level	t_{PLH}	0.10	0.30	0.50	µs	Rg = 47 Ω, Cg = 3 nF, f = 10 kHz, Duty Cycle = 50%	10, 11, 12, 13 14, 23	14
Propagation Delay Time to Low Output Level	t_{PHL}	0.10	0.27	0.50	µs			
Pulse Width Distortion	PWD			0.3	µs			15
Propagation Delay Difference Between Any Two Parts	PDD (t_{PHL} - t_{PLH})	-0.35		0.35	µs		34,35	10
Rise Time	t_r		0.1		µs		23	
Fall Time	t_f		0.1		µs			
UVLO Turn On Delay	$t_{UVLO\ ON}$		0.8		µs	V_O > 5 V, I_F = 10 mA	22	
UVLO Turn Off Delay	$t_{UVLO\ OFF}$		0.6		µs	V_O < 5 V, I_F = 10 mA		
Output High Level Common Mode Transient Immunity	$\|CM_H\|$	15	30		kV/µs	T_A = 25°C, I_F = 10 to 16 mA, V_{CM} = 1500 V, V_{CC} = 30 V	24	11, 12
Output Low Level Common Mode Transient Immunity	$\|CM_L\|$	15	30		kV/µs	T_A = 25°C, V_{CM} = 1500 V, V_F = 0 V, V_{CC} = 30 V		11, 13

Package Characteristics

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage**	V_{ISO}	2500			Vrms	RH < 50%, t = 1 min., T_A = 25°C		8, 9
Resistance (Input - Output)	R_{I-O}		10^{12}		Ω	V_{I-O} = 500 V_{DC}		9
Capacitance (Input - Output)	C_{I-O}		0.6		pF	f = 1 MHz		
LED-to-Case Thermal Resistance	θ_{LC}		391		°C/W	Thermocouple located at center underside of package	28	
LED-to-Detector Thermal Resistance	θ_{LD}		439		°C/W			
Detector-to-Case Thermal Resistance	θ_{DC}		119		°C/W			

*All typical values at T_A = 25°C and V_{CC} - V_{EE} = 30 V, unless otherwise noted.

**The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to your equipment level safety specification or HP Application Note 1074 entitled "Optocoupler Input-Output Endurance Voltage."

Notes:

1. Derate linearly above 70°C free-air temperature at a rate of 0.3 mA/°C.
2. Maximum pulse width = 10 µs, maximum duty cycle = 0.2%. This value is intended to allow for component tolerances for designs with I_O peak minimum = 0.5 A. See Applications section for additional details on limiting I_{OH} peak.
3. Derate linearly above 70°C free-air temperature at a rate of 4.8 mW/°C.
4. Derate linearly above 70°C free-air temperature at a rate of 5.4 mW/°C. The maximum LED junction temperature should not exceed 125°C.
5. Maximum pulse width = 50 µs, maximum duty cycle = 0.5%.
6. In this test V_{OH} is measured with a dc load current. When driving capacitive loads V_{OH} will approach V_{CC} as I_{OH} approaches zero amps.
7. Maximum pulse width = 1 ms, maximum duty cycle = 20%.
8. In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 3000 Vrms for 1 second (leakage detection current limit, $I_{I-O} \leq 5$ µA). This test is performed before the 100% production test for partial discharge (method b) shown in the VDE 0884 Insulation Characteristics Table, if applicable.
9. Device considered a two-terminal device: pins 1, 2, 3, and 4 shorted together and pins 5, 6, 7, and 8 shorted together.
10. The difference between t_{PHL} and t_{PLH} between any two HCPL-3150 parts under the same test condition.
11. Pins 1 and 4 need to be connected to LED common.
12. Common mode transient immunity in the high state is the maximum tolerable $|dV_{CM}/dt|$ of the common mode pulse, V_{CM}, to assure that the output will remain in the high state (i.e., $V_O > 15.0$ V).
13. Common mode transient immunity in a low state is the maximum tolerable $|dV_{CM}/dt|$ of the common mode pulse, V_{CM}, to assure that the output will remain in a low state (i.e., $V_O < 1.0$ V).
14. This load condition approximates the gate load of a 1200 V/25 A IGBT.
15. Pulse Width Distortion (PWD) is defined as $|t_{PHL}-t_{PLH}|$ for any given device.

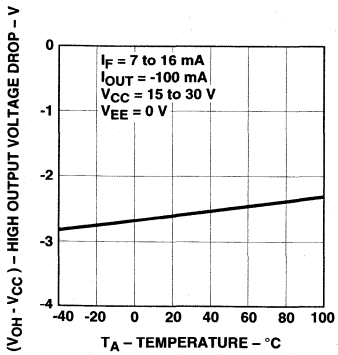


Figure 1. V_{OH} vs. Temperature.

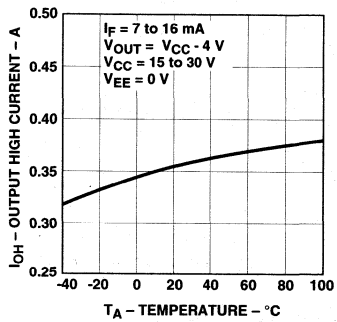


Figure 2. I_{OH} vs. Temperature.

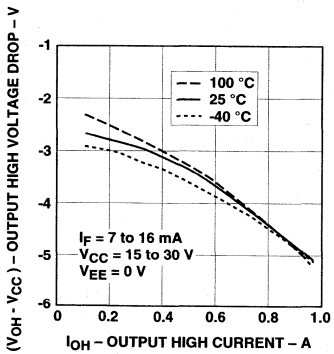


Figure 3. V_{OH} vs. I_{OH}.

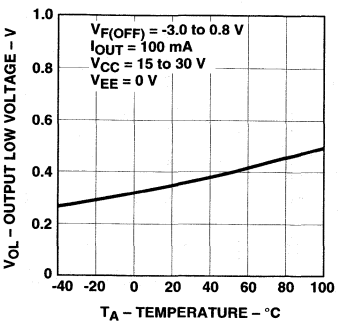


Figure 4. V_{OL} vs. Temperature.

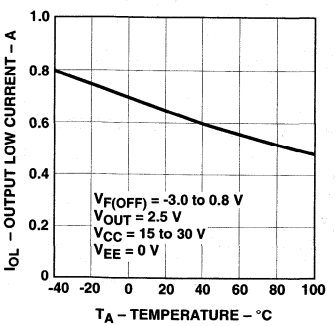


Figure 5. I_{OL} vs. Temperature.

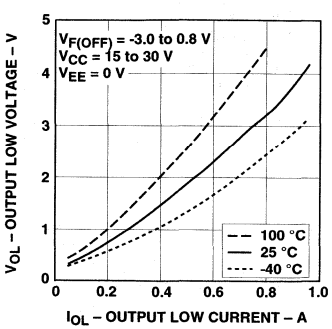


Figure 6. V_{OL} vs. I_{OL}.

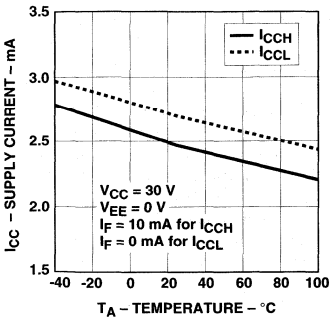


Figure 7. I_{CC} vs. Temperature.

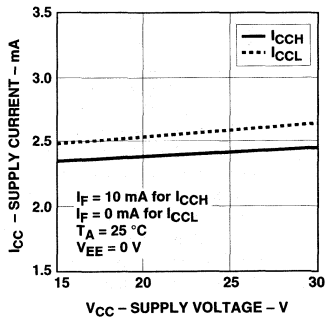


Figure 8. I_{CC} vs. V_{CC}.

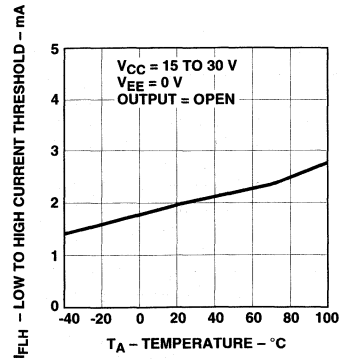


Figure 9. I_{FLH} vs. Temperature.

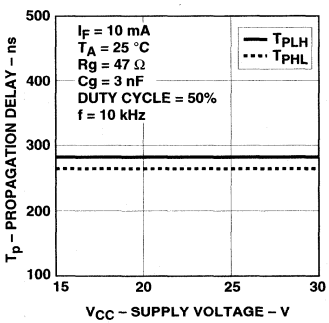


Figure 10. Propagation Delay vs. V_{CC}.

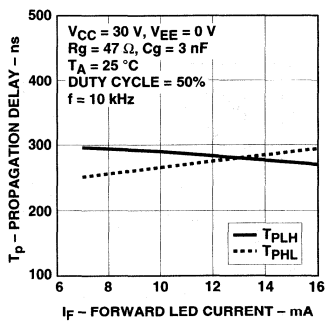


Figure 11. Propagation Delay vs. I_F.

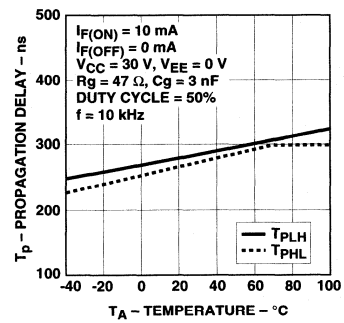


Figure 12. Propagation Delay vs. Temperature.

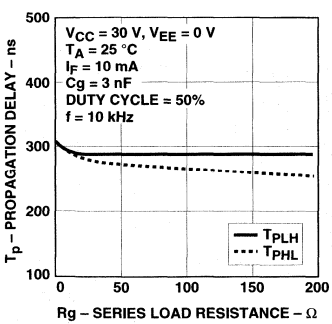


Figure 13. Propagation Delay vs. Rg.

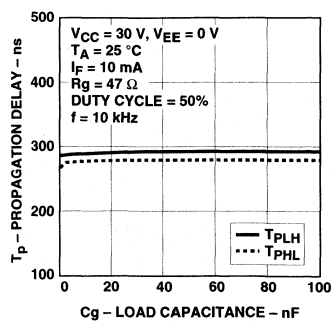


Figure 14. Propagation Delay vs. Cg.

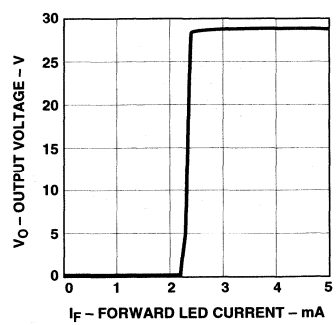


Figure 15. Transfer Characteristics.

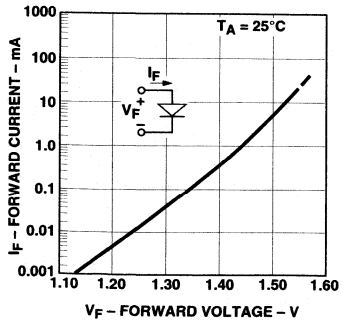


Figure 16. Input Current vs. Forward Voltage.

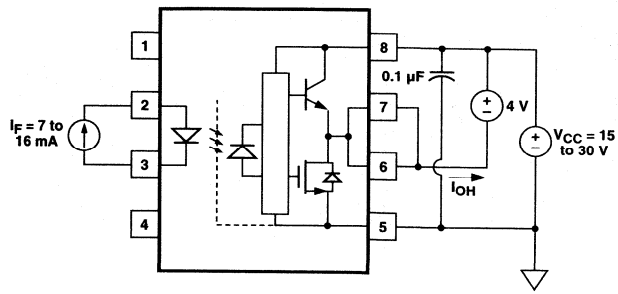


Figure 17. I_{OH} Test Circuit.

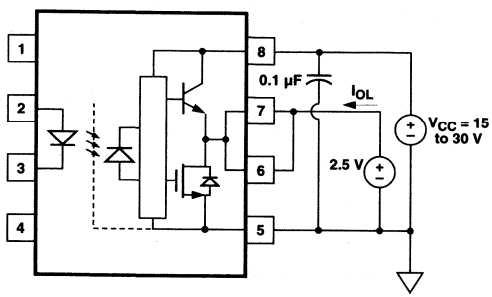


Figure 18. I_{OL} Test Circuit.

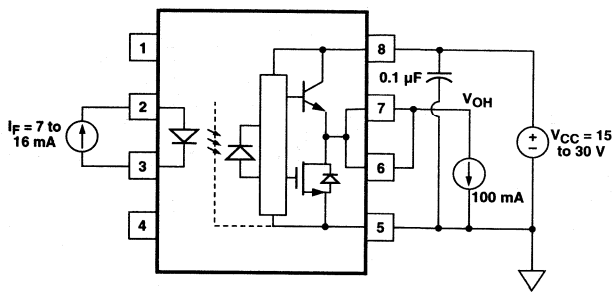


Figure 19. V_{OH} Test Circuit.

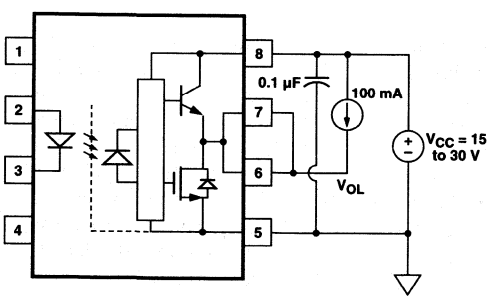


Figure 20. V_{OL} Test Circuit.

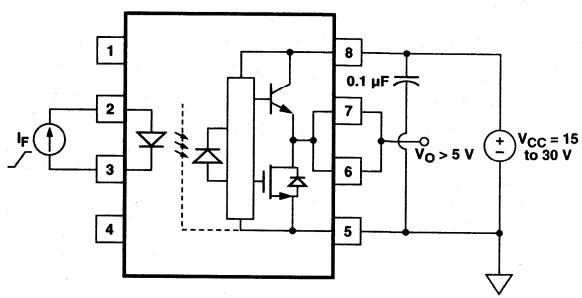


Figure 21. I_{FLH} Test Circuit.

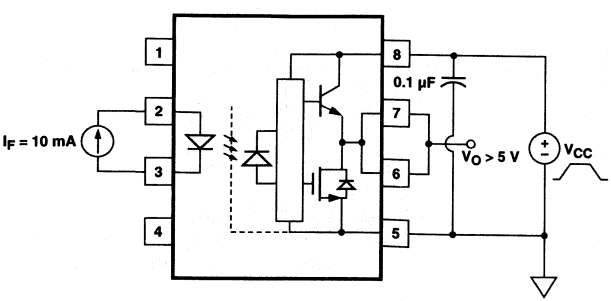


Figure 22. UVLO Test Circuit.

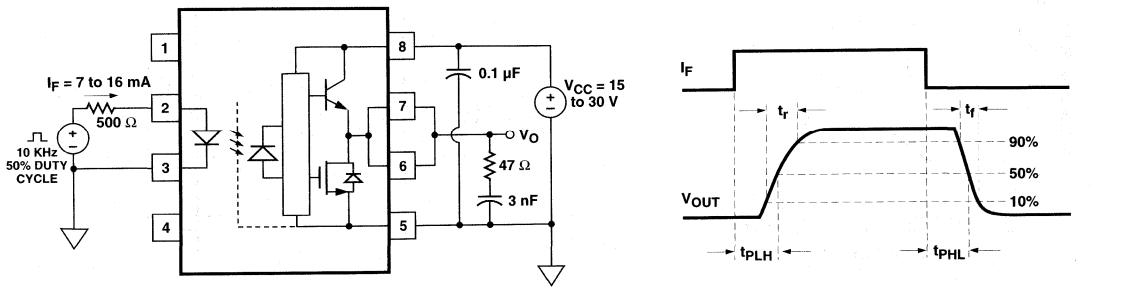


Figure 23. t_{PLH}, t_{PHL}, t_r, and t_f Test Circuit and Waveforms.

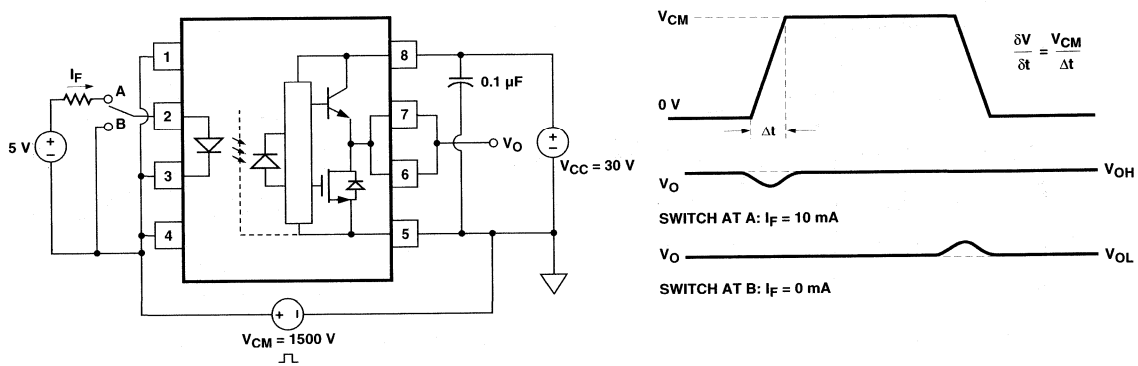


Figure 24. CMR Test Circuit and Waveforms.

Applications Information

Eliminating Negative IGBT Gate Drive

To keep the IGBT firmly off, the HCPL-3150 has a very low maximum V_{OL} specification of 1.0 V. The HCPL-3150 realizes this very low V_{OL} by using a DMOS transistor with 4 Ω (typical) on resistance in its pull down circuit. When the HCPL-3150 is in the low state, the IGBT gate is shorted to the emitter by Rg + 4 Ω. Minimizing Rg and the lead inductance from the HCPL-3150 to the IGBT gate and emitter (possibly by mounting the HCPL-3150 on a small PC board directly above the IGBT) can eliminate the need for negative IGBT gate drive in many applications as shown in Figure 25. Care should be taken with such a PC board design to avoid routing the IGBT collector or emitter traces close to the HCPL-3150 input as this can result in unwanted coupling of transient signals into the HCPL-3150 and degrade performance. (If the IGBT drain must be routed near the HCPL-3150 input, then the LED should be reverse-biased when in the off state, to prevent the transient signals coupled from the IGBT drain from turning on the HCPL-3150.)

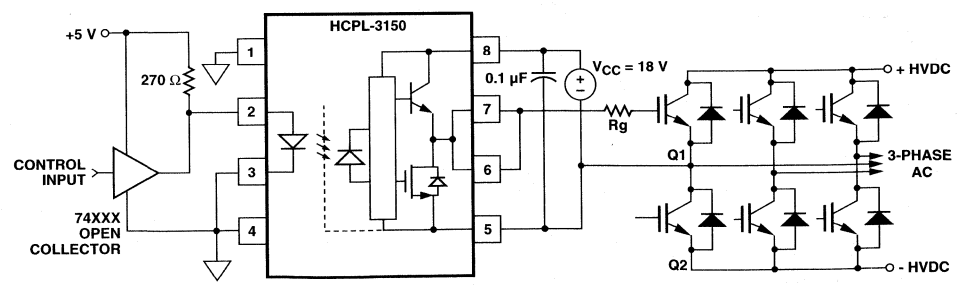


Figure 25. Recommended LED Drive and Application Circuit.

Selecting the Gate Resistor (Rg) to Minimize IGBT Switching Losses.

Step 1: Calculate Rg Minimum From the I_{OL} Peak Specification. The IGBT and Rg in Figure 26 can be analyzed as a simple RC circuit with a voltage supplied by the HCPL-3150.

$$Rg \geq \frac{(V_{CC} - V_{EE} - V_{OL})}{I_{OLPEAK}}$$

$$= \frac{(V_{CC} - V_{EE} - 1.7\ V)}{I_{OLPEAK}}$$

$$= \frac{(15\ V + 5\ V - 1.7\ V)}{0.6\ A}$$

$$= 30.5\ \Omega$$

The V_{OL} value of 2 V in the previous equation is a conservative value of V_{OL} at the peak current of 0.6 A (see Figure 6). At lower Rg values the voltage supplied by the HCPL-3150 is not an ideal voltage step. This results in lower peak currents (more margin) than predicted by this analysis. When negative gate drive is not used V_{EE} in the previous equation is equal to zero volts.

Step 2: Check the HCPL-3150 Power Dissipation and Increase Rg if Necessary. The HCPL-3150 total power dissipation (P_T) is equal to the sum of the emitter power (P_E) and the output power (P_O):

$$P_T = P_E + P_O$$

$$P_E = I_F \cdot V_F \cdot Duty\ Cycle$$

$$P_O = P_{O(BIAS)} + P_{O\ (SWITCHING)}$$

$$= I_{CC} \cdot (V_{CC} - V_{EE}) + E_{SW}(R_G, Q_G) \cdot f$$

For the circuit in Figure 26 with I_F (worst case) = 16 mA, Rg = 30.5 Ω, Max Duty Cycle = 80%, Qg = 500 nC, f = 20 kHz and T_A max = 90°C:

$$P_E = 16\ mA \cdot 1.8\ V \cdot 0.8 = 23\ mW$$

$$P_O = 4.25\ mA \cdot 20\ V + 4.0\ \mu J \cdot 20\ kHz$$

$$= 85\ mW + 80\ mW$$

$$= 165\ mW$$

$$> 154\ mW\ (P_{O(MAX)}\ @\ 90°C$$

$$= 250\ mW - 20C \cdot 4.8\ mW/C)$$

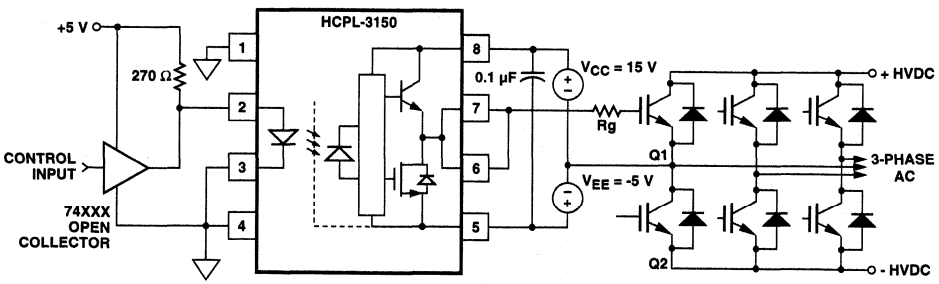


Figure 26. HCPL-3150 Typical Application Circuit with Negative IGBT Gate Drive.

P_E Parameter	Description
I_F	LED Current
V_F	LED On Voltage
Duty Cycle	Maximum LED Duty Cycle

P_O Parameter	Description
I_{CC}	Supply Current
V_{CC}	Positive Supply Voltage
V_{EE}	Negative Supply Voltage
E_{SW}(Rg,Qg)	Energy Dissipated in the HCPL-3150 for each IGBT Switching Cycle (See Figure 27)
f	Switching Frequency

The value of 4.25 mA for I_{CC} in the previous equation was obtained by derating the I_{CC} max of 5 mA (which occurs at -40°C) to I_{CC} max at 90°C (see Figure 7).

Since P_O for this case is greater than $P_{O(MAX)}$, Rg must be increased to reduce the HCPL-3150 power dissipation.

$$P_{O(SWITCHING\ MAX)} = P_{O(MAX)} - P_{O(BIAS)} = 154\ mW - 85\ mW = 69\ mW$$

$$E_{SW(MAX)} = \frac{P_{O(SWITCHINGMAX)}}{f} = \frac{69\ mW}{20\ kHz} = 3.45\ \mu J$$

For Qg = 500 nC, from Figure 27, a value of E_{SW} = 3.45 µJ gives a Rg = 41 Ω.

Thermal Model

The steady state thermal model for the HCPL-3150 is shown in Figure 28. The thermal resistance values given in this model can be used to calculate the temperatures at each node for a given operating condition. As shown by the model, all heat generated flows through θ_{CA} which raises the case temperature T_C accordingly. The value of θ_{CA} depends on the conditions of the board design and is, therefore, determined by the designer. The value of θ_{CA} = 83°C/W was obtained from thermal measurements using a 2.5 x 2.5 inch PC board, with small traces (no ground plane), a single HCPL-3150 soldered into the center of the board and still air. The absolute maximum power dissipation derating specifications assume a θ_{CA}value of 83°C/W.

From the thermal mode in Figure 28 the LED and detector IC junction temperatures can be expressed as:

$$T_{JE} = P_E \cdot (\theta_{LC} || (\theta_{LD} + \theta_{DC}) + \theta_{CA}) + P_D \cdot \left(\frac{\theta_{LC} \cdot \theta_{DC}}{\theta_{LC} + \theta_{DC} + \theta_{LD}} + \theta_{CA} \right) + T_A$$

$$T_{JD} = P_E \left(\frac{\theta_{LC} \cdot \theta_{DC}}{\theta_{LC} + \theta_{DC} + \theta_{LD}} + \theta_{CA} \right) + P_D \cdot (\theta_{DC} || (\theta_{LD} + \theta_{LC}) + \theta_{CA}) + T_A$$

Inserting the values for θ_{LC} and θ_{DC} shown in Figure 28 gives:

$$T_{JE} = P_E \cdot (230°C/W + \theta_{CA}) + P_D \cdot (49°C/W + \theta_{CA}) + T_A$$
$$T_{JD} = P_E \cdot (49°C/W + \theta_{CA}) + P_D \cdot (104°C/W + \theta_{CA}) + T_A$$

For example, given P_E = 45 mW, P_O = 250 mW, T_A = 70°C and θ_{CA} = 83°C/W:

$$T_{JE} = P_E \cdot 313°C/W + P_D \cdot 132°C/W + T_A = 45\ mW \cdot 313°C/W + 250\ mW \cdot 132°C/W + 70°C = 117°C$$

$$T_{JD} = P_E \cdot 132°C/W + P_D \cdot 187°C/W + T_A = 45\ mW \cdot 132C/W + 250\ mW \cdot 187°C/W + 70°C = 123°C$$

T_{JE} and T_{JD} should be limited to 125°C based on the board layout and part placement (θ_{CA}) specific to the application.

LED Drive Circuit Considerations for Ultra High CMR Performance

Without a detector shield, the dominant cause of optocoupler CMR failure is capacitive coupling from the input side of the optocoupler, through the package, to the detector IC as shown in Figure 29. The HCPL-3150 improves CMR performance by using a detector IC with an optically transparent Faraday shield, which diverts the capacitively coupled current away from the sensitive IC circuitry. However, this shield does not eliminate the capacitive coupling between the LED and optocoupler pins 5-8 as shown in Figure 30. This capacitive coupling causes perturbations in the LED current during common mode transients and becomes the major source of CMR failures for a shielded optocoupler. The main design objective of a high CMR LED drive circuit becomes keeping the LED in the proper state (on or off) during common mode transients. For example, the recommended application circuit (Figure 25), can achieve 15 kV/µs CMR while minimizing component complexity.

Techniques to keep the LED in the proper state are discussed in the next two sections.

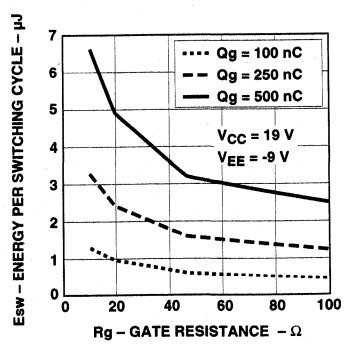
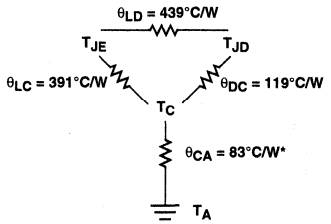


Figure 27. Energy Dissipated in the HCPL-3150 for Each IGBT Switching Cycle.



T_{JE} = LED junction temperature
T_{JD} = detector IC junction temperature
T_C = case temperature measured at the center of the package bottom
θ_{LC} = LED-to-case thermal resistance
θ_{LD} = LED-to-detector thermal resistance
θ_{DC} = detector-to-case thermal resistance
θ_{CA} = case-to-ambient thermal resistance
*θ_{CA} will depend on the board design and the placement of the part.

Figure 28. Thermal Model.

CMR with the LED On (CMR_H)

A high CMR LED drive circuit must keep the LED on during common mode transients. This is achieved by overdriving the LED current beyond the input threshold so that it is not pulled below the threshold during a transient. A minimum LED current of 10 mA provides adequate margin over the maximum I_{FLH} of 5 mA to achieve 15 kV/μs CMR.

CMR with the LED Off (CMR_L)

A high CMR LED drive circuit must keep the LED off ($V_F \leq V_{F(OFF)}$) during common mode transients. For example, during a $-dV_{CM}/dt$ transient in Figure 31, the current flowing through C_{LEDP} also flows through the R_{SAT} and V_{SAT} of the logic gate. As long as the low state voltage developed across the logic gate is less than $V_{F(OFF)}$, the LED will remain off and no common mode failure will occur.

The open collector drive circuit, shown in Figure 32, cannot keep the LED off during a $+dV_{CM}/dt$ transient, since all the current flowing through C_{LEDN} must be supplied by the LED, and it is not recommended for applications requiring ultra high CMR_L performance. Figure 33 is an alternative drive circuit which, like the recommended application circuit (Figure 25), does achieve ultra high CMR performance by shunting the LED in the off state.

Under Voltage Lockout Feature

The HCPL-3150 contains an under voltage lockout (UVLO) feature that is designed to protect the IGBT under fault conditions which cause the HCPL-3150 supply voltage (equivalent to the fully-charged IGBT gate voltage) to drop below a level necessary to keep the IGBT in a low resistance state. When the HCPL-3150 output is in the high state and the supply voltage drops below the HCPL-3150 V_{UVLO-} threshold ($9.5 < V_{UVLO-} < 12.0$), the optocoupler output will go into the low state with a typical delay, UVLO Turn Off Delay, of 0.6 μs. When the HCPL-3150 output is in the low state and the supply voltage rises above the HCPL-3150 V_{UVLO+} threshold ($11.0 < V_{UVLO+} < 13.5$), the optocoupler will go into the high state (assuming LED is "ON") with a typical delay, UVLO TURN On Delay, of 0.8 μs.

IPM Dead Time and Propagation Delay Specifications

The HCPL-3150 includes a Propagation Delay Difference (PDD) specification intended to help designers minimize "dead time" in their power inverter designs. Dead time is the time period during which both the high and low side power transistors (Q1 and Q2 in Figure 25) are off. Any overlap in Q1 and Q2 conduction will result in large currents flowing through the power devices from the high- to the low-voltage motor rails.

To minimize dead time in a given design, the turn on of LED2 should be delayed (relative to the

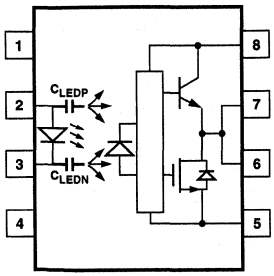


Figure 29. Optocoupler Input to Output Capacitance Model for Unshielded Optocouplers.

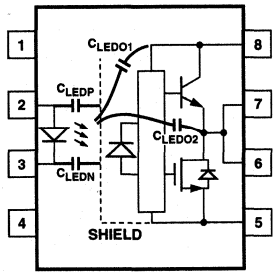


Figure 30. Optocoupler Input to Output Capacitance Model for Shielded Optocouplers.

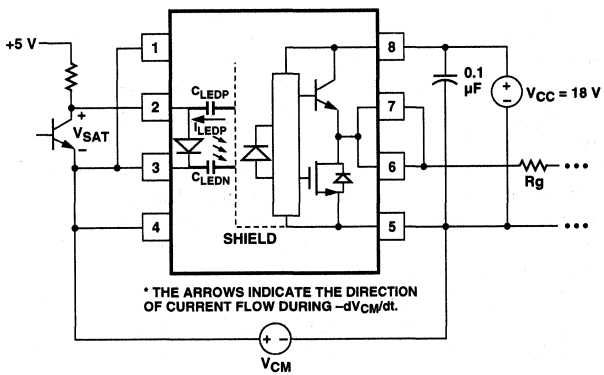


Figure 31. Equivalent Circuit for Figure 25 During Common Mode Transient.

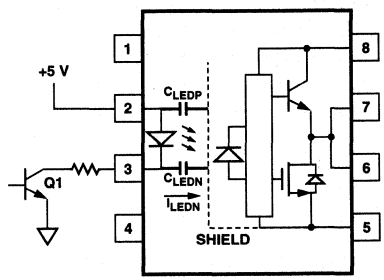


Figure 32. Not Recommended Open Collector Drive Circuit.

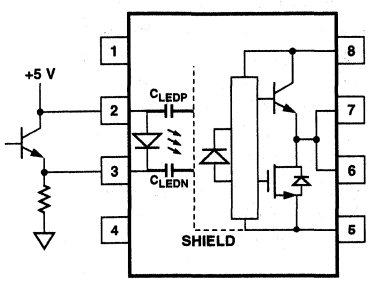


Figure 33. Recommended LED Drive Circuit for Ultra-High CMR.

turn off of LED1) so that under worst-case conditions, transistor Q1 has just turned off when transistor Q2 turns on, as shown in Figure 34. The amount of delay necessary to achieve this conditions is equal to the maximum value of the propagation delay difference specification, PDD_{MAX}, which is specified to be 350 ns over the operating temperature range of -40°C to 100°C.

Delaying the LED signal by the maximum propagation delay difference ensures that the minimum dead time is zero, but it does not tell a designer what the maximum dead time will be. The maximum dead time is equivalent to the difference between the maximum and minimum propagation delay difference specifications as shown in Figure 35. The maximum dead time for the HCPL-3150 is 700 ns (= 350 ns - (-350 ns)) over an operating temperature range of -40°C to 100°C.

Note that the propagation delays used to calculate PDD and dead time are taken at equal temperatures and test conditions since the optocouplers under consideration are typically mounted in close proximity to each other and are switching identical IGBTs.

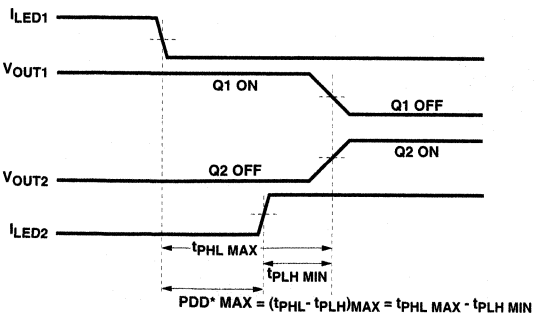


Figure 34. Minimum LED Skew for Zero Dead Time.

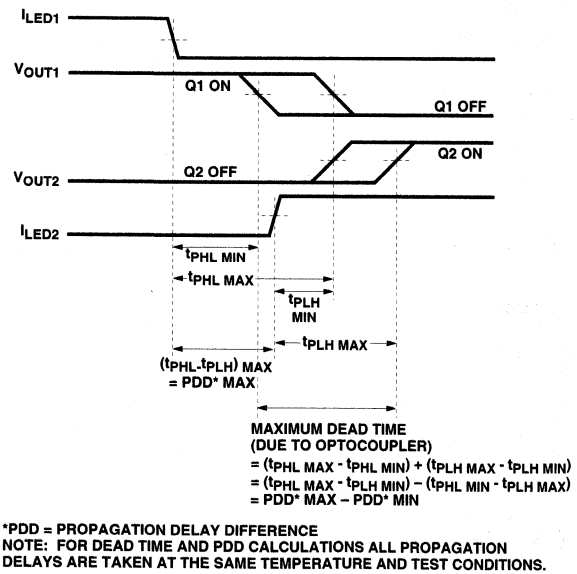


Figure 35. Waveforms for Dead Time.

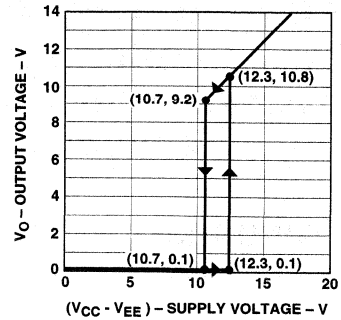


Figure 36.Under Voltage Lock Out.

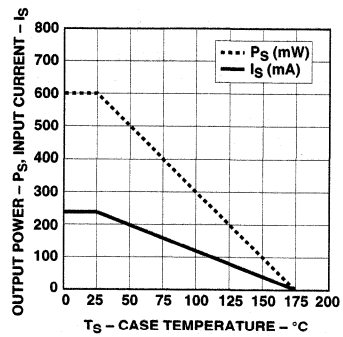


Figure 37. Thermal Derating Curve, Dependence of Safety Limiting Value with Case Temperature per VDE 0884.

HEWLETT® PACKARD

2.0 Amp IGBT Gate Drive Optocoupler with Integrated Over-current Protection and Fault Feedback

Preliminary Technical Data

HCPL-3160

Features

- **Integrated IGBT Desaturation Protection**
- **Integrated Optically Isolated IGBT Fault Status Feedback**
- **CMOS Compatible INPUT and FAULT Status Indicator**

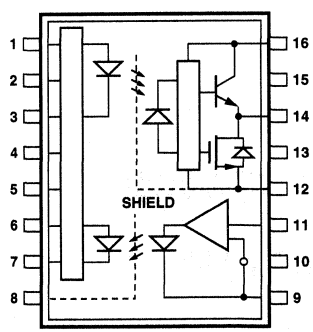
Actual Size

- **Small Printed Circuit Board Footprint (SO-16 Package)**
- **-40°C to 100°C Operating Temperature**
- **Suitable for Integration in Power Modules**
- **2.0 A Minimum Peak Output Current**
- **15 kV/μs Minimum Common Mode Rejection (CMR) at V_{CM} = 1500 V**
- **V_{IORM} = 890 V_{PEAK}**

Description

The HCPL-3160 provides low cost, area efficient IGBT gate drive that includes desaturation or over current detection and local IGBT shutdown. The integrated fault feedback optocoupler notifies the controller when the IGBT is shutdown due to a desaturation or over current condition.

Functional Diagram



This data sheet represents the latest information at the time of publication of this catalog. All specifications subject to change. Samples available Fall 1996.

Fault Circuit Operation

A typical desaturation protected IGBT gate drive application circuit using the HCPL-3160 is shown in Figure 1. The IGBT collector to emitter voltage is monitored through D_{DESAT}. When the IGPT is *on* and V_{DESAT} exceeds the internal reference voltage of 7 V the IGBT gate is "softly" turned-off by M2 to prevent large di/dt generation. The LED2 driver is also activated, which drives the internal feedback LED2 and notifies the controller of the IGBT fault by bringing the FAULT output low. The FAULT output remains low until RESET is brought low. (Note if a separate reset line is not required, RESET can be connected to Vin on the circuit board. In this case, the FAULT output will be reset on the next PWM cycle that Vin goes low.) The FAULT output is an open collector which allows the FAULT outputs from all the HCPL-3160s in a drive to be connected together in a "wired OR" forming a single fault bus for interfacing with the micro-controller. The ENABLE input can also be connected to this fault bus. With this connection all IGBTs in a drive are shutdown without micro-controller intervention once a fault is detected on a single IGBT.

C_{BLANK} disables the fault detection circuitry for a time period sufficient for normal IGBT turn-on. C_{BLANK} is held low by Q1 when the IGBT is off.

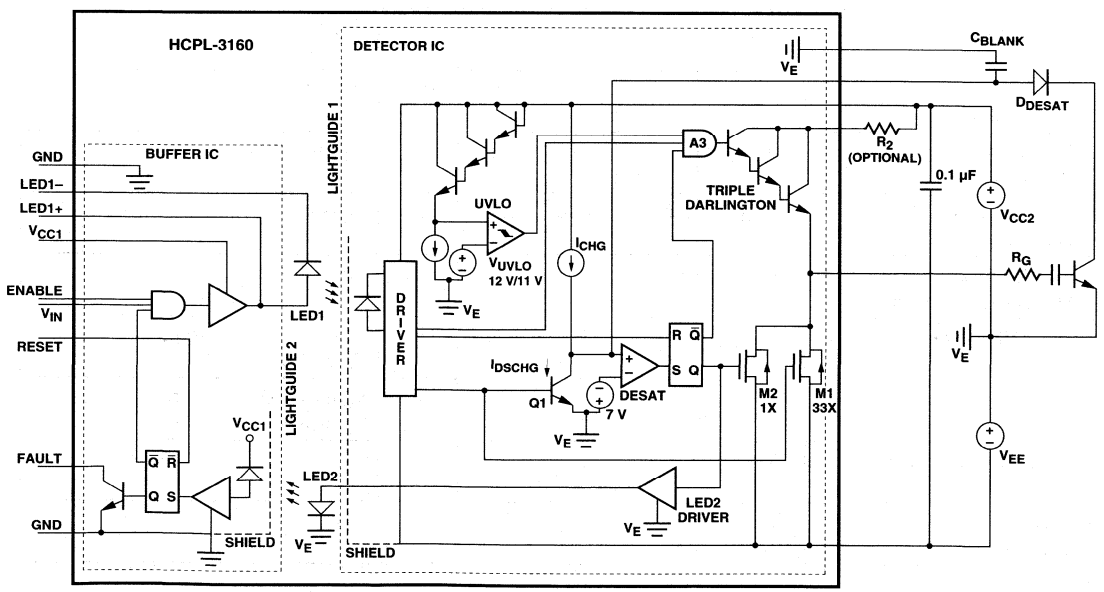


Figure 1. IGBT Gate Drive with Desaturation Protection and Fault Feedback.

Preliminary Electrical Specifications (DC)

Over recommended operating conditions (T_A = -40 to 100°C) unless otherwise specified.

Parameter	Symbol	Min.	Typ.*	Max.	Units	Conditions
Logic Low Voltages	INPUT RESET FAULT ENABLE			0.8	V	
Logic High Voltages	INPUT RESET FAULT ENABLE	2.0			V	
High Level Output Current	I_{OH}	0.5	1.5		A	$V_O = V_{CC2}$ -4 V
		2.0			A	$V_O = V_{CC2}$ 15 V
Low Level Output Current	I_{OL}	0.5	2.0		A	$V_O = V_{EE}$ + 2.5 V
		2.0			A	$V_O = V_{EE}$ + 15
High Level Output Voltage	V_{OH}	V_{CC2}-4	V_{CC2}-3		V	I_O = -100 mA
Low Level Output Voltage	V_{OL}		0.1	0.5	V	I_O = 100 mA
High Level Supply Current	I_{CC1H}			12	mA	Vin = 5 V, V_{CC1} = 5 V
High Level Supply Current	I_{CC1L}			2	mA	Vin = 0 V, V_{CC1} = 5 V
High Level Supply Current	I_{CC2H}		3	7	mA	output open
Low Level Supply Current	I_{CC2L}		3	7	mA	output open
Blanking Capacitor Charging Current	I_{CHG}	0.2	0.32	0.45	mA	Vdesat = 0 V
Blanking Capacitor Discharge Current	I_{DSCHG}		60		mA	Vdesat = 7 V
UVLO Threshold	V_{UVLO+}		13.0 (10.9)	13.4 (12.5)	V	V_{CC2} = 1.0 ms ramp, V_O > 5 V
	V_{UVLO-}	11.2 (8.7)	11.6 (9.5)		V	V_{CC2} = 1.0 ms ramp, V_O > 5 V
UVLO Hysteresis	V_{UVLO+} - V_{UVLO-}		1.4		V	
Desaturation Trip Voltage	V_{DESAT}	6.0	7.0	8.0	V	

*All typical values at T_A = 25°C and V_{CC2} - V_{EE} = 30 V, unless otherwise noted.

1) V_{UVLO+} and V_{UVLO-} are specified as the V_{CC2} at which V_O exceeds 5 V. The approximate output voltage just prior/after the UVLO transition is given in parenthesis.

Preliminary Switching Specifications (AC)

Over recommended operating conditions (T_A = -40 to 100°C) unless otherwise specified.

Parameter	Symbol	Min.	Typ.*	Max.	Units	Conditions
Propagation Delay Time to High Output Level	t_{PLH}	0.10	0.30	0.50	µs	Rg = 10 Ω, Cg = 10 nF, f = 10 kHz, Duty Cycle = 50%
Propagation Delay Time to Low Output Level	t_{PHL}	0.10		0.50	µs	
Pulse Width Distortion	pwd	-0.1		0.1	µs	
Propagation Delay Difference Between Any Two Parts	t_{PHL} - t_{PLH}	-0.4		0.4	µs	
Rise Time	t_r		0.1		µs	
Fall Time	t_f		0.1		µs	
Propagation Delay Time from Desat to Low Level Output	$t_{P(DS)}$			1.5	µs	Rg = 10 Ω, CG = 10 nF
Propagation Delay Time from Desat to Low Level FAULT Signal	$t_{PF(DS)}$			10	µs	RG = 10 Ω, CG = 10 nF
Minimum FAULT Signal Pulse Width	Δt_{FAULT}		2.0		µs	
UVLO Turn Off Delay	$t_{UVLO\ OFF}$		0.6		µs	
Output High Level Common Mode Transient Immunity	$\|CM_H\|$	15	30		kV/µs	T_A = 25°C, INPUT = 5 V, V_{CM} = 1500 V, V_{CC} = 30 V
Output Low Level Common Mode Transient Immunity	$\|CM_L\|$	15	30		kV/µs	T_A = 25°C, V_{CM} = 1500 V, INPUT = 0 V, V_{CC2} = 30 V

*All typical values at T_A = 25°C and V_{CC2} - V_{EE} = 30 V, unless otherwise noted.

HEWLETT® PACKARD

High CMR Isolation Amplifiers

Technical Data

HCPL-7800
HCPL-7800A
HCPL-7800B

Features

- **15 kV/μs Common-Mode Rejection at V_{CM} = 1000 V***
- **Compact, Auto-Insertable Standard 8-pin DIP Package**
- **4.6 μV/°C Offset Drift vs. Temperature**
- **0.9 mV Input Offset Voltage**
- **85 kHz Bandwidth**
- **0.1% Nonlinearity**
- **Worldwide Safety Approval: UL 1577 (3750 V rms/1 min), VDE 0884 and CSA**
- **Advanced Sigma-Delta (ΣΔ) A/D Converter Technology**
- **Fully Differential Circuit Topology**
- **1 μm CMOS IC Technology**

Applications

- **Motor Phase Current Sensing**
- **General Purpose Current Sensing**
- **High-Voltage Power Source Voltage Monitoring**
- **Switch-Mode Power Supply Signal Isolation**
- **General Purpose Analog Signal Isolation**
- **Transducer Isolation**

*The terms common-mode rejection (CMR) and isolation-mode rejection (IMR) are used interchangeably throughout this data sheet.

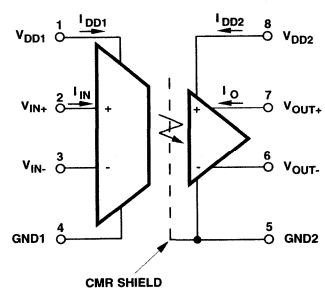
Description

The HCPL-7800 high CMR isolation amplifier provides a unique combination of features ideally suited for motor control circuit designers. The product provides the precision and stability needed to accurately monitor motor current in high-noise motor control environments, providing for smoother control (less "torque ripple") in various types of motor control applications.

This product paves the way for a smaller, lighter, easier to produce, high noise rejection, low cost solution to motor current sensing. The product can also be used for general analog signal isolation applications requiring high accuracy, stability and linearity under similarly severe noise conditions. For general applications, we recommend the HCPL-7800 which exhibits a part-to-part gain tolerance of ± 5%. For precision applications, HP offers the HCPL-7800A and HCPL-7800B, each with part-to-part gain tolerances of ± 1%.

The HCPL-7800 utilizes sigma-delta (ΣΔ) analog-to-digital converter technology, chopper stabilized amplifiers, and a fully differential circuit topology fabricated using HP's 1 μm CMOS IC process. The part also couples our high-efficiency, high-speed AlGaAs LED to a high-speed, noise-shielded detector

Functional Diagram



CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

5965-3592E

using our patented "light-pipe" optocoupler packaging technology.

Together, these features deliver unequaled isolation-mode noise rejection, as well as excellent offset and gain accuracy and stability over time and temperature. This performance is delivered in a compact, auto-insertable, industry standard 8-pin DIP package that meets worldwide regulatory safety standards (gull-wing surface mount option #300 also available).

Ordering Information:

HCPL-7800x

- No Specifier = ± 5% Gain Tol.; Mean Gain Value = 8.00
- A = ± 1% Gain Tol.; Mean Gain Value = 7.93
- B = ± 1% Gain Tol.; Mean Gain Value = 8.07

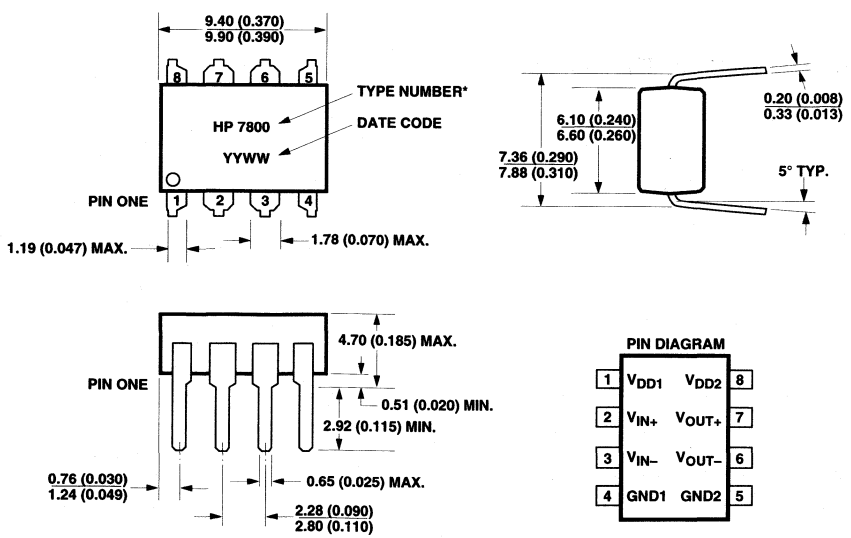
Option yyy

- 300 = Gull Wing Surface Mount Lead Option
- 500 = Tape/Reel Package Option (1 k min.)

Option datasheets available. Contact your Hewlett-Packard sales representative or authorized distributor for information.

Package Outline Drawings

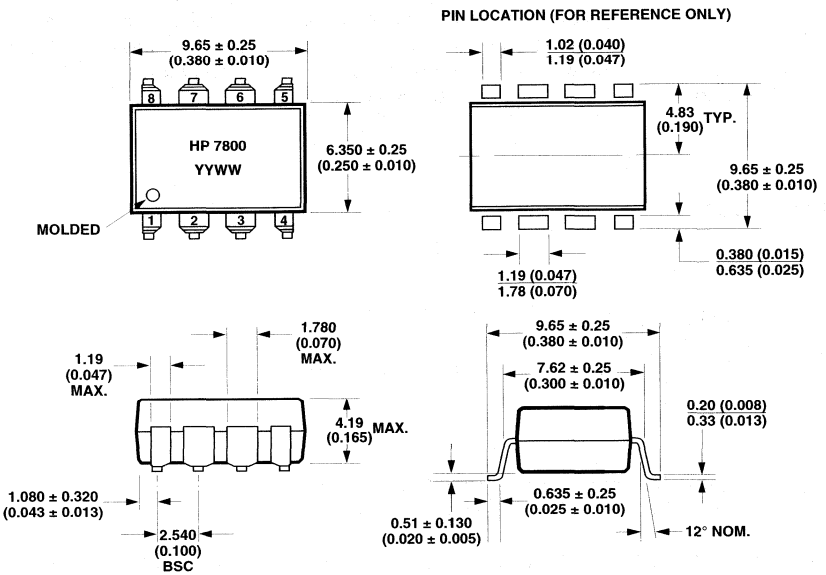
Standard DIP Package



DIMENSIONS IN MILLIMETERS AND (INCHES).

* TYPE NUMBER FOR: HCPL-7800 = 7800
HCPL-7800A = 7800A
HCPL-7800B = 7800B

Gull Wing Surface Mount Option 300*

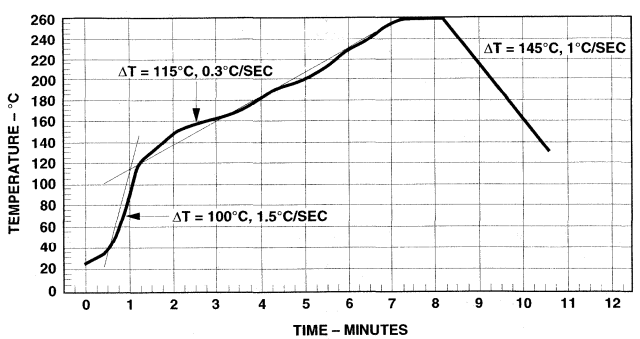


DIMENSIONS IN MILLIMETERS (INCHES).
TOLERANCES (UNLESS OTHERWISE SPECIFIED): xx.xx = 0.01
xx.xxx = 0.005

LEAD COPLANARITY
MAXIMUM: 0.102 (0.004)

* REFER TO OPTION 300 DATA SHEET FOR MORE INFORMATION.

Maximum Solder Reflow Thermal Profile



(NOTE: USE OF NON-CHLORINE ACTIVATED FLUXES IS RECOMMENDED.)

Regulatory Information

The HCPL-7800 has been approved by the following organizations:

UL

Recognized under UL 1577, Component Recognition Program, File E55361.

CSA

Approved under CSA Component Acceptance Notice #5, File CA 88324.

VDE

Approved according to VDE 0884/06.92.

Insulation and Safety Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min. External Air Gap (External Clearance)	L(IO1)	7.4	mm	Measured from input terminals to output terminals, shortest distance through air
Min. External Tracking Path (External Creepage)	L(IO2)	8.0	mm	Measured from input terminals to output terminals, shortest distance path along body
Min. Internal Plastic Gap (Internal Clearance)		0.5	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity
Tracking Resistance (Comparative Tracking Index)	CTI	175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		III a		Material Group (DIN VDE 0110, 1/89, Table 1)

Option 300 – surface mount classification is Class A in accordance with CECC 00802.

VDE 0884 (06.92) Insulation Characteristics

Description	Symbol	Characteristic	Unit
Installation classification per DIN VDE 0110, Table 1 for rated mains voltage ≤ 300 V rms for rated mains voltage ≤ 600 V rms		 I-IV I-III	
Climatic Classification		40/100/21	
Pollution Degree (DIN VDE 0110, Table 1)*		2	
Maximum Working Insulation Voltage	V_{IORM}	848	V peak
Input to Output Test Voltage, Method b** V_{PR} = 1.875 x V_{IORM}, Production test with t_p = 1 sec, Partial discharge < 5 pC	V_{PR}	1591	V peak
Input to Output Test Voltage, Method a** V_{PR} = 1.5 x V_{IORM}, Type and sample test with t_p = 60 sec, Partial discharge < 5 pC	V_{PR}	1273	V peak
Highest Allowable Overvoltage** (Transient Overvoltage t_{TR} = 10 sec)	V_{TR}	6000	V peak
Safety-limiting values (Maximum values allowed in the event of a failure, also see Figure 27) Case Temperature Input Power Output Power	 T_S $P_{S,Input}$ $P_{S,Output}$	 175 80 250	 °C mW mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	≥ $1x10^{12}$	Ω

*This part may also be used in Pollution Degree 3 environments where the rated mains voltage is ≤ 300 V rms (per DIN VDE 0110).
**Refer to the front of the optocoupler section of the current catalog for a more detailed description of VDE 0884 and other product safety requirements.

Note: Optocouplers providing safe electrical separation per VDE 0884 do so only within the safety-limiting values to which they are qualified. Protective cut-out switches must be used to ensure that the safety limits are not exceeded.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Note
Storage Temperature	T_S	-55	125	℃	
Ambient Operating Temperature	T_A	-40	100	℃	
Supply Voltages	V_{DD1}, V_{DD2}	0.0	5.5	V	
Steady-State Input Voltage	V_{IN+}, V_{IN-}	-2.0	V_{DD1} +0.5	V	
Two Second Transient Input Voltage		-6.0			
Output Voltages	V_{OUT+}, V_{OUT-}	-0.5	V_{DD2} +0.5	V	
Lead Solder Temperature (1.6 mm below seating plane, 10 sec.)	T_{LS}		260	℃	1
Reflow Temperature Profile	See **Package Outline Drawings** Section				

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit	Note
Ambient Operating Temperature	T_A	-40	85	℃	2
Supply Voltages	V_{DD1}, V_{DD2}	4.5	5.5	V	3
Input Voltage	V_{IN+}, V_{IN-}	-200	200	mV	4
Output Current	$\|I_O\|$		1	mA	5

DC Electrical Specifications

All specifications and figures are at the nominal operating condition of V_{IN+} = 0 V, V_{IN-} = 0 V, T_A = 25°C, V_{DD1} = 5.0 V, and V_{DD2} = 5.0 V, unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Note
Input Offset Voltage	V_{OS}	-1.8	-0.9	0.0	mV		1	
Input Offset Drift vs. Temperature	dV_{OS}/dT		-2.1		µV/°C		1, 2	6
Abs. Value of Input Offset Drift vs. Temperature	$\lvert dV_{OS}/dT \rvert$		4.6		µV/°C		1	7
Input Offset Drift vs. V_{DD1}	dV_{OS}/dV_{DD1}		30		µV/V		1, 3	8
Input Offset Drift vs. V_{DD2}	dV_{OS}/dV_{DD2}		-40		µV/V		1, 4	9
Gain (± 5% Tol.)	G	7.61	8.00	8.40		-200 mV < V_{IN+} < 200 mV	1, 5	10
Gain - A Version (± 1% Tol.)	G_A	7.85	7.93	8.01				
Gain - B Version (± 1% Tol.)	G_B	7.99	8.07	8.15				
Gain Drift vs. Temperature	dG/dT		0.001		%/°C		5, 6	11
Abs. Value of Gain Drift vs. Temperature	$\lvert dG/dT \rvert$		0.001		%/°C		5	12
Gain Drift vs. V_{DD1}	dG/dV_{DD1}		0.21		%/V		5, 7	13
Gain Drift vs. V_{DD2}	dG/dV_{DD2}		-0.06		%/V		5, 8	14
200 mV Nonlinearity	NL_{200}		0.2	0.35	%		5, 9	15
200 mV Nonlinearity Drift vs. Temperature	dNL_{200}/dT		-0.001		% pts/°C		5, 10	16
200 mV Nonlinearity Drift vs. V_{DD1}	dNL_{200}/dV_{DD1}		-0.005		% pts/V		5, 11	17
200 mV Nonlinearity Drift vs. V_{DD2}	dNL_{200}/dV_{DD2}		-0.007		% pts/V		5, 12	18
100 mV Nonlinearity	NL_{100}		0.1	0.25	%	-100 mV< V_{IN+} < 100 mV	5, 13	19
Maximum Input Voltage Before Output Clipping	$\lvert V_{IN+} \rvert_{max}$		300		mV		14	
Average Input Bias Current	I_{IN}		-670		nA		15, 16	20
Input Bias Current Temperature Coefficient	dI_{IN}/dT		3		nA/°C			
Average Input Resistance	R_{IN}		530		kΩ		15	20
Input Resistance Temperature Coefficient	dR_{IN}/dT		0.38		%/°C			
Input DC Common-Mode Rejection Ratio	$CMRR_{IN}$		72		dB			21
Output Resistance	R_O		11		Ω			5
Output Resistance Temperature Coefficient	dR_O/dT		0.6		%/°C			
Output Low Voltage	V_{OL}		1.18		V	$\lvert V_{IN+} \rvert$ = 500 mV	14	22
Output High Voltage	V_{OH}		3.61		V	I_{OUT+} = 0 A, I_{OUT-} = 0 A		
Output Common-Mode Voltage	V_{OCM}	2.20	2.39	2.60	V	-40°C < T_A < 85°C 4.5 V < V_{DD1} < 5.5 V	14	
Input Supply Current	I_{DD1}		10.7	15.5	mA		17	23
Output Supply Current	I_{DD2}		11.6	14.5	mA	V_{IN+} = 200 mV, -40°C < T_A < 85°C 4.5 V < V_{DD2} < 5.5 V	18	24
Output Short-Circuit Current	$\lvert I_{OSC} \rvert$		9.3		mA	V_{OUT} = 0 V or V_{DD2}		25

AC Electrical Specifications

All specifications and figures are at the nominal operating condition of V_{IN+} = 0 V, V_{IN-} = 0 V, T_A = 25°C, V_{DD1} = 5.0 V, and V_{DD2} = 5.0 V, unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Note
Rising Edge Isolation Mode Rejection	IMR_R	10	25		kV/µs	V_{IM} = 1 kV	19, 20	26
Falling Edge Isolation Mode Rejection	IMR_F	10	15		kV/µs			
Isolation Mode Rejection Ratio at 60 Hz	IMRR		>140		dB		19	27
Propagation Delay to 10%	t_{PD10}		2.0	3.3	µs	-40°C < T_A < 85°C	21, 22	
Propagation Delay to 50%	t_{PD50}		3.4	5.6	µs			
Propagation Delay to 90%	t_{PD90}		6.3	9.9	µs			
Rise/Fall Time (10%-90%)	$t_{R/F}$		4.3	6.6	µs			
Bandwidth (-3 dB)	f_{-3dB}	50	85		kHz		23, 24	
Bandwidth (-45°)	$f_{-45°}$		35		kHz			
RMS Input-Referred Noise	V_N		300		µV rms	Bandwidth = 100 kHz	25, 26	28
Power Supply Rejection	PSR		5		mV_{p-p}			29

Package Characteristics

All specifications and figures are at the nominal operating condition of V_{IN+} = 0 V, V_{IN-} = 0 V, T_A = 25°C, V_{DD1} = 5.0 V, and V_{DD2} = 5.0 V, unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions		Fig.	Note
Input-Output Momentary Withstand Voltage*	V_{ISO}	3750			V rms	t = 1 min., RH ≤ 50%			30, 31
Input-Output Resistance	R_{I-O}	10^{12}	10^{13}		Ω	T_A = 25°C	V_{I-O} = 500 Vdc		30
		10^{11}				T_A = 100°C			
Input-Output Capacitance	C_{I-O}		0.7		pF	f = 1 MHz			30
Input IC Junction-to-Case Thermal Resistance	θ_{jci}		96		°C/W				32
Output IC Junction-to-Case Thermal Resistance	θ_{jco}		114		°C/W				

*The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the VDE 0884 Insulation Characteristics Table (if applicable), your equipment level safety specification, or HP Application Note 1074, "Optocoupler Input-Output Endurance Voltage."

Notes:

General Note: Typical values represent the mean value of all characterization units at the nominal operating conditions. Typical drift specifications are determined by calculating the rate of change of the specified parameter versus the drift parameter (at nominal operating conditions) for each characterization unit, and then averaging the individual unit rates. The corresponding drift figures are normalized to the nominal operating conditions and show how much drift occurs as the particular drift parameter is varied from its nominal value, with all other parameters held at their nominal operating values. Figures show the mean drift of all characterization units as a group, as well as the ± 2-sigma statistical limits. Note that the typical drift specifications in the tables below may differ from the slopes of the mean curves shown in the corresponding figures.

1. HP recommends the use of non-chlorine activated fluxes.
2. The HCPL-7800 will operate properly at ambient temperatures up to 100°C but may not meet published specifications under these conditions.
3. DC performance can be best maintained by keeping V_{DD1} and V_{DD2} as close as possible to 5 V. See application section for circuit recommendations.
4. HP recommends operation with V_{IN-} = 0 V (tied to GND1). Limiting V_{IN+} to 100 mV will improve DC nonlinearity and nonlinearity drift. If V_{IN-} is brought above 800 mV with respect to GND1, an internal test mode may be activated. This test mode is not intended for customer use.
5. Although, statistically, the average difference in the output resistance of pins 6 and 7 is near zero, the standard deviation of the difference is 1.3 Ω due to normal process variations. Consequently, keeping the output current below 1 mA will ensure the best offset performance.
6. Data sheet value is the average change in offset voltage versus temperature at T_A = 25°C, with all other parameters held constant. This value is expressed as the change in offset voltage per °C change in temperature.
7. Data sheet value is the average magnitude of the change in offset voltage versus temperature at T_A = 25°C, with all other parameters held constant. This value is expressed as the change in magnitude per °C change in temperature.
8. Data sheet value is the average change in offset voltage versus input supply voltage at V_{DD1} = 5 V, with all other parameters held constant. This value is expressed as the change in offset voltage per volt change of the input supply voltage.
9. Data sheet value is the average change in offset voltage versus output supply voltage at V_{DD2} = 5 V, with all other parameters held constant. This value is expressed as the change in offset voltage per volt change of the output supply voltage.
10. Gain is defined as the slope of the best-fit line of differential output voltage (V_{OUT+} - V_{OUT-}) versus differential input voltage (V_{IN+} -V_{IN-}) over the specified input range.
11. Data sheet value is the average change in gain versus temperature at T_A = 25°C, with all other parameters held constant. This value is expressed as the percentage change in gain per °C change in temperature.
12. Data sheet value is the average magnitude of the change in gain versus temperature at T_A = 25°C, with all other parameters held constant. This value is expressed as the percentage change in magnitude per °C change in temperature.
13. Data sheet value is the average change in gain versus input supply voltage at V_{DD1} = 5 V, with all other parameters held constant. This value is expressed as the percentage change in gain per volt change of the input supply voltage.
14. Data sheet value is the average change in gain versus output supply voltage at V_{DD2} = 5 V, with all other parameters held constant. This value is expressed as the percentage change in gain per volt change of the output supply voltage.
15. Nonlinearity is defined as the maximum deviation of the output voltage from the best-fit gain line (see Note 10), expressed as a percentage of the full-scale differential output voltage range. For example, an input range of ± 200 mV generates a full-scale differential output range of 3.2 V (± 1.6 V); a maximum output deviation of 6.4 mV would therefore correspond to a nonlinearity of 0.2%.
16. Data sheet value is the average change in nonlinearity versus temperature at T_A = 25°C, with all other parameters held constant. This value is expressed as the number of percentage points that the nonlinearity will change per °C change in temperature. For example, if the temperature is increased from 25°C to 35°C, the nonlinearity typically will decrease by 0.01 percentage points (10°C times -0.001 % pts/°C) from 0.2% to 0.19%.
17. Data sheet value is the average change in nonlinearity versus input supply voltage at V_{DD1} = 5 V, with all other parameters held constant. This value is expressed as the number of percentage points that the nonlinearity will change per volt change of the input supply voltage.
18. Data sheet value is the average change in nonlinearity versus output supply voltage at V_{DD2} = 5 V, with all other parameters held constant. This value is expressed as the number of percentage points that the nonlinearity will change per volt change of the output supply voltage.
19. NL_{100} is the nonlinearity specified over an input voltage range of ± 100 mV.
20. Because of the switched-capacitor nature of the input sigma-delta converter, time-averaged values are shown.
21. This parameter is defined as the ratio of the differential signal gain (signal applied differentially between pins 2 and 3) to the common-mode gain (input pins tied together and the signal applied to both inputs at the same time), expressed in dB.
22. When the differential input signal exceeds approximately 300 mV, the outputs will limit at the typical values shown.
23. The maximum specified input supply current occurs when the differential input voltage (V_{IN+} - V_{IN-}) = 0 V. The input supply current decreases approximately 1.3 mA per 1 V decrease in V_{DD1}.
24. The maximum specified output supply current occurs when the differential input voltage (V_{IN+} - V_{IN-}) = 200 mV, the maximum recommended operating input voltage. However, the output supply current will continue to rise for differential input voltages up to approximately 300 mV, beyond which the output supply current remains constant.

25. Short circuit current is the amount of output current generated when either output is shorted to V_{DD2} or ground.
26. IMR (also known as CMR or Common Mode Rejection) specifies the minimum rate of rise of an isolation mode noise signal at which small output perturbations begin to appear. These output perturbations can occur with both the rising and falling edges of the isolation-mode wave form and may be of either polarity. When the perturbations first appear, they occur only occasionally and with relatively small peak amplitudes (typically 20-30 mV at the output of the recommended application circuit). As the magnitude of the isolation mode transients increase, the regularity and amplitude of the perturbations also increase. See applications section for more information.
27. IMRR is defined as the ratio of differential signal gain (signal applied differentially between pins 2 and 3) to the isolation mode gain (input pins tied to pin 4 and the signal applied between the input and the output of the isolation amplifier) at 60 Hz, expressed in dB.
28. Output noise comes from two primary sources: chopper noise and sigma-delta quantization noise. Chopper noise results from chopper stabilization of the output op-amps. It occurs at a specific frequency (typically 200 kHz at room temperature), and is not attenuated by the internal output filter. A filter circuit can be easily added to the external post-amplifier to reduce the total rms output noise. The internal output filter does eliminate most, but not all, of the sigma-delta quantization noise. The magnitude of the output quantization noise is very small at lower frequencies (below 10 kHz) and increases with increasing frequency. See applications section for more information.
29. Data sheet value is the differential amplitude of the transient at the output of the HCPL-7800 when a 1 V_{pk-pk}, 1 MHz square wave with 5 ns rise and fall times is applied to both V_{DD1} and V_{DD2}.
30. This is a two-terminal measurement: pins 1-4 are shorted together and pins 5-8 are shorted together.
31. In accordance with UL1577, for devices with minimum V_{ISO} specified at 3750 V_{rms}, each optocoupler is proof-tested by applying an insulation test voltage greater-than-or-equal-to 4500 V_{rms} for one second (leak current detection limit, $I_{I-O} < 5\ \mu A$). This test is performed before the method b, 100% production test for partial discharge shown in the VDE 0884 Insulation Characteristics Table.
32. Case temperature was measured with a thermocouple located in the center of the underside of the package.

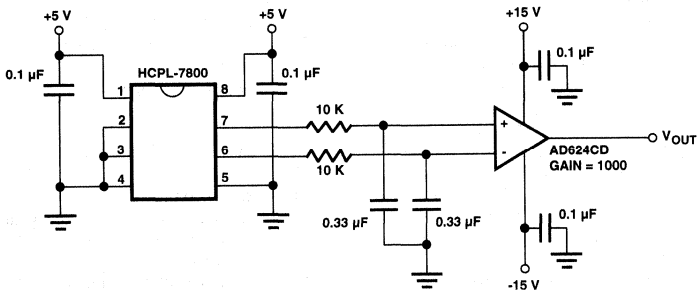


Figure 1. Input Offset Voltage Test Circuit.

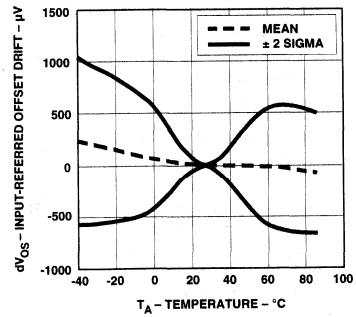


Figure 2. Input-Referred Offset Drift vs. Temperature.

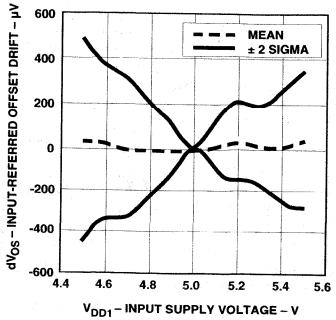


Figure 3. Input-Referred Offset Drift vs. V_{DD1} (V_{DD2} = 5 V).

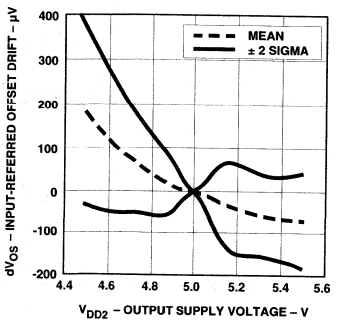


Figure 4. Input-Referred Offset Drift vs. V_{DD2} (V_{DD1} = 5 V).

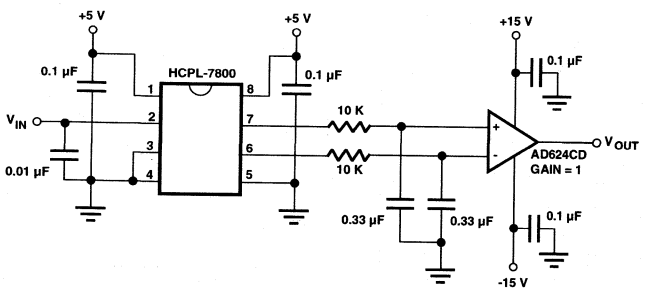


Figure 5. Gain and Nonlinearity Test Circuit.

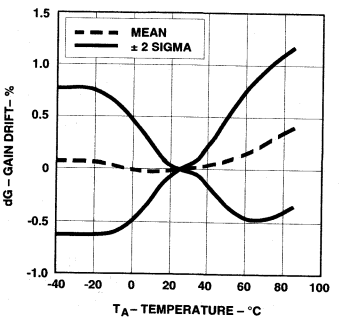


Figure 6. Gain Drift vs. Temperature.

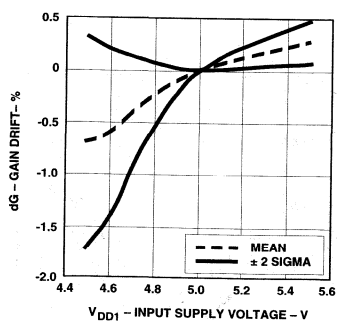


Figure 7. Gain Drift vs. V_{DD1} (V_{DD2} = 5 V).

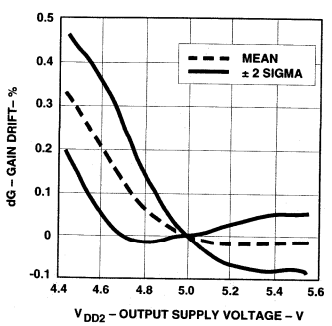


Figure 8. Gain Drift vs. V_{DD2} (V_{DD1} = 5 V).

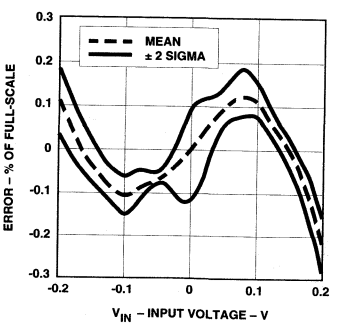


Figure 9. 200 mV Nonlinearity Error Plot.

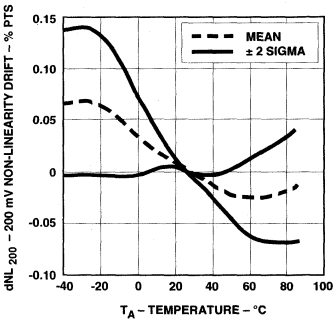


Figure 10. 200 mV Nonlinearity Drift vs. Temperature.

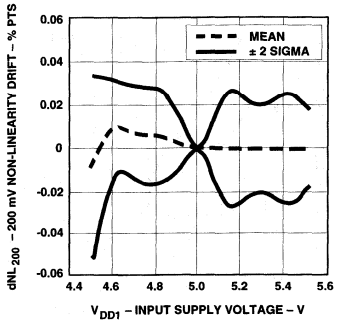


Figure 11. 200 mV Nonlinearity Drift vs. V_{DD1} (V_{DD2} = 5 V).

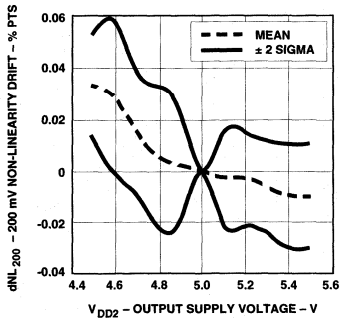


Figure 12. 200 mV Nonlinearity Drift vs. V_{DD2} (V_{DD1} = 5 V).

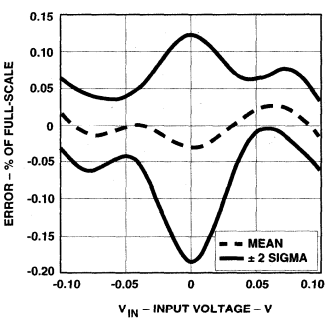


Figure 13. 100 mV Nonlinearity Error Plot.

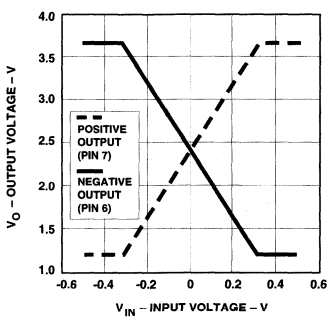


Figure 14. Typical Output Voltages vs. Input Voltage.

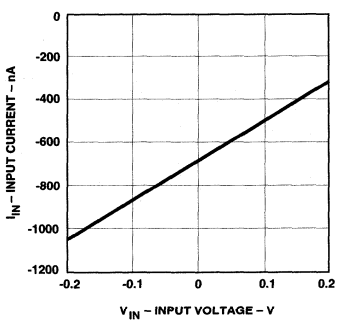


Figure 15. Typical Input Current vs. Input Voltage.

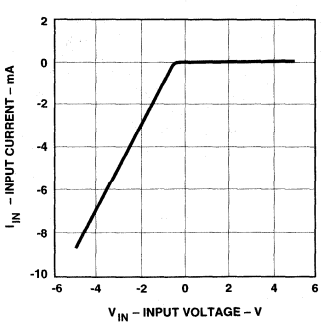


Figure 16. Typical Input Current vs. Input Voltage.

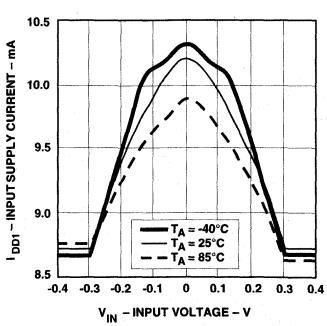


Figure 17. Typical Input Supply Current vs. Input Voltage.

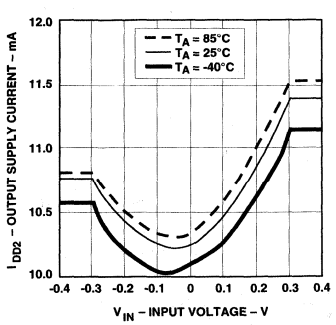


Figure 18. Typical Output Supply Current vs. Input Voltage.

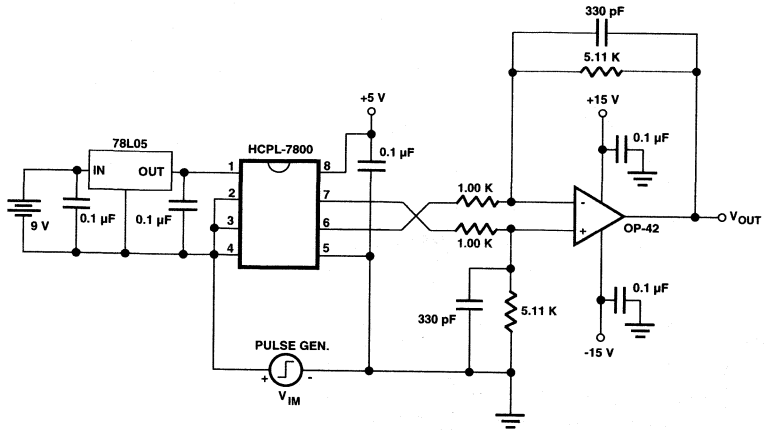


Figure 19. Isolation Mode Rejection Test Circuit.

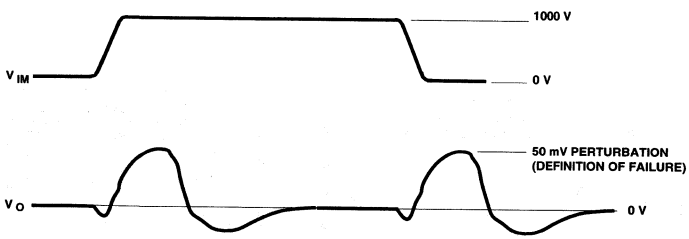


Figure 20. Typical IMR Failure Waveform.

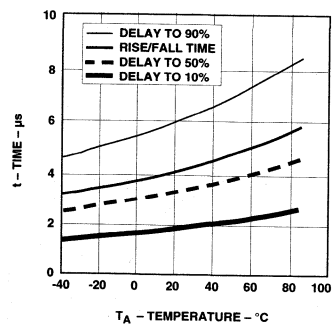


Figure 21. Typical Propagation Delays and Rise/Fall Time vs. Temperature.

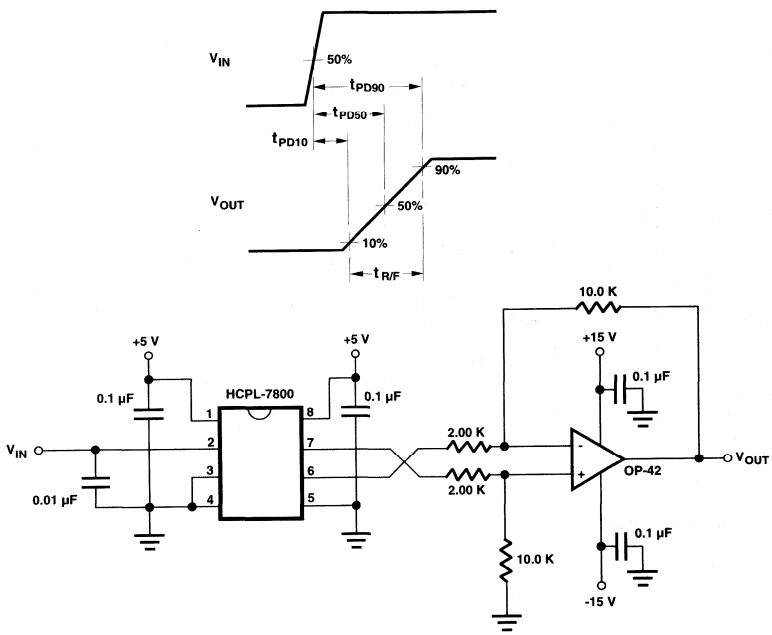


Figure 22. Propagation Delay and Rise/Fall Time Test Circuit.

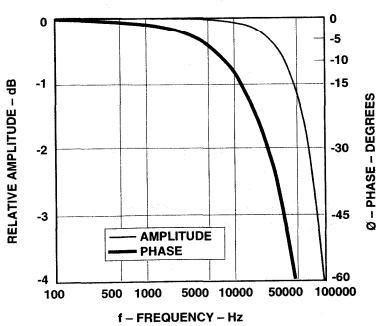


Figure 23. Typical Amplitude and Phase Response vs. Frequency.

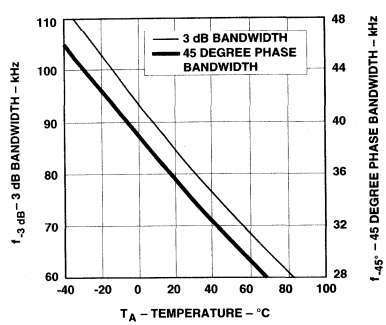


Figure 24. Typical 3 dB and 45° Bandwidths vs. Temperature.

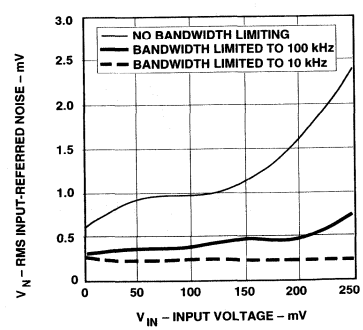


Figure 25. Typical RMS Input-Referred Noise vs. Input Voltage.

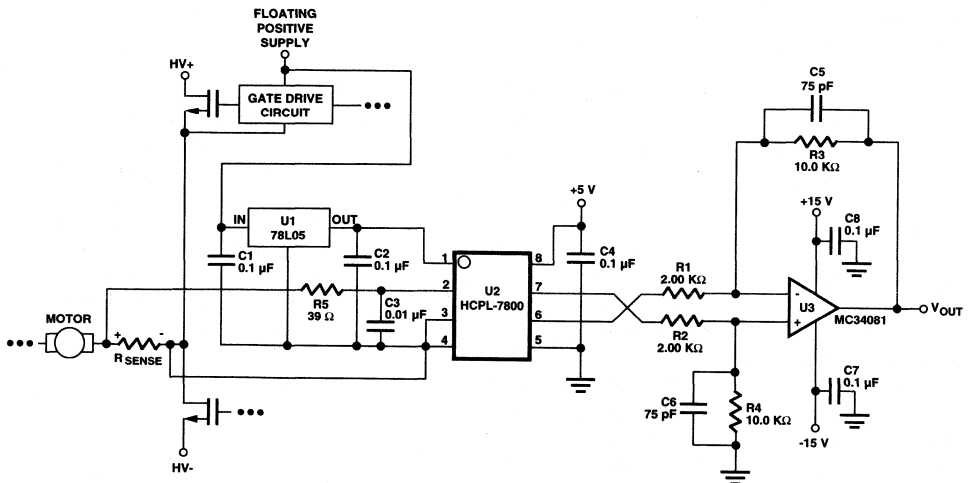


Figure 26. Recommended Application Circuit.

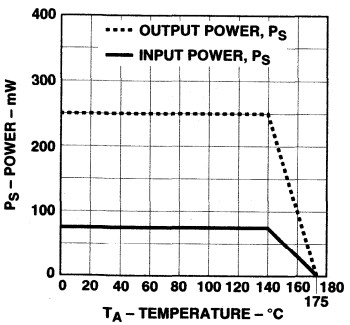


Figure 27. Dependence of Safety-Limiting Parameters on Ambient Temperature.

Applications Information

Functional Description

Figure 28 shows the primary functional blocks of the HCPL-7800. In operation, the sigma-delta analog-to-digital converter converts the analog input signal into a high-speed serial bit stream, the time average of which is directly proportional to the input signal. This high speed stream of digital data is encoded and optically transmitted to the detector circuit. The detected signal is decoded and converted into accurate analog voltage levels, which are then filtered to produce the final output signal.

To help maintain device accuracy over time and temperature, internal amplifiers are chopper-stabilized. Additionally, the encoder circuit eliminates the effects of pulse-width distortion of the optically transmitted data by generating one pulse for every edge (both rising and falling) of the converter data to be transmitted, essentially converting the *widths* of the sigma-delta output pulses into the *positions* of the encoder output pulses. A significant benefit of this coding scheme is that any non-ideal characteristics of the LED (such as non-linearity and drift over time and temperature) have little, if any, effect on the performance of the HCPL-7800.

Circuit Information

The recommended application circuit is shown in Figure 26. A floating power supply (which in many applications could be the same supply that is used to drive the high-side power transistor) is regulated to 5 V using a simple three-terminal voltage regulator. The input of the HCPL-7800 is connected directly to the current sensing resistor. The differential output of the isolation amplifier is converted to a ground-referenced single-ended output voltage with a simple differential amplifier circuit. Although the application circuit is relatively simple, a few general recommendations should be followed to ensure optimal performance.

As shown in Figure 26, 0.1 µF bypass capacitors should be located as close as possible to the input and output power supply pins of the HCPL-7800. Notice that pin 2 (V_{IN+}) is bypassed with a 0.01 µF capacitor to reduce input offset voltage that can be caused by the combination of long input leads and the switched-capacitor nature of the input circuit.

With pin 3 (V_{IN-}) tied directly to pin 4 (GND1), the power-supply return line also functions as the sense line for the negative side of the current-sensing resistor; this allows a single twisted pair of wire to connect the isolation amplifier to the sense resistor. In some applications, however, better performance may be obtained by connecting pins 2 and 3 (V_{IN+} and V_{IN-}) directly across the sense resistor with twisted pair wire and using a separate wire for the power supply return line. Both input pins should be bypassed with 0.01 µF capacitors close to the isolation amplifier. In either case, it is recommended that twisted-pair wire be used to connect the isolation amplifier to the current-sensing resistor to minimize electro-magnetic interference of the sense signal.

To obtain optimal CMR performance, the layout of the printed circuit board (PCB) should minimize any stray coupling by maintaining the maximum possible distance between the input and output sides of the circuit and ensuring that any ground plane on the PCB does not pass directly below the HCPL-7800. An example single-sided PCB layout for the recommended application circuit is shown in Figure 29. The trace pattern is shown in "X-ray" view as it would be seen from the top of the PCB; a mirror image of this layout can be used to generate a PCB.

An inexpensive 78L05 three-terminal regulator is shown in the recommended application circuit. Because the performance of the isolation amplifier can be affected by changes in the power supply voltages, using regulators with tighter output voltage tolerances will result in better overall circuit performance. Many different regulators that provide tighter output voltage tolerances than the 78L05 can be used, including: TL780-05 (Texas Instruments), LM340LAZ-5.0 and LP2950CZ-5.0 (National Semiconductor).

The op-amp used in the external post-amplifier circuit should be of sufficiently high precision so that it does not contribute a significant amount of offset or offset drift relative to the contribution from the isolation amplifier. Generally, op-amps with bipolar input stages exhibit better offset performance than op-amps with JFET or MOSFET input stages.

In addition, the op-amp should also have enough bandwidth and slew rate so that it does not adversely affect the response speed of the overall circuit. The post-amplifier circuit includes a pair of capacitors (C5 and C6) that form a single-pole low-pass filter; these capacitors allow the bandwidth of the post-amp to be adjusted independently of the gain and are useful for reducing the output noise from the isolation amplifier. Many different op-amps could be used in the circuit, including: MC34082A (Motorola), TL032A, TLO52A, and TLC277 (Texas Instruments), LF412A (National Semiconductor).

The gain-setting resistors in the post-amp should have a tolerance of 1% or better to ensure adequate CMRR and adequate gain tolerance for the overall circuit. Resistor networks can be used that have much better ratio tolerances than can be achieved using discrete resistors. A resistor network also reduces the total number of components for the circuit as well as the required board space.

The current-sensing resistor should have a relatively low value of resistance to minimize power dissipation, a fairly low inductance to accurately reflect high-frequency signal components, and a reasonably tight tolerance to maintain overall circuit accuracy. Although decreasing the value of the sense resistor decreases power dissipation, it also decreases the full-scale input voltage making iso-amp offset voltage effects more significant. These two

conflicting considerations, therefore, must be weighed against each other in selecting an appropriate sense resistor for a particular application. To maintain circuit accuracy, it is recommended that the sense resistor and the isolation amplifier circuit be located as close as possible to one another. Although it is possible to buy current-sensing resistors from established vendors (e.g., the LVR-1, -3 and -5 resistors from Dale), it is also possible to make a sense resistor using a short piece of wire or even a trace on a PC board.

Figures 30 and 31 illustrate the response of the overall isolation amplifier circuit shown in Figure 26. Figure 30 shows the response of the circuit to a ± 200 mV 20 kHz sine wave input and Figure 31 the response of the circuit to a ± 200 mV 20 kHz square wave input. Both figures demonstrate the fast, well-behaved response of the HCPL-7800.

Figure 32 shows how quickly the isolation amplifier recovers from an overdrive condition generated by a 2 kHz square wave swinging between 0 and 500 mV (note that the time scale is different from the previous figures). The first wave form is the output of the application circuit with the filter capacitors removed to show the actual response of the isolation amplifier. The second wave form is the response of the same circuit with the capacitors installed. The recovery time and overshoot are relatively independent of the amplitude and polarity of the overdrive signal, as well as its duration.

For more information, refer to Application Note 1059.

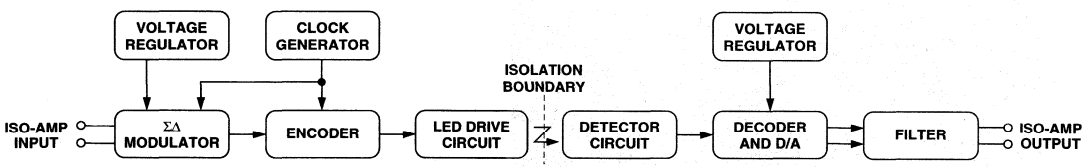


Figure 28. HCPL-7800 Block Diagram.

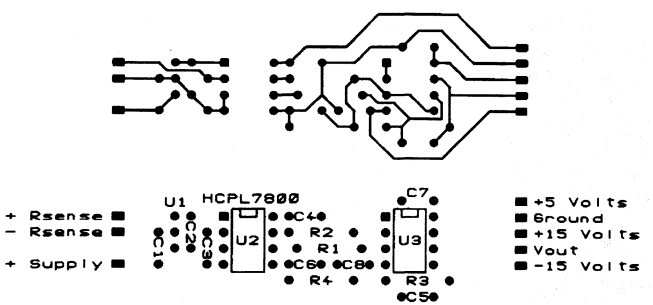


Figure 29. PC Board Trace Pattern and Loading Diagram Example.

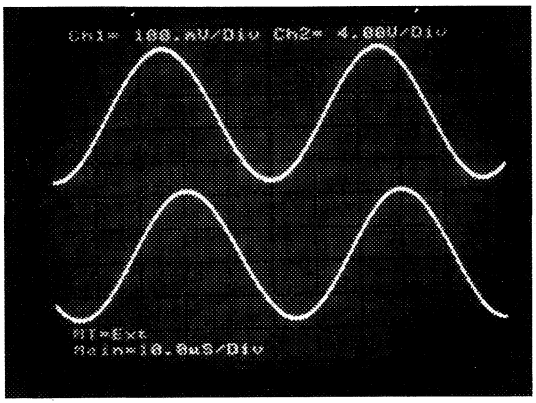


Figure 30. Application Circuit Sine Wave Response.

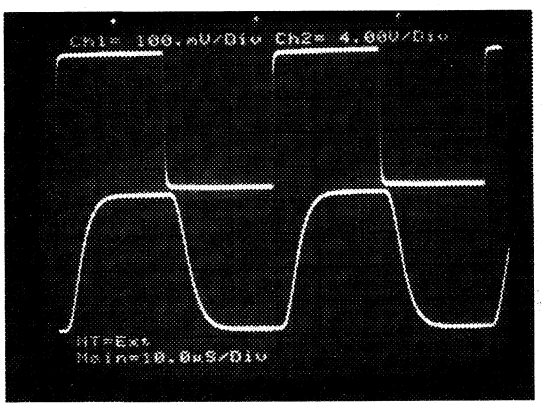


Figure 31. Application Circuit Square Wave Response.

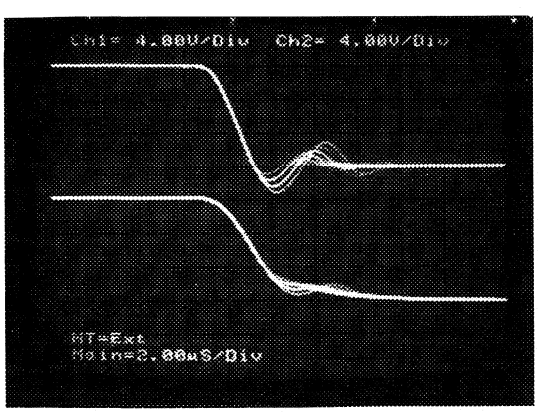


Figure 32. Application Circuit Overload Recovery Waveform.

High CMR Analog Isolation Amplifiers

Technical Data

HCPL-7820
HCPL-7825

Features

- **Fast Propagation Delays for Over-Current and Fault Detection Sensing**
- **High Common Mode Rejection (CMR): 30 kV/μs at V_{CM} = 1000 V***
- **3% Gain Tolerance: HCPL-7820**
  5% Gain Tolerance: HCPL-7825
- **0.05% Nonlinearity**
- **Low Offset Voltage and Offset Drift vs. Temperature**
- **200 kHz Bandwidth**
- **Performance Specified for Common Motor Control Applications over -40°C to 100°C Temperature Range**
- **Worldwide Safety and Regulatory Approval: UL 1577 (3750 V rms/1 Min), VDE 0884 and CSA**
- **Compact Auto-Insertable Standard 8-Pin DIP Package**
- **Advanced Sigma-Delta (ΣΔ) A/D Converter Technology**
- **1 μm CMOS IC Technology**

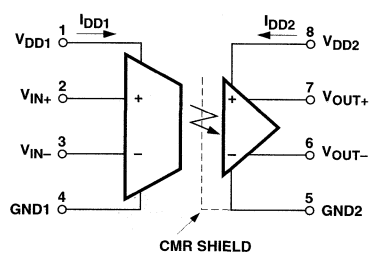
Applications

- **Motor Phase and Rail Current Sensing**
- **General Purpose Current Sensing and Monitoring**
- **High-Voltage Monitoring**
- **Switched Mode Power Supply Signal Isolation**
- **General Purpose Analog Signal Isolation**
- **Transducer Isolation**

Description

The HCPL-7820/7825 high CMR isolation amplifier consists of a sigma-delta analog-to-digital converter optically coupled to an integrated output digital-to-analog converter. When used with a shunt resistor in the current path, the HCPL-7820/7825 provides a cost-effective, auto-insertion compatible current sense solution. Fast propagation delays allow this part to be used in either motor drive or inverter applications for either phase current monitoring or rail current fault detection applications. High isolation mode rejection makes this product suitable for noisy electrical environments, such as those generated by the high switching rates of power IGBTs. Low offset voltage together with low offset change vs. temperature permits accurate use of auto-calibration techniques. Tight gain tolerance with good nonlinearity further provide the characteristics needed to insure highly accurate motor speed control. A high operating temperature range with specified performance parameters allow

Functional Diagram



A 0.1 μF bypass capacitor must be connected between pins 1 and 4 and between pins 5 and 8.

*The terms common-mode rejection (CMR) and isolation-mode rejection (IMR) are used interchangeably throughout this data sheet.

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

this device to be used in hostile industrial environments. This performance is delivered in an auto-insertable, industry standard 8-pin DIP package that meets major worldwide regulatory and safety approval ratings to help ensure that your equipment can be certified in many geographic areas.

Ordering Information

HCPL-782x

- 0 = ± 3% Gain Tolerance
- 5 = ± 5% Gain Tolerance

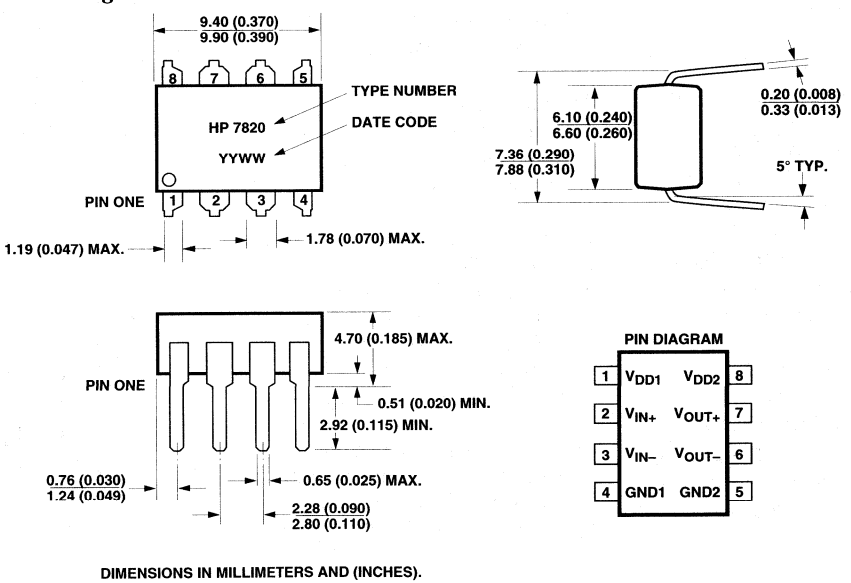
Option yyy

- 300 = Gull Wing Surface Mount Lead Option
- 500 = Tape/Reel Package Option (1 k min.)

Option datasheets available. Contact your Hewlett-Packard sales representative or authorized distributor for information.

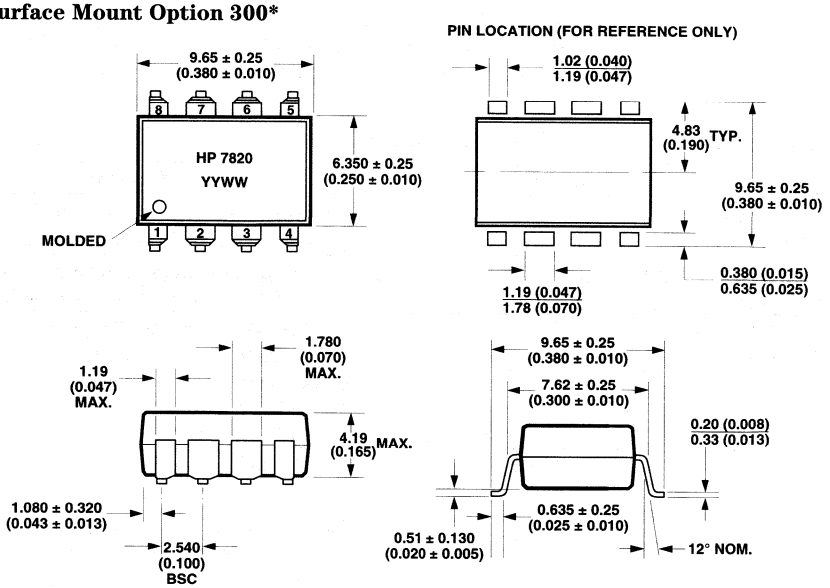
Package Outline Drawings

Standard DIP Package



DIMENSIONS IN MILLIMETERS AND (INCHES).

Gull Wing Surface Mount Option 300*

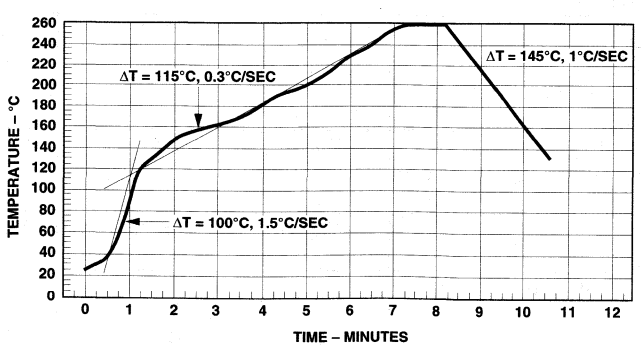


DIMENSIONS IN MILLIMETERS (INCHES).
TOLERANCES (UNLESS OTHERWISE SPECIFIED): xx.xx = 0.01
xx.xxx = 0.005

LEAD COPLANARITY
MAXIMUM: 0.102 (0.004)

*Refer to Option 300 Data Sheet for more information.

Maximum Solder Reflow Thermal Profile



(NOTE: USE OF NON-CHLORINE ACTIVATED FLUXES IS RECOMMENDED.)

Regulatory Information

The HCPL-7820/7825 has been approved by the following organizations:

UL

Recognized under UL 1577, Component Recognition Program, FILE E55361.

CSA

Approved under CSA Component Acceptance Notice #5, File CA 88324.

VDE

Approved according to VDE 0884/06.92.

Insulation and Safety Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min. External Air Gap (External Clearance)	L(IO1)	7.4	mm	Measured from input terminals to output terminals, shortest distance through air
Min. External Tracking Path (External Creepage)	L(IO2)	8.0	mm	Measured from input terminals to output terminals, shortest distance path along body
Min. Internal Plastic Gap (Internal Clearance)		0.5	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity
Tracking Resistance (Comparative Tracking Index)	CTI	175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		III a		Material Group (DIN VDE 0110, 1/89, Table 1)

Option 300 – surface mount classification is Class A in accordance with CECC 00802.

VDE 0884 (06.92) Insulation Characteristics

Description	Symbol	Characteristic	Unit
Installation classification per DIN VDE 0110, Table 1 for rated mains voltage ≤ 300 V rms for rated mains voltage ≤ 600 V rms		 I-IV I-III	
Climatic Classification		40/100/21	
Pollution Degree (DIN VDE 0110, Table 1)*		2	
Maximum Working Insulation Voltage	V_{IORM}	848	V peak
Input to Output Test Voltage, Method b** V_{PR} = 1.875 x V_{IORM}, Production test with t_p = 1 sec, Partial discharge < 5 pC	V_{PR}	1591	V peak
Input to Output Test Voltage, Method a** V_{PR} = 1.5 x V_{IORM}, Type and sample test with t_p = 60 sec, Partial discharge < 5 pC	V_{PR}	1273	V peak
Highest Allowable Overvoltage** (Transient Overvoltage t_{TR} = 10 sec)	V_{TR}	6000	V peak
Safety-limiting values (Maximum values allowed in the event of a failure, also see Figure 22) Case Temperature Input Power Output Power	 T_S $P_{S,Input}$ $P_{S,Output}$	 175 80 250	 °C mW mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	$\geq 1 \times 10^{12}$	Ω

*This part may also be used in Pollution Degree 3 environments where the rated mains voltage is ≤ 300 V rms (per DIN VDE 0110).
**Refer to the front of the optocoupler section of the current catalog for a more detailed description of VDE 0884 and other product safety requirements.

Note: Optocouplers providing safe electrical separation per VDE 0884 do so only within the safety-limiting values to which they are qualified. Protective cut-out switches must be used to ensure that the safety limits are not exceeded.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Note
Storage Temperature	T_S	-55	125	°C	
Ambient Operating Temperature	T_A	-40	100	°C	
Supply Voltages	V_{DD1}, V_{DD2}	0.0	5.5	V	
Steady-State Input Voltage	V_{IN+}, V_{IN-}	-2.0	V_{DD1} +0.5	V	
Two Second Transient Input Voltage		-6.0			
Output Voltages	V_{OUT+}, V_{OUT-}	-0.5	V_{DD2} +0.5	V	
Lead Solder Temperature (1.6 mm below seating plane, 10 sec.)	T_{LS}		260	°C	1
Reflow Temperature Profile	See **Package Outline Drawings** Section				

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit	Note
Ambient Operating Temperature	T_A	-40	100	°C	
Supply Voltages	V_{DD1}, V_{DD2}	4.5	5.5	V	
Input Voltage	V_{IN+}, V_{IN-}	-200	200	mV	2

DC Electrical Specifications

All specifications are at the nominal (typical) operating conditions of V_{IN+} = 0 V, V_{IN-} = 0 V, T_A = 25°C, V_{DD1} = 5 V and V_{DD2} = 5 V, unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Note
Input Offset Voltage	V_{OS}	-0.8	0.45	1.7	mV		1	3
		-2.0	0.45	2.9		-40°C ≤ T_A ≤ 100°C 4.5 V ≤ (V_{DD1}, V_{DD2}) ≤ 5.5 V	1,2,3	
Absolute Value of Input Offset Change vs. Temperature	$\lvert\Delta V_{OS}/\Delta T\rvert$		7.8		µV/°C		1,2	3,4
Gain: HCPL-7820	G	7.76	8.00	8.24	V/V	-200 mV ≤ V_{IN+} ≤ 200 mV	5	
		7.60	8.00	8.40		-200 mV ≤ V_{IN+} ≤ 200 mV -40°C ≤ T_A ≤ 100°C 4.5 V ≤ (V_{DD1}, V_{DD2}) ≤ 5.5 V	5,6,7	
Gain: HCPL-7825	G	7.60	8.00	8.40	V/V	-200 mV ≤ V_{IN+} ≤ 200 mV	5	
		7.44	8.00	8.56		-200 mV ≤ V_{IN+} ≤ 200 mV -40°C ≤ T_A ≤ 100°C 4.5 V ≤ (V_{DD1}, V_{DD2}) ≤ 5.5 V	5,6,7	
200 mV Nonlinearity	NL_{200}		0.06	0.15	%	-200 mV ≤ V_{IN+} ≤ 200 mV	5,8	5
				0.3		-200 mV ≤ V_{IN+} ≤ 200 mV -40°C ≤ T_A ≤ 100°C 4.5 V ≤ (V_{DD1}, V_{DD2}) ≤ 5.5 V	5,8, 9,10, 12	
100 mV Nonlinearity	NL_{100}		0.03	0.08		-100 mV ≤ V_{IN+} ≤ 100 mV	5,8	
				0.1		-100 mV ≤ V_{IN+} ≤ 100 mV -40°C ≤ T_A ≤ 100°C 4.5 V ≤ (V_{DD1}, V_{DD2}) ≤ 5.5 V	5,8, 9,11, 12	
Maximum Input Voltage Before Output Clipping	$\lvert V_{IN+}\rvert_{max}$		320		mV		4	
Average Input Bias Current	I_{IN}		-1		µA		13	6
Average Input Resistance	R_{IN}		280		kΩ			
Input DC Common-Mode Rejection Ratio	$CMRR_{IN}$		52		dB			
Output Resistance	R_O		1.2		Ω			
Output Low Voltage	V_{OL}		1.30		V	V_{IN+} = 400 mV	4	7
Output High Voltage	V_{OH}		3.90		V	V_{IN+} = -400 mV		
Output Common-Mode Voltage	V_{OCM}	2.30	2.60	2.90	V	-400 mV < V_{IN+} < 400 mV -40°C ≤ T_A ≤ 100°C 4.5 V ≤ (V_{DD1}, V_{DD2}) ≤ 5.5 V		
Input Supply Current	I_{DD1}		11.1	17.0	mA		14	
Output Supply Current	I_{DD2}		10.0	14.0	mA		15	
Output Short-Circuit Current	$\lvert I_{OSC}\rvert$		12		mA	V_{OUT} = 0 V or V_{DD2}		8

AC Electrical Specifications

All specifications and figures are at the nominal (typical) operating conditions of V_{IN+} = 0 V, V_{IN-} = 0 V, T_A = 25°C, V_{DD1} = 5 V and V_{DD2} = 5 V, unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Note
Isolation Mode Rejection	IMR	20	30		kV/μs	V_{IM} = 1 kV -40°C < T_A ≤ 100°C 4.5 V ≤ (V_{DD1}, V_{DD2}) ≤ 5.5 V	16	9
Isolation Mode Rejection Ratio at 60 Hz	IMRR		>140		dB			10
Propagation Delay to 50%	t_{PD50}	1.20	1.85	2.85	μs	V_{IN+} = 0 to 100 mV step -40°C ≤ T_A ≤ 100°C 4.5 V ≤ (V_{DD1}, V_{DD2}) ≤ 5.5 V	17,18	
Propagation Delay to 90%	t_{PD90}	1.60	2.75	4.10				
Rise/Fall Time (10-90%)	$t_{R/F}$	0.85	1.50	2.25				
Small-Signal Bandwidth (-3 dB)	f_{-3dB}	150	200	380	kHz	-40°C ≤ T_A ≤ 100°C 4.5 V ≤ (V_{DD1}, V_{DD2}) ≤ 5.5 V	17,19, 20	
Small-Signal Bandwidth (-45°)	$f_{-45°}$		85					
RMS Input-Referred Noise	V_N		1.4		mV rms	In recommended application circuit	21,24	11
Power Supply Rejection	PSR		150		mV p-p			12

Package Characteristics

All specifications and figures are at the nominal (typical) operating conditions of V_{IN+} = 0 V, V_{IN-} = 0 V, T_A = 25°C, V_{DD1} = 5 V and V_{DD2} = 5 V, unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage*	V_{ISO}	3750			V rms	t = 1 min., RH ≤ 50%		13,14
Input-Output Resistance	R_{I-O}	10^{12}	10^{13}		Ω	T_A = 25°C, V_{I-O} = 500 Vdc		13
		10^{11}				T_A = 100°C		
Input-Output Capacitance	C_{I-O}		0.7		pF	f = 1 MHz		
Input IC Junction-to-Case Thermal Resistance	θ_{jci}		96		°C/W	Thermocouple located at center underside of package		
Output IC Junction-to-Case Thermal Resistance	θ_{jco}		114		°C/W			

*The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the VDE 0884 Insulation Characteristics Table (if applicable), your equipment level safety specification, or HP Application Note 1074, "Optocoupler Input-Output Endurance Voltage."

Notes:

1. HP recommends the use of non-chlorine activated fluxes.
2. If V_{IN-} is brought above V_{DD1}-2 V with respect to GND1 an internal test mode may be activated. This test mode is not intended for customer use.
3. Exact offset value is dependent on layout of external bypass capacitors. The offset value in the data sheet corresponds to HP's recommended layout (see Figures 26 and 27).
4. Data sheet value is the average magnitude of the difference in offset voltage from T_A = 25°C to T_A = 100°C, expressed in microvolts per °C.
5. Nonlinearity is defined as half of the peak-to-peak deviation from the best-fit gain line, expressed as a percentage of the full-scale differential output voltage.
6. Because of the switched-capacitor nature of the input sigma-delta A/D converter, time-averaged values are shown.
7. When the differential input signal exceeds approximately 320 mV, the outputs will limit at the typical values shown.
8. Short-circuit current is the amount of output current generated when either output is shorted to V_{DD2} or ground.
9. IMR (also known as CMR or Common Mode Rejection) specifies the minimum rate of rise of an isolation mode noise signal at which small output perturbations begin to appear. These output perturbations can occur with both the rising and falling edges of the isolation mode waveform and may be of either polarity. A CMR failure is defined as a perturbation exceeding 200 mV at the output of the recommended application circuit (Figure 24). See applications section for more information on CMR.
10. IMRR is defined as the ratio of differential signal gain (signal applied differentially between pins 2 and 3) to the isolation mode gain (input pins tied to pin 4 and the signal applied between the input and the output of the isolation amplifier) at 60 Hz, expressed in dB.
11. Output noise comes from two primary sources: chopper noise and sigma-delta quantization noise. Chopper noise results from chopper stabilization of the output op-amps. It occurs at a specific frequency (typically 500 kHz) and is not attenuated by the on-chip output filter. The on-chip filter does eliminate most, but not all, of the sigma-delta quantization noise. An external filter circuit may be easily added to the external post-amplifier to reduce the total RMS output noise. See applications section for more information.
12. Data sheet value is the amplitude of the transient at the differential output of the HCPL-7820/7825 when a 1 V_{p-p}, 1 MHz square wave with 200 ns rise and fall times (measured at pins 1 and 8) is applied to both V_{DD1} and V_{DD2}.
13. This is a two-terminal measurement: pins 1-4 are shorted together and pins 5-8 are shorted together.
14. In accordance with UL 1577, for devices with minimum V_{ISO} specified at 3750 V rms, each optocoupler is proof-tested by applying an insulation test voltage greater than 4500 V rms for one second (leakage current detection limit I_{I-O} < 5 μA). This test is performed before the method b, 100% production test for partial discharge shown in the VDE 0884 Insulation Characteristics Table.

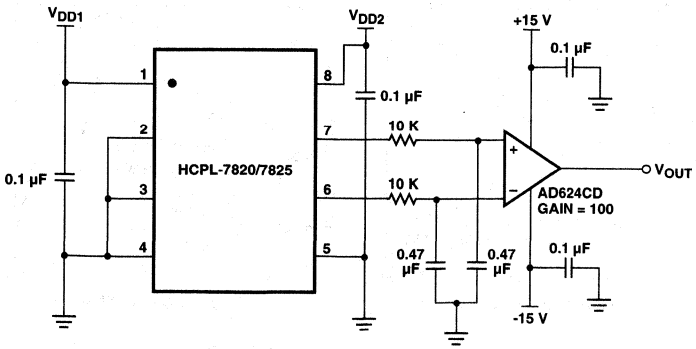


Figure 1. Input Offset Voltage Test Circuit.

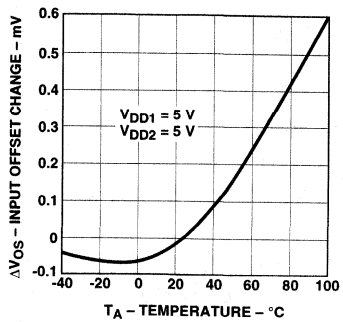


Figure 2. Input Offset Change vs. Temperature.

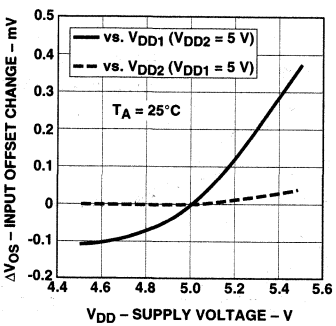


Figure 3. Input Offset Change vs. V_{DD1} and V_{DD2}.

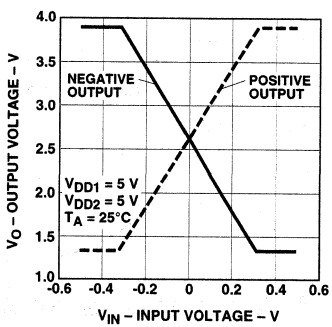


Figure 4. Output Voltages vs. Input Voltage.

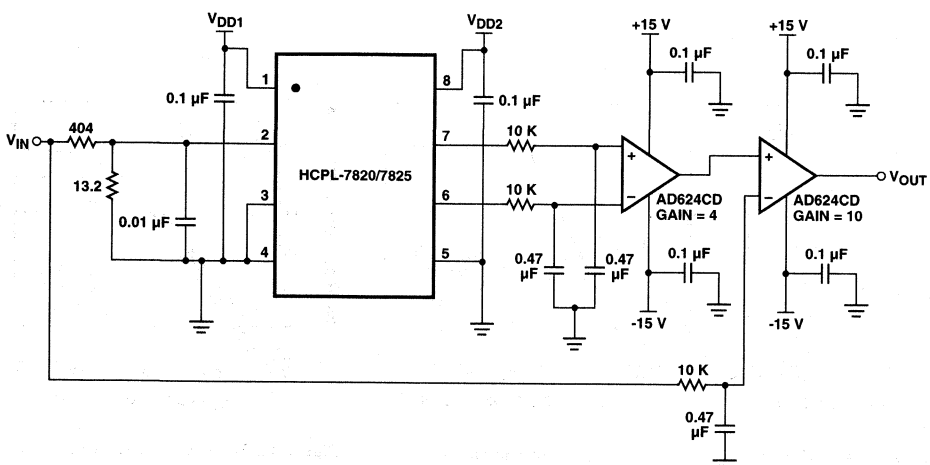


Figure 5. Gain and Nonlinearity Test Circuit.

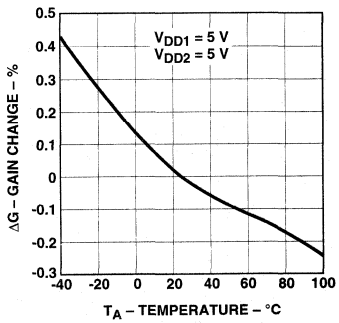


Figure 6. Gain Change vs. Temperature.

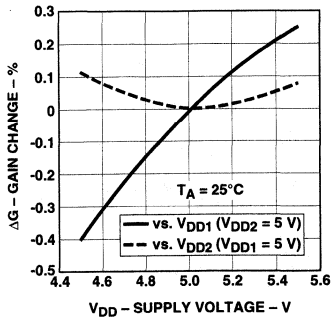


Figure 7. Gain Change vs. V_{DD1} and V_{DD2}.

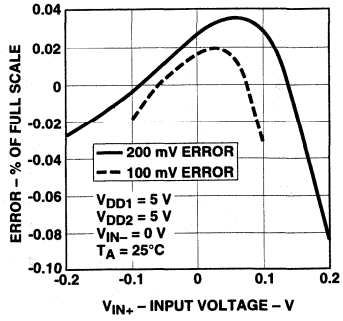


Figure 8. Nonlinearity Error Plot vs. Input Voltage.

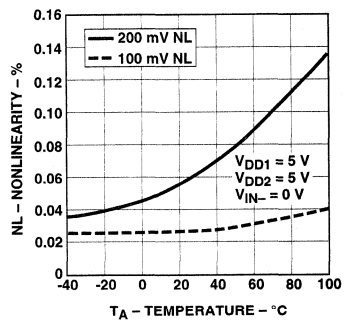


Figure 9. Nonlinearity vs. Temperature.

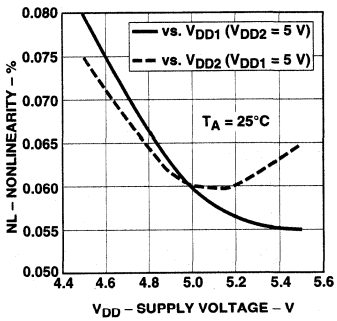


Figure 10. 200 mV Nonlinearity vs. V_{DD1} and V_{DD2}.

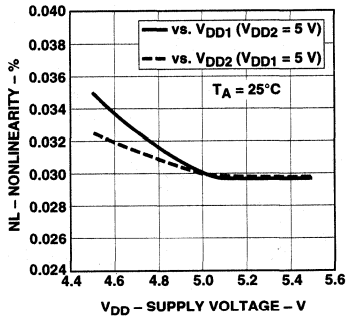


Figure 11. 100 mV Nonlinearity vs. V_{DD1} and V_{DD2}.

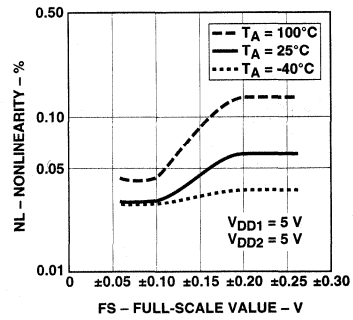


Figure 12. Nonlinearity vs. Full-Scale Value.

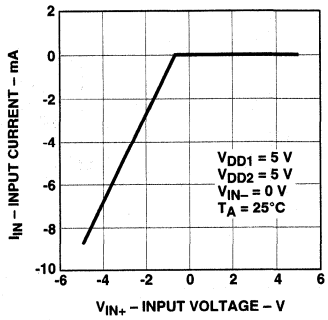


Figure 13. Input Current vs. Input Voltage.

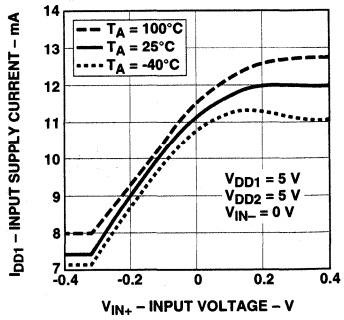


Figure 14. Input Supply Current vs. Input Voltage.

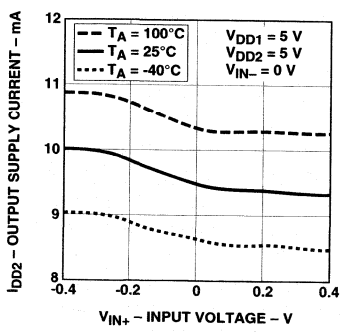


Figure 15. Output Supply Current vs. Input Voltage.

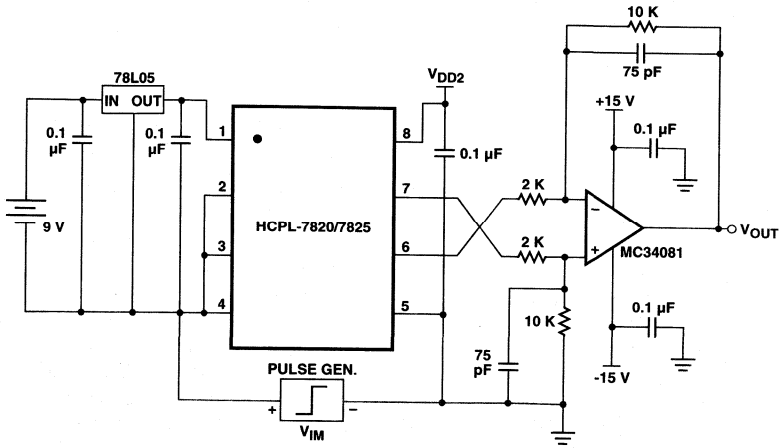


Figure 16. Isolation Mode Rejection Test Circuit.

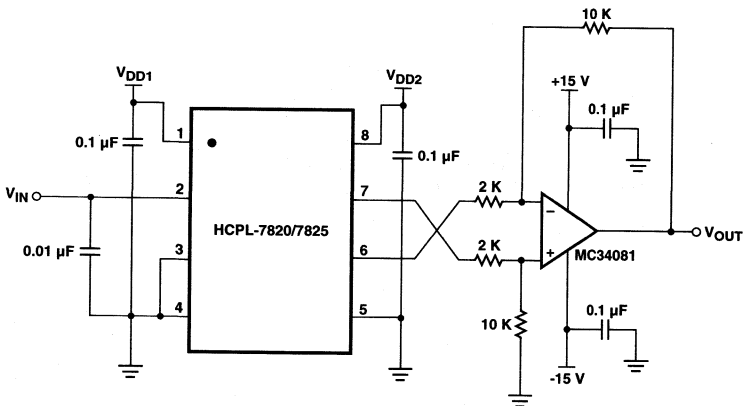


Figure 17. Propagation Delay, Rise/Fall Time and Bandwidth Test Circuit.

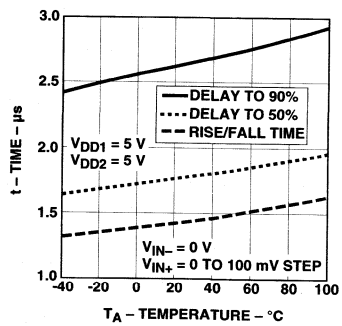


Figure 18. Propagation Delays and Rise/Fall Time vs. Temperature.

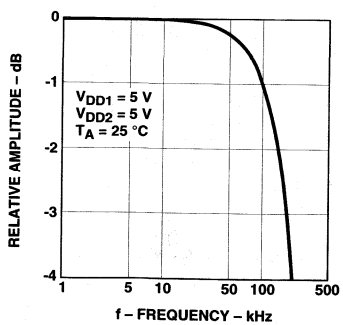


Figure 19. Amplitude Response vs. Frequency.

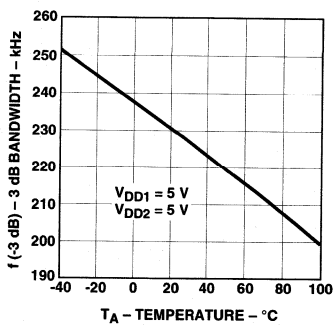


Figure 20. 3 dB Bandwidth vs. Temperature.

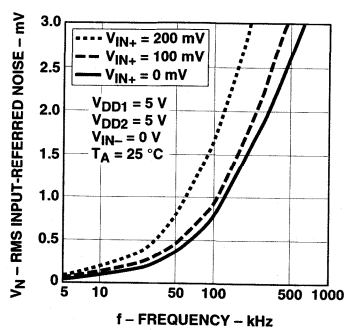


Figure 21. RMS Input-Referred Noise vs. Recommended Application Circuit Bandwidth.

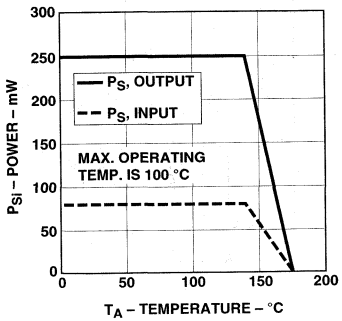


Figure 22. Dependence of Safety-Limiting Values on Temperature.

Applications Information

Functional Description

Figure 23 shows the primary functional blocks of the HCPL-7820/7825. In operation, the sigma-delta modulator converts the analog input signal into a high-speed serial bit stream. The time average of this bit stream is directly proportional to the input signal. This stream of digital data is encoded and optically transmitted to the detector circuit. The detected signal is decoded and converted back into an analog signal, which is filtered to obtain the final output signal.

Application Circuit

The recommended application circuit is shown in Figure 24. A floating power supply (which in many applications could be the same supply that is used to drive the high-side power transistor) is regulated to 5 V using a simple three-terminal voltage regulator (U1). The voltage from the current sensing resistor, or shunt (R_{SENSE}), is applied to the input of

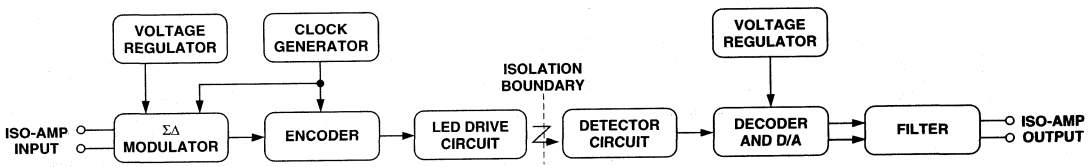


Figure 23. HCPL-7820/7825 Block Diagram.

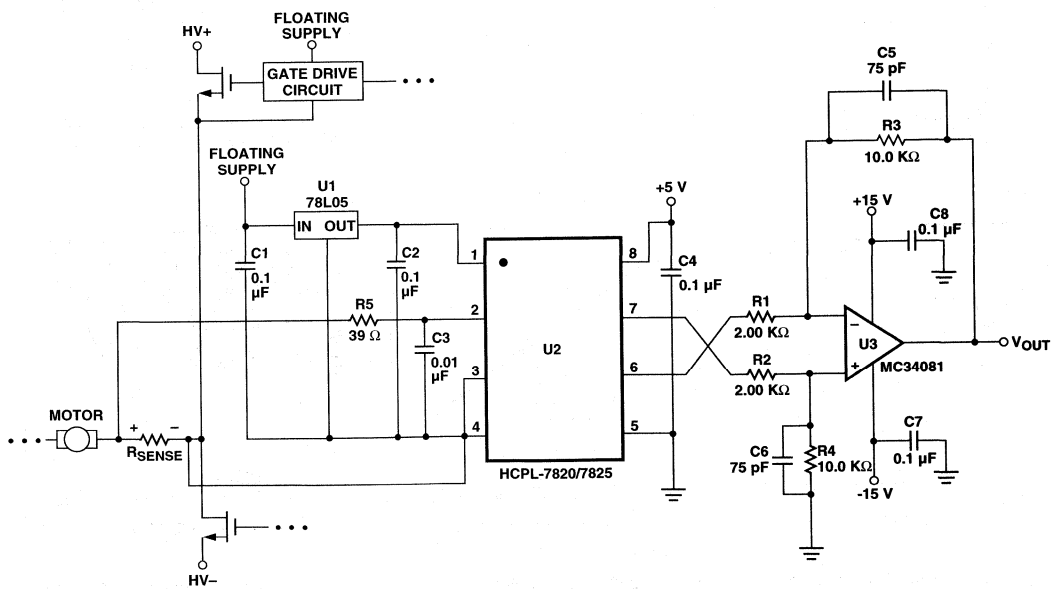


Figure 24. Recommended Application Circuit.

the HCPL-7820/7825 through an RC anti-aliasing filter (R5, C3). And finally, the differential output of the isolation amplifier is converted to a ground-referenced single-ended output voltage with a simple differential amplifier circuit (U3 and associated components). Although the application circuit is relatively simple, a few recommendations should be followed to ensure optimal performance.

Supplies and Bypassing

As mentioned above, an inexpensive 78L05 three-terminal regulator can be used to reduce the gate-drive power supply voltage to 5 V. To help attenuate high-frequency power supply noise or ripple, a resistor or inductor can be used in series with the input of the regulator to form a low-pass filter with the regulator's input bypass capacitor.

As shown in Figure 24, 0.1 μF bypass capacitors (C2, C4) should be located as close as possible to the input and output power supply pins of the HCPL-7820/7825. The bypass capacitors are required because of the high-speed digital nature of the signals inside the isolation amplifier. A 0.01 μF bypass capacitor (C3) is also recommended at the input pin(s) due to the switched-capacitor nature of the input circuit. The input bypass capacitor should be at least 1000 pF to maintain gain accuracy of the isolation amplifier. Inductive coupling between the input power-supply bypass capacitor and the input circuit, which includes the input bypass capacitor and the input leads of the HCPL-7820/7825, can introduce additional DC offset in the circuit. Several steps can be taken to minimize the mutual coupling between the two parts of the circuit, thereby improving the offset performance of the design. Separate the two bypass capacitors C2 and C3 as much as possible (even putting them on opposite sides of the PC board), while keeping the total lead lengths, including traces, of each bypass capacitor less than 20 mm. PC board traces should be made as short as possible and placed close together or over ground plane to minimize loop area and pickup of stray magnetic fields. Avoid using sockets, as they will typically increase both loop area and inductance. And finally, using capacitors with small body size and orienting them perpendicular to each other on the PC board can also help. For more information concerning inductive coupling, see the Application Note *Designing with Hewlett-Packard Isolation Amplifiers.*

Shunt Resistor Selection

The current-sensing shunt resistor should have low resistance (to minimize power dissipation), low inductance (to minimize di/dt induced voltage spikes which could adversely affect operation), and reasonable tolerance (to maintain overall circuit accuracy). The value of the shunt should be chosen as a compromise between minimizing power dissipation by making the shunt resistance smaller and improving circuit accuracy by making it larger and using more of the input range of the HCPL-7820/7825. Hewlett-Packard recommends 4 different shunts which can be used to sense average currents in motor drives up to 35 A and 35 hp. Table 1 shows the maximum current and horsepower range for each of the LVR-series shunts from Dale. Even higher currents can be sensed with lower value shunts available from vendors such as Dale, IRC, and Isotek (Isabellenhuette). When sensing currents large enough to cause significant heating of the shunt, the temperature coefficient of the shunt can introduce nonlinearity due to the amplitude dependent temperature rise of the shunt. Using a heat sink for the shunt or using a shunt with a lower tempco can help minimize this effect. The Application Note *Designing with Hewlett-Packard Isolation Amplifiers* contains additional information on designing with current shunts.

The recommended method for connecting the isolation amplifier to the shunt resistor is shown in

Table 1. Current Shunt Summary

Shunt Resistor Part Number	Shunt Resistance	Maximum Power Dissipation	Maximum RMS Current	Maximum Horsepower Range
LVR-3.05-1%	50 mΩ	3 W	3 A	0.8-3.0 hp
LVR-3.02-1%	20 mΩ	3 W	8 A	2.2-8.0 hp
LVR-3.01-1%	10 mΩ	3 W	15 A	4.1-15 hp
LVR-5.005-1%	5 mΩ	5 W	35 A	9.6-35 hp

Figure 24. Pin 2 (V_{IN+}) is connected to the positive terminal of the shunt resistor, while pin 3 (V_{IN-}) is shorted to pin 4 (GND1), with the power-supply return path functioning as the sense line to the negative terminal of the current shunt. This allows a single pair of wires or PC board traces to connect the isolation amplifier circuit to the shunt resistor. In some applications, however, supply currents flowing through the power-supply return path may cause offset or noise problems. In this case, better performance may be obtained by connecting pin 3 to the negative terminal of the shunt resistor separately from the power supply return path. When connected this way, both input pins should be bypassed. Whether two or three wires are used, it is recommended that twisted-pair wire or very close PC board traces be used to connect the current shunt to the isolation amplifier circuit to minimize electromagnetic interference to the sense signal.

The 39 Ω resistor in series with the input lead forms a low-pass anti-aliasing filter with the input bypass capacitor with a 400 kHz bandwidth. The resistor performs another important function as well; it dampens any ringing which might be present in the circuit formed by the shunt, the input bypass capacitor, and the wires or traces connecting the two. Undamped ringing of the input circuit near the input sampling frequency can alias into the baseband producing what might appear to be noise at the output of the device.

PC Board Layout

In addition to affecting offset, the layout of the PC board can also affect the common mode rejection (CMR) performance of the isolation amplifier, due primarily to stray capacitive coupling between the input and the output circuits. To obtain optimal CMR performance, the layout of the printed circuit board (PCB) should minimize any stray coupling by maintaining the maximum possible distance between the input and output sides of the circuit and ensuring that any ground plane on the PCB does not pass directly below or extend much wider than the HCPL-7820/7825. Using surface-mount components can help achieve many of the PCB objectives discussed in the preceding paragraphs. An example through-hole PCB layout illustrating some of the more important layout recommendations is shown in Figures 26 and 27. See the Application Note *Designing with Hewlett-Packard Isolation Amplifiers* for more information on PCB layout considerations.

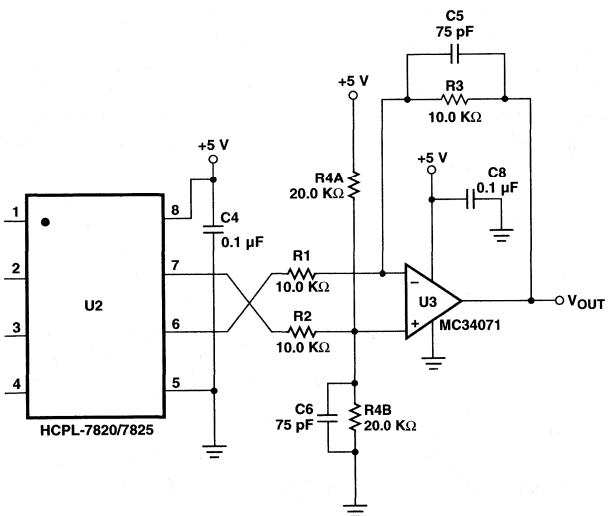


Figure 25. Single-Supply Post-Amplifier Circuit.

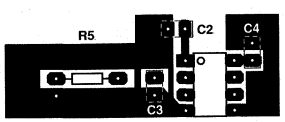


Figure 26. Top Layer of Printed Circuit Board Layout.

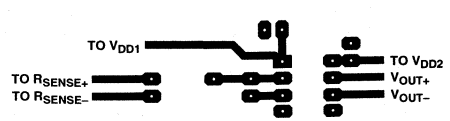


Figure 27. Bottom Layer of Printed Circuit Board Layout.

Post-Amplifier Circuit

The recommended application circuit (Figure 24) includes a post-amplifier circuit that serves three functions: to reference the output signal to the desired level (usually ground), to amplify the signal to appropriate levels, and to help filter output noise. The particular op-amp used in the post-amp is not critical; however, it should have low enough offset and high enough bandwidth and slew rate so that it does not adversely affect circuit performance. The offset of the op-amp should be low relative to the output offset of the HCPL-7820/7825, or less than about 5 mV.

To maintain overall circuit bandwidth, the post-amplifier circuit should have a bandwidth at least twice the minimum bandwidth of the isolation amplifier, or about 400 kHz. To obtain a bandwidth of 400 kHz with a gain of 5, the op-amp should have a gain-bandwidth greater than 2 MHz. The post-amplifier circuit includes a pair of capacitors (C5 and C6) that form a single-pole low-pass filter. These capacitors allow the bandwidth of the post-amp to be adjusted independently of the gain and are useful for reducing the output noise from the isolation amplifier (doubling the capacitor values halves the circuit bandwidth). The component values shown in Figure 24 form a differential amplifier with a gain of 5 and a cutoff frequency of approximately 200 kHz and were chosen as a compromise between low noise and fast response times. The overall recommended application circuit has a bandwidth of 130 kHz, a rise time of 2.6 µs and delay to 90% of 4.2 µs.

The gain-setting resistors in the post-amp should have a tolerance of 1% or better to ensure adequate CMRR and gain tolerance for the overall circuit. Resistor networks with even better ratio tolerances can be used which offer better performance, as well as reducing the total component count and board space.

The post-amplifier circuit can be easily modified to allow for single-supply operation. Figure 25 shows a schematic for a post-amplifier for use in 5 V single-supply applications. One additional resistor is needed and the gain is decreased to allow circuit operation over the full input voltage range. See the Application Note *Designing with Hewlett-Packard Isolation Amplifiers* for more information on the post-amplifier circuit.

Other Information

As mentioned above, reducing the bandwidth of the post amplifier circuit reduces the amount of output noise. Figure 21 shows how the output noise changes as a function of the post-amplifier bandwidth. The post-amplifier circuit exhibits a first-order low-pass filter characteristic. For the same filter bandwidth, a higher-order filter can achieve even better attenuation of modulation noise due to the second-order noise shaping of the sigma-delta modulator. For more information on the noise characteristics of the HCPL-7820/7825, see the Application Note *Designing with Hewlett-Packard Isolation Amplifiers.*

The HCPL-7820/7825 can also be used to isolate signals with amplitudes larger than its recommended input range with the use of a resistive voltage divider at its input. The only restrictions are that the impedance of the divider be relatively small (less than 1 kΩ) so that the input resistance (280 kΩ) and input bias current (1 µA) do not affect the accuracy of the measurement. An input bypass capacitor is still required, although the 39 Ω series damping resistor is not (the resistance of the voltage divider provides the same function). The low-pass filter formed by the divider resistance and the input bypass capacitor may limit the achievable bandwidth.

HEWLETT® PACKARD

Analog Isolation Amplifier

Technical Data

HCPL-7840

Features

- **High Common Mode Rejection (CMR): 15 kV/µs at V_{CM} = 1000 V**
- **5% Gain Tolerance**
- **0.1% Nonlinearity**
- **Low Offset Voltage and Offset Temperature Coefficient**
- **100 kHz Bandwidth**
- **Performance Specified Over -40°C to 85°C Temperature Range**
- **Recognized Under UL 1577 and CSA Approved for Dielectric Withstand Proof Test Voltage of 2500 Vac, 1 Minute**
- **Standard 8-Pin DIP Package**

Applications

- **Motor Phase and Rail Current Sensing**
- **Inverter Current Sensing**
- **Switched Mode Power Supply Signal Isolation**
- **General Purpose Current Sensing and Monitoring**
- **General Purpose Analog Signal Isolation**

Description

The HCPL-7840 isolation amplifier provides accurate, electrically isolated and amplified representations of voltage and current.

When used with a shunt resistor in the current path, the HCPL-7840 offers superior reliability, cost effectiveness, size and autoinsertability compared with the traditional solutions such as current transformers and Hall-effect sensors.

The HCPL-7840 consists of a sigma-delta analog-to-digital converter optically coupled to a digital-to-analog converter. Superior performance in design critical specifications such as common-mode rejection, offset voltage, nonlinearity, operating temperature range and regulatory compliance make the HCPL-7840 the clear choice for designing reliable, lower-cost, reduced-size products such as motor controllers and inverters.

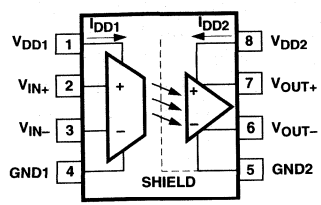
Common-mode rejection of 15 kV/µs makes the HCPL-7840 suitable for noisy electrical environments such as those generated by the high switching rates of power IGBTs.

Low offset voltage together with a low offset voltage temperature coefficient permits accurate use of auto-calibration techniques.

Gain tolerance of 5% with 0.1% nonlinearity further provide the performance necessary for accurate feedback and control.

A wide operating temperature range with specified performance allows the HCPL-7840 to be used in hostile industrial environments.

Functional Diagram



A 0.1 F bypass capacitor must be connected between pins 1 and 4 and between pins 5 and 8.

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

5965-4784E

Ordering Information

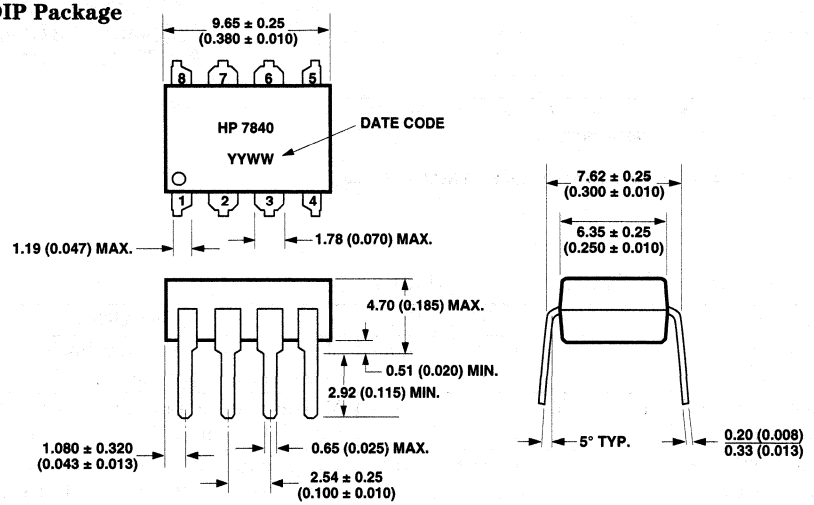
HCPL-7840#xxx

No option = Standard DIP Package, 50 per tube
300 = Gull Wing Surface Mount Lead Option, 50 per tube
500 = Tape/Reel Package Option (1 K min.), 1000 per reel

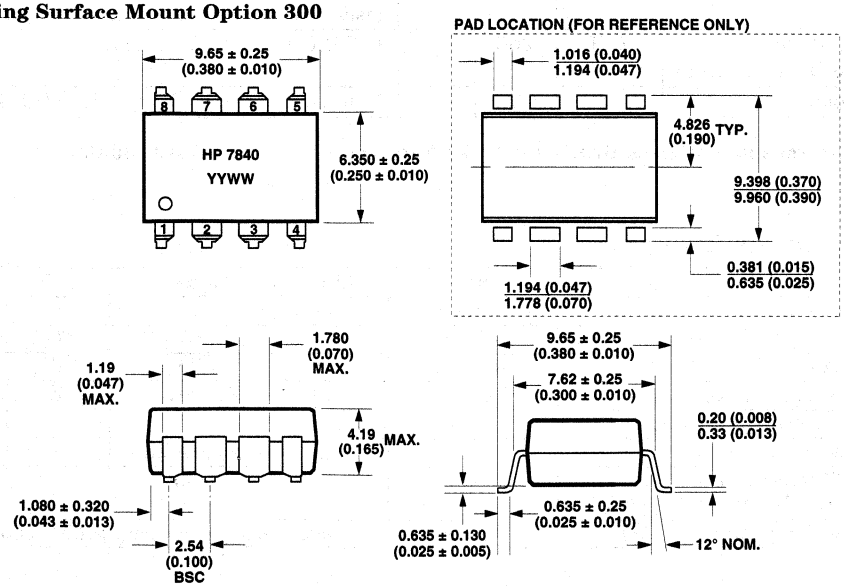
Option data sheets available. Contact your Hewlett-Packard sales representative or authorized distributor for more information.

Package Outline Drawings

Standard DIP Package



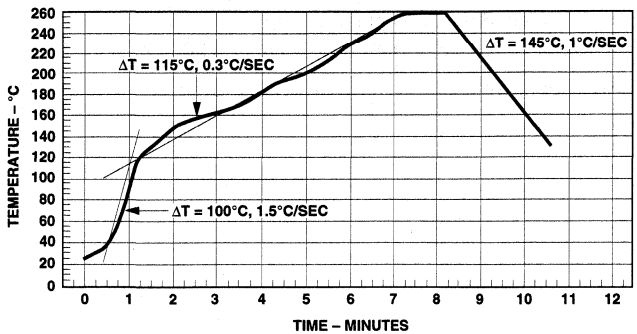
Gull Wing Surface Mount Option 300



DIMENSIONS IN MILLIMETERS (INCHES).
TOLERANCES (UNLESS OTHERWISE SPECIFIED): xx.xx = 0.01
xx.xxx = 0.005

LEAD COPLANARITY
MAXIMUM: 0.102 (0.004)

Maximum Solder Reflow Thermal Profile



(NOTE: USE OF NON-CHLORINE ACTIVATED FLUXES IS RECOMMENDED.)

Regulatory Information

The HCPL-7840 has been approved by the following organizations:

UL Recognized under UL 1577, Component Recognition Program, File E55361.

CSA Approved under CSA Component Acceptance Notice #5, File CA 88324.

Insulation and Safety Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min. External Air Gap (External Clearance)	L(IO1)	7.1	mm	Measured from input terminals to output terminals, shortest distance through air.
Min. External Tracking Path (External Creepage)	L(IO2)	7.4	mm	Measured from input terminals to output terminals, shortest distance path along body.
Min. Internal Plastic Gap (Internal Clearance)		0.08	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity.
Tracking Resistance (Comparative Tracking Index)	CTI	200	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Option 300 - surface mount classification is Class A in accordance with CECC 00802.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Note
Storage Temperature	T_S	-55	125	°C	
Ambient Operating Temperature	T_A	-40	85	°C	
Supply Voltages	V_{DD1}, V_{DD2}	0.0	5.5	V	
Steady-State Input Voltage	V_{IN+}, V_{IN-}	-2.0	V_{DD1} +0.5	V	1
2 Second Transient Input Voltage		-6.0			
Output Voltages	V_{OUT+}, V_{OUT-}	-0.5	V_{DD2} +0.5	V	
Lead Solder Temperature (10 sec., 1.6 mm below seating plane)	T_{LS}		260	°C	
Solder Reflow Temperature Profile	See Maximum Solder Reflow Thermal Profile Section				

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit	Note
Ambient Operating Temperature	T_A	-40	85	°C	
Supply Voltages	V_{DD1}, V_{DD2}	4.5	5.5	V	
Input Voltage	V_{IN+},V_{IN-}	-200	200	mV	1

DC Electrical Specifications

All specifications, typicals and figures are at the nominal operating conditions of V_{IN+} = 0 V, V_{IN-} = 0 V, T_A = 25°C, V_{DD1} = 5 V and V_{DD2} = 5 V, unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Note
Input Offset Voltage	V_{OS}	-1.2	-0.2	1.0	mV		1	2
		-3.0	-0.2	2.0		-40°C ≤ T_A ≤ 85°C 4.5 ≤ (V_{DD1}, V_{DD2}) ≤ 5.5 V	1,2,3	
Gain	G	7.60	8.00	8.40	V/V	-200 ≤ V_{IN+} ≤ 200 mV	5	
		7.44	8.00	8.56		-200 ≤ V_{IN+} ≤ 200 mV -40°C ≤ T_A ≤ 85°C 4.5 ≤ (V_{DD1}, V_{DD2}) ≤ 5.5 V	5,6,7	
200 mV Nonlinearity	NL_{200}		0.1	0.2	%	-200 ≤ V_{IN+} ≤ 200 mV	5, 8	3
				0.4		-200 ≤ V_{IN+} ≤ 200 mV -40°C ≤ T_A ≤ 85°C 4.5 ≤ (V_{DD1}, V_{DD2}) ≤ 5.5 V	5,8,9 10,12	
100 mV Nonlinearity	NL_{100}		0.05	0.1		-100 ≤ V_{IN+} ≤ 100 mV	5, 8	
				0.2		-100 ≤ V_{IN+} ≤ 100 mV -40°C ≤ T_A ≤ 85°C 4.5 ≤ (V_{DD1}, V_{DD2}) ≤ 5.5 V	5,8,9 11,12	
Maximum Input Voltage Before Output Clipping	$\lvert V_{IN+} \rvert_{MAX}$		320		mV		4	
Average Input Bias Current	I_{IN}		-0.57		µA		13	4
Average Input Resistance	R_{IN}		480		kΩ			
Input DC Common-Mode Rejection Ratio	$CMRR_{IN}$		69		dB			5
Output Resistance	R_O		1		Ω			
Output Low Voltage	V_{OL}		1.28		V	V_{IN+} = 400 mV	4	6
Output High Voltage	V_{OH}		3.84		V	V_{IN+} = -400 mV		
Output Common-Mode Voltage	V_{OCM}	2.20	2.56	2.80	V	-400 < V_{IN+} < 400 mV -40°C ≤ T_A ≤ 85°C		
Input Supply Current	I_{DD1}		8.7	15.5	mA	4.5 ≤ (V_{DD1}, V_{DD2}) ≤ 5.5 V	14	
Output Supply Current	I_{DD2}		8.8	14.5	mA		15	
Output Short-Circuit Current	$\lvert I_{OSC} \rvert$		11		mA	V_{OUT} = 0 V or V_{DD2}		7

AC Electrical Specifications

All specifications, typicals and figures are at the nominal operating conditions of V_{IN+} = 0 V, V_{IN-} = 0 V, T_A = 25°C, V_{DD1} = 5 V and V_{DD2} = 5 V, unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Note
Common Mode Rejection	CMR	10	15		kV/µs	V_{CM} = 1 kV 4.5 ≤ (V_{DD1}, V_{DD2}) ≤ 5.5 V	16	8
Common Mode Rejection Ratio at 60 Hz	CMRR		>140		dB			9
Propagation Delay to 50%	t_{PD50}		3.7	6.5	µs	V_{IN+} = 0 to 100 mV step -40°C ≤ T_A ≤ 85°C 4.5 ≤ (V_{DD1}, V_{DD2}) ≤ 5.5 V	17,18	
Propagation Delay to 90%	t_{PD90}		5.7	9.9				
Rise/Fall Time (10-90%)	$t_{R/F}$		3.4	6.6				
Small-Signal Bandwidth (-3 dB)	$f_{-3\ dB}$	50	100		kHz	-40°C ≤ T_A ≤ 85°C 4.5 ≤ (V_{DD1}, V_{DD2}) ≤ 5.5 V	17, 19, 20	
Small-Signal Bandwidth (-45°)	$f_{-45°}$		33					
RMS Input-Referred Noise	V_N		0.6		mV_{rms}	In recommended application circuit	21, 23	10
Power Supply Rejection	PSR		570		mV_{P-P}			11

Package Characteristics

All specifications, typicals and figures are at the nominal operating conditions of V_{IN+} = 0 V, V_{IN-} = 0 V, T_A = 25°C, V_{DD1} = 5 V and V_{DD2} = 5 V, unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage*	V_{ISO}	2500			V_{rms}	t = 1 min., RH ≤ 50%		12,13
Input-Output Resistance	R_{I-O}		10^{12}		Ω	V_{I-O} = 500 Vdc		13
Input-Output Capacitance	C_{I-O}		0.6		pF	f = 1 MHz V_{I-O} = 0 Vdc		

*The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating, refer to the VDE 0884 Insulation Characteristics Table (if applicable), your equipment level safety specification, or HP Application Note 1074, "Optocoupler Input-Output Endurance Voltage."

Notes:

1. If V_{IN-} is brought above V_{DD1} - 2 V with respect to GND1 an internal test mode may be activated. This test mode is not intended for customer use.
2. Exact offset value is dependent on layout of external bypass capacitors. The offset value in the data sheet corresponds to HP's recommended layout (see Figures 25 and 26).
3. Nonlinearity is defined as half of the peak-to-peak output deviation from the best-fit gain line, expressed as a percentage of the full-scale differential output voltage.
4. Because of the switched capacitor nature of the sigma-delta A/D converter, time-averaged values are shown.
5. $CMRR_{IN}$ is defined as the ratio of the gain for differential inputs applied between pins 2 and 3 to the gain for common mode inputs applied to both pins 2 and 3 with respect to pin 4.
6. When the differential input signal exceeds approximately 320 mV, the outputs will limit at the typical values shown.
7. Short-circuit current is the amount of output current generated when either output is shorted to V_{DD2} or ground. HP does not recommend operation under these conditions.
8. CMR (also known as IMR or Isolation Mode Rejection) specifies the minimum rate of rise of a common mode noise signal applied across the isolation boundary at which small output perturbations begin to appear. These output perturbations can occur with both the rising and falling edges of the common mode waveform and may be of either polarity. A CMR failure is defined as a perturbation exceeding 200 mV at the output of the recommended application circuit (Figure 23). See applications section for more information on CMR.
9. CMRR is defined as the ratio of differential signal gain (signal applied differentially between pins 2 and 3) to the common mode gain (input pins tied to pin 4 and the signal applied between the input and the output of the isolation amplifier) at 60 Hz, expressed in dB.
10. Output noise comes from two primary sources: chopper noise and sigma-delta quantization noise. Chopper noise results from chopper stabilization of the output op-amps. It occurs at a specific frequency (typically 500 kHz) and is not attenuated by the on-chip output filter. The on-chip filter does eliminate most, but not all, of the sigma-delta quantization noise. An external filter circuit may be easily added to the external post-amplifier to reduce the total RMS output noise. See applications section for more information.
11. Data sheet value is the amplitude of the transient at the differential output of the HCPL-7840 when a 1 V_{P-P}, 1 MHz square wave with 100 ns rise and fall times (measured at pins 1 and 8) is applied to both V_{DD1} and V_{DD2}.
12. In accordance with UL1577, each isolation amplifer is proof tested by applying an insulation test voltage ≥ 3000 V_{RMS} for 1 second (leakage current detection limit $I_{I-O} \leq 5\ \mu A$).
13. Device considered a two terminal device: Pins 1, 2, 3 and 4 connected together; pins 5, 6, 7 and 8 connected together.

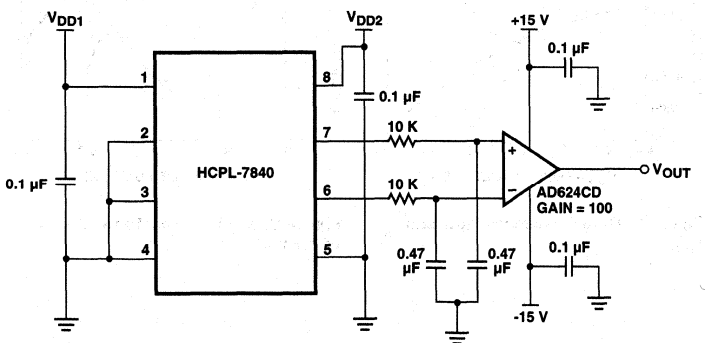


Figure 1. Input Offset Voltage Test Circuit.

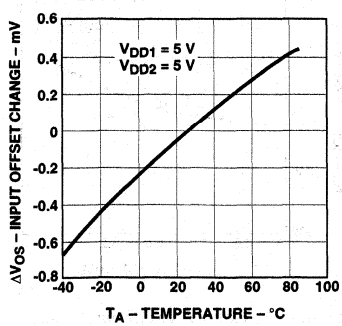


Figure 2. Input Offset Change vs. Temperature.

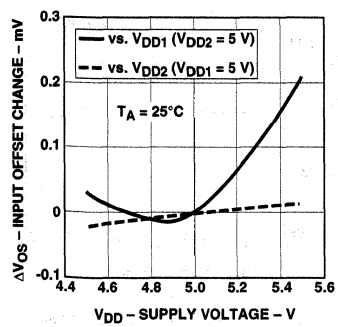


Figure 3. Input Offset Change vs. V_{DD1} and V_{DD2}.

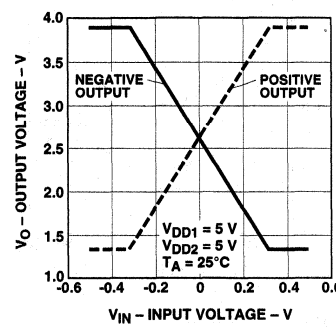


Figure 4. Output Voltages vs. Input Voltage.

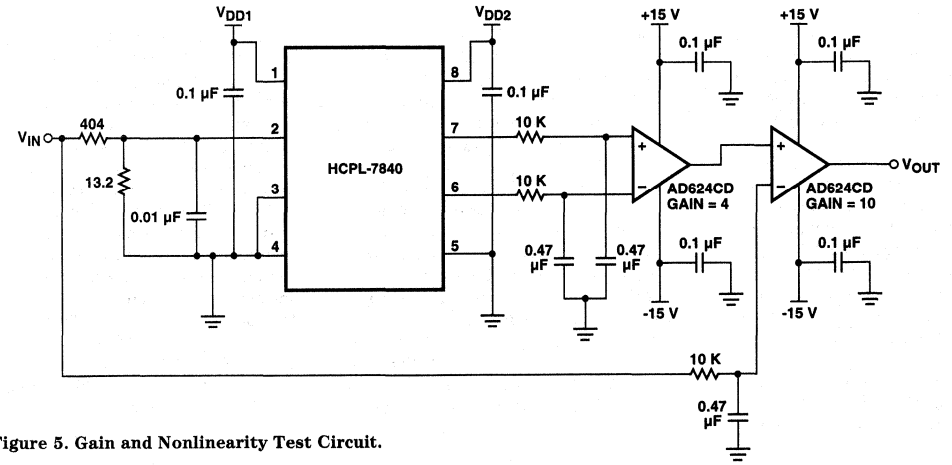


Figure 5. Gain and Nonlinearity Test Circuit.

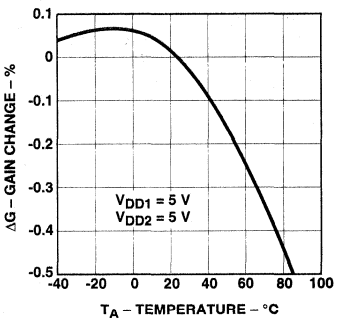


Figure 6. Gain Change vs. Temperature.

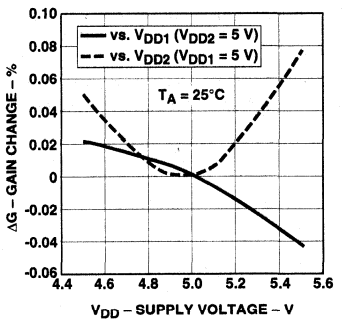


Figure 7. Gain Change vs. V_{DD1} and V_{DD2}.

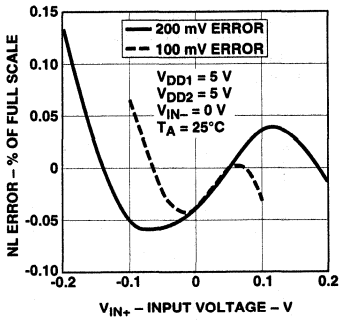


Figure 8. Nonlinearity Error Plot vs. Input Voltage.

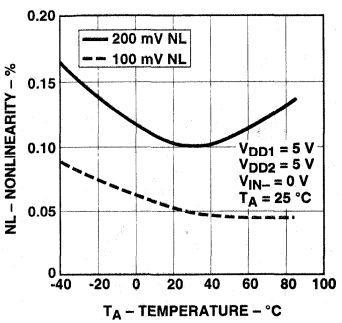
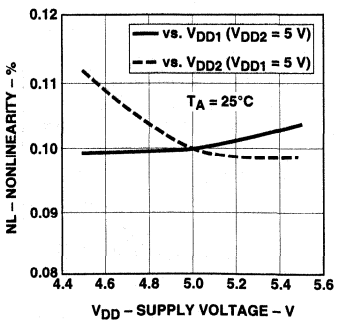


Figure 9. Nonlinearity vs. Temperature.



Fibure 10. 200 mV Nonlinearity vs. V_{DD1} and V_{DD2}.

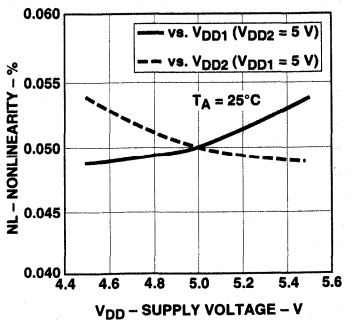


Figure 11. 100 mV Nonlinearity vs. V_{DD1} and V_{DD2}.

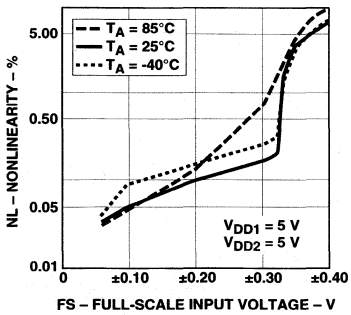


Figure 12. Nonlinearity vs. Full-Scale Input Voltage.

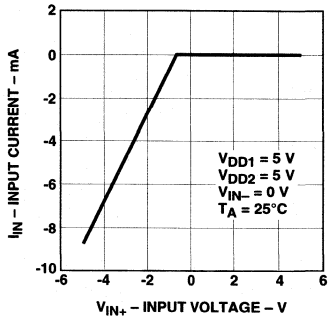


Figure 13. Input Current vs. Input Voltage.

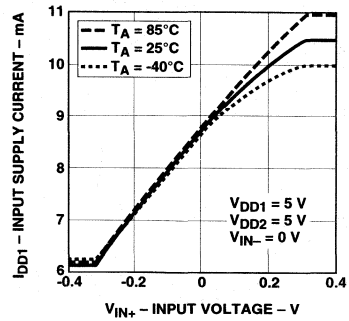


Figure 14. Input Supply Current vs. Input Voltage.

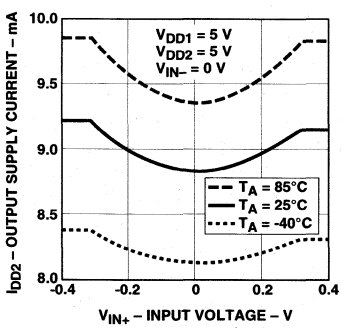


Figure 15. Output Supply Current vs. Input Voltage.

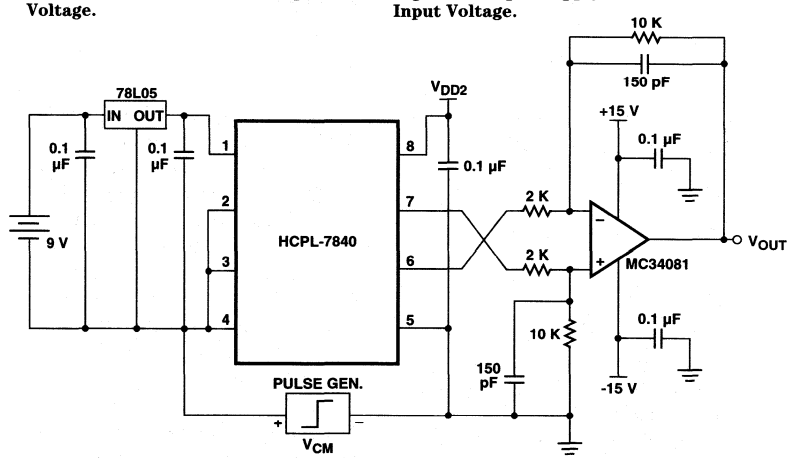
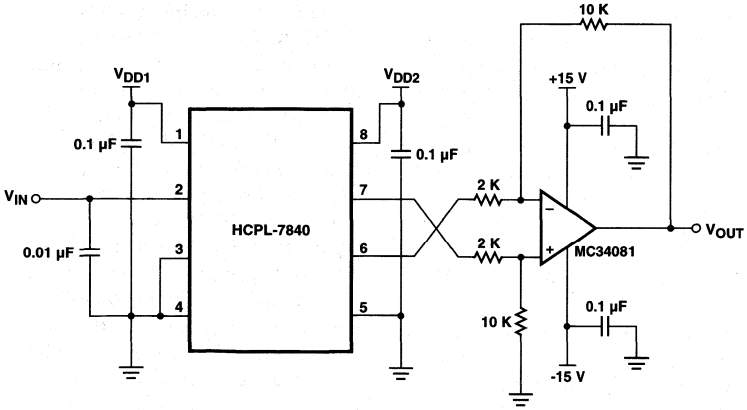


Figure 16. Common Mode Rejection Test Circuit.



V_{IN} IMPEDANCE LESS THAN 10 Ω.

Figure 17. Propagation Delay, Rise/Fall Time and Bandwidth Test Circuit.

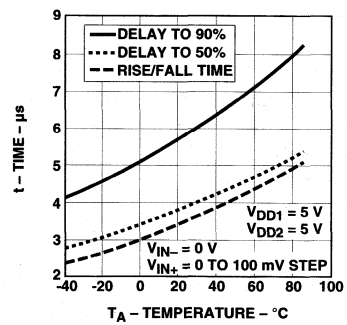


Figure 18. Propagation Delays and Rise/Fall Time vs. Temperature.

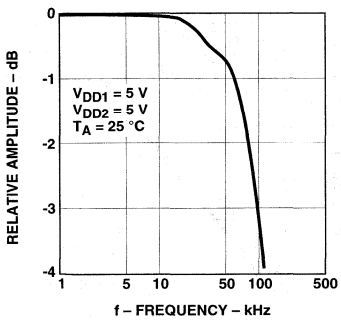


Figure 19. Amplitude Response vs. Frequency.

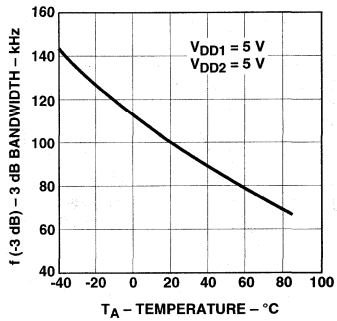


Figure 20. 3 dB Bandwidth vs. Temperature

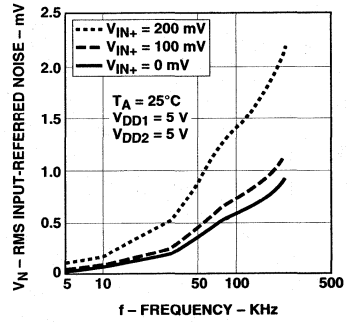


Figure 21. RMS Input-Referred Noise vs. Recommended Application Circuit Bandwidth.

Applications Information

Functional Description

Figure 22 shows the primary functional blocks of the HCPL-7840. In operation, the sigma-delta modulator converts the analog input signal into a high-speed serial bit stream. The time average of this bit stream is directly proportional to the input signal. This stream of digital data is encoded and optically transmitted to the detector circuit. The detected signal is decoded and converted back into an analog signal, which is filtered to obtain the final output signal.

Application Circuit

The recommended application circuit is shown in Figure 23. A floating power supply (which in many applications could be the same supply that is used to drive the high-side power transistor) is regulated to 5 V using a simple three-terminal voltage regulator (U1). The voltage from the current sensing resistor, or shunt (Rsense), is applied to the input of the HCPL-7840 through an RC anti-aliasing filter (R5, C3). And finally, the differential output of the isolation amplifier is converted to a ground-referenced single-ended output voltage with a simple differential amplifier circuit (U3 and associated components). Although the application circuit is relatively simple, a few recommendations should be followed to ensure optimal performance.

Supplies and Bypassing

As mentioned above, an inexpensive 78L05 three-terminal regulator can be used to reduce the gate-drive power supply voltage to 5 V. To help attenuate high frequency power supply noise or ripple, a resistor or inductor can be used in series with the input of the regulator to form a low-pass filter with the regulator's input bypass capacitor.

As shown in Figure 23, 0.1 µF bypass capacitors (C2, C4) should be located as close as possible to the input and output power supply pins of the HCPL-7840. The bypass capacitors are required because of the high-speed digital nature of the signals inside the isolation amplifier. A 0.01 µF bypass capacitor (C3) is also recommended at the input pin(s) due to the switched-capacitor nature of the input circuit. The input bypass capacitor should be at least 1000 pF to maintain gain accuracy of the isolation amplifier.

Inductive coupling between the input power-supply bypass capacitor and the input circuit, including the input bypass capacitor and the input leads of the HCPL-7840, can introduce additional DC offset in the circuit. Several steps can be taken to minimize the mutual coupling between the two parts of the circuit, thereby improving the offset performance of the design. Separate the two bypass capacitors C2 and C3 as much as possible (even putting them on opposite sides of the PC board), while keeping the total lead lengths, including traces, of each bypass capacitor less than 20 mm. PC board traces should be made as short as possible and

placed close together or over ground plane to minimize loop area and pickup of stray magnetic fields. Avoid using sockets, as they will typically increase both loop area and inductance. And finally, using capacitors with small body size and orienting them perpendicular to each other on the PC board can also help. For more information concerning this effect, see Application Note 1078, *Designing with Hewlett-Packard Isolation Amplifiers*.

Shunt Resistor Selection

The current-sensing shunt resistor should have low resistance (to minimize power dissipation), low inductance (to minimize di/dt induced voltage spikes which could adversely affect operation), and reasonable tolerance (to maintain overall circuit accuracy). The value of the shunt should be chosen as a compromise between minimizing power dissipation by making the shunt resistance smaller and improving circuit accuracy by making it larger and utilizing the full input range of the HCPL-7840. Hewlett-Packard recommends four different shunts which can be used to sense average currents in motor drives up to 35 A and 35 hp. Table 1 shows the maximum current and horsepower range for each of the LVR-series shunts from Dale. Even higher currents can be sensed with lower value shunts available from vendors such as Dale, IRC, and Isotek (Isabellenhuette). When sensing currents large enough to cause significant heating of the shunt, the temperature coefficient of the shunt can introduce nonlinearity due to the signal dependent temperature rise of the shunt. Using a heat sink for the shunt or using a shunt with a lower tempco can help minimize this effect. The Application Note 1078, *Designing with Hewlett-Packard Isolation Amplifiers*, contains additional information on designing with current shunts.

The recommended method for connecting the isolation amplifier to the shunt resistor is shown in Figure 23. Pin 2 (V_{IN+}) is connected to the positive terminal of the shunt resistor, while pin 3 (V_{IN-}) is shorted to pin 4 (GND1), with the power-supply return path functioning as the sense line to the negative terminal of the current shunt. This allows a single pair of wires or PC board traces to connect the isolation amplifier circuit to the shunt resistor. In some applications, however, supply currents flowing through the power-supply return path may cause offset or noise problems. In this case, better performance may be obtained by connecting pin 3 to the negative terminal of the shunt resistor separate from the power supply return path. When connected this way, both input pins should be bypassed. Whether two or three wires are used, it is recommended that twisted-pair wire or very close PC board traces be used to connect the current shunt to the isolation amplifier circuit to minimize electromagnetic interference to the sense signal.

The 68 Ω resistor in series with the input lead forms a low-pass anti-aliasing filter with the input bypass capacitor with a 200 kHz bandwidth. The resistor performs another important function as well; it dampens any ringing which might be present in the circuit formed by the shunt, the input bypass capacitor, and the wires or traces connecting the two. Undamped ringing of the input circuit near the input sampling frequency can alias into the baseband producing what might appear to be noise at the output of the device. To be effective, the damping resistor should be at least 39 Ω.

PC Board Layout

In addition to affecting offset, the layout of the PC board can also affect the common mode rejection (CMR) performance of the isolation amplifier, due primarily to stray capacitive coupling between the input and the output circuits. To obtain optimal CMR performance, the layout of the printed circuit board (PCB) should minimize any stray coupling by maintaining the maximum possible distance between the input and output sides of the circuit and ensuring that any ground plane on the PCB does not pass directly below the HCPL-7840. Using surface mount components can help achieve many of the PCB objectives discussed in the preceding paragraphs. An example through-hole PCB layout illustrating some of the more important layout recommendations is shown in Figures 25 and 26. See Application Note 1078, *Designing with Hewlett-Packard Isolation Amplifiers*, for more information on PCB layout considerations.

Post-Amplifier Circuit

The recommended application circuit (Figure 23) includes a post-amplifier circuit that serves three functions: to reference the output signal to the desired level (usually ground), to amplify the signal to appropriate levels, and

to help filter output noise. The particular op-amp used in the post-amp is not critical; however, it should have low enough offset and high enough bandwidth and slew rate so that it does not adversely affect circuit performance. The offset of the op-amp should be low relative to the output offset of the HCPL-7840, or less than about 5 mV.

To maintain overall circuit bandwidth, the post-amplifier circuit should have a bandwidth at least twice the minimum bandwidth of the isolation amplifier, or about 200 kHz. To obtain a bandwidth of 200 kHz with a gain of 5, the op-amp should have a gain-bandwidth greater than 1 MHz. The post-amplifier circuit includes a pair of capacitors (C5 and C6) that form a single-pole low-pass filter. These capacitors allow the bandwidth of the post-amp to be adjusted independently of the gain and are useful for reducing the output noise from the isolation amplifier (doubling the capacitor values halves the circuit bandwidth). The component values shown in Figure 23 form a differential amplifier with a gain of 5 and a cutoff frequency of approximately 100 kHz and were chosen as a compromise between low noise and fast response times. The overall recommended application circuit has a bandwidth of 66 kHz, a rise time of 5.2 µs and delay to 90% of 8.5 µs.

The gain-setting resistors in the post-amp should have a tolerance of 1% or better to ensure adequate CMRR and gain tolerance for the overall circuit. Resistor networks with even better ratio tolerances can be used which offer better performance, as well as reducing the total component count and board space.

The post-amplifier circuit can be easily modified to allow for single-supply operation. Figure 24 shows a schematic for a post amplifier for use in 5 V single supply applications. One additional resistor is needed and the gain is decreased to 1 to allow circuit operation over the full input voltage range. See Application Note 1078, *Designing with Hewlett-Packard Isolation Amplifiers*, for more information on the post-amplifier circuit.

Other Information

As mentioned above, reducing the bandwidth of the post amplifier circuit reduces the amount of output noise. Figure 21 shows how the output noise changes as a function of the post-amplifier bandwidth. The post-amplifier circuit exhibits a first-order low-pass filter characteristic. For the same filter bandwidth, a higher-order filter can achieve even better attenuation of modulation noise due to the second-order noise shaping of the sigma-delta modulator. For more information on the noise characteristics of the HCPL-7840, see Application Note 1078, *Designing with Hewlett-Packard Isolation Amplifiers*.

The HCPL-7840 can also be used to isolate signals with amplitudes larger than its recommended input range through the use of a resistive voltage divider at its input. The only restrictions are that the impedance of the divider be relatively small (less than 1 KΩ so that the input resistance (480 KΩ) and input bias current (0.6 A) do not affect the accuracy of the measurement. An input bypass capacitor is still required, although the 68 Ω series damping resistor is not (the resistance of the voltage divider provides the same function). The low pass filter formed by the divider resistance and the input bypass capacitor may limit the achievable bandwidth.

Table 1. Current Shunt Summary

Shunt Resistor Part Number	Shunt Resistance	Maximum Power Dissipation	Maximum Average Current	Maximum Horsepower Range
LVR-3.05-1%	50 mΩ	3 W	3 A	0.8-3.0 hp
LVR-3.02-1%	20 mΩ	3 W	8 A	2.2-8.0 hp
LVR-3.01-1%	10 mΩ	3 W	15 A	4.1-15 hp
LVR-5.005-1%	5 mΩ	5 W	35 A	9.6-35 hp

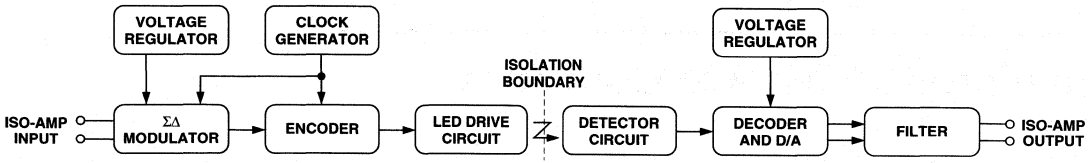


Figure 22. HCPL-7840 Block Diagram.

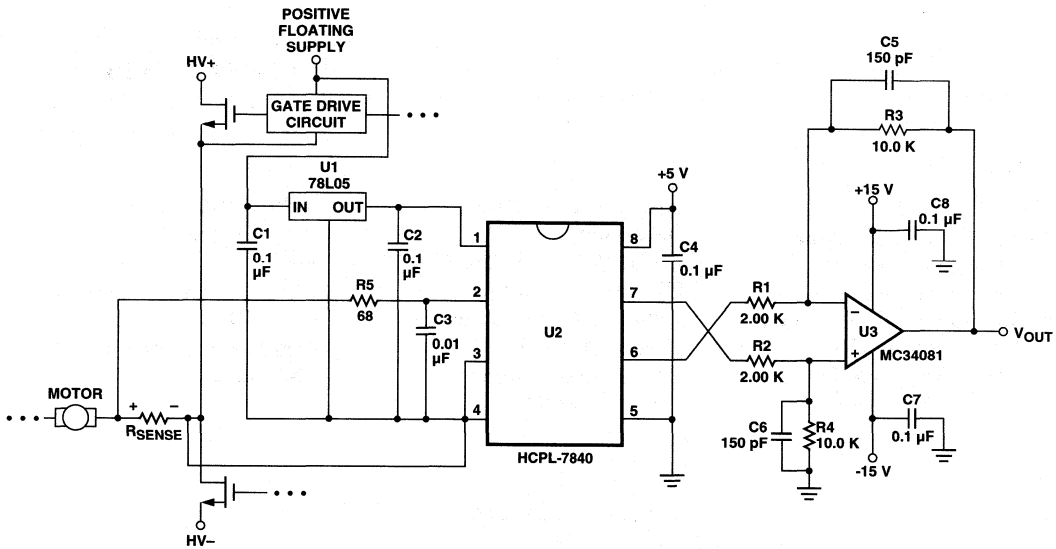


Figure 23. Recommended Application Circuit.

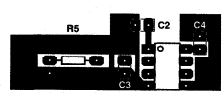


Figure 25. Top Layer of Printed Circuit Board Layout.

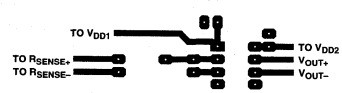


Figure 26. Bottom Layer of Printed Circuit Board Layout.

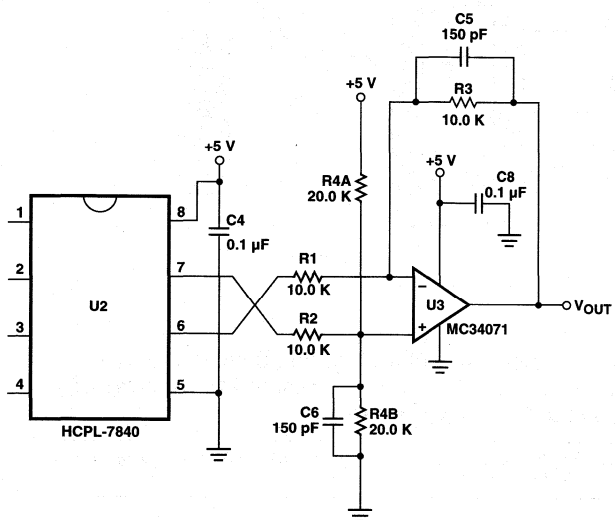


Figure 24. Single-Supply Post-Amplifier Circuit.

HEWLETT® PACKARD

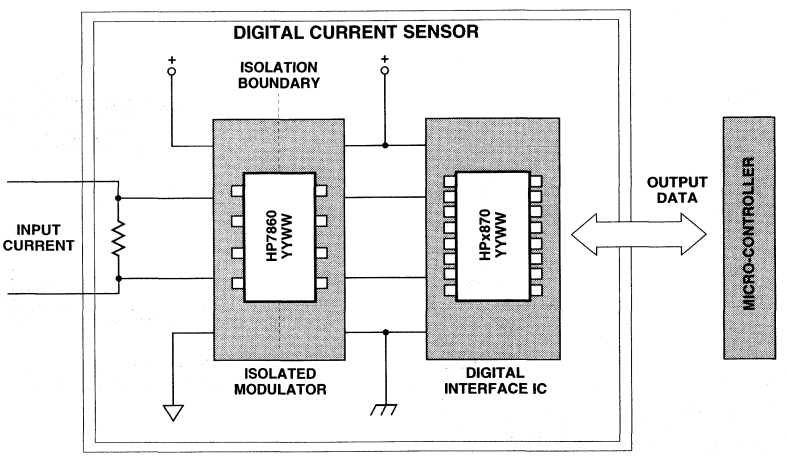
Isolated 15-bit A/D Converter

Technical Data

HCPL-7860
HCPL-0870, -7870

Features

- **12-bit Linearity**
- **700 ns Conversion Time (Pre-Trigger Mode 2)**
- **5 Conversion Modes for Resolution/Speed Trade-Off; 12-bit Effective Resolution with 18 µs Signal Delay (14-bit with 94 µs)**
- **Fast 3 µs Over-Range Detection**
- **Serial I/O (SPI®, QSPI® and Microwire® Compatible)**
- **± 200 mV Input Range with Single 5 V Supply**
- **1% Internal Reference Voltage Matching**
- **Offset Calibration**
- **-40°C to +85°C Operating Temperature Range**
- **15 kV/µs Isolation Transient Immunity**
- **Regulatory Approvals; UL, CSA, VDE**



Hewlett-Packard's Isolated A/D Converter delivers the reliability, small size, superior isolation and over-temperature performance motor drive designers need to ***accurately measure current at half the price of traditional solutions.***

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

SPI and QSPI are trademarks of Motorola Corp.
Microwire is a trademark of National Semiconductor Inc.

Digital Current Sensing Circuit

As shown in Figure 1, using the Isolated 2-chip A/D converter to sense current can be as simple as connecting a current-sensing resistor, or shunt, to the input and reading output data through the 3-wire serial output interface. By choosing the appropriate shunt resistance, any range of current can be monitored, from less than 1 A to more than 100 A.

Even better performance can be achieved by fully utilizing the more advanced features of the Isolated A/D converter, such as the pre-trigger circuit which can reduce conversion time to less than 1 µs, the fast over-range detector for quickly detecting short circuits, different conversion modes giving various resolution/speed trade-offs, offset calibration mode to eliminate initial offset from measurements, and an adjustable threshold detector for detecting non-short circuit overload conditions.

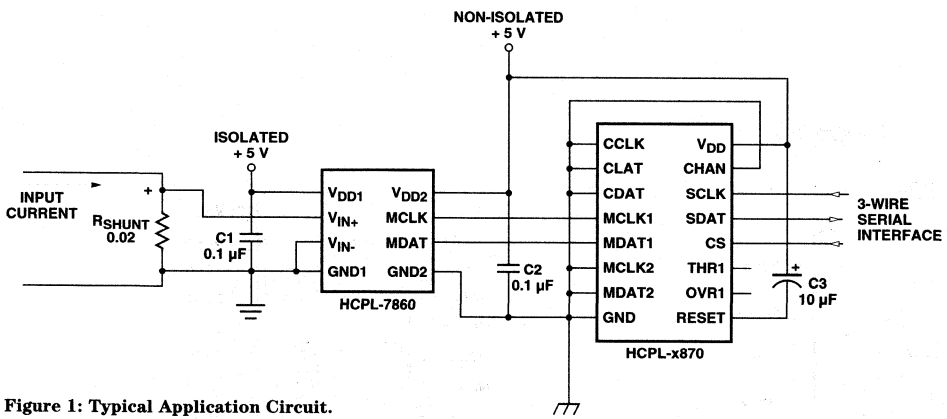


Figure 1: Typical Application Circuit.

Product Overview

Description

The HCPL-7860 Isolated Modulator and the HCPL-x870 Digital Interface IC together form an isolated programmable two-chip analog-to-digital converter. The isolated modulator allows direct measurement of motor phase currents in power inverters while the digital interface IC can be programmed to optimize the conversion speed and resolution trade-off.

In operation, the HCPL-7860 Isolated Modulator (optocoupler with 3750 V_{RMS} dielectric withstand voltage rating) converts a low-bandwidth analog input into a high-speed one-bit data stream by means of a sigma-delta ($\Sigma\Delta$) oversampling modulator. This modulation provides for high noise margins and excellent immunity against isolation-mode transients. The modulator data and on-chip sampling clock are encoded and transmitted across the isolation boundary where they are recovered and decoded into separate high-speed clock and data channels.

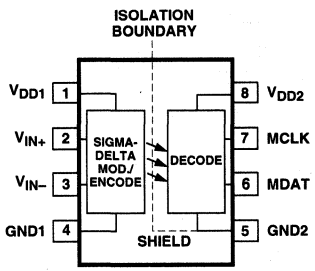
The Digital Interface IC converts the single-bit data stream from the Isolated Modulator into fifteen-bit output words and provides a serial output interface that is compatible with SPI®, QSPI®, and Microwire® protocols, allowing direct connection to a microcontroller. The Digital Interface IC is available in two package styles: the HCPL-7870 is in a 16-pin DIP package and the HCPL-0870 is in a 300-mil wide SO-16 surface-mount package. Features of the Digital Interface IC include five different conversion modes, three different pre-trigger modes, offset calibration, fast over-range detection, and adjustable threshold detection. Programmable features are configured via the Serial Configuration port. A second multiplexed input is available to allow measurements with a second

isolated modulator without additional hardware. Because the two inputs are multiplexed, only one conversion at a time can be made and not all features are available for the second channel. The available features for both channels are shown in the table at right.

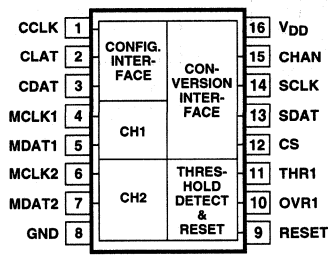
HCPL-x870 Digital Interface IC

Feature	Channel #1	Channel #2
Conversion Mode	✓	✓
Offset Calibration	✓	✓
Pre-Trigger Mode	✓	
Over-Range Detection	✓	
Adjustable Threshold Detection	✓	

Functional Diagrams



HCPL-7860 Isolated Modulator



HCPL-x870 Digital Interface IC

Pin Description, Isolated Modulator

Symbol	Description
V_{DD1}	Supply voltage input (4.5 V to 5.5 V)
V_{IN+}	Positive input (± 200 mV recommended)
V_{IN-}	Negative input (normally connected to GND1)
GND1	Input ground

Symbol	Description
V_{DD2}	Supply voltage input (4.5 V to 5.5 V)
MCLK	Clock output (10 MHz typical)
MDAT	Serial data output
GND2	Output ground

Pin Description, Digital Interface IC

Symbol	Description
CCLK	Clock input for the Serial Configuration Interface (SCI). Serial Configuration data is clocked in on the rising edge of CCLK.
CLAT	Latch input for the Serial Configuration Interface (SCI). The last 8 data bits clocked in on CDAT by CCLK are latched into the appropriate configuration register on the rising edge of CLAT.
CDAT	Data input for the Serial Configuration Interface (SCI). Serial configuration data is clocked in MSB first.
MCLK1	Channel 1 Isolated Modulator clock input. Input Data on MDAT1 is clocked in on the rising edge of MCLK1.
MDAT1	Channel 1 Isolated Modulator data input.
MCLK2	Channel 2 Isolated Modulator clock input. Input Data on MDAT2 is clocked in on the rising edge of MCLK2.
MDAT2	Channel 2 Isolated Modulator data input.
GND	Digital ground.

Symbol	Description
V_{DD}	Supply voltage (4.5 V to 5.5 V).
CHAN	Channel select input. The input level on CHAN determines which channel of data is used during the next conversion cycle. An input low selects channel 1, a high selects channel 2.
SCLK	Serial clock input. Serial data is clocked out of SDAT on the falling edge of SCLK.
SDAT	Serial data output. SDAT changes from high impedance to a logic low output at the start of a conversion cycle. SDAT then goes high to indicate that data is ready to be clocked out. SDAT returns to a high-impedance state after all data has been clocked out and CS has been brought high.
CS	Conversion start input. Conversion begins on the falling edge of CS. CS should remain low during the entire conversion cycle and then be brought high to conclude the cycle.
THR1	Continuous, programmable-threshold detection for channel 1 input data. A high level output on THR1 indicates that the magnitude of the channel 1 input signal is beyond a user programmable threshold level between 160 mV and 310 mV. This signal continuously monitors channel 1 independent of the channel select (CHAN) signal.
OVR1	High speed continuous over-range detection for channel 1 input data. A high level output on OVR1 indicates that the magnitude of the channel 1 input is beyond full-scale. This signal continuously monitors channel 1 independent of the CHAN signal.
RESET	Master reset input. A logic high input for at least 100 ns asynchronously resets all configuration registers to their default values and zeroes the Offset Calibration registers.

Isolated A/D Converter Performance

Electrical Specifications

Unless otherwise noted, all specifications are at V_{IN+} = -200 mV to +200 mV and V_{IN-} = 0 V; all Typical specifications are at T_A = 25°C and V_{DD1} = V_{DD2} = V_{DD} = 5 V; all Minimum/Maximum specifications are at T_A = -40°C to +85°C, V_{DD1} = V_{DD2} = V_{DD} = 4.5 to 5.5 V.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
STATIC CONVERTER CHARACTERISTICS								
Resolution		15			bits			1
Integral Nonlinearity	INL		6	30	LSB		3	2
			0.025	0.14	%		4	
Differential Nonlinearity	DNL			1	LSB			3
Uncalibrated Input Offset	V_{OS}	-1	1	2.5	mV	V_{IN+} = 0 V	5	
Offset Drift vs. Temperature	dV_{OS}/dT_A		4		µV/°C			4
Offset drift vs. V_{DD1}	dV_{OS}/dV_{DD1}		0.7		mV/V			
Internal Reference Voltage	V_{REF}		326		mV			
Absolute Reference Voltage Tolerance		-4		4	%		6	5
Reference Voltage Matching		-1		1	%	T_A = 25°C. See Note 5		
V_{REF} Drift vs. Temperature	dV_{REF}/dT_A		190		ppm/°C			
V_{REF} Drift vs. V_{DD1}	dV_{REF}/dV_{DD1}		0.9		%			
Full Scale Input Range		$-V_{REF}$		$+V_{REF}$	mV			6
Recommended Input Voltage Range		-200		+200				
DYNAMIC CONVERTER CHARACTERISTICS (Digital Interface IC is set to Conversion Mode 3.)								
Signal-to-Noise Ratio	SNR	62	73		dB	V_{IN+} = 35 Hz, 400 mV_{pk-pk} (141 mV_{rms}) sine wave.	2,9	
Total Harmonic Distortion	THD		-67					
Signal-to-(Noise + Distortion)	SND		66					
Effective Number of Bits	ENOB	10	12		bits		8	7
Conversion Time	t_{C2}		0.7	1.0	µs	Pre-Trigger Mode 2	7, 14	8
	t_{C1}		18	22		Pre-Trigger Mode 1		
	t_{C0}		37	44		Pre-Trigger Mode 0		
Signal Delay	t_{DSIG}		18	22			10	9
Over-Range Detect Time	t_{OVR1}	2.0	2.7	4.2		V_{IN+} = 0 to 400 mV step waveform	12	10
Threshold Detect Time	t_{THR1}		10					11
Signal Bandwidth	BW	18	22		kHz		11	12
Isolation Transient Immunity	CMR	15	20		kV/µs	V_{ISO} = 1 kV		13

Notes:

1. Resolution is defined as the total number of output bits. The useable accuracy of any A/D converter is a function of its linearity and signal-to-noise ratio, rather than how many total bits it has.
2. Integral nonlinearity is defined as one-half the peak-to-peak deviation of the best-fit line through the transfer curve for V_{IN+} = -200 mV to +200 mV, expressed either as the number of LSBs or as a percent of measured input range (400 mV).
3. Differential nonlinearity is defined as the deviation of the actual difference from the ideal difference between midpoints of successive output codes, expressed in LSBs.
4. Data sheet value is the average magnitude of the difference in offset voltage from T_A = 25°C to T_A = -40°C, expressed in microvolts per °C.
5. All units within each HCPL-7860 standard packaging increment (either 50 per tube or 1000 per reel) have an Absolute Reference Voltage tolerance of ± 1%. An Absolute Reference Voltage tolerance of ± 4% is guaranteed between standard packaging increments.
6. Beyond the full-scale input range the output is either all zeroes or all ones.
7. The effective number of bits (or effective resolution) is defined by the equation ENOB = (SNR-1.76)/6.02 and represents the resolution of an ideal, quantization-noise limited A/D converter with the same SNR.
8. Conversion time is defined as the time from when the convert start signal CS is brought low to when SDAT goes high, indicating that output data is ready to be clocked out. This can be as small as a few cycles of the isolated modulator clock and is determined by the frequency of the isolated modulator clock and the selected Conversion and Pre-Trigger modes. For determining the true signal delay characteristics of the A/D converter for closed-loop phase margin calculations, the signal delay specification should be used.
9. Signal delay is defined as the effective delay of the input signal through the Isolated A/D converter. It can be measured by applying a -200 mV to ± 200 mV step at the input of modulator and adjusting the relative delay of the convert start signal CS so that the output of the converter is at mid-scale. The signal delay is the elapsed time from when the step signal is applied at the input to when output data is ready at the end of the conversion cycle. The signal delay is the most important specification for determining the true signal delay characteristics of the A/D converter and should be used for determining phase margins in closed-loop applications. The signal delay is determined by the frequency of the modulator clock and which Conversion Mode is selected, and is independent of the selected Pre-Trigger Mode and, therefore, conversion time.
10. The minimum and maximum over-range detection time is determined by the frequency of the channel 1 isolated modulator clock.
11. The minimum and maximum threshold detection time is determined by the user-defined configuration of the adjustable threshold detection circuit and the frequency of the channel 1 isolated modulator clock. See the Applications Information section for further detail. The specified times apply for the default configuration.
12. The signal bandwidth is the frequency at which the magnitude of the output signal has decreased 3 dB below its low-frequency value. The signal bandwidth is determined by the frequency of the modulator clock and the selected Conversion Mode.
13. The isolation transient immunity (also known as Common-Mode Rejection) specifies the minimum rate-of-rise of an isolation-mode signal applied across the isolation boundary beyond which the modulator clock or data signals are corrupted.

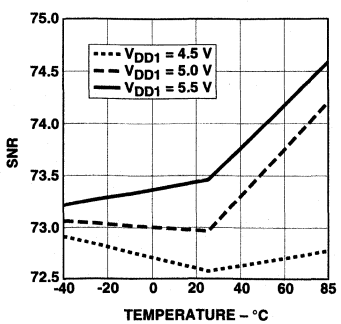


Figure 2. SNR vs. Temperature.

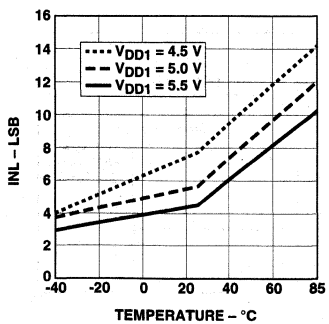


Figure 3. INL (Bits) vs. Temperature.

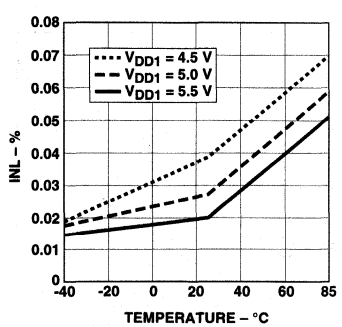


Figure 4. INL (%) vs. Temperature.

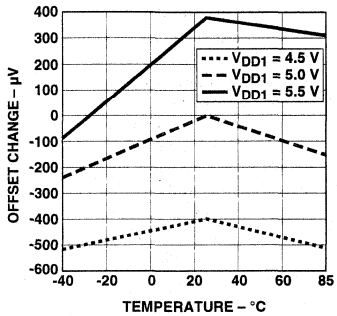


Figure 5. Offset Change vs. Temperature.

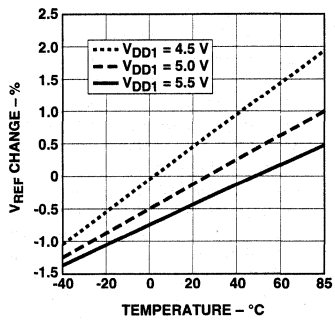


Figure 6. V_{REF} Change vs. Temperature.

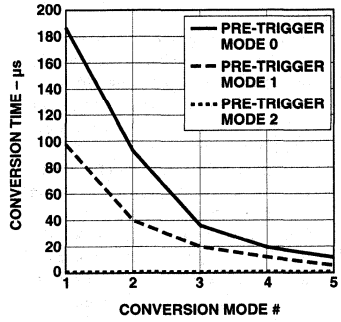


Figure 7. Conversion Time vs. Conversion Mode.

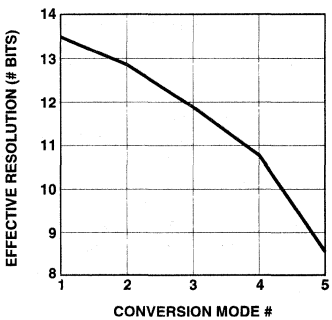


Figure 8. Effective Resolution vs. Conversion Mode.

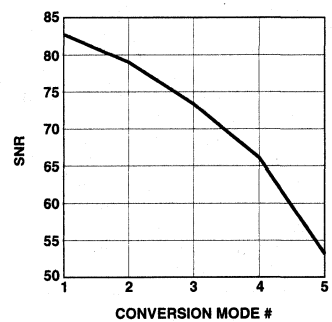


Figure 9. SNR vs. Conversion Mode.

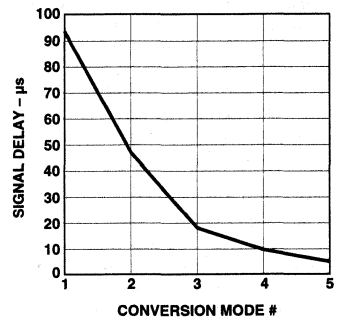


Figure 10. Signal Delay vs. Conversion Mode.

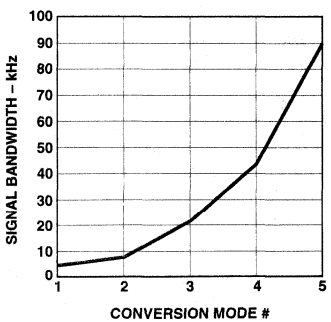


Figure 11. Signal Bandwidth vs. Conversion Mode.

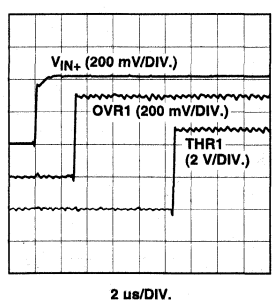


Figure 12. Over-Range and Threshold Detect Times.

Isolated Modulator

Ordering Information

Specify Part Number followed by Option Number (if desired).

Example:

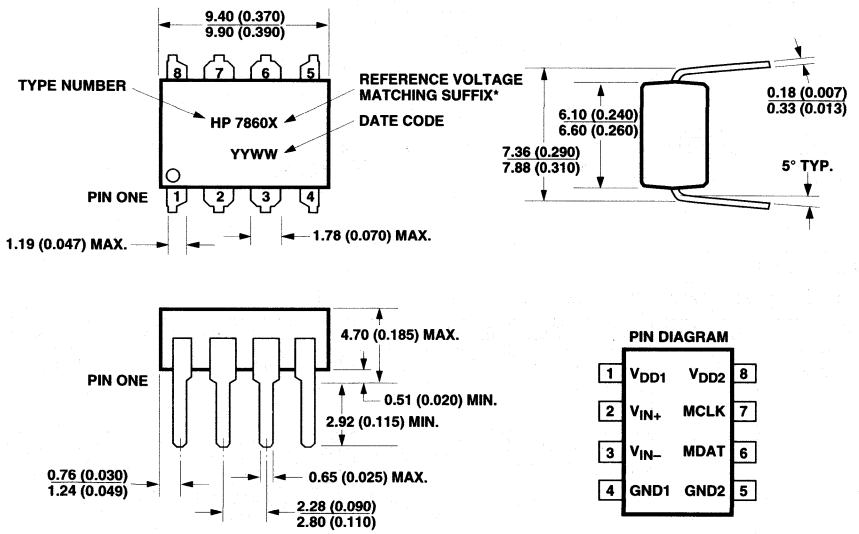
HCPL-7860#XXX

- No Option = Standard DIP package, 50 per tube.
- 300 = Gull Wing Surface Mount Option, 50 per tube.
- 500 = Tape and Reel Packaging Option, 1000 per reel.

Option data sheets available. Contact Hewlett-Packard sales representative or authorized distributor.

Package Outline Drawings

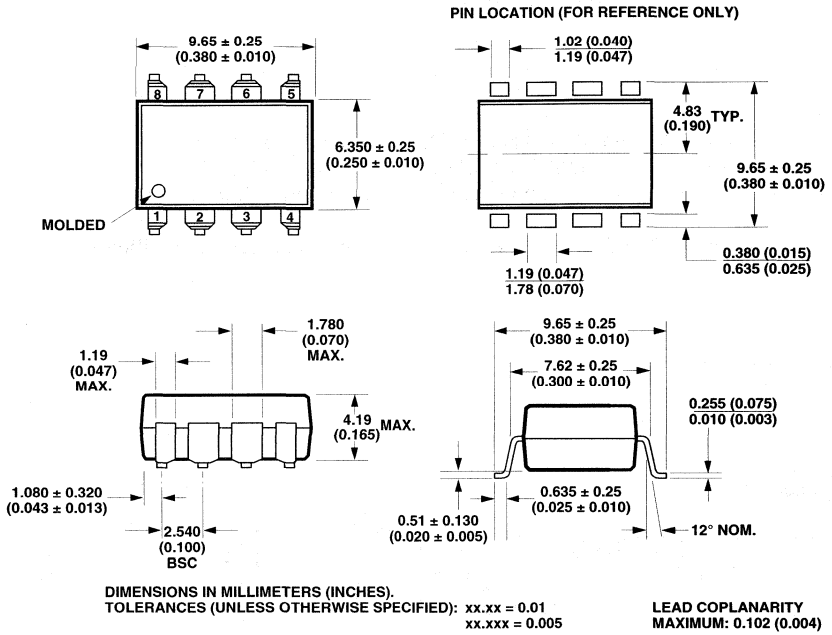
8-pin DIP Package



DIMENSIONS IN MILLIMETERS AND (INCHES).

*ALL UNITS WITHIN EACH HCPL-7860 STANDARD PACKAGING INCREMENT (EITHER 50 PER TUBE OR 1000 PER REEL) HAVE A COMMON MARKING SUFFIX TO REPRESENT AN ABSOLUTE REFERENCE VOLTAGE TOLERANCE OF ± 1%. AN ABSOLUTE REFERENCE VOLTAGE TOLERANCE OF ± 4% IS GUARANTEED BETWEEN STANDARD PACKAGING INCREMENTS.

8-pin DIP Gull Wing Surface Mount Option 300



DIMENSIONS IN MILLIMETERS (INCHES).
TOLERANCES (UNLESS OTHERWISE SPECIFIED): xx.xx = 0.01
xx.xxx = 0.005

LEAD COPLANARITY
MAXIMUM: 0.102 (0.004)

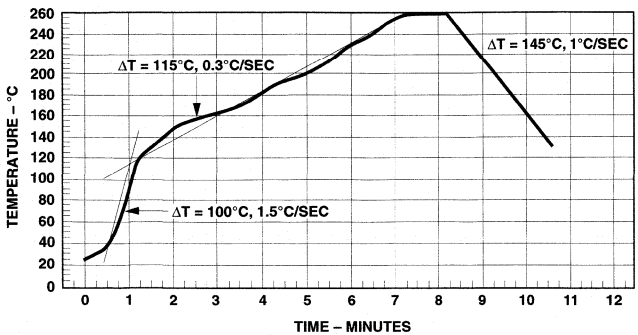
Package Characteristics

Unless otherwise noted, all specifications are at $T_A = +25°C$.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Note
Input-Output Momentary Withstand Voltage (See note ** below)	V_{ISO}	3750			V_{rms}	RH ≤ 50%, t = 1 min.	14,15
Resistance (Input - Output)	R_{I-O}	10^{12}	10^{13}		Ω	V_{I-O} = 500 Vdc	15
		10^{11}				T_A = 100°C	
Capacitance (Input - Output)	C_{I-O}		0.7		pF	f = 1 MHz	
Input IC Junction-to-Case Thermal Resistance	θ_{jci}		96		°C/W	Thermocouple located at center underside of package	
Output IC Junction-to-Case Thermal Resistance	θ_{jco}		114		°C/W		

** The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to your equipment level safety specification or HP Application Note 1074, *Optocoupler Input-Output Endurance Voltage*.

Maximum Solder Reflow Thermal Profile



(NOTE: USE OF NON-CHLORINE ACTIVATED FLUXES IS RECOMMENDED.)

Regulatory Information

The HCPL-7860 (isolated modulator) has been approved by the following organizations:

UL
Recognized under UL 1577, Component Recognition Program, File E55361.

VDE (Pending)
Approved under VDE 0884/06.92 with V_{IORM} = 848 V_{PEAK}.

CSA
Approved under CSA Component Acceptance Notice #5, File CA 88324.

VDE 0884 Insulation Characteristics

Description	Symbol	Characteristic	Unit
Installation classification per DIN VDE 0110/1.89, Table 1 for rated mains voltage ≤ 300 V_{rms} for rated mains voltage ≤ 600 V_{rms}		 I - IV I - III	
Climatic Classification		40/85/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	848	V_{PEAK}
Input to Output Test Voltage, Method b* V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial Discharge < 5 pC	V_{PR}	1590	V_{PEAK}
Input to Output Test Voltage, Method a* V_{IORM} x 1.5 = V_{PR}, Type and Sample Test, t_m = 60 sec, Partial Discharge < 5 pC	V_{PR}	1273	V_{PEAK}
Highest Allowable Overvoltage (Transient Overvoltage t_{ini} = 10 sec)	V_{IOTM}	6000	V_{PEAK}
Safety-Limiting Values–Maximum Values Allowed in the Event of a Failure, also see Figure 13. Case Temperature Input Power Output Power	 T_S $I_{S, INPUT}$ $P_{S, OUTPUT}$	 175 80 250	 °C mW mW
Insulation Resistance at T_{SI}, V_{IO} = 500 V	R_S	≥ 10^9	Ω

*Refer to the optocoupler section of the Optoelectronics Designer's Catalog, under Product Safety Regulations section, (VDE 0884) for a detailed description of Method a and Method b partial discharge test profiles.

Note: Isolation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuits in application.

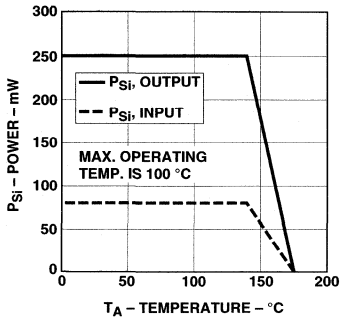


Figure 13. Dependence of Safety-Limiting Values on Temperature.

Insulation and Safety Related Specifications

Parameter	Symbol	Value	Units	Conditions
Minimum External Air Gap (Clearance)	L(I01)	7.4	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(I02)	8.0	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Plastic Gap (Internal Clearance)		0.5	mm	Insulation thickness between emitter and detector; also known as distance through insulation.
Tracking Resistance (Comparative Tracking Index)	CTI	175	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Option 300 - surface mount classification is Class A in accordance with CECC 00802.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	T_S	-55	125	°C	
Ambient Operating Temperature	T_A	-40	+85	°C	
Supply Voltages	V_{DD1}, V_{DD2}	0	5.5	Volts	
Steady-State Input Voltage	V_{IN+}, V_{IN-}	-2.0	V_{DD1} + 0.5	Volts	16
Two Second Transient Input Voltage		-6.0			
Output Voltages	MCLK, MDAT	-0.5	V_{DD2} +0.5	Volts	
Lead Solder Temperature	260 °C for 10 sec., 1.6 mm below seating plane				17
Solder Reflow Temperature Profile	See Maximum Solder Reflow Thermal Profile section				

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Note
Ambient Operating Temperature	T_A	-40	+85	°C	
Supply Voltages	V_{DD1}, V_{DD2}	4.5	5.5	V	
Input Voltage	V_{IN+}, V_{IN-}	-200	+200	mV	16

Electrical Specifications, Isolated Modulator

Unless otherwise noted, all specifications are at V_{IN+} = 0 V and V_{IN-} = 0 V, all Typical specifications are at T_A = 25°C and V_{DD1} = V_{DD2} = 5 V, and all Minimum and Maximum specifications apply over the following ranges: T_A = -40°C to +85°C, V_{DD1} = 4.5 to 5.5 V and V_{DD2} = 4.5 to 5.5 V.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Average Input Bias Current	I_{IN}		-1.0		µA		14	18
Average Input Resistance	R_{IN}		270		kΩ			
Input DC Common-Mode Rejection Ratio	$CMRR_{IN}$		55		dB			19
Output Logic High Voltage	V_{OH}	3.9	4.9		V	I_{OUT} = -100 µA		
Output Logic Low Voltage	V_{OL}		0.3	0.6	V	I_{OUT} = 1.6 mA		
Output Short Circuit Current	$\|I_{OSC}\|$		10		mA	V_{OUT} = V_{DD2} or GND2		20
Input Supply Current	I_{DD1}		9.5	15	mA	V_{IN+} = -350 mV	15	
Output Supply Current	I_{DD2}		8.8	15	mA	to +350 mV	16	
Output Clock Frequency	f_{CLK}	9	11	14	MHz		17	
Data Hold Time	t_{HDDAT}		15		ns			21

Notes:

14. In accordance with UL1577, for devices with minimum V_{ISO} specified at 3750 V_{rms}, each isolated modulator (optocoupler) is proof-tested by applying an insulation test voltage greater than 4500 Vrms for one second (leakage current detection limit I_{I-O} < 5 µa). This test is performed before the Method b, 100% production test for partial discharge shown in VDE 0884 Insulation Characteristics Table.
15. This is a two-terminal measurement: pins 1-4 are shorted together and pins 5-8 are shorted together.
16. If V_{IN-} (pin 3) is brought above V_{DD1} - 2 V with respect to GND1 an internal optical-coupling test mode may be activated. This test mode is not intended for customer use.
17. HP recommends the use of non-chlorinated solder fluxes.
18. Because of the switched-capacitor nature of the isolated modulator, time averaged values are shown.
19. $CMRR_{IN}$ is defined as the ratio of the gain for differential inputs applied between V_{IN+} and V_{IN-} to the gain for common-mode inputs applied to both V_{IN+} and V_{IN-} with respect to input ground GND1.
20. Short-circuit current is the amount of output current generated when either output is shorted to V_{DD2} or GND2. Use under these conditions is not recommended.
21. Data hold time is amount of time that the data output MDAT will stay stable following the rising edge of output clock MCLK.

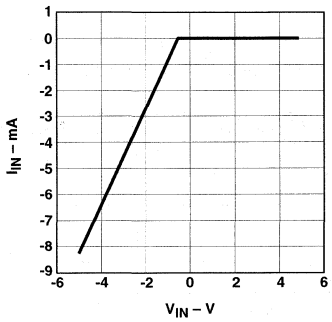


Figure 14. I_{IN} vs. V_{IN}.

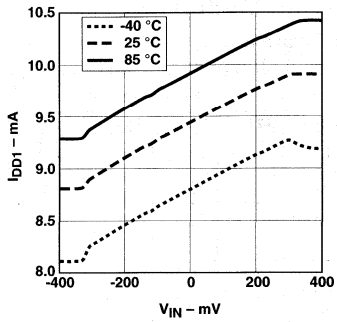


Figure 15. I_{DD1} vs. V_{IN}.

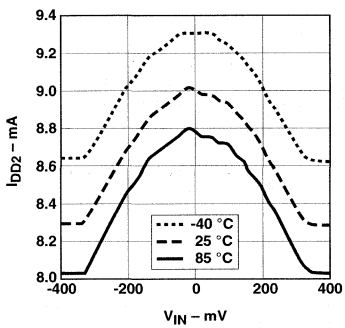


Figure 16. I_{DD2} vs. V_{IN}.

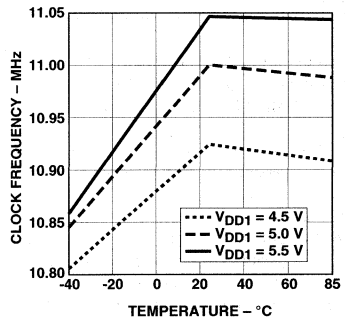


Figure 17. Clock Frequency vs. Temperature.

Digital Interface IC

Ordering Information

Specify Part Number followed by Option Number (if desired).

Example

HCPL-7870 Standard 16-pin DIP package, 25 per tube.

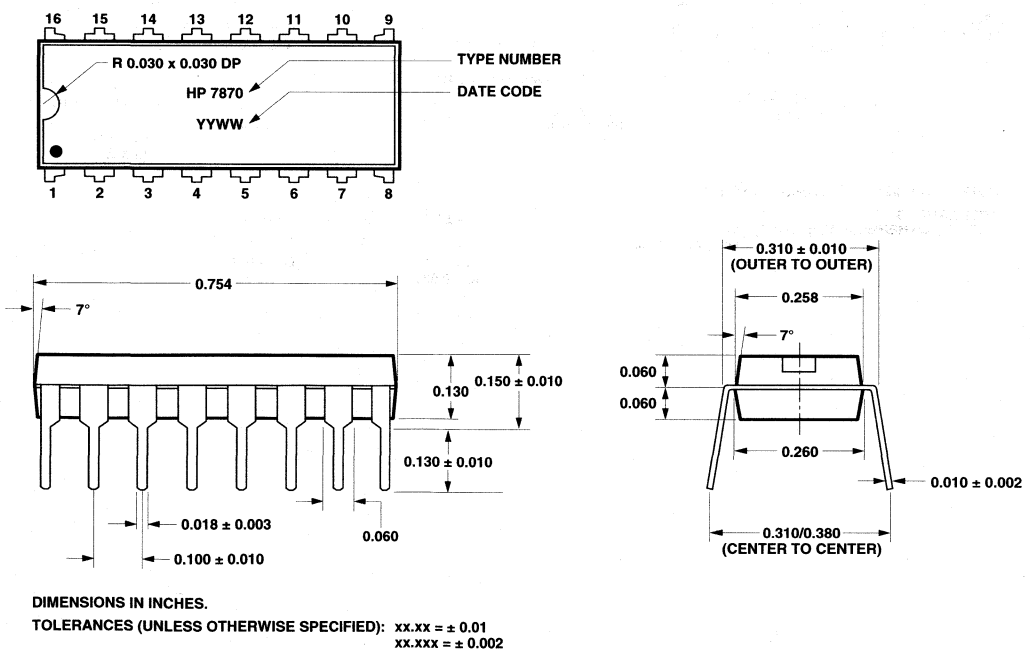
HCPL-0870#XXX

- No Option = Standard 16-pin SO package, 47 per tube.
- 500 = Tape and Reel Packaging Option, 1000 per reel.

Option data sheets available. Contact Hewlett-Packard sales representative or authorized distributor.

Package Outline Drawings

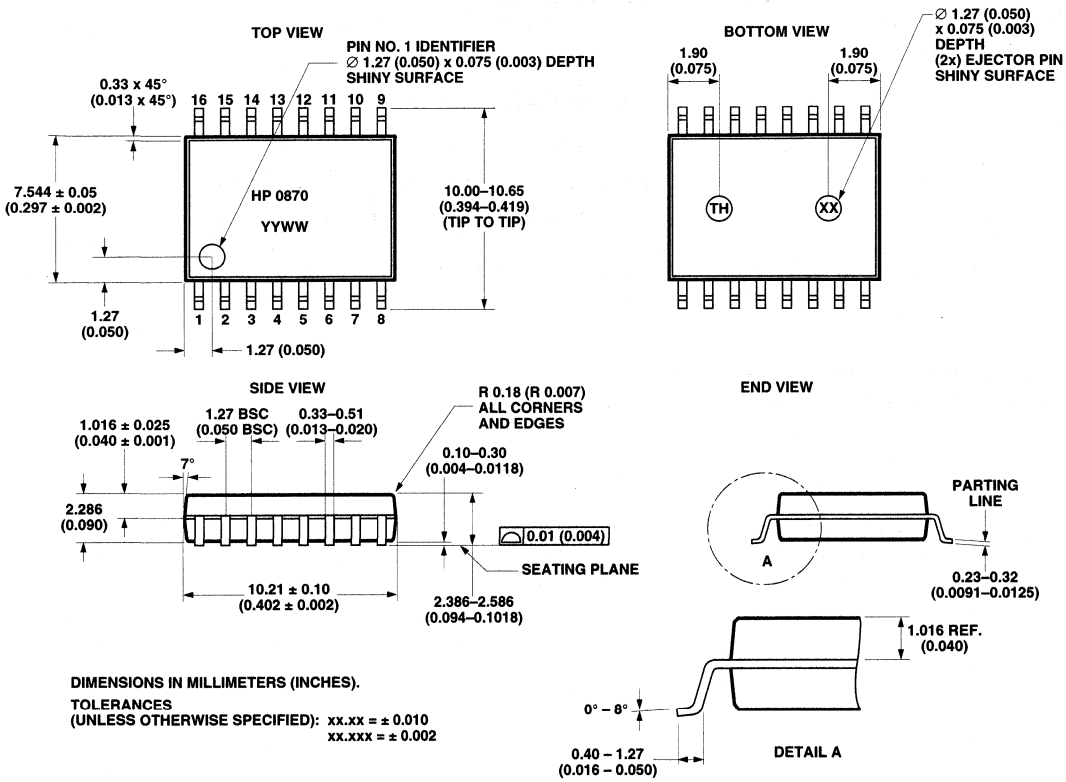
Standard 16-pin DIP Package



DIMENSIONS IN INCHES.

TOLERANCES (UNLESS OTHERWISE SPECIFIED): xx.xx = ± 0.01
xx.xxx = ± 0.002

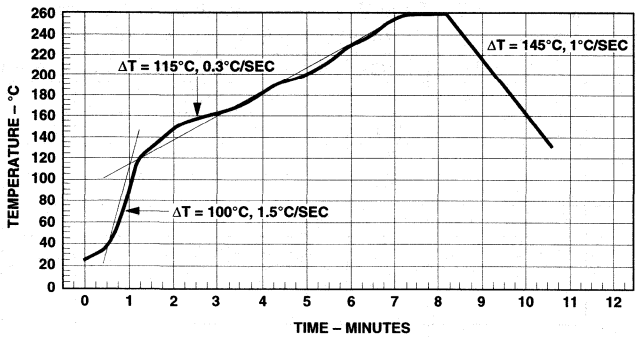
Standard 16-pin SO Package



DIMENSIONS IN MILLIMETERS (INCHES).

TOLERANCES
(UNLESS OTHERWISE SPECIFIED): xx.xx = ± 0.010
xx.xxx = ± 0.002

Maximum Solder Reflow Thermal Profile



(NOTE: USE OF NON-CHLORINE ACTIVATED FLUXES IS RECOMMENDED.)

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	T_S	-55	+125	°C	
Ambient Operating Temperature	T_A	-40	+85	°C	
Supply Voltage	V_{DD}	0	5.5	V	
Input Voltage	All Inputs	-0.5	V_{DD} + 0.5	V	
Output Voltage	All Outputs	-0.5	V_{DD} + 0.5	V	
Lead Solder Temperature	260°C for 10 seconds, 1.6 mm below seating plane				17
Solder Reflow Temperature Profile	See Reflow Thermal Profile				

Note:
17. HP recommends the use of non-chlorinated solder fluxes.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Note
Ambient Operating Temperature	T_A	-40	+85	°C	
Supply Voltage	V_{DD}	4.5	5.5	V	
Input Voltage	All Inputs	0	V_{DD}	V	

Electrical Specifications, Digital Interface IC

Unless otherwise noted, all Typical specifications are at T_A = 25°C and V_{DD} = 5 V, and all Minimum and Maximum specifications apply over the following ranges: T_A = -40°C to +85°C and V_{DD} = 4.5 to 5.5 V.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Supply Current	I_{DD}		20	35	mA	f_{CLK} = 10 MHz		
DC Input Current	I_{IN}		0.001	10	µA			
Input Logic Low Voltage	V_{IL}			0.8	V			
Input Logic High Voltage	V_{IH}	2.0			V			
Output Logic Low Voltage	V_{OL}		0.15	0.4	V	I_{OUT} = 4 mA		
Output Logic High Voltage	V_{OH}	4.3	5.0		V	I_{OUT} = -400 µA		
Clock Frequency (CCLK, MCLK and SCLK)	f_{CLK}			20	MHz			
Clock Period (CCLK, MCLK and SCLK)	t_{PER}	50			ns		18, 19	
Clock High Level Pulse Width (CCLK, MCLK and SCLK)	t_{PWH}	20			ns			
Clock Low Level Pulse Width (CCLK, MCLK and SCLK)	t_{PWL}	20						
Setup Time from DAT to Rising Edge of CLK (CDAT, CCLK, MDAT and MCLK)	t_{SUCLK}	10					18	
DAT Hold Time after Rising Edge of CLK (CDAT, CCLK, MDAT and MCLK)	t_{HDCLK}	10						
Setup Time from Falling Edge of CLAT to First Rising Edge of CCLK	t_{SUCL1}	20						
Setup Time from Last Rising Edge of CCLK to Rising Edge of CLAT	t_{SUCL2}	20						
Delay Time from Falling Edge of SCLK to SDAT	t_{DSDAT}			15			19	
Setup Time from Data Ready to First Falling Edge of SCLK	t_{SUS}	200						
Setup Time from CHAN to falling edge of CS	t_{SUCHS}	20						
Reset High Level Pulse Width	t_{PWR}	100						

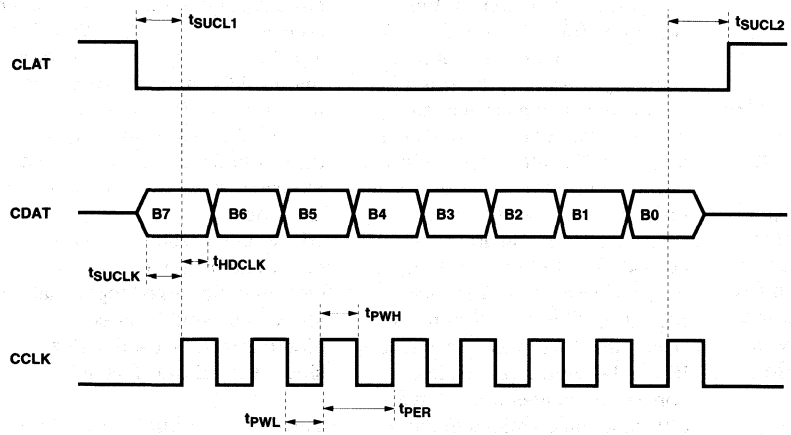


Figure 18. Serial Configuration Interface Timing.

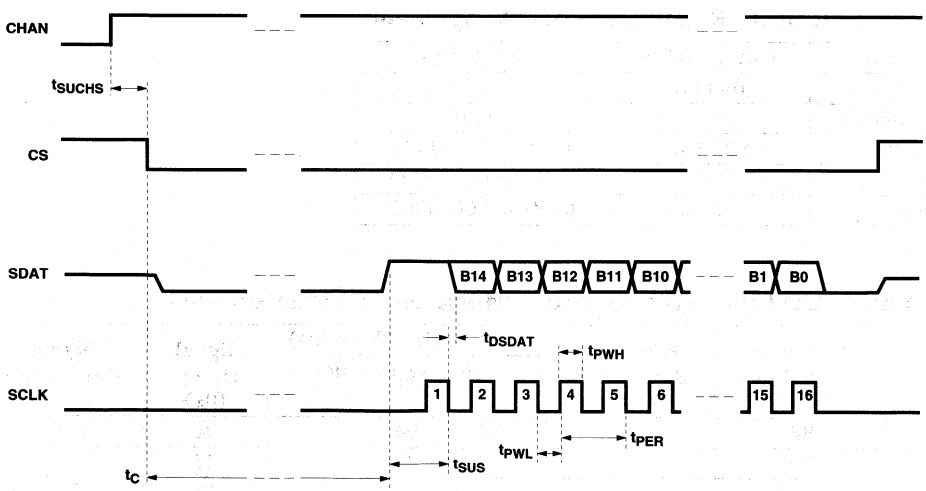


Figure 19. Conversion Timing.

Applications Information

Product Description

The HCPL-7860 Isolated Modulator (optocoupler) uses sigma-delta modulation to convert an analog input signal into a high-speed (10 MHz) single-bit digital data stream; the time average of the modulator's single-bit data is directly proportional to the input signal. The isolated modulator's other main function is to provide galvanic isolation between the analog input and the digital output. An internal voltage reference determines the full-scale analog input range of the modulator (approximately ± 320 mV); an input range of ± 200 mV is recommended to achieve optimal performance.

The primary functions of the HCPL-x870 Digital Interface IC are to derive a multi-bit output signal by averaging the single-bit modulator data, as well as to provide a direct microcontroller interface. The effective resolution of the multi-bit output signal is a function of the length of time (measured in modulator clock cycles) over which the average is taken; averaging over longer periods of time results in higher resolution. The Digital Interface IC can be configured for five conversion modes which have different combinations of speed and resolution to achieve the desired level of performance.

Other functions of the HCPL-x870 Digital Interface IC include a Phase Locked Loop based pre-trigger circuit that can either give more precise control of the effective sampling time or reduce conversion time to less than 1 µs, a fast over-range detection circuit that rapidly indicates when the magnitude of the input signal is beyond full-scale, an adjustable threshold detection circuit that indicates when the magnitude of the input signal is above a user-adjustable threshold level, an offset calibration circuit, and a second multiplexed input that allows a second Isolated Modulator to be used with a single Digital Interface IC.

The digital output format of the Isolated A/D Converter is 15 bits of unsigned binary data. The input full-scale range and code assignment is shown in Table 1 below. Although the output contains 15 bits of data, the effective resolution is lower and is determined by selected conversion mode as shown in Table 2 below.

Table 1. Input Full-Scale Range and Code Assignment.

Analog Input	Voltage Input	Digital Output
Full Scale Range	640 mV	32768 LSBs
Minimum Step Size	20 µV	1 LSB
+Full Scale	+320 mV	111111111111111
Zero	0 mV	100000000000000
-Full Scale	-320 mV	000000000000000

Table 2. Isolated A/D Converter Typical Performance Characteristics.

Conversion Mode	Signal-to-Noise Ratio (dB)	Effective Resolution (bits)	Conversion Time (µs) Pre-Trigger Mode			Signal Delay (µs)	Signal Bandwidth (kHz)
			0	**1**	**2**		
1	83	13.5	188	94		94	3.4
2	79	12.8	95	47		47	6.9
3	73	11.9	37	18	0.7	18	22
4	***66***	***10.7***	***19***	10		***10***	***45***
5	53	8.5	10	5		5	90

Note: Bold italic type indicates Default values.

Digital Interface Timing

Power Up/Reset

At power up, the digital interface IC should be reset either manually, by bringing the RESET pin (pin 9) high for at least 100 ns, or automatically by connecting a 10 µF capacitor between the RESET pin and V_{DD} (pin 16). The RESET pin operates asynchronously and places the IC in its default configuration, as specified in the Digital Interface Configuration section.

Conversion Timing

Figure 19 illustrates the timing for one complete conversion cycle. A conversion cycle is initiated on the falling edge of the convert start signal (CS); CS should be held low during the entire conversion cycle. When CS is brought low, the serial output data line (SDAT) changes from a high-impedance to the low state, indicating that the converter is busy. A rising edge on SDAT indicates that data is ready to be clocked out. The output data is clocked out on the negative edges of the serial clock pulses (SCLK), MSB first. A total of 16 pulses is needed to clock out all of the data. After the last clock pulse, CS should be brought high again, causing SDAT to return to a high-impedance state, completing the conversion cycle. If the external circuit uses the positive edges of SCLK to clock in the data, then a total of sixteen bits is clocked in, the first bit is always high (indicating that data is ready) followed by 15 data bits. If fewer than 16 cycles of SCLK are input before CS is brought high, the conversion cycle will terminate and SDAT will go to the high-impedance state after a few cycles of the Isolated Modulator's clock.

The amount of time between the falling edge of CS and the rising edge of SDAT depends on which conversion and pre-trigger modes are selected; it can be as low as 0.7 µs when using pre-trigger mode 2, as explained in the Digital Interface Configuration section.

Serial Configuration Timing

The HCPL-x870 Digital Interface IC is programmed using the Serial Configuration Interface (SCI) which consists of the clock (CCLK), data (CDAT), and enable/latch (CLAT) signals. Figure 18 illustrates the timing for the serial configuration interface. To send a byte of configuration data to the HCPL-x870, first bring CLAT low. Then clock in the eight bits of the configuration byte (MSB first) using CDAT and the rising edge of CCLK. After the last bit has been clocked in, bringing CLAT high again will latch the data into the appropriate configuration register inside the interface IC. If more than eight bits are clocked in before CLAT is brought high, only the last eight bits will be used. Refer to the Digital Interface Configuration section to determine appropriate configuration data. If the default configuration of the digital interface IC is acceptable, then CCLK, CDIN and CLAT may be connected to either V_{DD} or GND.

Channel Select Timing

The channel select signal (CHAN) determines which input channel will be used for the next conversion cycle. A logic low level selects channel one, a high level selects channel 2. CHAN should not be changed during a conversion cycle. The state of the CHAN signal has no effect on the behavior of either the over-range detection circuit (OVR1) or the adjustable threshold detection circuit (THR1). Both OVR1 and THR1 continuously monitor channel 1 independent of the CHAN signal. CHAN also does not affect the behavior of the pre-trigger circuit, which is tied to the conversion timing of channel 1, as explained in the Digital Interface Configuration section.

Digital Interface Configuration

Configuration Registers

The Digital Interface IC contains four 6-bit configuration registers that control its behavior. The two LSBs of any byte clocked into the serial configuration port (CDAT, CCLK, CLAT) are used as address bits to determine which register the data will be loaded into. Registers 0 and 1 (with address bits 00 and 01) specify the conversion and offset calibration modes of channels 1 and 2, register 2 (address bits 10) specifies the behavior of the adjustable threshold circuit, and register 3 (address bits 11) specifies which pre-trigger mode to use for channel 1. These registers are illustrated in Table 3 below, with default values indicated in bold italic type. Note that there are several reserved bits which should always be set low and that the configuration registers should not be changed during a conversion cycle.

Table 3. Register Configuration.

	Configuration Data Bits						Address Bits	
Register	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0	Channel 1 Conversion Mode				Channel 1 Offset Cal	Reserved		
	High	***High***	***Low***	***Low***	***Low***	***Low***	Low	Low
1	Channel 2 Conversion Mode				Channel 2 Offset Cal	Reserved		
	High	***High***	***Low***	***Low***	***Low***	***Low***	Low	High
2	Threshold Detection Time		Threshold Level					
	High	***Low***	***Low***	***Low***	***Low***	***Low***	High	Low
3	Pre-Trigger Mode		Reserved					
	Low	***Low***	***Low***	***Low***	***Low***	***Low***	High	High

Note: Bold italic type indicates default values. Reserved bits should be set low.

Conversion Mode

The conversion mode determines the speed/resolution trade-off for the Isolated A/D converter. The four MSBs of registers 0 and 1 determine the conversion mode for the appropriate channel. The bit settings for choosing a particular conversion mode are shown in Table 4 below. See Table 2 for a summary of how performance changes as a function of conversion mode setting. Combinations of data bits not specified in Table 4 below are not recommended.

Table 4. Conversion Mode Configuration.

Conversion Mode	Configuration Data Bits			
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**
1	Low	High	Low	High
2	Low	Low	High	High
3	High	High	High	Low
4	***High***	***High***	***Low***	***Low***
5	High	Low	High	Low

Note: Bold italic type indicates default values.

Pre-Trigger Mode

The pre-trigger mode refers to the operation of a PLL-based circuit that affects the sampling behavior and conversion time of the A/D converter when channel 1 is selected. The PLL pre-trigger circuit has two modes of operation; the first mode allows more precise control of the time at which the analog input voltage is effectively sampled, while the second mode essentially eliminates the time between when the external convert start command is given and when output data is available (reducing it to less than 1 µs). A brief description of how the A/D converter works with the pre-trigger circuit disabled will help explain how the pre-trigger circuit affects operation when it is enabled.

With the pre-trigger circuit is disabled (pre-trigger mode 0), Figure 20 illustrates the relationship between the convert start command, the weighting function used to average the modulator data, and the data ready signal. The weighted averaging of the modulator data begins immediately following the convert start command. The weighting function increases for half of the conversion cycle and then decreases back to zero, at which time the data ready signal is given, completing the conversion cycle. The analog signal is effectively sampled at the peak of the weighting function, half-way through the conversion cycle. This is the default mode.

If the convert start signal is periodic (i.e., at a fixed frequency) and the PLL pre-trigger circuit is enabled (pre-trigger modes 1 or 2), either the peak of the weighting function or the end of the conversion cycle can be aligned to the external convert start command, as shown in Figure 20. The Digital Interface IC can therefore synchronize the conversion cycle so that either the beginning, the middle, or the end of the conversion is aligned with the external convert start command, depending on whether pre-trigger mode 0, 1, or 2 is selected, respectively. The only requirement is that the convert start signal for channel 1 be periodic. If the signal is not periodic and pre-trigger mode 1 or 2 is selected, then the pre-trigger circuit will not function properly.

An important distinction should be made concerning the difference between conversion time and signal delay. As can be seen in Figure 20, the amount of time from the peak of the weighting function (when the input signal is being sampled) to when output data is ready is the same for all three modes. This is the actual delay of the analog signal through the A/D converter and is independent of the "conversion time," which is simply the time between the convert start signal and the data ready signal. Because signal delay is the true measure of how much phase shift the A/D converter adds to the signal, it should be used when making calculations of phase margin and loop stability in feedback systems.

There are different reasons for using each of the pre-trigger modes. If the signal is not

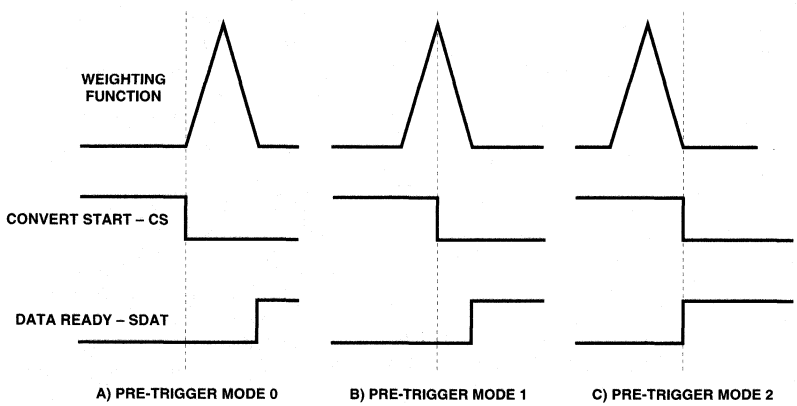


Figure 20. Pre-Trigger Modes 0, 1, and 2.

periodic, then the pre-trigger circuit should be disabled by selecting pre-trigger mode 0. If the most time-accurate sampling of the input signal is desired, then mode 1 should be selected. If the shortest possible conversion time is desired, then mode 2 should be selected.

The pre-trigger circuit functions only with channel 1; the circuit ignores any convert start signals while channel 2 is selected with the CHAN input. This allows conversions on channel 2 to be performed between conversions on channel 1 without affecting the operation of the pre-trigger circuit. As long as the convert start signals are periodic while channel 1 is selected, then the pre-trigger circuit will function properly.

The three different pre-trigger modes are selected using bits 6 and 7 of register 3, as shown in Table 5 below.

Table 5. Pre-Trigger Mode Configuration.

Pre-Trigger Mode	Configuration Data Bits	
	Bit 7	Bit 6
0	***Low***	***Low***
1	Low	High
2	High	Don't Care

Note: Bold italic type indicates default values.

Offset Calibration

The offset calibration circuit can be used to separately calibrate the offsets of both channels 1 and 2. The offset calibration circuit contains a separate offset register for each channel. After an offset calibration sequence, the offset registers will contain a value equal to the measured offset, which will then be subtracted from all subsequent conversions. A hardware reset (bringing the RESET pin high for at least 100 ns) is required to reset the offset calibration registers to zero.

The following sequence is recommended for performing an offset calibration:

1. Select the appropriate channel using the CHAN pin (low = channel 1, high = channel 2).
2. Force zero volts at the input of the selected isolated modulator.
3. Send a configuration data byte to the appropriate register for the selected channel (register 0 for channel 1, register 1 for channel 2). Bit 3 of the configuration byte should be set high to enable offset calibration mode and bits 4 through 7 should be set to select conversion mode 1 to achieve the highest resolution measurement of the offset.
4. Perform one complete conversion cycle by bringing CS low until SDAT goes high, indicating completion of the conversion cycle. Because bit 3 of the configuration has been set high, the uncalibrated output data from the conversion will be stored in the appropriate offset calibration register and will be subtracted from all subsequent conversions on that channel. If multiple conversion cycles are performed while the offset calibration mode is enabled, the uncalibrated data from the last conversion cycle will be stored in the offset calibration register.
5. Send another configuration byte to the appropriate register for the selected channel, setting bit 3 low to disable calibration mode and setting bits 4 through 7 to select the desired conversion mode for subsequent conversions on that channel.

To calibrate both channels, perform the above sequence for each channel. The offset calibration sequence can be performed as often as needed. The table below summarizes how to turn the offset calibration mode on or off using bit 3 of configuration registers 0 and 1.

Table 6. Offset Calibration Configuration.

Offset Calibration Mode	Configuration Data Bits
	Bit 3
Off	***Low***
On	High

Note: Bold italic type indicates default values.

Over-Range Detection

The over-range detection circuit allows fast detection of when the magnitude of the input signal on channel 1 is near or beyond full scale, causing the OVR1 output to go high. This circuit can be very useful in current-sensing applications for quickly detecting when a short-circuit occurs. The over-range detection circuit works by detecting when the modulator output data has not changed state for at least 25 clock cycles in a row, indicating that the input signal is near or beyond full-scale, positive or negative. Typical response time to over-range signals is less than 3 µs.

The over-range circuit actually begins to indicate an over-range condition when the magnitude of the input signal exceeds approximately 250 mV; it starts to generate periodic short pulses on OVR1 which get longer and more frequent as the input signal approaches full scale. The OVR1 output stays high continuously when the input is beyond full scale.

The over-range detection circuit continuously monitors channel 1 independent of which channel is selected with the CHAN signal. This allows continuous monitoring of channel 1 for faults while converting an input signal on channel 2.

Adjustable Threshold Detection

The adjustable threshold detector causes the THR1 output to go high when the magnitude of the input signal on channel 1 exceeds a user-defined threshold level. The threshold level can be set to one of 16 different values between approximately 160 mV and 310 mV. The adjustable threshold detector uses a smaller version of the main conversion circuit in combination with a digital comparator to detect when the magnitude of the input signal on channel 1 is beyond the defined threshold level. As with the main conversion circuit, there is a trade-off between speed and resolution with the threshold detector; selecting faster detection times exhibit more noise as the signal passes through the threshold, while slower detection times offer lower noise. Both the detection time and threshold level are programmable using bits 2 through 7 of configuration register 2, as shown in Tables 7 and 8 below.

As with the over-range detector, the adjustable threshold detector continuously monitors channel 1 independent of which channel is selected with the CHAN signal. This allows continuous monitoring of channel 1 for faults while converting Channel 2.

Table 7. Threshold Detection Configuration.

Threshold Detection Time	Configuration Data Bits	
	Bit 7	Bit 6
2 - 6 µs	Low	Low
3 - 10 µs	Low	High
5 - 20 µs	***High***	***Low***
10 - 35 µs	High	High

Note: Bold italic type indicates default values.

Table 8. Threshold Level Configuration.

Threshold Level	Configuration Data Bits			
	Bit 5	Bit 4	Bit 3	Bit 2
±160 mV	***Low***	***Low***	***Low***	***Low***
± 170 mV	Low	Low	Low	High
± 180 mV			High	Low
± 190 mV				High
± 200 mV		High	Low	Low
± 210 mV				High
± 220 mV			High	Low
± 230 mV				High
± 240 mV	High	Low	Low	Low
± 250 mV				High
± 260 mV			High	Low
± 270 mV				High
± 280 mV		High	Low	Low
± 290 mV				High
± 300 mV			High	Low
± 310 mV				High

Note: Bold italic type indicates default values.

Analog Interfacing

Power Supplies and Bypassing

The recommended application circuit is shown in Figure 21. A floating power supply (which in many applications could be the same supply that is used to drive the high-side power transistor) is regulated to 5 V using a simple zener diode (D1); the value of resistor R1 should be chosen to supply sufficient current from the existing floating supply. The voltage from the current sensing resistor or shunt (Rsense) is applied to the input of the HCPL-7860 (U2) through an RC anti-aliasing filter (R2 and C2). And finally, the output clock and data of the isolated modulator are connected to the digital interface IC. Although the application circuit is relatively simple, a few recommendations should be followed to ensure optimal performance.

The power supply for the isolated modulator is most often obtained from the same supply used to power the power transistor gate drive circuit. If a dedicated supply is required, in many cases it is possible to add an additional winding on an existing transformer. Otherwise, some sort of simple isolated supply can be used, such as a line powered transformer or a high-frequency DC-DC converter.

An inexpensive 78L05 three-terminal regulator can also be used to reduce the floating supply voltage to 5 V. To help attenuate high-frequency power supply noise or ripple, a resistor or inductor can be used in series with the input of the regulator to form a low-pass filter with the regulator's input bypass capacitor.

As shown in Figure 21, 0.1 µF bypass capacitors (C1 and C3) should be located as close as possible to the input and output power-supply pins of the isolated modulator (U2). The bypass capacitors are required because of the high-speed digital nature of the signals inside the isolated modulator. A 0.01 µF bypass capacitor (C2) is also recommended at the input due to the switched-capacitor nature of the input circuit. The input bypass capacitor also forms part of the anti-aliasing filter, which is recommended to prevent high-frequency noise from aliasing down to lower frequencies and interfering with the input signal.

PC Board Layout

The design of the printed circuit board (PCB) should follow good layout practices, such as keeping bypass capacitors close to the supply pins, keeping output signals away from input signals, the use of ground and power planes, etc. In addition, the layout of the PCB can also affect the isolation transient immunity (CMR) of the isolated modulator, due primarily to stray capacitive coupling between the input and the output circuits. To obtain optimal CMR performance, the layout of the PC board should minimize any stray coupling by maintaining the maximum possible distance between the input and output sides of the circuit and ensuring

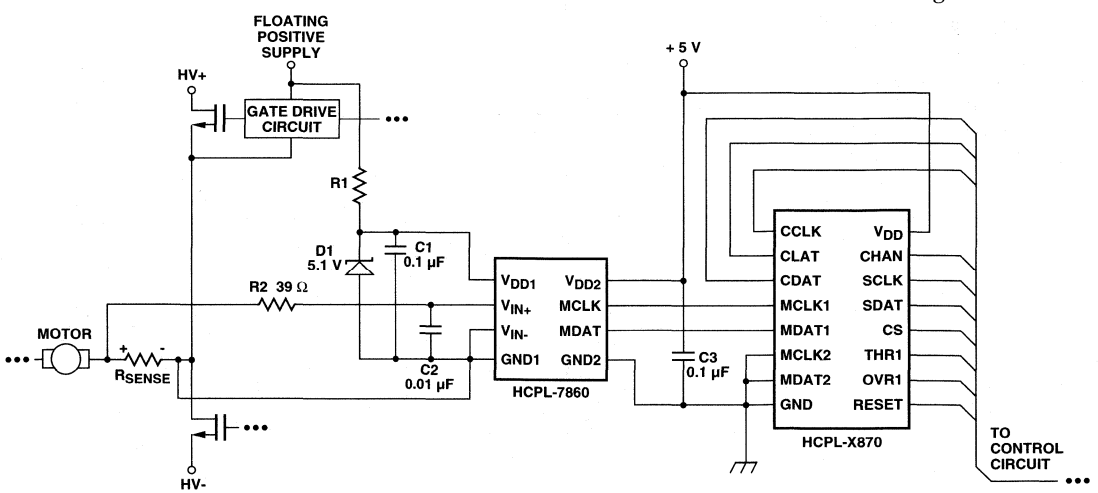


Figure 21. Recommended Application Circuit.

that any ground or power plane on the PC board does not pass directly below or extend much wider than the body of the isolated modulator.

Shunt Resistors

The current-sensing shunt resistor should have low resistance (to minimize power dissipation), low inductance (to minimize di/dt induced voltage spikes which could adversely affect operation), and reasonable tolerance (to maintain overall circuit accuracy). Choosing a particular value for the shunt is usually a compromise between minimizing power dissipation and maximizing accuracy. Smaller shunt resistances decrease power dissipation, while larger shunt resistances can improve circuit accuracy by utilizing the full input range of the isolated modulator.

The first step in selecting a shunt is determining how much current the shunt will be sensing. The graph in Figure 22 shows the RMS current in each phase of a three-phase induction motor as a function of average motor output power (in horsepower, hp) and motor drive supply voltage. The

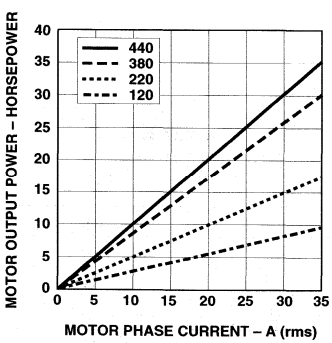


Figure 22. Motor Output Horsepower vs. Motor Phase Current and Supply Voltage.

maximum value of the shunt is determined by the current being measured and the maximum recommended input voltage of the isolated modulator. The maximum shunt resistance can be calculated by taking the maximum recommended input voltage and dividing by the peak current that the shunt should see during normal operation. For example, if a motor will have a maximum RMS current of 10 A and can experience up to 50% overloads during normal operation, then the peak current is 21.1 A (=10x1.414x1.5). Assuming a maximum input voltage of 200 mV, the maximum value of shunt resistance in this case would be about 10 mΩ.

The maximum average power dissipation in the shunt can also be easily calculated by multiplying the shunt resistance times the square of the maximum RMS current, which is about 1 W in the previous example.

If the power dissipation in the shunt is too high, the resistance of the shunt can be decreased below the maximum value to decrease power dissipation. The minimum value of the shunt is limited by precision and accuracy requirements of the design. As the shunt value is reduced, the output voltage across the shunt is also reduced, which means that the offset and noise, which are fixed, become a larger percentage of the signal amplitude. The selected value of the shunt will fall somewhere between the minimum and maximum values, depending on the particular requirements of a specific design.

When sensing currents large enough to cause significant heating of the shunt, the temperature coefficient (tempco) of the shunt can introduce nonlinearity due to the signal dependent temperature rise of the shunt. The effect increases as the shunt-to-ambient thermal resistance increases. This effect can be minimized either by reducing the thermal resistance of the shunt or by using a shunt with a lower tempco. Lowering the thermal resistance can be accomplished by repositioning the shunt on the PC board, by using larger PC board traces to carry away more heat, or by using a heat sink.

For a two-terminal shunt, as the value of shunt resistance decreases, the resistance of the leads becomes a significant percentage of the total shunt resistance. This has two primary effects on shunt accuracy. First, the effective resistance of the shunt can become dependent on factors such as how long the leads are, how they are bent, how far they are inserted into the board, and how far solder wicks up the lead during assembly (these issues will be discussed in more detail shortly). Second, the leads are typically made from a material such as copper, which has a much higher tempco than the material from which the resistive element itself is made, resulting in a higher tempco for the shunt overall.

Both of these effects are eliminated when a four-terminal shunt is used. A four-terminal shunt has two additional terminals that are Kelvin-connected directly across the resistive element itself; these two terminals are used to monitor the voltage across the resistive element while the other two terminals are used to carry the load current. Because of the Kelvin connection, any voltage

drops across the leads carrying the load current should have no impact on the measured voltage.

Several four-terminal shunts from Isotek (Isabellenhütte) suitable for sensing currents in motor drives up to 71 A_{rms} (71 hp or 53 kW) are shown in Table 9; the maximum current and motor power range for each of the PBV-series shunts are indicated. For shunt resistances from 50 mΩ down to 10 mΩ, the maximum current is limited by the input voltage range of the isolated modulator. For the 5 mΩ and 2 mΩ shunts, a heat sink may be required due to the increased power dissipation at higher currents.

When laying out a PC board for the shunts, a couple of points should be kept in mind. The Kelvin connections to the shunt should be brought together under the body of the shunt and then run very close to each other to the input of the isolated modulator; this minimizes the loop area of the connection and reduces the possibility of stray magnetic fields from interfering with the measured signal. If the shunt is not located on the same PC board as the isolated modulator circuit, a tightly twisted pair of wires can accomplish the same thing.

Also, multiple layers of the PC board can be used to increase current carrying capacity. Numerous plated-through vias should surround each non-Kelvin terminal of the shunt to help distribute the current between the layers of the PC board. The PC board should use 2 or 4 oz. copper for the layers, resulting in a current carrying capacity in excess of 20 A. Making the current carrying traces on the PC board fairly large can also improve the shunt's power dissipation capability by acting as a heat sink. Liberal use of vias where the load current enters and exits the PC board is also recommended.

Shunt Connections

The recommended method for connecting the isolated modulator to the shunt resistor is shown in Figure 21. V_{IN+} (pin 2 of the HPCL-7860) is connected to the positive terminal of the shunt resistor, while V_{IN-} (pin 3) is shorted to GND1 (pin 4), with the power-supply return path functioning as the sense line to the negative terminal of the current shunt. This allows a single pair of wires or PC board traces to connect the isolated modulator circuit to the shunt resistor. By referencing the input circuit to the negative side of the sense resistor, any load current induced noise transients on the shunt are seen as a common-mode signal and will not interfere with the current-sense signal. This is important because the large load currents flowing through the motor drive, along with the parasitic inductances inherent in the wiring of the circuit, can generate both noise spikes and offsets that are relatively large compared to the small voltages that are being measured across the current shunt.

If the same power supply is used both for the gate drive circuit and for the current sensing circuit, it is very important that the connection from GND1 of the isolated modulator to the sense resistor be the *only* return path for supply current to the gate drive power supply in order to eliminate potential ground loop problems. The only direct connection between the isolated modulator circuit and the gate drive circuit should be the positive power supply line.

Table 9. Isotek (Isabellenhütte) Four-Terminal Shunt Summary.

Shunt Resistor Part Number	Shunt Resistance	Tol.	Maximum RMS Current	Motor Power Range 120 V_{ac}-440 V_{ac}	
	mΩ	%	A	hp	kW
PBV-R050-0.5	50	0.5	3	0.8-3	0.6-2
PBV-R020-0.5	20	0.5	7	2-7	1.4-5
PBV-R010-0.5	10	0.5	14	4-14	3-10
PBV-R005-0.5	5	0.5	25 [28]	7-25 [8-28]	5-19 [6-21]
PBV-R002-0.5	2	0.5	39 [71]	11-39 [19-71]	8-29 [14-53]

Note: Values in brackets are with a heatsink for the shunt.

In some applications, however, supply currents flowing through the power-supply return path may cause offset or noise problems. In this case, better performance may be obtained by connecting V_{IN+} and V_{IN-} directly across the shunt resistor with two conductors, and connecting GND1 to the shunt resistor with a third conductor for the power-supply return path, as shown in Figure 23. When connected this way, both input pins should be bypassed. To minimize electromagnetic interference of the sense signal, all of the conductors (whether two or three are used) connecting the isolated modulator to the sense resistor should be either twisted pair wire or closely spaced traces on a PC board.

The 39 Ω resistor in series with the input lead (R2) forms a low-pass anti-aliasing filter with the 0.01 µF input bypass capacitor (C2) with a 400 kHz bandwidth. The resistor performs another important function as well; it dampens any ringing which might be present in the circuit formed by the shunt, the input bypass capacitor, and the inductance of wires or traces connecting the two. Undamped ringing of the input circuit near the input sampling frequency can alias into the baseband producing what might appear to be noise at the output of the device.

Voltage Sensing

The HCPL-7860 Isolated Modulator can also be used to isolate signals with amplitudes larger than its recommended input range with the use of a resistive voltage divider at its input. The only restrictions are that the impedance of the divider be relatively small (less than 1 kΩ) so that the input resistance (280 kΩ) and input bias current (1 µA) do not affect the accuracy of the measurement. An input bypass capacitor is still required, although the 39 Ω series damping resistor is not (the resistance of the voltage divider provides the same function). The low-pass filter formed by the divider resistance and the input bypass capacitor may limit the achievable bandwidth. To obtain higher bandwidth, the input bypass capacitor (C2) can be reduced, but it should not be reduced much below 1000 pF to maintain adequate input bypassing of the isolated modulator.

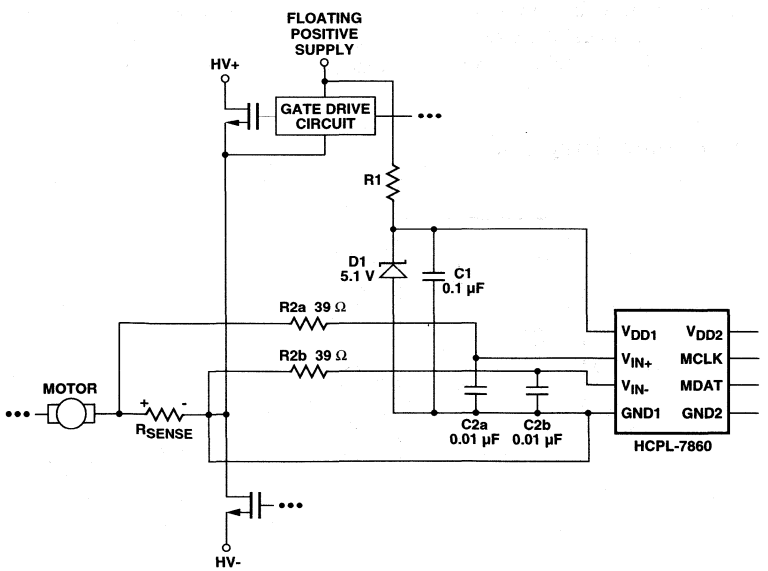


Figure 23. Schematic for Three Conductor Shunt Connection.

HEWLETT® PACKARD

8 MBd Low Input Current Optocoupler

Technical Data

HCPL-2300

Features

- **Guaranteed Low Thresholds: I_F = 0.5 mA, $V_F \leq 1.5$ V**
- **High Speed: Guaranteed 5 MBd over Temperature**
- **Versatile: Compatible with TTL, LSTTL and CMOS**
- **Efficient 820 nm AlGaAs LED**
- **Internal Shield for Guaranteed Common Mode Rejection**
- **Schottky Clamped, Open Collector Output with Optional Integrated Pull-Up Resistor**
- **Static and Dynamic Performance Guaranteed from -40°C to 85°C**
- **Safety Approval**
  UL Recognized -2500 V rms for 1 minute
  CSA Approved
  VDE 0884 Approved with V_{IORM} = 630 V peak (Option 060)

Applications

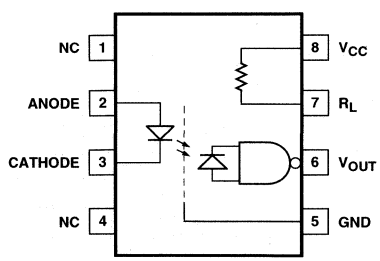
- **Ground Loop Elimination**
- **Computer-Peripheral Interfaces**
- **Level Shifting**
- **Microprocessor System Interfaces**
- **Digital Isolation for A/D, D/A Conversion**
- **RS-232-C Interface**
- **High Speed, Long Distance Isolated Line Receiver**

Description

The HCPL-2300 optocoupler combines an 820 nm AlGaAs photon emitting diode with an integrated high gain photon detector. This combination of Hewlett-Packard designed and manufactured semiconductor devices brings new high performance capabilities to designers of isolated logic and data communication circuits.

The new low current, high speed AlGaAs emitter manufactured with a unique diffused junction, has the virtue of fast rise and fall times at low drive currents. Figure 6 illustrates the propagation delay vs. input current characteristic. These unique

Functional Diagram



A 0.1 pF bypass capacitor must be connected between pins 5 and 8.

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

5965-3587E

characteristics enable this device to be used in an RS-232-C interface with ground loop isolation and improved common mode rejection. As a line receiver, the HCPL-2300 will operate over longer line lengths for a given data rate because of lower I_F and V_F specifications.

The output of the shielded integrated detector circuit is an open collector Schottky clamped transistor. The shield, which shunts capacitively coupled common mode noise to ground, provides a guaranteed transient immunity specification of 100 V/μs. The output circuit includes an optional integrated 1000 Ω pull-up resistor for the open collector. This gives designers the flexibility to use the internal resistor for pull-up to five volt logic or to use an external resistor for connection to supply voltages up to 18 V (CMOS logic voltage).

The Electrical and Switching Characteristics of the HCPL-2300 are guaranteed over a temperature range of -40°C to 85°C. This enables the user to confidently design a circuit which will operate under a broad range of operating conditions.

Ordering Information

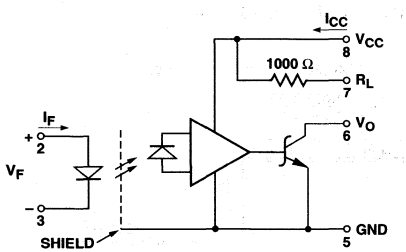
Specify part number followed by Option Number (if desired).

HCPL-2300# XXX

- 060 = VDE 0884 V_{IORM} = 630 V peak Option
- 300 = Gull Wing Surface Mount Lead Option
- 500 = Tape/Reel Package Option (1 K min)

Option data sheets available. Contact your Hewlett-Packard sales representative or authorized distributor for information.

Schematic



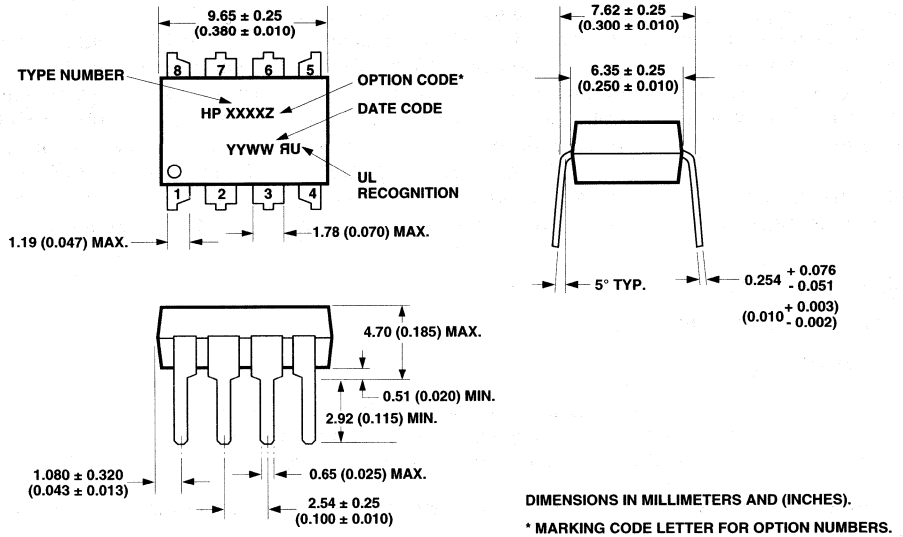
A 0.1 μF CAPACITOR MUST BE CONNECTED BETWEEN PINS 8 AND 5 (SEE NOTE 1).

TRUTH TABLE (POSITIVE LOGIC)

LED	OUTPUT
ON	L
OFF	H

Package Outline Drawings

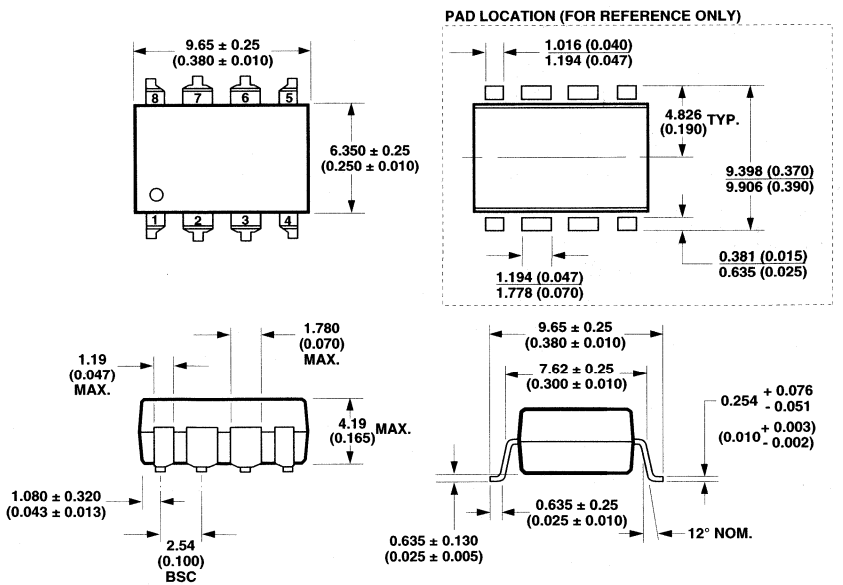
8-Pin DIP Package (HCPL-2300)



DIMENSIONS IN MILLIMETERS AND (INCHES).

* MARKING CODE LETTER FOR OPTION NUMBERS.
"V" = OPTION 060
OPTION NUMBERS 300 AND 500 NOT MARKED.

8-Pin DIP Package with Gull Wing Surface Mount Option 300 (HCPL-2300)



DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES).

Thermal Profile (Option #300)

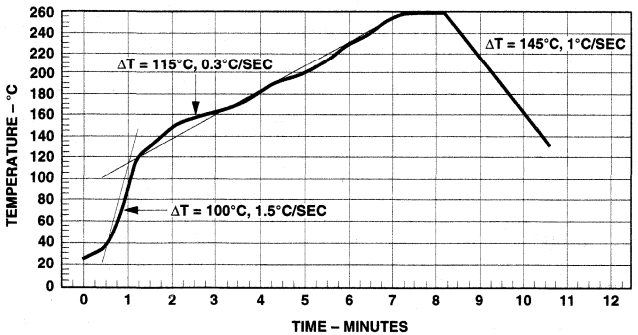


Figure 1. Maximum Solder Reflow Thermal Profile.
(Note: Use of non-chlorine activated fluxes is recommended.)

Regulatory Information

The HCPL-2300 has been approved by the following organizations:

CSA

Approved under CSA Component Acceptance Notice #5, File CA 88324.

UL

Recognized under UL 1577, Component Recognition Program, File E55361.

VDE

Approved according to VDE 0884/06.92 (Option 060 only)

Insulation and Safety Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min. External Air Gap (External Clearance)	L(IO1)	7.1	mm	Measured from input terminals to output terminals, shortest distance through air
Min. External Tracking Path (External Creepage)	L(IO2)	7.4	mm	Measured from input terminals to output terminals, shortest distance path along body
Min. Internal Plastic Gap (Internal Clearance)		0.08	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity
Tracking Resistance (Comparative Tracking Index)	CTI	200	Volts	DIN IEC 112/VDE 0303 PART 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Option 300 – surface mount classification is Class A in accordance with CECC 00802.

VDE 0884 Insulation Related Characteristics (HCPL-2300 Option 060 ONLY)

Description	Symbol	Characteristic	Units
Installation classification per DIN VDE 0110/1.89, Table 1			
for rated mains voltage ≤ 300 V rms		I-IV	
for rated mains voltage ≤ 450 V rms		I-III	
Climatic Classification		55/85/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	630	V_{peak}
Input to Output Test Voltage, Method b* V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial Discharge < 5 pC	V_{PR}	1181	V_{peak}
Input to Output Test Voltage, Method a* V_{IORM} x 1.5 = V_{PR}, Type and sample test, t_m = 60 sec, Partial Discharge < 5 pC	V_{PR}	945	V_{peak}
Highest Allowable Overvoltage* (Transient Overvoltage, t_{ini} = 10 sec)	V_{IOTM}	6000	V_{peak}
Safety Limiting Values (Maximum values allowed in the event of a failure, also see Figure 11, Thermal Derating curve.)			
Case Temperature	T_S	175	°C
Input Current	$I_{S,INPUT}$	230	mA
Output Power	$P_{S,OUTPUT}$	600	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	$\geq 10^9$	Ω

*Refer to the front of the optocoupler section of the current catalog, under Product Safety Regulations section, (VDE 0884), for a detailed description.

Note: Isolation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuits in application.

Absolute Maximum Ratings

(No Derating Required up to 55°C)

Storage Temperature, T_S ..... -55°C to +125°C
Operating Temperature, T_A ..... -40°C to +85°C
Lead Solder Temperature, max ..... 260°C for 10 s
(1.6 mm below seating plane)
Average Forward Input Current - I_F ..... 5 mA[2]
Reverse Input Voltage, V_R ..... 3.0 V
Supply Voltage, V_{CC} ..... 0 V to 7.0 V
Pull-Up Resistor Voltage, V_{RL} ..... -0.5 V to V_{CC}
Output Collector Current, I_O ..... -25 to 25 mA
Input Power Dissipation, P_I ..... 10 mW
Output Collector Power Dissipation, P_O ..... 40 mW
Output Collector Voltage, V_O ..... -0.5 V to 18 V
Infrared and Vapor Phase Reflow Temperature
(Option #300) ..... see Fig. 1, Thermal Profile

Recommended Operating Conditions

Parameter		Symbol	Min.	Max.	Units
Input Voltage, Low Level		V_{FL}	-2.5	0.8	V
Input Current High Level	0°C to 85°C	I_{FH}	0.5	1.0	mA
	-40°C to 85°C		0.5	0.75	
Supply Voltage, Output		V_{CC}	4.75	5.25	V
Fan Out (TTL Load)		N		5	
Operating Temperature		T_A	-40	85	°C

DC Electrical Specifications

For -40°C ≤ T_A ≤ 85°C, 4.75 V ≤ V_{CC} ≤ 5.25 V, V_{FL} ≤ 0.8 V, unless otherwise specified.
All typicals at T_A = 25°C and V_{CC} = 5 V, unless otherwise specified. See note 1.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
High Level Output Current	I_{OH}		0.05	250	µA	V_F = 0.8 V, V_O = 18 V	4	
Low Level Output Voltage	V_{OL}		0.4	0.5	V	I_F = 0.5 mA I_{OL} (Sinking) = 8 mA	3	
High Level Supply Current	I_{CCH}		4.0	6.3	mA	I_F = 0 mA, V_{CC} = 5.25 V		
Low Level Supply Current	I_{CCL}		6.2	10.0	mA	I_F = 1.0 mA, V_{CC} = 5.25 V		
Input Forward Voltage	V_F	1.0	1.3	1.5	V	T_A = 25°C | I_F = 1.0 mA	2	
		0.85		1.65				
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$		-1.6		mV/°C	I_F = 1.0 mA		
Input Reverse Breakdown Voltage	BV_R	3.0			V	I_R = 10 µA		
Input Capacitance	C_{IN}		18		pF	V_F = 0 V, f = 1 MHz		
Internal Pull-up Resistor	R_L	680	1000	1700	Ω	T_A = 25°C		

Switching Specifications

For -40°C ≤ T_A ≤ 85°C, 0.5 mA ≤ I_{FH} ≤ 0.75 mA;
For 0°C ≤ T_A ≤ 85°C, 0.5 mA ≤ I_{FH} ≤ 1.0 mA; With 4.75 V ≤ V_{CC} ≤ 5.25 V, V_{FL} ≤ 0.8 V, unless otherwise specified. All typicals at T_A = 25°C and V_{CC} = 5 V, I_{FH} = 0.625 mA, unless otherwise specified. See note 1.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to Logic High Output Level	t_{PLH}		95		ns	C_P = 0 pF	5, 6, 8	4, 8
			85	160		C_P = 20 pF	5, 8	
Propagation Delay Time to Logic Low Output Level	t_{PHL}		110		ns	C_P = 0 pF	5, 6, 8	5, 8
			35	200		C_P = 20 pF	5, 8	
Output Rise Time (10-90%)	t_r		40		ns	C_P = 20 pF	7, 8	8
Output Fall Time (90-10%)	t_f		20		ns			
Common Mode Transient Immunity at High Output Level	$\|CM_H\|$	100	400		V/µs	V_{CM} = 50 V (peak), V_O (min.) = 2 V, R_L = 560 Ω, I_F = 0 mA	9, 10	6
Common Mode Transient Immunity at Low Output Level	$\|CM_L\|$	100	400		V/µs	V_{CM} = 50 V (peak), V_O (max.) = 0.8 V, R_L = 560 Ω, I_F = 0.5 mA	9, 10	7

Package Characteristics

For -40°C ≤ T_A ≤ 85°C, unless otherwise specified. All typicals at T_A = 25°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Notes
Input-Output Momentary Withstand Voltage*	V_{ISO}	2500			V rms	RH ≤ 50%, t = 1 min, T_A = 25°C		3, 9
Resistance, Input-Output	R_{I-O}		10^{12}		Ω	V_{I-O} = 500 V		3
Capacitance, Input-Output	C_{I-O}		0.6		pF	f = 1 MHz		3

*The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the VDE 0884 Insulation Characteristics Table (if applicable), your equipment level safety specification, or HP Application Note 1074, "Optocoupler Input-Output Endurance Voltage."

Notes:

1. Bypassing the power supply line is required with a 0.1 µF ceramic disc capacitor adjacent to each optocoupler as illustrated in Figure 19. The power supply bus for the optocoupler(s) should be separate from the bus for any active loads, otherwise a larger value of bypass capacitor (up to 0.5 µF) may be needed to suppress regenerative feedback via the power supply.
2. Peaking circuits may produce transient input currents up to 100 mA, 500 ns maximum pulse width, provided average current does not exceed 5 mA.
3. Device considered a two terminal device: pins 1, 2, 3, and 4 shorted together, and pins 5, 6, 7, and 8 shorted together.
4. The t_{PLH} propagation delay is measured from the 50% point on the trailing edge of the input pulse to the 1.5 V point on the trailing edge of the output pulse.
5. The t_{PHL} propagation delay is measured from the 50% point on the leading edge of the input pulse to the 1.5 V point on the leading edge of the output pulse.
6. CM_H is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state (i.e., V_{OUT} > 2.0 V).
7. CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state (i.e., V_{OUT} < 0.8 V).
8. C_P is the peaking capacitance. Refer to test circuit in Figure 8.
9. In accordance with UL 1577, each optocoupler is momentary withstand proof tested by applying an insulation test voltage ≥ 3000 Vrms for 1 second (leakage detection current limit, I_{I-O} ≤ 5 µA). This test is performed before the 100% production test for partial discharge (Method b) shown in the VDE 0884 Insulation Characteristics Table, if applicable.

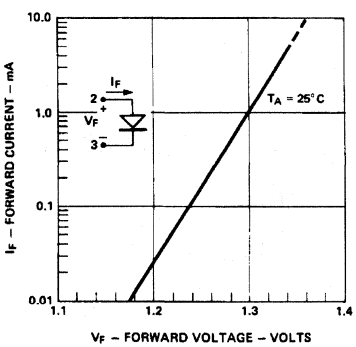


Figure 2. Typical Input Diode Forward Characteristics.

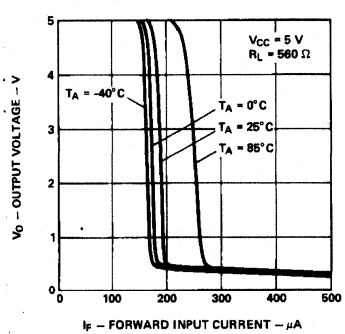


Figure 3. Typical Output Voltage vs. Forward Input Current vs. Temperature.

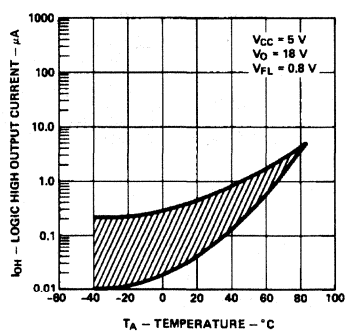


Figure 4. Typical Logic High Output Current vs. Temperature.

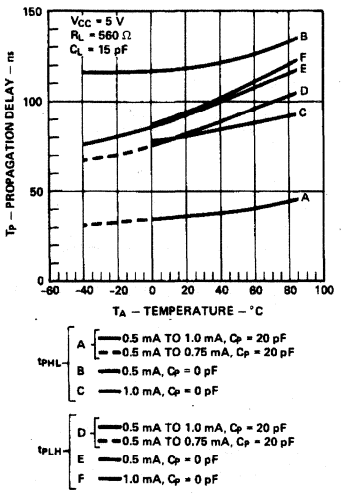


Figure 5. Typical Propagation Delay vs. Temperature and Forward Current with and without Application of a Peaking Capacitor.

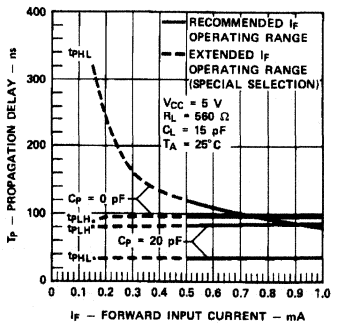


Figure 6. Typical Propagation Delay vs. Forward Current.

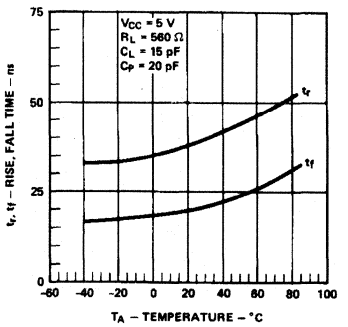


Figure 7. Typical Rise, Fall Time vs. Temperature.

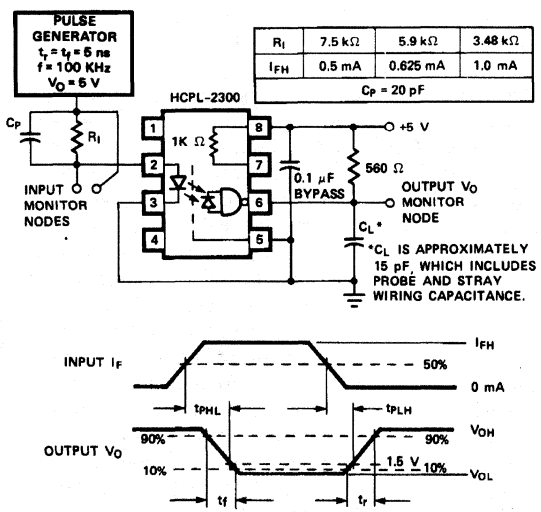


Figure 8. Test Circuit for t_{PHL}, t_{PLH}, t_r, and t_f.

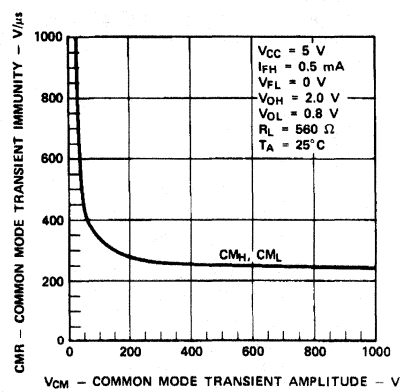


Figure 9. Typical Common Mode Transient Immunity vs. Common Mode Transient Amplitude.

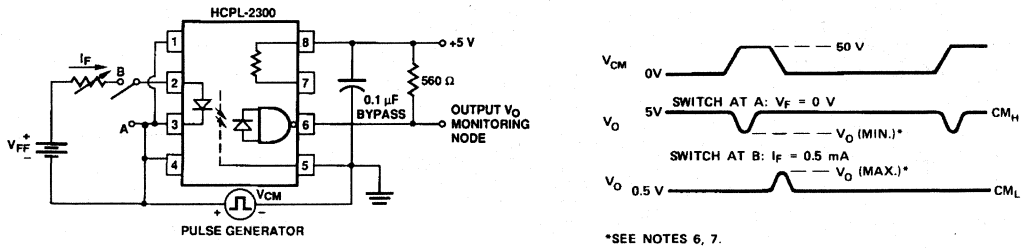


Figure 10. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

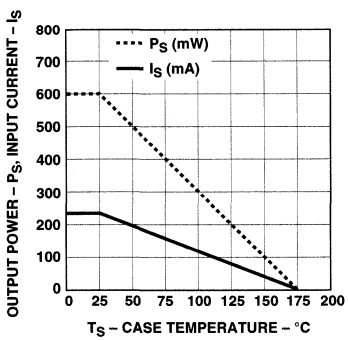


Figure 11. Thermal Derating Curve, Dependence of Safety Limiting Value with Case Temperature per VDE 0884.

Applications

The HCPL-2300 optocoupler has the unique combination of low 0.5 mA LED operating drive current at a 5 MBd speed performance. Low power supply current requirement of 10 mA maximum at 5.25 V and the ability to provide isolation between logic systems fulfills numerous applications ranging from logic level translations, line receiver and party line receiver applications, microprocessor I/O port isolation, etc. The open collector output allows for wired-OR arrangement. Specific interface circuits are illustrated in Figures 12-16, and 18 with corresponding component values, performance data and recommended layout in Figures 17 and 19.

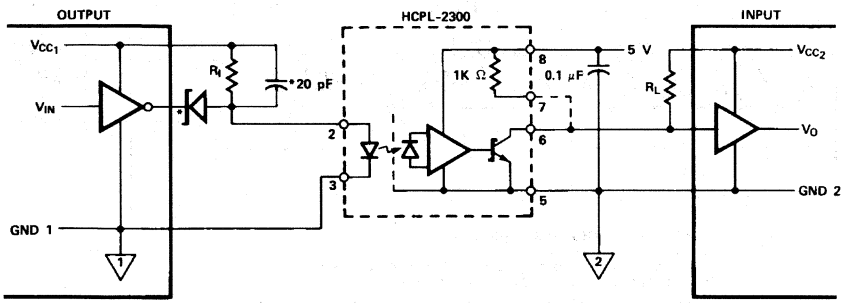
For -40°C to 85°C operating temperature range, a mid-range LED forward current (I_F) of 0.625 mA is recommended in order to prevent overdriving the integrated circuit detector due to increased LED efficiency at temperatures between 0°C and -40°C. For narrower temperature range of 0°C to 85°C, a suggested operating LED current of 0.75 mA is recommended for the mid-range operating point and for minimal propagation delay skew. A peaking capacitance of 20 pF in parallel with the current limiting resistor for the LED shortens t_{PHL} by approximately 33% and t_{PLH} by 13%. Maintaining LED forward voltage (V_F) below 0.8 V will guarantee that the HCPL-2300 output is off.

The recommended shunt drive technique for TTL/LSTTL/CMOS of Figure 12 provides for optimal speed performance, no leakage current path through the LED, and reduced common mode influences associated with series switching of a "floating" LED. Alternate series drive techniques with either an active CMOS inverter or an open collector TTL/LSTTL inverter are illustrated in Figures 13 and 14 respectively. Open collector leakage current of 250 μA has been compensated by the 3.16 KΩ resistor (Figure 14) at the expense of twice the operating forward current.

An application of the HCPL-2300 as an unbalanced line receiver for use in long line twisted wire pair communication links is shown in Figure 15. Low LED I_F and V_F allow longer line length, higher speed and multiple stations on the line in comparison to higher I_F, V_F optocouplers. Greater speed performance along with nearly infinite common mode immunity are achieved via the balanced split phase circuit of Figure 16. Basic balanced differential line receiver can be accomplished with one HCPL-2300 in Figure 16, but with a typical 400 V/μs common mode immunity. Data rate versus distance for both the above unbalanced and balanced line receiver applications are compared in Figure 17. The RS-232-C interface circuit of Figure 18

provides guaranteed minimum common mode immunity of 100 V/μs while maintaining the 2:1 dynamic range of I_F.

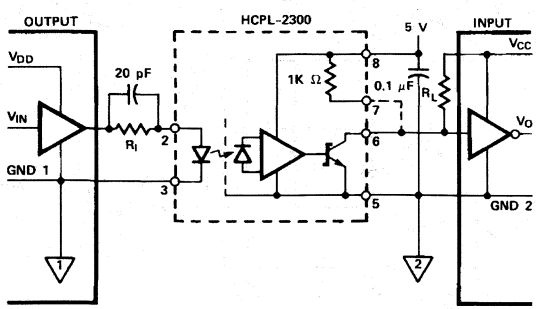
A recommended layout for use with an internal 1000 Ω resistor or an external pull-up resistor and required V_{CC} bypass capacitor is given in Figure 19. V_{CC1} is used with an external pull-up resistor for output voltage levels (V_O) greater than or equal to 5 V. As illustrated in Figure 19, an optional V_{CC} and GND trace can be located between the input and the output leads of the HCPL-2300 to provide additional noise immunity at the compromise of insulation capability (V_{I-O}).



V_{IN} V_{DC}	V_{CC1} V_{DC}	R_I kΩ	R_L kΩ	V_{CC2} V_{DC}
5	5	6.19	1 (INTERNAL)	5
10	10	14.7	2.37	10
15	15	21.5	3.16	15

*SCHOTTKY DIODE (HP 5082-2800, OR EQUIVALENT) AND 20 pF CAPACITOR ARE NOT REQUIRED FOR UNITS WITH OPEN COLLECTOR OUTPUT.

Figure 12. Recommended Shunt Drive Circuit for Interfacing between TTL/LSTTL/CMOS Logic Systems.



V_{IN} V_{DC}	V_{DD} V_{DC}	R_I kΩ	R_L kΩ	V_{CC} V_{DC}
5	5	5.11	1 (INTERNAL)	5
10	10	13.3	2.37	10
15	15	19.6	3.16	15

Figure 13. Active CMOS Series Drive Circuit.

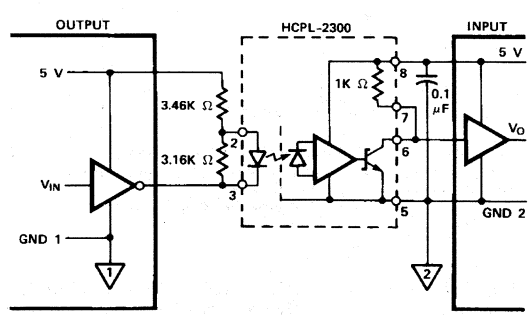


Figure 14. Series Drive from Open Collector TTL/LSTTL Units.

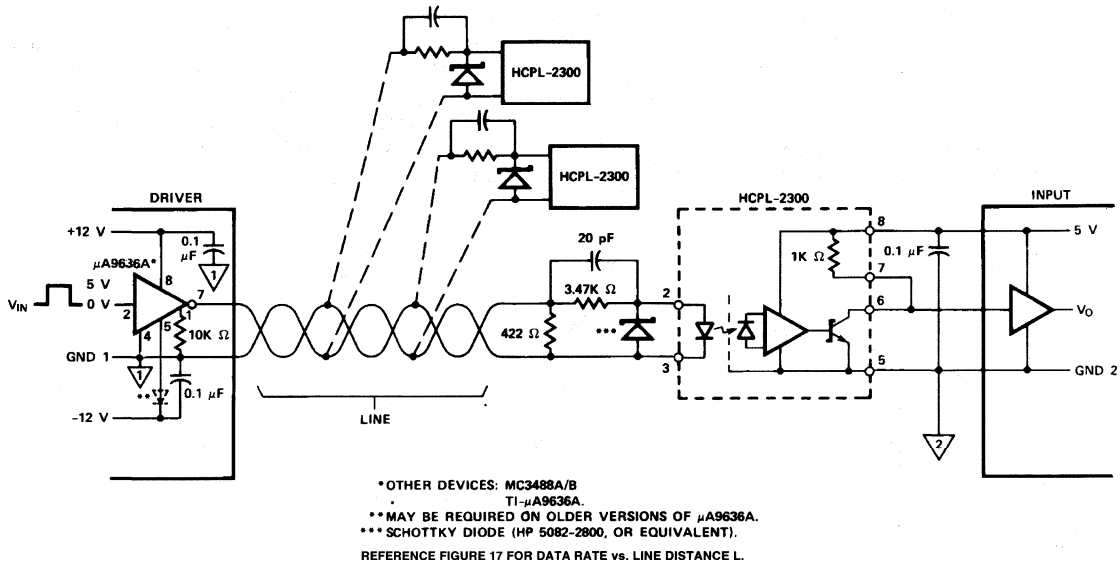


Figure 15. Application of HCPL-2300 as Isolated, Unbalanced Line Receiver(s).

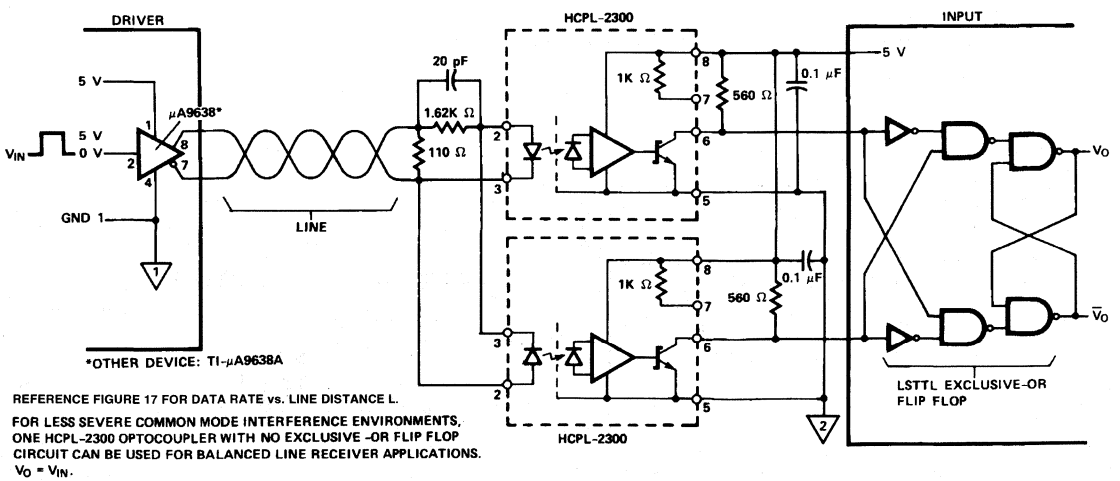


Figure 16. Application of Two HCPL-2300 Units Operating as an Isolated, High Speed, Balanced, Split Phase Line Receiver with Significantly Enhanced Common Mode Immunity.

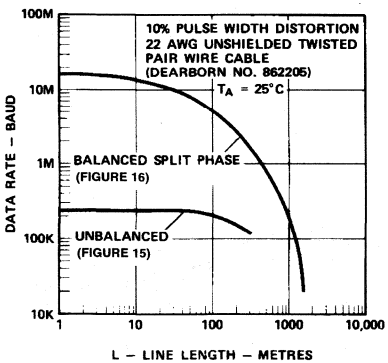


Figure 17. Typical Point to Point Data Rate vs. Length of Line for Unbalanced (Figure 15) and Balanced (Figure 16) Line Receivers Using HCPL-2300 Optocouplers.

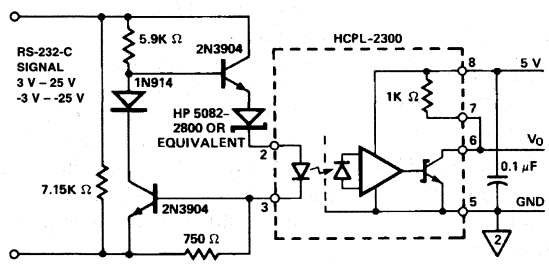


Figure 18. RS-232-C Interface Circuit with HCPL-2300. $0°C < T_A < 85°C$.

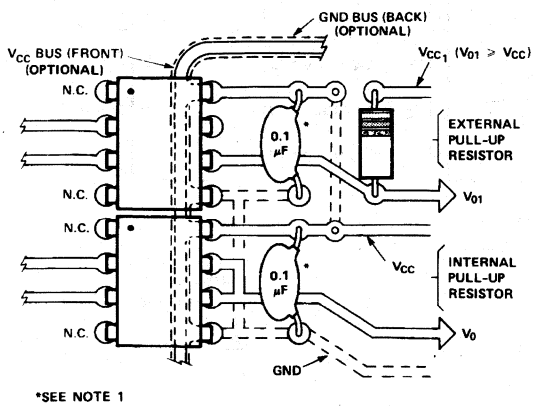


Figure 19. Recommended Printed Circuit Board Layout.

HEWLETT® PACKARD

20 MBd High CMR Logic Gate Optocouplers

Technical Data

HCPL-2400
HCPL-2430

Features

- **High Speed: 40 MBd Typical Data Rate**
- **High Common Mode Rejection:**
  HCPL-2400: 10 kV/µs at V_{CM} = 300 V (Typical)
- **AC Performance Guaranteed over Temperature**
- **High Speed AlGaAs Emitter**
- **Compatible with TTL, STTL, LSTTL, and HCMOS Logic Families**
- **Totem Pole and Tri State Output (No Pull Up Resistor Required)**
- **Safety Approval**
  UL Recognized – 2500 V rms for 1 minute per UL1577
  VDE 0884 Approved with V_{IORM} = 630 V peak (Option 060) for HCPL-2400
  CSA Approved
- **High Power Supply Noise Immunity**
- **MIL-STD-1772 Version Available (HCPL-5400/1 and HCPL-5430/1)**

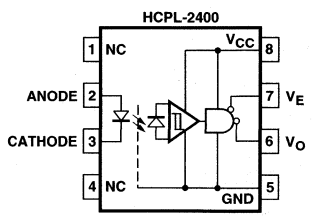
Applications

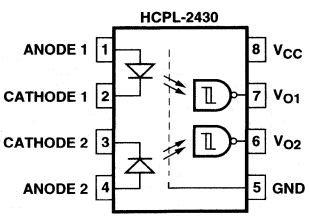
- **Isolation of High Speed Logic Systems**
- **Computer-Peripheral Interfaces**
- **Switching Power Supplies**
- **Isolated Bus Driver (Networking Applications)**
- **Ground Loop Elimination**
- **High Speed Disk Drive I/O**
- **Digital Isolation for A/D, D/A Conversion**
- **Pulse Transformer Replacement**

Description

The HCPL-2400 and HCPL-2430 high speed optocouplers combine an 820 nm AlGaAs light emitting diode with a high speed photodetector. This combination results in very high data rate capability and low input current. The totem pole output (HCPL-2430) or three state output (HCPL-2400) eliminates the need for a pull up resistor and allows for direct drive of data buses.

Functional Diagram





TRUTH TABLE (POSITIVE LOGIC)

LED	ENABLE	OUTPUT
ON	L	L
OFF	L	H
ON	H	Z
OFF	H	Z

TRUTH TABLE (POSITIVE LOGIC)

LED	OUTPUT
ON	L
OFF	H

A 0.1 µF bypass capacitor must be connected between pins 5 and 8.

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

5965-3586E

The detector has optical receiver input stage with built-in Schmitt trigger to provide logic compatible waveforms, eliminating the need for additional waveshaping. The hysteresis provides differential mode noise immunity and minimizes the potential for output signal chatter.

The electrical and switching characteristics of the HCPL-2400 and HCPL-2430 are guaranteed over the temperature range of 0°C to 70°C.

These optocouplers are compatible with TTL, STTL, LSTTL, and HCMOS logic families. When Schottky type TTL devices (STTL) are used, a data rate performance of 20 MBd over temperature is guaranteed when using the application circuit of Figure 13. Typical data rates are 40 MBd.

Selection Guide

8-Pin DIP (300 Mil)		Minimum CMR		Minimum Input On Current (mA)	Maximum Propagation Delay (ns)	Hermetic Package
Single Channel Package	Dual Channel Package	dV/dt (V/μs)	V_{CM} (V)			
HCPL-2400		1000	300	4	60	
	HCPL-2430	1000	50	4	60	
		500	50	6	60	HCPL-540X*
		500	50	6	60	HCPL-543X*
		500	50	6	60	HCPL-643X*

*Technical data for the Hermetic HCPL-5400/01, HCPL-5430/31, and HCPL-6430/31 are on separate HP publications.

Ordering Information

Specify Part Number followed by Option Number (if desired).

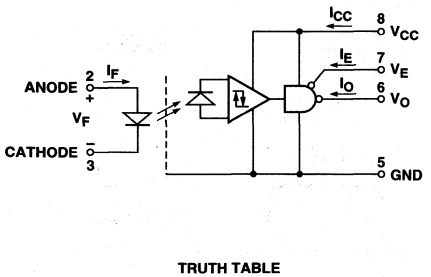
Example:

HCPL-2400#XXX

- 060 = VDE 0884 V_{IORM} = 630 V peak Option*
- 300 = Gull Wing Surface Mount Option
- 500 = Tape and Reel Packaging Option

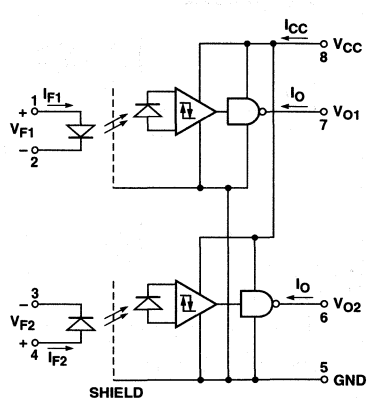
*For HCPL-2400 only.

Schematic



TRUTH TABLE (POSITIVE LOGIC)

LED	ENABLE	OUTPUT
ON	L	L
OFF	L	H
ON	H	Z
OFF	H	Z

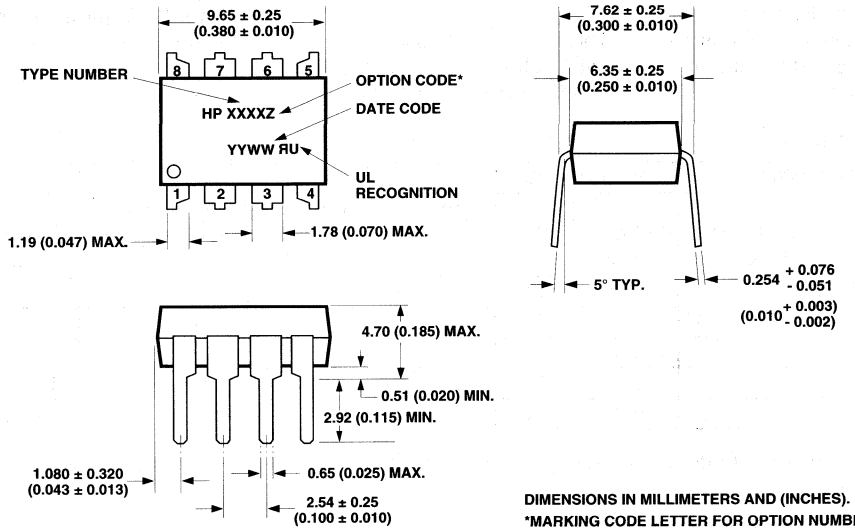


TRUTH TABLE (POSITIVE LOGIC)

LED	OUTPUT
ON	L
OFF	H

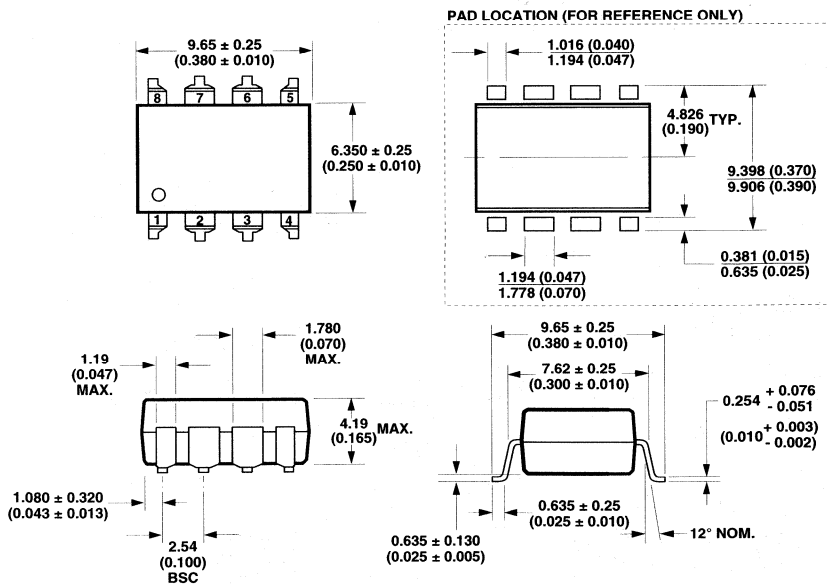
Package Outline Drawings

8-Pin DIP Package (HCPL-2400, HCPL-2430)



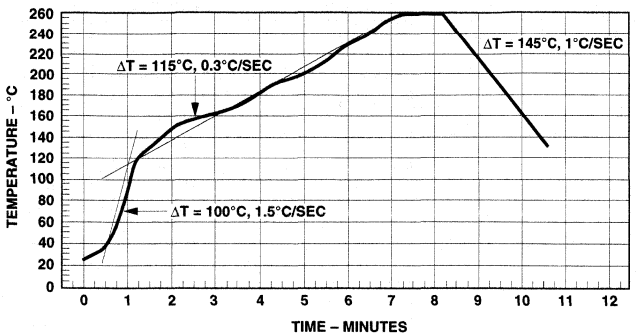
DIMENSIONS IN MILLIMETERS AND (INCHES).
*MARKING CODE LETTER FOR OPTION NUMBERS
"V" = OPTION 060
OPTION NUMBERS 300 AND 500 NOT MARKED.

8-Pin DIP Package with Gull Wing Surface Mount Option 300 (HCPL-2400, HCPL-2430)



DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES).

Solder Reflow Temperature Profile (Gull Wing Surface Mount Option 300 Parts)



Note: Use of nonchlorine activated fluxes is highly recommended.

Regulatory Information

The HCPL-24XX has been approved by the following organizations:

UL

Recognized under UL 1577, Component Recognition Program, File E55361.

VDE

Approved according to VDE 0884/06.92 (Option 060 only).

CSA

Approved under CSA Component Acceptance Notice #5, File CA 88324.

Insulation and Safety Related Specifications

Parameter	Symbol	Value	Units	Conditions
Minimum External Air Gap (External Clearance)	L(101)	7.1	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L(102)	7.4	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity.
Tracking Resistance (Comparative Tracking Index)	CTI	200	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Option 300 - surface mount classification is Class A in accordance with CECC 00802.

VDE 0884 Insulation Related Characteristics (HCPL-2400 OPTION 060 ONLY)

Description	Symbol	Characteristic	Units
Installation classification per DIN VDE 0110/1.89, Table 1			
for rated mains voltage ≤ 300 V rms		I-IV	
for rated mains voltage ≤ 450 V rms		I-III	
Climatic Classification		55/85/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	630	V peak
Input to Output Test Voltage, Method b* V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial Discharge < 5 pC	V_{PR}	1181	V peak
Input to Output Test Voltage, Method a* V_{IORM} x 1.5 = V_{PR}, Type and sample test, t_m = 60 sec, Partial Discharge < 5 pC	V_{PR}	945	V peak
Highest Allowable Overvoltage* (Transient Overvoltage, t_{ini} = 10 sec)	V_{IOTM}	6000	V peak
Safety Limiting Values (Maximum values allowed in the event of a failure, also see Figure 12, Thermal Derating curve.)			
Case Temperature	T_S	175	°C
Input Current	$I_{S,INPUT}$	230	mA
Output Power	$P_{S,OUTPUT}$	600	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	$\geq 10^9$	Ω

*Refer to the front of the optocoupler section of the current catalog, under Product Safety Regulations section (VDE 0884) for a detailed description.

Note: Isolation characteristics are guaranteed only within the safety maximum ratings which must ben ensured by protective circuits in application.

Absolute Maximum Ratings

(No derating required up to 70°C)

Parameter	Symbol	Minimum	Maximum	Units	Note
Storage Temperature	T_S	-55	125	°C	
Operating Temperature	T_A	-40	85	°C	
Average Forward Input Current	$I_{F(AVG)}$		10	mA	
Peak Forward Input Current	I_{FPK}		20	mA	12
Reverse Input Voltage	V_R		2	V	
Three State Enable Voltage (HCPL-2400 Only)	V_E	-0.5	10	V	
Supply Voltage	V_{CC}	0	7	V	
Average Output Collector Current	I_O	-25	25	mA	
Output Collector Voltage	V_O	-0.5	10	V	
Output Voltage	V_O	-0.5	18	V	
Output Collector Power Dissipation (Each Channel)	P_O		40	mW	
Total Package Power Dissipation (Each Channel)	P_T		350	mW	
Lead Solder Temperature (for Through Hole Devices)	260°C for 10 sec., 1.6 mm below seating plane				
Reflow Temperature Profile (Option #300)	See **Package Outline Drawings** section				

Recommended Operating Conditions

Parameter	Symbol	Minimum	Maximum	Units
Power Supply Voltage	V_{CC}	4.75	5.25	V
Forward Input Current (ON)	$I_{F(ON)}$	4	8	mA
Forward Input Voltage (OFF)	$V_{F(OFF)}$		0.8	V
Fan Out	N		5	TTL Loads
Enable Voltage (Low) HCPL-2400 Only)	V_{EL}	0	0.8	V
Enable Voltage (High) HCPL-2400 Only)	V_{EH}	2	V_{CC}	V
Operating Temperature	T_A	0	70	°C

Electrical Specifications

$0°C \le T_A \le 70°C$, $4.75\ V \le V_{CC} \le 5.25\ V$, $4\ mA \le I_{F(ON)} \le 8\ mA$, $0\ V \le V_{F(OFF)} \le 0.8\ V$. All typicals at $T_A = 25°C$, $V_{CC} = 5\ V$, $I_{F(ON)} = 6.0\ mA$, $V_{F(OFF)} = 0\ V$, except where noted. See Note 11.

Parameter	Symbol	Device HCPL-	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Logic Low Output Voltage	V_{OL}				0.5	V	I_{OL} = 8.0 mA (5 TTL Loads)	1	
Logic High Output Voltage	V_{OH}		2.4 2.7			V	I_{OH} = -4.0 mA I_{OH} = -0.4 mA	2	
Output Leakage Current	I_{OHH}				100	µA	V_O = 5.25 V, V_F = 0.8 V		
Logic High Enable Current	V_{EH}	2400	2.0			V			
Logic Low Enable Voltage	V_{EL}	2400			0.8	V			
Logic High Enable Current	I_{EH}	2400			20	µA	V_E = 2.4 V		
					100		V_E = 5.25 V		
Logic Low Enable Current	I_{EL}	2400		-0.28	-0.4	mA	V_E = 0.4 V		
Logic Low Supply Current	I_{CCL}	2400		19	26	mA	V_{CC} = 5.25 V, V_E = 0 V, I_O = Open		
		2430		34	46		V_{CC} = 5.25 V, I_O = Open		
Logic High Supply Current	I_{CCH}	2400		17	26	mA	V_{CC} = 5.25 V, V_E = 0 V, I_O = Open		
		2430		32	42		V_{CC} = 5.25 V, I_O = Open		
High Impedance State Supply Current	I_{CCZ}	2400		22	28	mA	V_{CC} = 5.25 V, V_E = 5.25 V		
High Impedance State Output Current	I_{OZL}	2400			20	µA	V_O = 0.4 V, V_E = 2 V		
	I_{OZH}				20	µA	V_O = 2.4 V		
	I_{OZH}				100	µA	V_O = 5.25 V		
Logic Low Short Circuit Output Current	I_{OSL}			52		mA	$V_O = V_{CC}$ = 5.25 V, I_F = 8 mA		2
Logic High Short Circuit Output Current	I_{OSH}			-45		mA	V_{CC} = 5.25 V, I_F = 0 mA, V_O = GND		2
Input Current Hysteresis	I_{HYS}		0.25			mA	V_{CC} = 5 V	3	
Input Forward Voltage	V_F		1.1	1.3	1.5		T_A = 25°C, I_F = 8 mA		
			1.0		1.55			4	
Input Reverse Breakdown Voltage	BV_R		3.0	5.0		V	T_A = 25°C, I_R = 10 µA		
			2.0						
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			-1.44		mV/°C	I_F = 6 mA	4	
Input Capacitance	C_{IN}			20		pF	f = 1 MHz, V_F = 0 V		

*All typical values at $T_A = 25°C$ and $V_{CC} = 5\ V$, unless otherwise noted.

Switching Specifications

$0°C \le T_A \le 70°C$, $4.75\ V \le V_{CC} \le 5.25\ V$, $4\ mA \le I_{F(ON)} \le 8\ mA$, $0\ V \le V_{F(OFF)} \le 0.8\ V$. All typicals at $T_A = 25°C$, $V_{CC} = 5\ V$, $I_{F(ON)} = 6.0\ mA$, $V_{F(OFF)} = 0\ V$, except where noted. See Note 11.

Parameter	Symbol	Device HCPL-	Min.	Typ.*	Max.	Units	Test Conditions	Figure	Note
Propagation Delay Time to Logic Low Output Level	t_{PHL}				55	ns	$I_{F(ON)} = 7\ mA$	5, 6, 7	1, 4, 5, 6
			15	33	60				
Propagation Delay Time to Logic High Output Level	t_{PLH}				55	ns	$I_{F(ON)} = 7\ mA$	5, 6, 7	1, 4, 5, 6
			15	30	60				
Pulse Width Distortion	$\lvert t_{PHL}-t_{PLH} \rvert$			2	15	ns	$I_{F(ON)} = 7\ mA$	5, 8	6
				5	25				
Propagation Delay Skew	t_{PSK}				35	ns	Per Notes & Text	15, 16	7
Output Rise Time	t_r			20		ns		5	
Output Fall Time	t_f			10		ns		5	
Output Enable Time to Logic High	t_{PZH}	2400		15		ns		9, 10	
Output Enable Time to Logic Low	t_{PZL}	2400		30		ns		9, 10	
Output Disable Time from Logic High	t_{PHZ}	2400		20		ns		9, 10	
Output Disable Time from Logic Low	t_{PLZ}	2400		15		ns		9, 10	
Logic High Common Mode Transient Immunity	$\lvert CM_H \rvert$		1000	10,000		V/μs	$V_{CM} = 300\ V$, $T_A = 25°C$, $I_F = 0\ mA$	11	9
Logic Low Common Mode Transient Immunity	$\lvert CM_L \rvert$		1000	10,000		V/μs	$V_{CM} = 300\ V$, $T_A = 25°C$, $I_F = 4\ mA$	11	9
Power Supply Noise Immunity	PSNI			0.5		V_{p-p}	$V_{CC} = 5.0\ V$, $48\ Hz \le = F_{AC} \le 50\ MHz$		10

*All typical values at $T_A = 25°C$ and $V_{CC} = 5\ V$, unless otherwise noted.

Package Characteristics

Parameter	Sym.	Device	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage**	V_{ISO}		2500			V rms	RH ≤ 50%, t = 1 min., T_A = 25°C		3, 13
Input-Output Resistance	R_{I-O}			10^{12}		Ω	V_{I-O} = 500 Vdc		3
Input-Output Capacitance	C_{I-O}			0.6		pF	f = 1 MHz V_{I-O} = 0 Vdc		
Input-Input Insulation Leakage Current	I_{I-I}	2430		0.005		μA	RH ≤ 45% t = 5 s, V_{I-I} = 500 Vdc		8
Resistance (Input-Input)	R_{I-I}	2430		10^{11}		Ω	V_{I-I} = 500 Vdc		8
Capacitance (Input-Input)	C_{I-I}	2430		0.25		pF	f = 1 MHz		8

*All typical values are at T_A = 25°C.
**The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the VDE 0884 Insulation Related Characteristics Table (if applicable), your equipment level safety specification or HP Application Note 1074 entitled "Optocoupler Input-Output Endurance Voltage," publication number 5963-2203E.

Notes:

1. Each channel.
2. Duration of output short circuit time not to exceed 10 ms.
3. Device considered a two terminal device: pins 1, 2, 3, and 4 shorted together, and pins 5, 6, 7, and 8 shorted together.
4. t_{PHL} propagation delay is measured from the 50% level on the rising edge of the input current pulse to the 1.5 V level on the falling edge of the output pulse. The t_{PLH} propagation delay is measured from the 50% level on the falling edge of the input current pulse to the 1.5 V level on the rising edge of the output pulse.
5. The typical data shown is indicative of what can be expected using the application circuit in Figure 13.
6. This specification simulates the worst case operating conditions of the HCPL-2400 over the recommended operating temperature and V_{CC} range with the suggested application circuit of Figure 13.
7. Propagation delay skew is discussed later in this data sheet.
8. Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.
9. Common mode transient immunity in a Logic High level is the maximum tolerable (positive) dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (i.e., V_O > 2.0 V. Common mode transient immunity in a Logic Low level is the maximum tolerable (negative) dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., V_O < 0.8 V).
10. Power Supply Noise Immunity is the peak to peak amplitude of the ac ripple voltage on the V_{CC} line that the device will withstand and still remain in the desired logic state. For desired logic high state, $V_{OH(MIN)}$ > 2.0 V, and for desired logic low state, $V_{OL(MAX)}$ < 0.8 V.
11. Use of a 0.1 μF bypass capacitor connected between pins 8 and 5 adjacent to the device is required.
12. Peak Forward Input Current pulse width < 50 μs at 1 KHz maximum repetition rate.
13. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 3000 V rms for one second (leakage detection current limit, I_{I-O} ≤ 5 μA). This test is performed before the 100% Production test shown in the VDE 0884 Insulation Related Characteristics Table, if applicable.

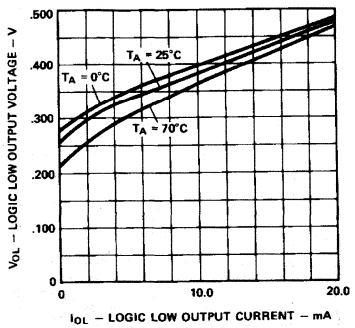


Figure 1. Typical Logic Low Output Voltage vs. Logic Low Output Current.

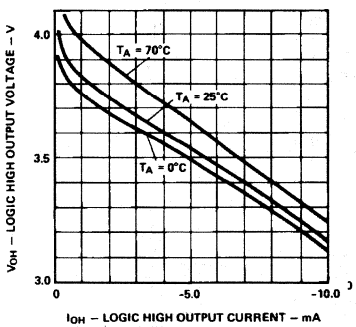


Figure 2. Typical Logic High Output Voltage vs. Logic High Output Current.

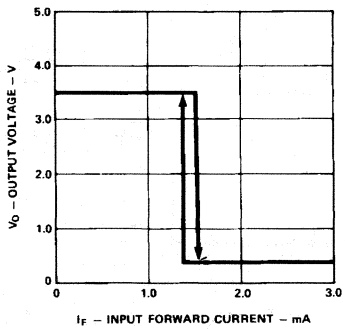


Figure 3. Typical Output Voltage vs. Input Forward Current.

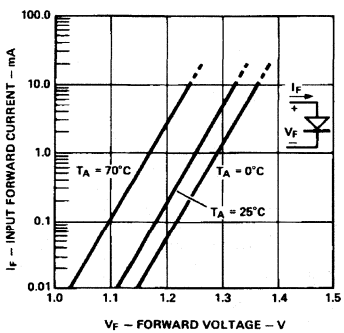


Figure 4. Typical Diode Input Forward Current Characteristic.

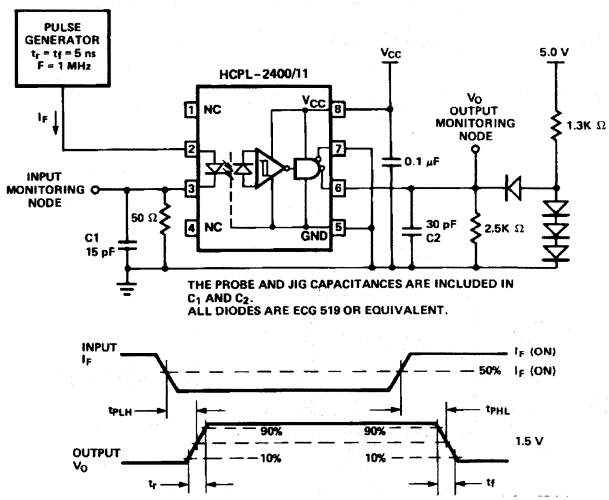


Figure 5. Test Circuit for t_{PLH}, t_{PHL}, t_r, and t_f.

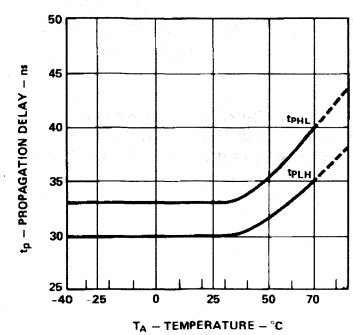


Figure 6. Typical Propagation Delay vs. Ambient Temperature.

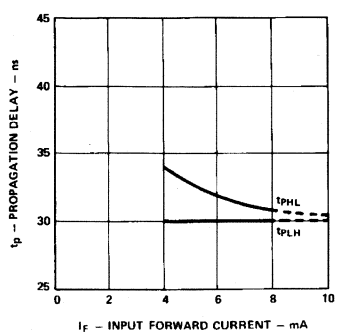


Figure 7. Typical Propagation Delay vs. Input Forward Current.

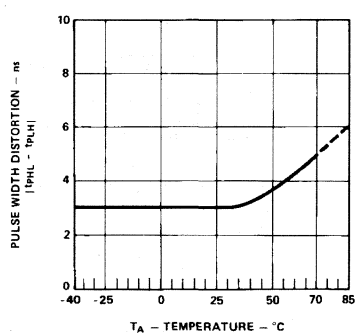


Figure 8. Typical Pulse Width Distortion vs. Ambient Temperature.

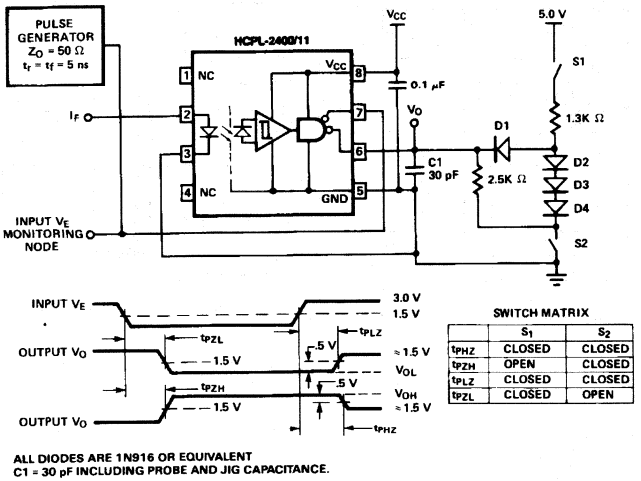


Figure 9. Test Circuit for t_{PHZ}, t_{PZH}, t_{PLZ} and t_{PZL}.

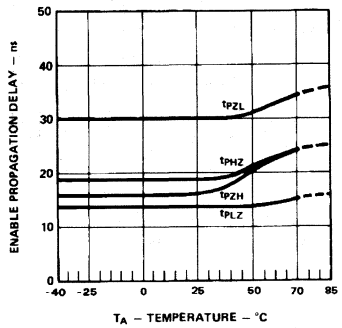


Figure 10. Typical Enable Propagation Delay vs. Ambient Temperature.

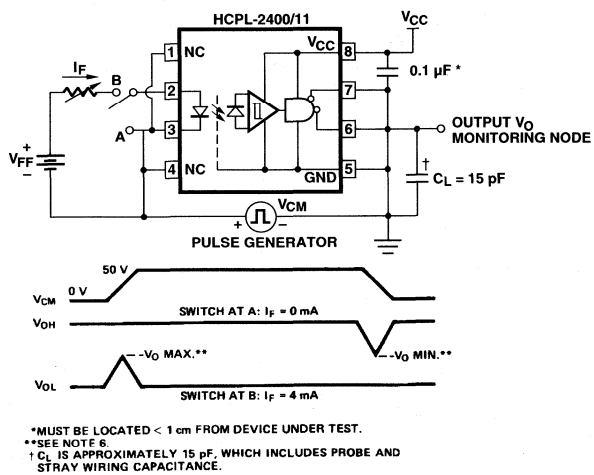


Figure 11. Test Diagram for Common Mode Transient Immunity and Typical Waveforms.

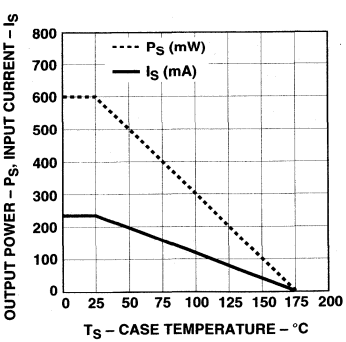


Figure 12. Thermal Derating Curve, Dependence of Safety Limiting Value with Case Temperature per VDE 0884.

Applications

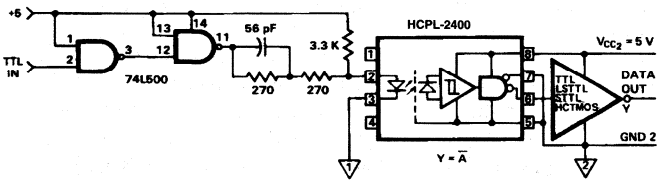


Figure 13. Recommended 20 MBd HCPL-2400/30 Interface Circuit.

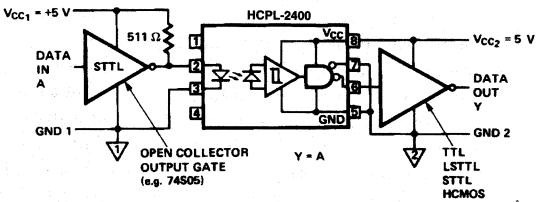


Figure 14. Alternative HCPL-2400/30 Interface Circuit.

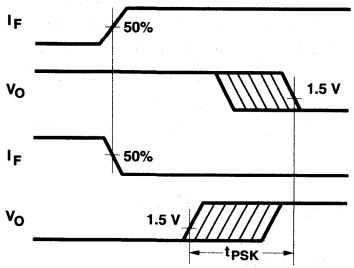


Figure 15. Illustration of Propagation Delay Skew – t_{PSK}.

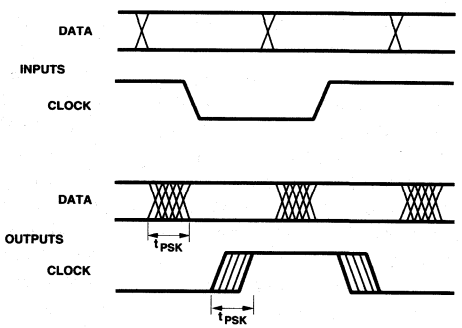


Figure 16. Parallel Data Transmission Example.

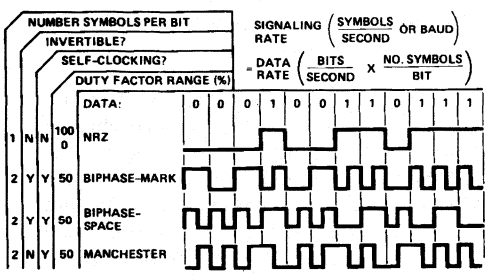


Figure 17. Modulation Code Selections.

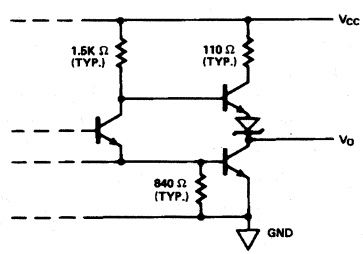


Figure 18. Typical HCPL-2400/30 Output Schematic.

Propagation Delay, Pulse-Width Distortion and Propagation Delay Skew

Propagation delay is a figure of merit which describes how quickly a logic signal propagates through a system. The propagation delay from low to high (t_{PLH}) is the amount of time required for an input signal to propagate to the output, causing the output to change from low to high. Similarly, the propagation delay from high to low (t_{PHL}) is the amount of time required for the input signal to propagate to the output, causing the output to change from high to low (see Figure 5).

Pulse-width distortion (PWD) results when t_{PLH} and t_{PHL} differ in value. PWD is defined as the difference between t_{PLH} and t_{PHL} and often determines the maximum data rate capability of a transmission system. PWD can be expressed in percent by dividing the PWD (in ns) by the minimum pulse width (in ns) being transmitted. Typically, PWD on the order of 20-30% of the minimum pulse width is tolerable; the exact figure depends on the particular application (RS232, RS422, T-1, etc.).

Propagation delay skew, t_{PSK}, is an important parameter to consider in parallel data applications where synchronization of signals on parallel data lines is a concern. If the parallel data is being sent through a group of optocouplers, differences in propagation delays will cause the data to arrive at the outputs of the optocouplers at different times. If this difference in propagation delays is large enough, it will determine the maximum rate at which parallel data can be sent through the optocouplers.

Propagation delay skew is defined as the difference between the minimum and maximum propagation delays, either t_{PLH} or t_{PHL}, for any given group of optocouplers which are operating under the same conditions (i.e., the same drive current, supply voltage, output load, and operating temperature). As illustrated in Figure 15, if the inputs of a group of optocouplers are switched either ON or OFF at the same time, t_{PSK} is the difference between the shortest propagation delay, either t_{PLH} or t_{PHL}, and the longest propagation delay, either t_{PLH} or t_{PHL}.

As mentioned earlier, t_{PSK} can determine the maximum parallel data transmission rate. Figure 16 is the timing diagram of a typical parallel data application with both the clock and the data lines being sent through optocouplers. The figure shows data and clock signals at the inputs and outputs of the optocouplers. To obtain the maximum data transmission rate, both edges of the clock signals are being used to clock the data; if only one edge were used, the clock signal would need to be twice as fast.

Propagation delay skew represents the uncertainty of where an edge might be after being sent through an optocoupler. Figure 16 shows that there will be uncertainty in both the data and the clock lines. It is important that these two areas of uncertainty not overlap, otherwise the clock signal might arrive before all of the data outputs have settled, or some of the data outputs may start to change before the clock signal has arrived. From these considerations, the absolute minimum pulse width that can be sent through optocouplers in a parallel application is twice t_{PHZ}. A cautious design should use a slightly longer pulse width to ensure that any additional uncertainty in the rest of the circuit does not cause a problem.

The HCPL-2400/30 optocouplers offer the advantages of guaranteed specifications for propagation delays, pulse-width distortion, and propagation delay skew over the recommended temperature, input current, and power supply ranges.

Application Circuit

A recommended LED drive circuit is shown in Figure 13. This circuit utilizes several techniques to minimize the total pulse-width distortion at the output of the optocoupler. By using two inverting TTL gates connected in series, the inherent pulse-width distortion of each gate cancels the distortion of the other gate. For best results, the two series-connected gates should be from the same package.

The circuit in Figure 13 also uses techniques known as prebias and peaking to enhance the performance of the optocoupler LED. Prebias is a small forward voltage applied to the LED when the LED is off. This small prebias voltage partially charges the junction capacitance of the LED, allowing the LED to turn on more quickly. The speed of the LED is further increased by applying

momentary current peaks to the LED during the turn-on and turn-off transitions of the drive current. These peak currents help to charge and discharge the capacitances of the LED more quickly, shortening the time required for the LED to turn on and off.

Switching performance of the HCPL-2400/30 optocouplers is not sensitive to the TTL logic family used in the recommended drive circuit. The typical and worst-case switching parameters given in the data sheet can be met using common 74LS TTL inverting gates or buffers. Use of faster TTL families will slightly reduce the overall propagation delays from the input of the drive circuit to the output of the optocoupler, but will not necessarily result in lower pulse-width distortion or propagation delay skew. This reduction in overall propagation delay is due to shorter delays in the drive circuit, not to changes in the propagation delays of the optocoupler; optocoupler propagation delays are not affected by the speed of the logic used in the drive circuit.

HEWLETT® PACKARD

High CMR Line Receiver Optocouplers

Technical Data

HCPL-2602
HCPL-2612

Features

- **1000 V/μs Minimum Common Mode Rejection (CMR) at V_{CM} = 50 V for HCPL-2602 and 3.5 kV/μs Minimum CMR at V_{CM} = 300 V for HCPL-2612**
- **Line Termination Included – No Extra Circuitry Required**
- **Accepts a Broad Range of Drive Conditions**
- **LED Protection Minimizes LED Efficiency Degradation**
- **High Speed: 10 MBd (Limited by Transmission Line in Many Applications)**
- **Guaranteed AC and DC Performance over Temperature: 0°C to 70°C**
- **External Base Lead Allows "LED Peaking" and LED Current Adjustment**
- **Safety Approval**
  UL Recognized – 2500 V rms for 1 Minute
  CSA Approved
- **MIL-STD-1772 Version Available (HCPL-1930/1)**

Applications

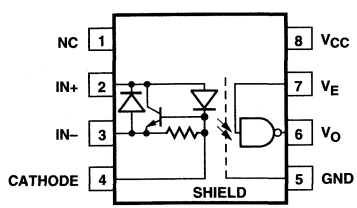
- **Isolated Line Receiver**
- **Computer-Peripheral Interface**
- **Microprocessor System Interface**
- **Digital Isolation for A/D, D/A Conversion**
- **Current Sensing**
- **Instrument Input/Output Isolation**
- **Ground Loop Elimination**
- **Pulse Transformer Replacement**
- **Power Transistor Isolation in Motor Drives**

Description

The HCPL-2602/12 are optically coupled line receivers that combine a GaAsP light emitting diode, an input current regulator and an integrated high gain photo detector. The input regulator serves as a line termination for line receiver applications. It clamps the line voltage and regulates the LED current so line reflections do not interfere with circuit performance.

The regulator allows a typical LED current of 8.5 mA before it starts to shunt excess current. The output of the detector IC is

Functional Diagram



TRUTH TABLE (POSITIVE LOGIC)

LED	ENABLE	OUTPUT
ON	H	L
OFF	H	H
ON	L	H
OFF	L	H
ON	NC	L
OFF	NC	H

A 0.1 μF bypass capacitor must be connected between pins 5 and 8.

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

5965-3585E

an open collector Schottky clamped transistor. An enable input gates the detector. The internal detector shield provides a guaranteed common mode transient immunity specification of 1000 V/µs for the 2602, and 3500 V/µs for the 2612.

DC specifications are defined similar to TTL logic. The optocoupler ac and dc operational parameters are guaranteed from 0°C to 70°C allowing trouble-free interfacing with digital logic circuits. An input current of 5 mA will sink an eight gate fan-out (TTL) at the output.

The HCPL-2602/12 are useful as line receivers in high noise environments that conventional line receivers cannot tolerate. The higher LED threshold voltage provides improved immunity to differential noise and the internally shielded detector provides orders of magnitude improvement in common mode rejection with little or no sacrifice in speed.

Selection Guide

Minimum CMR		Input On-Current (mA)	Output Enable	8-Pin DIP (300 Mil)		Small-Outline SO-8		Widebody (400 Mil)	Hermetic
dV/dt (V/µs)	V_{CM} (V)			Single Channel Package	Dual Channel Package	Single Channel Package	Dual Channel Package	Single Channel Package	Single and Dual Channel Packages
NA	NA	5	YES	6N137		HCPL-0600		HCNW137	
			NO		HCPL-2630		HCPL-0630		
5,000	50		YES	HCPL-2601		HCPL-0601		HCNW2601	
			NO		HCPL-2631		HCPL-0631		
10,000	1,000		YES	HCPL-2611		HCPL-0611		HCNW2611	
			NO		HCPL-4661		HCPL-0661		
1,000	50		YES	HCPL-2602[1]					
3,500	300		YES	HCPL-2612[1]					
1,000	50	3	YES	HCPL-261A		HCPL-061A			
			NO		HCPL-263A		HCPL-063A		
1,000[2]	1,000		YES	HCPL-261N		HCPL-061N			
			NO		HCPL-263N		HCPL-063N		
1,000	50	12.5	[3]						HCPL-193X HCPL-56XX HCPL-66XX

Notes:
1. HCPL-2602/2612 devices include input current regulator.
2. 15 kV/µs with V_{CM} = 1 kV can be achieved using HP application circuit.
3. Enable is available for single channel products only, except for HCPL-193X devices.

Ordering Information

Specify Part Number followed by Option Number (if desired).

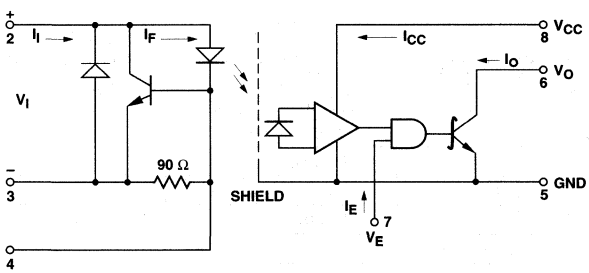
Example:

HCPL-2602#XXX

- 300 = Gull Wing Surface Mount Option
- 500 = Tape and Reel Packaging Option

Option data sheets available. Contact your Hewlett-Packard sales representative or authorized distributor for information.

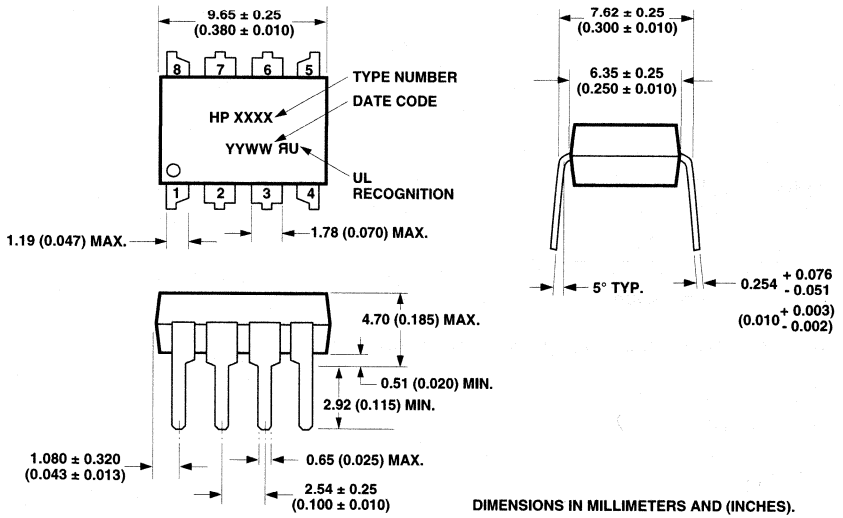
Schematic



USE OF A 0.1 µF BYPASS CAPACITOR CONNECTED BETWEEN PINS 5 AND 8 IS REQUIRED (SEE NOTE 1).

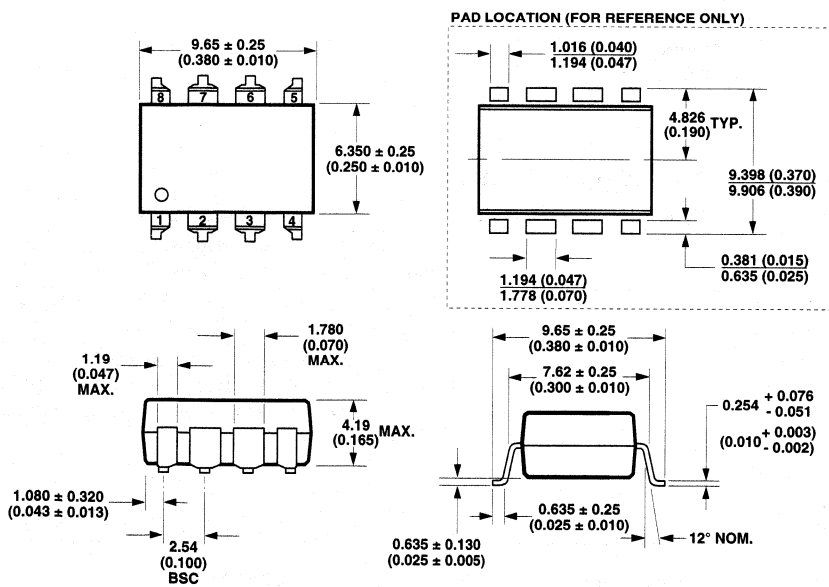
Package Outline Drawings

8-Pin DIP Package



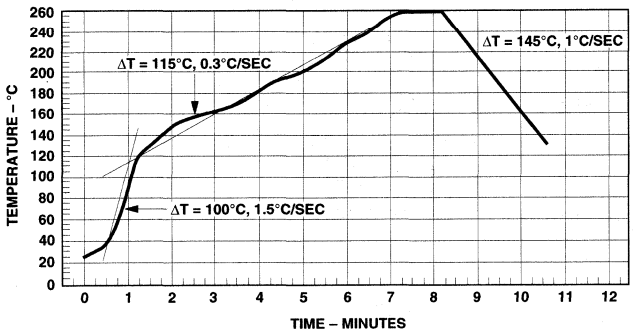
DIMENSIONS IN MILLIMETERS AND (INCHES).

8-Pin DIP Package with Gull Wing Surface Mount Option 300



DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES).

Solder Reflow Temperature Profile (Gull Wing Surface Mount Option 300 Parts)



Note: Use of nonchlorine activated fluxes is highly recommended.

Regulatory Information

The HCPL-2602/2612 have been approved by the following organizations:

UL

Recognized under UL 1577, Component Recognition Program, File E55361.

CSA

Approved under CSA Component Acceptance Notice #5, File CA 88324.

Insulation and Safety Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min. External Air Gap (External Clearance)	L(I01)	7.1	mm	Measured from input terminals to output terminals, shortest distance through air.
Min. External Tracking Path (External Creepage)	L(I02)	7.4	mm	Measured from input terminals to output terminals, shortest distance path along body.
Min. Internal Plastic Gap (Internal Clearance)		0.08	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity.
Tracking Resistance (Comparative Tracking Index)	CTI	200	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Option 300 - surface mount classification is Class A in accordance with CECC 00802.

Absolute Maximum Ratings (No Derating Required up to 85°C)

Parameter	Symbol	Min.	Max.	Units
Storage Temperature	T_S	-55	125	°C
Operating Temperature	T_A	-40	85	°C
Forward Input Current	I_I		60	mA
Reverse Input Current	I_{IR}		60	mA
Input Current, Pin 4		-10	10	mA
Supply Voltage (1 Minute Maximum)	V_{CC}		7	V
Enable Input Voltage (Not to Exceed V_{CC} by more than 500 mV)	V_E		V_{CC} + 0.5	V
Output Collector Current	I_O		50	mA
Output Collector Voltage (Selection for Higher Output Voltages up to 20 V is Available.)	V_O		7	V
Output Collector Power Dissipation	P_O		40	mW
Lead Solder Temperature	T_{LS}	260°C for 10 sec., 1.6 mm below seating plane		
Solder Reflow Temperature Profile		See Package Outline Drawings section		

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Input Current, Low Level	I_{IL}	0	250	µA
Input Current, High Level	I_{IH}	5*	60	mA
Supply Voltage, Output	V_{CC}	4.5	5.5	V
High Level Enable Voltage	V_{EH}	2.0	V_{CC}	V
Low Level Enable Voltage	V_{EL}	0	0.8	V
Fan Out (@ R_L = 1 kΩ)	N		5	TTL Loads
Output Pull-up Resistor	R_L	330	4 K	Ω
Operating Temperature	T_A	0	70	°C

*The initial switching threshold is 5 mA or less. It is recommended that an input current between 6.3 mA and 10 mA be used to obtain best performance and to provide at least 20% LED degradation guardband.

Electrical Characteristics

Over recommended temperature (T_A = 0°C to +70°C) unless otherwise specified. See note 1.

Parameter	Sym.	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
High Level Output Current	I_{OH}		5.5	100	µA	V_{CC} = 5.5 V, V_O = 5.5 V, I_I = 250 µA, V_E = 2.0 V	1	
Low Level Output Voltage	V_{OL}		0.35	0.6	V	V_{CC} = 5.5 V, I_I = 5 mA, V_E = 2.0 V, I_{OL} (Sinking) = 13 mA	2, 4, 5, 14	
High Level Supply Current	I_{CCH}		7.5	10	mA	V_{CC} = 5.5 V, I_I = 0 mA, V_E = 0.5 V		
Low Level Supply Current	I_{CCL}		10	13	mA	V_{CC} = 5.5 V, I_I = 60 mA, V_E = 0.5 V		
High Level Enable Current	I_{EH}		-0.7	-1.6	mA	V_{CC} = 5.5 V, V_E = 2.0 V		
Low Level Enable Current	I_{EL}		-0.9	-1.6	mA	V_{CC} = 5.5 V, V_E = 0.5 V		
High Level Enable Voltage	V_{EH}	2.0			V			10
Low Level Enable Voltage	V_{EL}			0.8	V			
Input Voltage	V_I		2.0	2.4	V	I_I = 5 mA	3	
			2.3	2.7		I_I = 60 mA		
Input Reverse Voltage	V_R		0.75	0.95	V	I_R = 5 mA		
Input Capacitance	C_{IN}		90		pF	V_I = 0 V, f = 1 MHz		

*All typicals at V_{CC} = 5 V, T_A = 25°C.

Switching Specifications

Over recommended temperature (T_A = 0°C to +70°C), V_{CC} = 5 V, I_I = 7.5 mA, unless otherwise specified.

Parameter	Symbol	Device	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to High Output Level	t_{PLH}		20	48	75	ns	T_A = 25°C	6, 7, 8	3
					100	ns			
Propagation Delay Time to Low Output Level	t_{PHL}		25	50	75	ns	T_A = 25°C	6, 7, 8	4
					100	ns			
Pulse Width Distortion	$\|t_{PHL}-t_{PLH}\|$			3.5	35	ns	R_L = 350 Ω, C_L = 15 pF	9	13
Propagation Delay Skew	t_{PSK}				40	ns			12, 13
Output Rise Time (10-90%)	t_r			24		ns		12	
Output Fall Time (90-10%)	t_f			10		ns		12	
Propagation Delay Time of Enable from V_{EH} to V_{EL}	t_{ELH}			30		ns	R_L = 350 Ω, C_L = 15 pF, V_{EL} = 0 V, V_{EH} = 3 V	10, 11	5
Propagation Delay Time of Enable from V_{EL} to V_{EH}	t_{EHL}			20		ns	R_L = 350 Ω, C_L = 15 pF, V_{EL} = 0 V, V_{EH} = 3 V	10, 11	6
Common Mode Transient Immunity at High Output Level	$\|CM_H\|$	HCPL-2602	1000	10,000		V/µs	V_{CM} = 50 V; $V_{O(MIN)}$ = 2 V, R_L = 350 Ω, I_I = 0 mA, T_A = 25°C	13	7, 9, 10
		HCPL-2612	3500	15,000			V_{CM} = 300 V		
Common Mode Transient Immunity at Low Output Level	$\|CM_L\|$	HCPL-2602	1000	10,000		V/µs	V_{CM} = 50 V; $V_{O(MAX)}$ = 0.8 V, R_L = 350 Ω, I_I = 7.5 mA, T_A = 25°C	13	8, 9 10
		HCPL-2612	3500	15,000			V_{CM} = 300 V		

*All typicals at V_{CC} = 5 V, T_A = 25°C.

Package Characteristics

All Typicals at T_A = 25°C

Parameter	Sym.	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage*	V_{ISO}	2500			V rms	RH ≤ 50%, t = 1 min., T_A = 25°C		2, 11
Input-Output Resistance	R_{I-O}		10^{12}		Ω	V_{I-O} = 500 Vdc		2
Input-Output Capacitance	C_{I-O}		0.6		pF	f = 1 MHz		2

*The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the VDE 0884 Insulation Characteristics Table (if applicable), your equipment level safety specification or HP Application Note 1074 entitled "Optocoupler Input-Output Endurance Voltage."

Notes:

1. Bypassing of the power supply line is required, with a 0.1 µF ceramic disc capacitor adjacent to each optocoupler as illustrated in Figure 15. Total lead length between both ends of the capacitor and the isolator pins should not exceed 20 mm.
2. Device considered a two terminal device: pins 1, 2, 3, and 4 shorted together, and pins 5, 6, 7, and 8 shorted together.
3. The t_{PLH} propagation delay is measured from the 3.75 mA point on the falling edge of the input pulse to the 1.5 V point on the rising edge of the output pulse.
4. The t_{PHL} propagation delay is measured from the 3.75 mA point on the rising edge of the input pulse to the 1.5 V point on the falling edge of the output pulse.
5. The t_{ELH} enable propagation delay is measured from the 1.5 V point on the falling edge of the enable input pulse to the 1.5 V point on the rising edge of the output pulse.
6. The t_{EHL} enable propagation delay is measured from the 1.5 V point on the rising edge of the enable input pulse to the 1.5 V point on the falling edge of the output pulse.
7. CM_H is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state (i.e., $V_{OUT} > 2.0$ V).
8. CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state (i.e., $V_{OUT} < 0.8$ V).
9. For sinusoidal voltages,
$$\left|\frac{dv_{CM}}{dt}\right|_{max} = \pi f_{CM} V_{CM} \text{ (p-p)}$$
10. No external pull up is required for a high logic state on the enable input. If the V_E pin is not used, tying V_E to V_{CC} will result in improved CMR performance.
11. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage of ≥ 3000 for one second (leakage detection current limit, $I_{i-o} \leq 5$ µA).
12. t_{PSK} is equal to the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between units at any given temperature within the operating condition range.
13. See application section titled "Propagation Delay, Pulse-Width Distortion and Propagation Delay Skew" for more information.

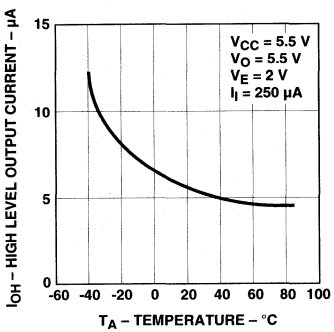


Figure 1. Typical High Level Output Current vs. Temperature.

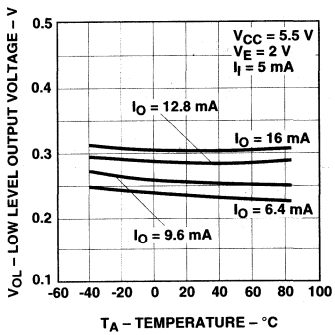


Figure 2. Typical Low Level Output Voltage vs. Temperature.

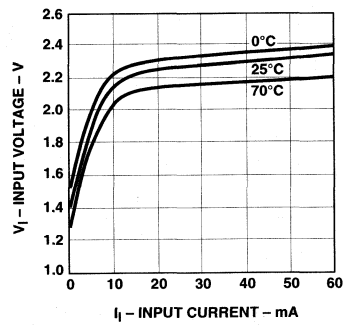


Figure 3. Typical Input Characteristics.

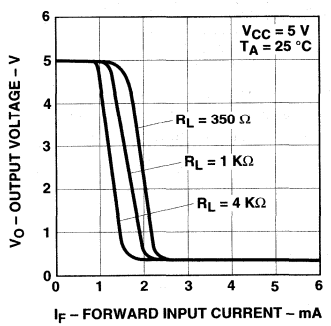


Figure 4. Typical Output Voltage vs. Forward Input Current.

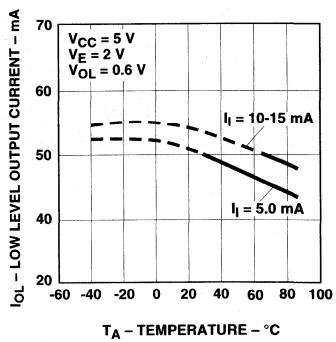


Figure 5. Typical Low Level Output Current vs. Temperature.

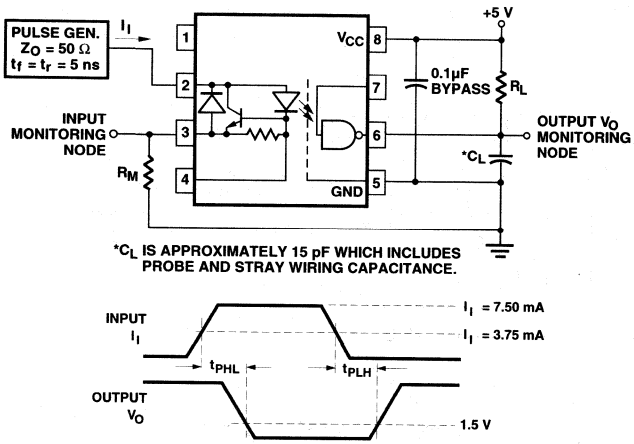


Figure 6. Test Circuit for t_{PHL} and t_{PLH}.

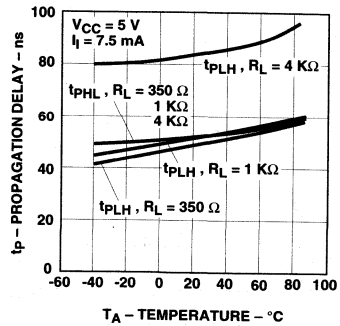


Figure 7. Typical Propagation Delay vs. Temperature.

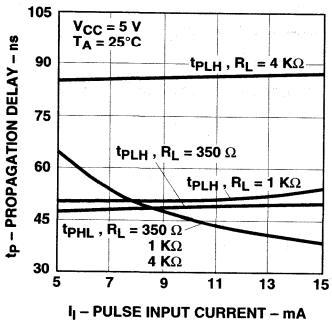


Figure 8. Typical Propagation Delay vs. Pulse Input Current.

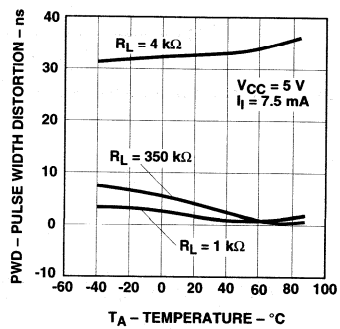


Figure 9. Typical Pulse Width Distortion vs. Temperature.

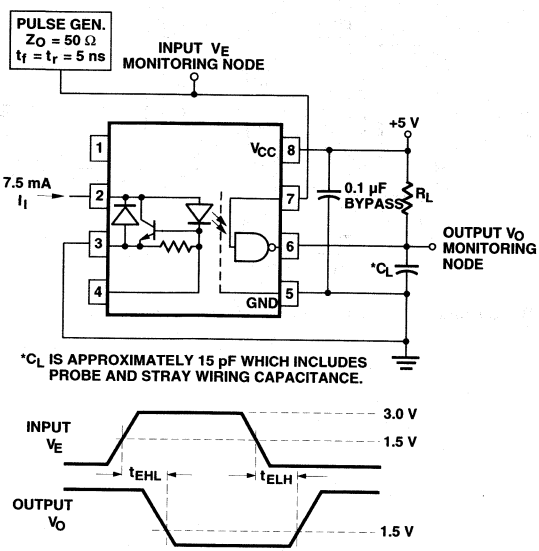


Figure 10. Test Circuit for t_{EHL} and t_{ELH}.

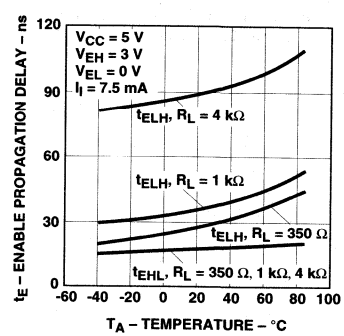


Figure 11. Typical Enable Propagation Delay vs. Temperature.

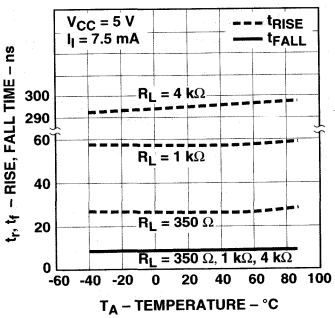


Figure 12. Typical Rise and Fall Time vs. Temperature.

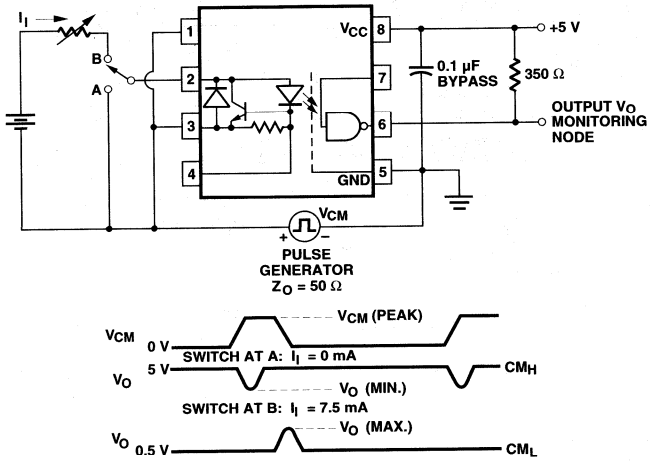


Figure 13. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

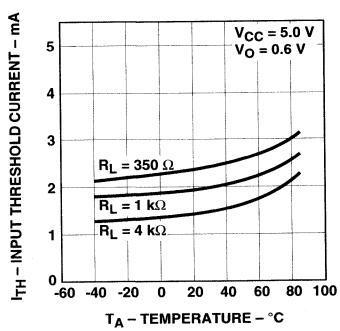


Figure 14. Typical Input Threshold Current vs. Temperature.

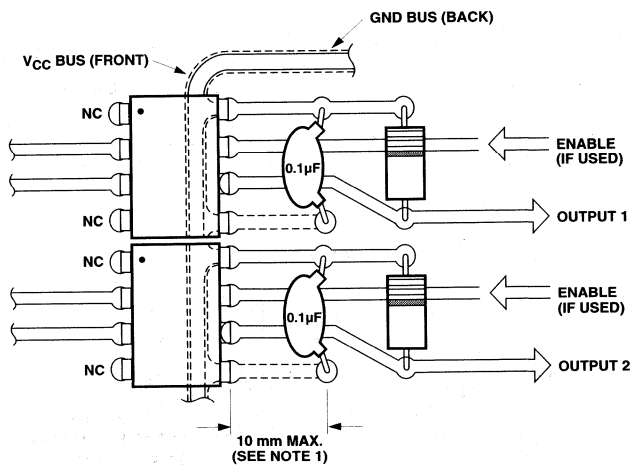


Figure 15. Recommended Printed Circuit Board Layout.

Using the HCPL-2602/12 Line Receiver Optocouplers

The primary objectives to fulfill when connecting an optocoupler to a transmission line are to provide a minimum, but not excessive, LED current and to properly terminate the line. The internal regulator in the HCPL-2602/12 simplifies this task. Excess current from variable drive conditions such as line length variations, line driver differences, and power supply fluctuations are shunted by the regulator. In fact, with the LED current regulated, the line current can be increased to improve the immunity of the system to differential-mode-noise and to enhance the data rate capability. The designer must keep in mind the 60 mA input current maximum rating of the HCPL-2602/12 in such cases, and may need to use series limiting or shunting to prevent overstress.

Design of the termination circuit is also simplified; in most cases the transmission line can simply be connected directly to the input terminals of the HCPL-2602/12 without the need for additional series or shunt resistors. If reversing line drive is used it may be desirable to use two HCPL-2602/12 or an external Schottky diode to optimize data rate.

Polarity Non-Reversing Drive

High data rates can be obtained with the HCPL-2602/12 with polarity non-reversing drive. Figure (a) illustrates how a 74S140 line driver can be used with the HCPL-2602/12 and shielded, twisted pair or coax cable without any additional components. There are some reflections due to the "active termination," but they do not interfere with circuit performance because the regulator clamps the line voltage. At longer line lengths, t_{PLH} increases faster than t_{PHL} since the switching threshold is not exactly halfway between asymptotic line conditions. If optimum data rate is desired, a series resistor and peaking capacitor can be used to equalize t_{PLH} and t_{PHL}. In general, the peaking capacitance should be as large as possible; however, if it is too large it may keep the regulator from achieving turn-off during the negative (or zero) excursions of the input signal. A safe rule:

make $C \leq 16t$

where:

C = peaking capacitance in picofarads

t = data bit interval in nanoseconds

Polarity Reversing Drive

A single HCPL-2602/12 can also be used with polarity reversing drive (Figure b). Current reversal is obtained by way of the substrate isolation diode (substrate to collector). Some reduction of data rate occurs, however, because the substrate diode stores charge, which must be removed when the current changes to the forward direction. The effect of this is a longer t_{PHL}. This effect can be eliminated and data rate improved considerably by use of a Schottky diode on the input of the HCPL-2602/12.

For optimum noise rejection as well as balanced delays, a split-phase termination should be used along with a flip-flop at the output (Figure c). The result of current reversal in split-phase operation is seen in Figure (c) with switches A and B both OPEN. The coupler inputs are then connected in ANTI-SERIES; however, because of the higher steady-state termination voltage, in comparison to the single HCPL-2602/12 termination, the forward current in the substrate diode is lower and consequently there is less junction charge to deal with when switching.

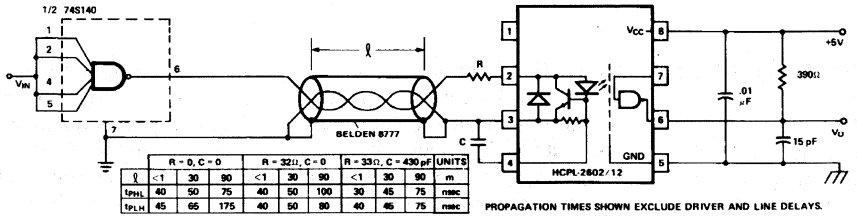
Closing switch B with A open is done mainly to enhance common mode rejection, but also reduces propagation delay slightly because line-to-line capacitance offers a slight peaking effect. With switches A and B both CLOSED, the shield acts as a current return path which prevents either input substrate diode from becoming reversed biased. Thus the data rate is optimized as shown in Figure (c).

Improved Noise Rejection

Use of additional logic at the output of two HCPL-2602/12s, operated in the split phase termination, will greatly improve system noise rejection in addition to balancing propagation delays as discussed earlier.

A NAND flip-flop offers infinite common mode rejection (CMR) for NEGATIVELY sloped common mode transients but requires $t_{PHL} > t_{PLH}$ for proper operation. A NOR flip-flop has infinite CMR for POSITIVELY sloped transients but requires $t_{PHL} < t_{PLH}$ for proper operation. An exclusive-OR flip-flop has infinite CMR for common mode transients of EITHER polarity and operates with either $t_{PHL} > t_{PLH}$ or $t_{PHL} < t_{PLH}$.

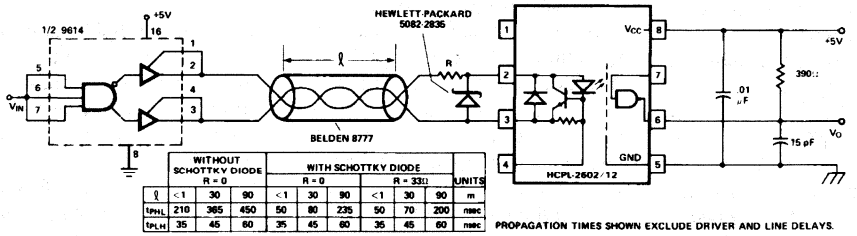
With the line driver and transmission line shown in Figure (c), $t_{PHL} > t_{PLH}$, so NAND gates are preferred in the R-S flip-flop. A higher drive amplitude or



	R = 0, C = 0			R = 32Ω, C = 0			R = 33Ω, C = 430 pF			UNITS
ℓ	<1	30	90	<1	30	90	<1	30	90	m
t_{PHL}	40	50	75	40	50	100	30	45	75	nsec
t_{PLH}	45	65	175	40	50	80	40	45	75	nsec

PROPAGATION TIMES SHOWN EXCLUDE DRIVER AND LINE DELAYS.

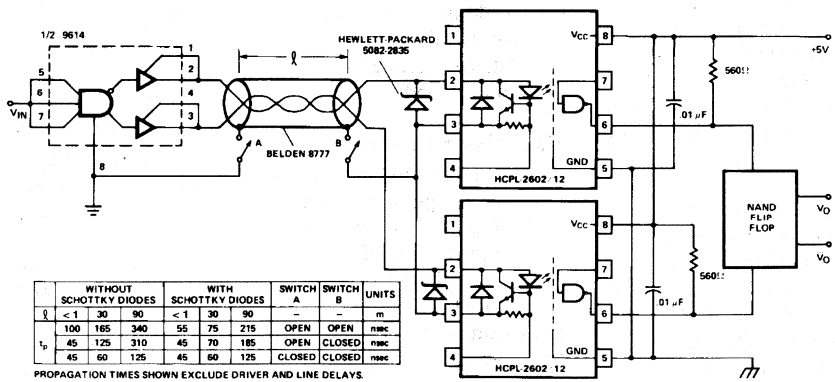
Figure a. Polarity Non-Reversing.



	WITHOUT SCHOTTKY DIODE R = 0			WITH SCHOTTKY DIODE R = 0			WITH SCHOTTKY DIODE R = 33Ω			UNITS
ℓ	<1	30	90	<1	30	90	<1	30	90	m
t_{PHL}	210	365	450	50	80	235	50	70	200	nsec
t_{PLH}	35	45	60	35	45	60	35	45	60	nsec

PROPAGATION TIMES SHOWN EXCLUDE DRIVER AND LINE DELAYS.

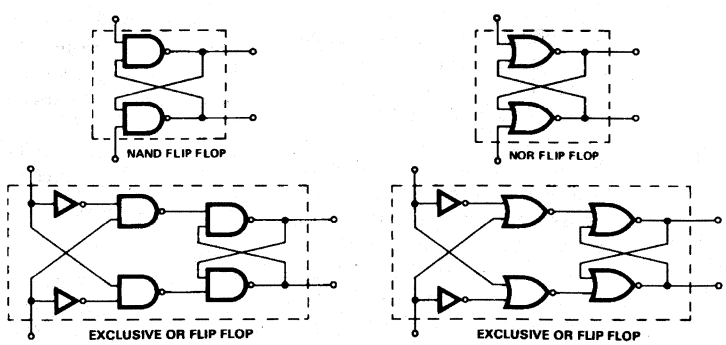
Figure b. Polarity Reversing, Single Ended.



	WITHOUT SCHOTTKY DIODES			WITH SCHOTTKY DIODES			SWITCH A	SWITCH B	UNITS
ℓ	< 1	30	90	< 1	30	90	–	–	m
t_p	100	165	340	55	75	215	OPEN	OPEN	nsec
	45	125	310	45	70	185	OPEN	CLOSED	nsec
	45	60	125	45	60	125	CLOSED	CLOSED	nsec

PROPAGATION TIMES SHOWN EXCLUDE DRIVER AND LINE DELAYS.

Figure c. Polarity Reversing, Split Phase.



NAND flip flop tolerates simultaneously HIGH inputs; NOR flip flop tolerates simultaneously LOW inputs; EXCLUSIVE-OR flip flop tolerates simultaneously HIGH OR LOW inputs without causing either of the outputs to change.

Figure d. Flip-Flop Configurations.

different circuit configuration could make $t_{PHL} < t_{PLH}$, in which case NOR gates would be preferred. If it is not known whether $t_{PHL} > t_{PLH}$ or $t_{PHL} < t_{PLH}$, or if the drive conditions may vary over the boundary for these conditions, the exclusive-OR flip-flop of Figure (d) should be used.

RS-422 and RS-423

Line drivers designed for RS-422 and RS-423 generally provide adequate voltage and current for operating the HCPL-2602/12. Most drivers also have characteristics allowing the HCPL-2602/12 to be connected directly to the driver terminals. Worst case drive conditions, however, would require current shunting to prevent overstress of the HCPL-2602/12.

Propagation Delay, Pulse-Width Distortion and Propagation Delay Skew

Propagation delay is a figure of merit which describes how quickly a logic signal propagates through a system. The propagation delay from low to high (t_{PLH}) is the amount of time required for an input signal to propagate to the output, causing the output to change from low to high. Similarly, the propagation delay from high to low (t_{PHL}) is the amount of time required for the input signal to propagate to the output, causing the output to change from high to low (see Figure 6).

Pulse-width distortion (PWD) results when t_{PLH} and t_{PHL} differ in value. PWD is defined as the difference between t_{PLH} and t_{PHL} and often determines the maximum data rate capability of a transmission system. PWD can be expressed in percent by dividing the PWD (in ns) by the minimum pulse width (in ns) being transmitted. Typically, PWD on the order of 20-30% of the minimum pulse width is tolerable; the exact figure depends on the particular application (RS232, RS422, T-1, etc.).

Propagation delay skew, t_{PSK}, is an important parameter to consider in parallel data applications where synchronization of signals on parallel data lines is a concern. If the parallel data is being sent through a group of optocouplers, differences in propagation delays will cause the data to arrive at the outputs of the optocouplers at different times. If this difference in propagation delays is large enough, it will determine the maximum rate at which parallel data can be sent through the optocouplers.

Propagation delay skew is defined as the difference between the minimum and maximum propagation delays, either t_{PLH} or t_{PHL}, for any given group of optocouplers which are operating under the same conditions (i.e., the same drive current, supply voltage, output load, and operating temperature). As illustrated in Figure 16, if the inputs of a group of optocouplers are switched either ON or OFF at the same time, t_{PSK} is the difference between the shortest propagation delay, either t_{PHL} or t_{PHL}, and the longest propagation delay, either t_{PLH} or t_{PHL}.

As mentioned earlier, t_{PSK} can determine the maximum parallel data transmission rate. Figure 17 is the timing diagram of a typical parallel data application with both the clock and the data lines being sent through optocouplers. The figure shows data and clock signals at the inputs and outputs of the optocouplers. To obtain the maximum data transmission rate, both edges of the clock signal are being used to clock the data; if only one edge were used, the clock signal would need to be twice as fast.

Propagation delay skew represents the uncertainty of where an edge might be after being sent through an optocoupler. Figure 17 shows that there will be uncertainty in both the data and the clock lines. It is important that these two areas of uncertainty not overlap, otherwise the clock signal might arrive before all of the data outputs have settled, or some of the data outputs may start to change before the clock signal has arrived. From these considerations, the absolute minimum pulse width that can be sent through optocouplers in a parallel application is twice t_{PSK}. A cautious design should use a slightly longer pulse width to ensure that any additional uncertainty in the rest of the circuit does not cause a problem.

The t_{PSK} specified optocouplers offer the advantages of guaranteed specifications for propagation delays, pulse-width distortion and propagation delay skew over the recommended temperature, input current, and power supply ranges.

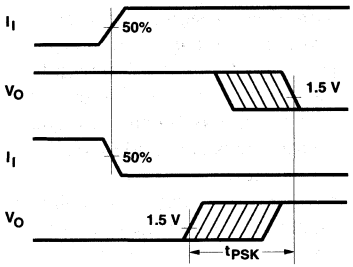


Figure 16. Illustration of Propagation Delay Skew - t_{PSK}.

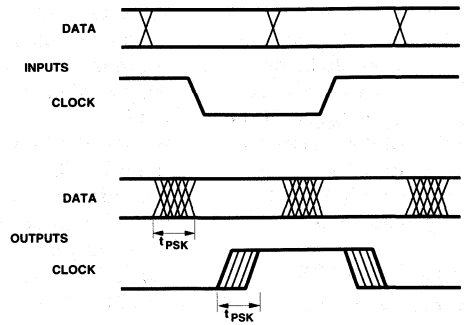


Figure 17. Parallel Data Transmission Example.

Power Bipolar Transistor Base Drive Optocoupler

Technical Data

HCPL-3000

Features

- **High Output Current**
  I_{O2} (2.0 A Peak, 0.6 A Continuous)
  I_{O1} (1.0 A Peak, 0.5 A Continuous)
- **1.5 kV/μs Minimum Common Mode Rejection (CMR) at V_{CM} = 600 V**
- **Wide V_{CC} Range (5.4 to 13 Volts)**
- **2 μs Typical Propagation Delay**
- **Recognized under UL 1577 for Dielectric Withstand Proof Test Voltage of 5000 Vac, 1 Minute**

Applications

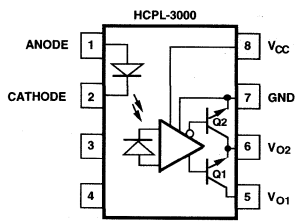
- **Isolated Bipolar Transistor Base Drive**
- **AC and DC Motor Drives**
- **General Purpose Industrial Inverters**
- **Uninterruptable Power Supply**

Description

The HCPL-3000 consists of a Silicon-doped GaAs LED optically coupled to an integrated circuit with a power output stage. This optocoupler is suited for driving power bipolar transistors and power Darlington devices used in motor control inverter applications. The high peak and steady state current capabilities of the output stage allow for direct interfacing to the power device without the need for an intermediate amplifier stage. With a CMR rating of 1.5 kV/μs this optocoupler readily rejects transients found in inverter applications.

The LED controls the state of the output stage. Transistor Q2 in the output stage is on with the LED off, allowing the base of the power device to be held low. Turning on the LED turns off transistor Q2 and switches on transistor Q1 in the output stage which provides current to drive the base of a power bipolar device.

Functional Diagram



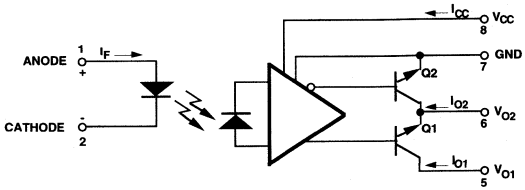
TRUTH TABLE

LED	OUTPUT	Q1	Q2
ON	HIGH LEVEL	ON	OFF
OFF	LOW LEVEL	OFF	ON

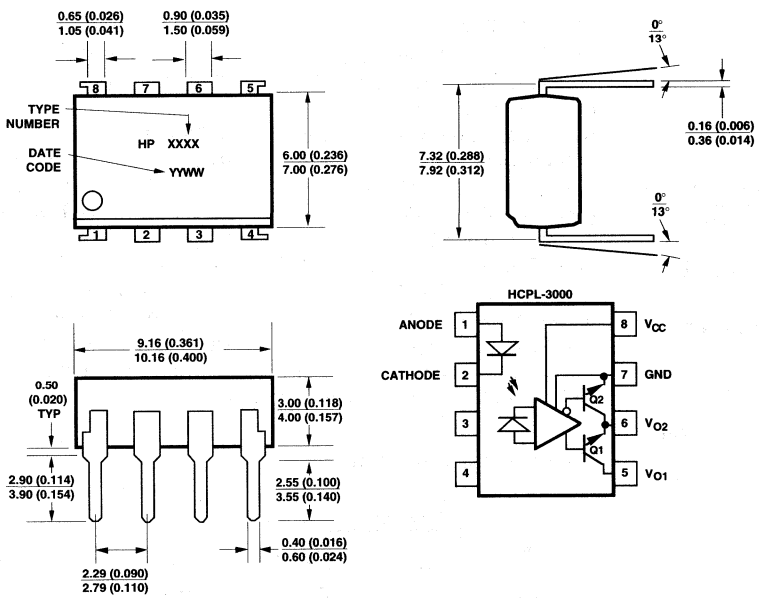
THE USE OF A 0.1μF BYPASS CAPACITOR CONNECTED BETWEEN PINS 8 AND 7 IS RECOMMENDED. ALSO, CURRENT LIMITING RESISTORS ARE RECOMMENDED (SEE FIGURE 1, NOTE 2, AND NOTE 7).

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Schematic



Outline Drawing



Regulatory Information

The HCPL-3000 has been approved by the following organizations:

UL

Recognized under UL 1577, Component Recognition Program, File E55361.

Demonstrated ESD Performance

Human Body Model: MIL-STD-883 Method 3015.7: Class 2

Machine Model: EIAJ IC-121-1988 (1988.3.28 Version 2), Test Method 20, Condition C: 1200 V

Insulation and Safety Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min. External Air Gap (External Clearance)	L(IO1)	6.0	mm	Shortest distance measured through air, between two conductive leads, input to output
Min. External Tracking Path (External Creepage)	L(IO2)	6.0	mm	Shortest distance path measured along outside surface of optocoupler body between the input and output leads
Min. Internal Plastic Gap (Internal Clearance)		0.15	mm	Through insulation distance conductor to conductor inside the optocoupler cavity

Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Unit	Conditions	Fig.	Note
Storage Temperature		T_S	-55	125	°C			
Operating Temperature		T_A	-20	80	°C			
Input	Continuous Current	I_F		25	mA		9	1
	Reverse Voltage	V_R		6	V	T_A = 25°C		
Supply Voltage		V_{CC}		18	V			
Output 1	Continuous Current	I_{O1}		0.5	A		10,11	1
	Peak Current			1.0	A	Pulse Width < 5 µs, Duty cycle = 1%		1
	Voltage	V_{O1}		18	V			
Output 2	Continuous Current	I_{O2}		0.6	A		10,11,12	1
	Peak Current			2.0	A	Pulse Width < 5 µs, Duty cycle = 1%	12	1
Output Power Dissipation		P_O		500	mW		10	1
Total Power Dissipation		P_T		550	mW		11	1
Lead Solder Temperature		260°C for 10 s, 1.0 mm below seating plane						

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage	V_{CC}	5.4	13	V
Input Current (ON)	$I_{F(ON)}$	8*	20	mA
Input Current (OFF)	$I_{F(OFF)}$	-	0.2	mA
Operating Temperature	T_A	-20	80	°C

*The initial switching threshold is 5 mA or less.

Recommended Protection for Output Transistors

During switching transitions, the output transistors Q1 and Q2 of the HCPL-3000 can conduct large amounts of current. Figure 1 describes a recommended circuit design showing current limiting resistors R_1 and R_2 which are necessary in order to prevent damage to the output transistors Q1 and Q2 (see Note 7). A bypass capacitor C_1 is also recommended to reduce power supply noise.

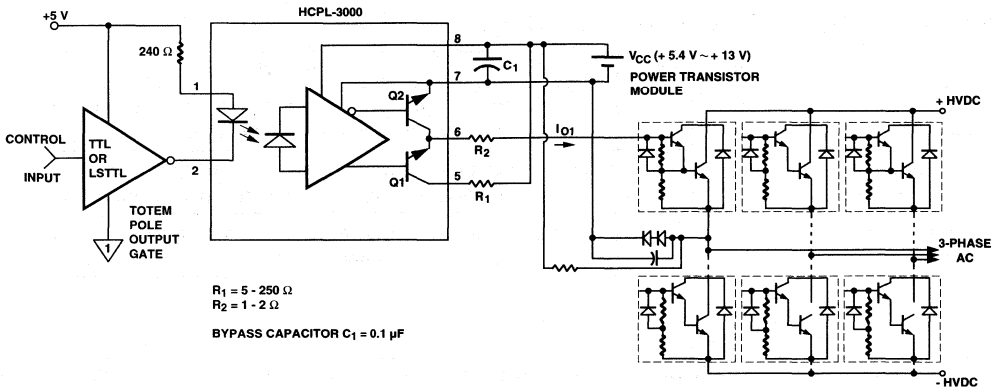


Figure 1. Recommended Output Transistor Protection and Typical Application Circuit.

Electrical Specifications

Over recommended temperature (T_A = -20°C to +80°C) unless otherwise specified.

Parameter		Sym.	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Input Forward Voltage		V_F	-	1.1	1.4	V	I_F = 5 mA, T_A = 25°C	13	
			0.6	0.9	-	V	I_F = 0.2 mA, T_A = 25°C		
Input Reverse Current		I_R	-	-	10	μA	V_R = 3 V, T_A = 25°C		
Input Capacitance		C_{IN}	-	30	250	pF	V_F = 0 V, f = 1 kHz, T_A = 25°C		
Output 1	Low Level Voltage	V_{O1L}	-	0.2	0.4	V	V_{CC} = 6 V, I_{O1} = 0.4 A, R_{L2} = 10 Ω, I_F = 5 mA	2, 16, 17	2
	Leakage Current	I_{O1L}	-	-	200	μA	V_{CC} = V_{O1} = 13 V, V_{O2} = 0 V, I_F = 0 mA	4	
Output 2	High Level Voltage	V_{O2H}	4.5	5.0	-	V	V_{CC} = 6 V, I_{O2} = -0.4 A I_F = 5 mA, V_{O1} = 6 V	3, 18, 19	2
	Low Level Voltage	V_{O2L}	-	0.2	0.4	V	V_{CC} = 6 V, I_{O2} = 0.5 A, I_F = 0 mA	20, 21	
	Leakage Current	I_{O2L}	-	-	200	μA	V_{CC} = 13 V, I_F = 5 mA, V_{O2} = 13 V	5	
Supply Current	High Level	I_{CCH}	-	9	13	mA	T_A = 25°C	22	2
			-	-	17		V_{CC} = 6 V, I_F = 5 mA		
	Low Level	I_{CCL}	-	11	15	mA	T_A = 25°C	23	
			-	-	20		V_{CC} = 6 V, I_F = 0 mA		
Low to High Threshold Input Current		I_{FLH}	0.3	1.5	3.0	mA	T_A = 25°C	6, 14, 15	3
			0.2	-	5.0	mA	V_{CC} = 6 V, R_{L1} = 5 Ω, R_{L2} = 10 Ω		

Switching Specifications (T_A = 25°C)

Parameter	Sym.	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to High Output Level	t_{PLH}	-	2	5	µs	V_{CC} = 6 V, I_F = 5 mA, R_{L1} = 5 Ω, R_{L2} = 10 Ω	7, 24, 25	2, 6
Propagation Delay Time to Low Output Level	t_{PHL}	-	2	5				
Rise Time	t_r	-	0.2	1				
Fall Time	t_f	-	0.1	1				
Output High Level Common Mode Transient Immunity	$\|CM_H\|$	1500	-	-	V/µs	V_{CM} = 600 V Peak, I_F = 5mA, R_{L1} = 470 Ω, R_{L2} = 1 kΩ, ΔV_{02H} = 0.5 V	8	2
Output Low Level Common Mode Transient Immunity	$\|CM_L\|$	1500	-	-	V/µs	V_{CM} = 600 V Peak, I_F = 0 mA, R_{L1} = 470 Ω, R_{L2} = 1 kΩ, ΔV_{02L} = 0.5 V		

Package Characteristics

Parameter	Sym.	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage*	V_{ISO}	5000			V rms	RH = 40% to 60%, t = 1 min., T_A = 25°C		4, 5
Resistance (Input-Output)	R_{I-O}	$5x10^{10}$	10^{11}	–	Ω	V_{I-O} = 500 V, T_A = 25°C, RH = 40% to 60%		4
Capacitance (Input-Output)	C_{I-O}	–	1.2	–	pF	f = 1 MHz		4

*The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the VDE 0884 Insulation Characteristics Table (if applicable), your equipment level safety specification, or HP Application Note 1074, "Optocoupler Input-Output Endurance Voltage."

Notes:

1. Derate absolute maximum ratings with ambient temperatures as shown in Figures 9, 10, and 11.
2. A bypass capacitor of 0.01 µF or more is needed near the device between V_{CC} and GND when measuring output and transfer characteristics.
3. I_{FLH} represents the forward current when the output goes from low to high.
4. Device considered a two terminal device; pins 1-4 are shorted together and pin 5-8 are shorted together.
5. For devices with minimum V_{ISO} specified at 5000 V rms, in accordance with UL1577, each optocoupler is proof-tested by applying an insulation test voltage ≥ 6000 Vrms for one second (leakage current detection limit, $I_{I-O} \leq$ 200 µA).
6. The t_{PLH} and t_{PHL} propagation delays are measured from the 50% level of the input pulse to the 50% level of the output pulse.
7. R_1 sets the base current (I_{O1} in Figure 1) supplied to the power bipolar device. R_2 limits the peak current seen by Q2 when the device is turning off. For more applications and circuit design information see Application Note "Power Transistor Gate/Base Drive Optocouplers."

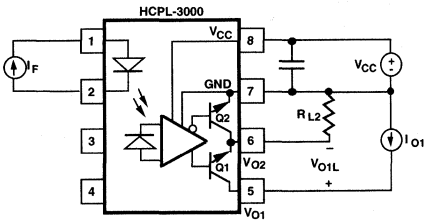


Figure 2. Test Circuit for Low Level Output Voltage V_{O1L}.

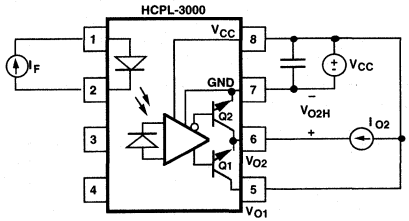


Figure 3. Test Circuit for High Level Output Voltage V_{O2H}.

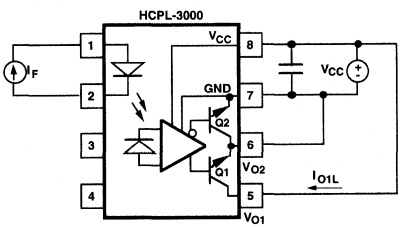


Figure 4. Test Circuit for Leakage Current I_{O1L}.

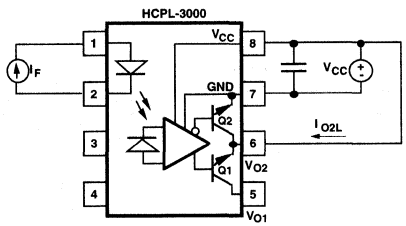


Figure 5. Test Circuit for Leakage Current I_{O2L}.

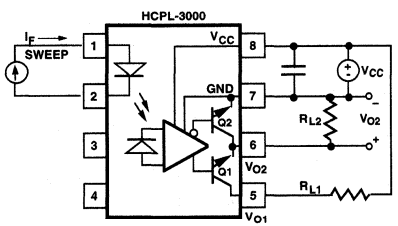


Figure 6. Test Circuit for Threshold Input Current I_{FLH}.

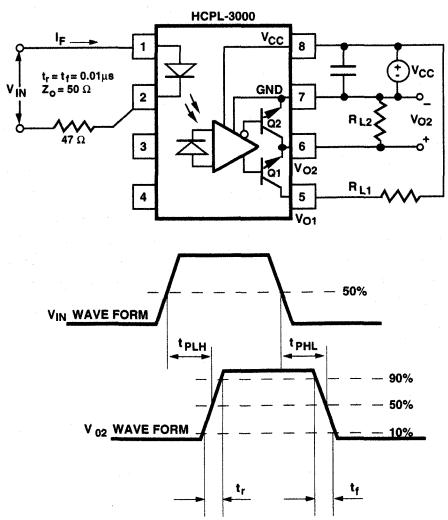


Figure 7. Test Circuit for t_{PLH}, t_{PHL}, t_r and t_f.

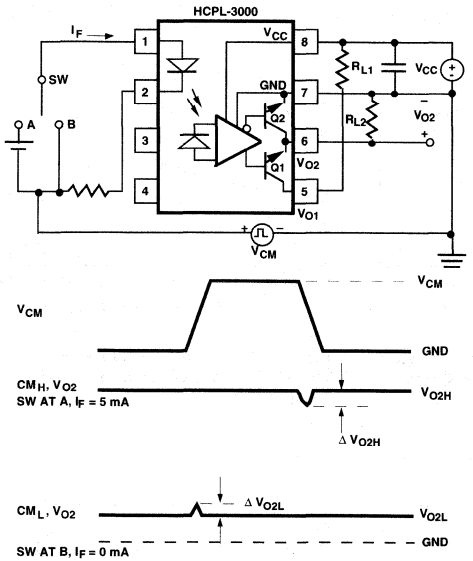


Figure 8. Test Circuit for CM_H and CM_L.

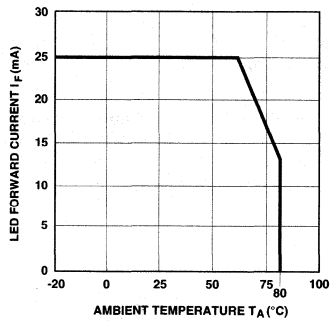


Figure 9. LED Forward Current vs. Ambient Temperature.

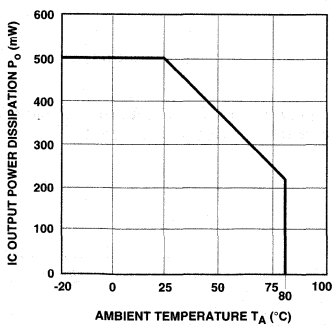


Figure 10. Maximum IC Output Power Dissipation vs. Ambient Temperature.

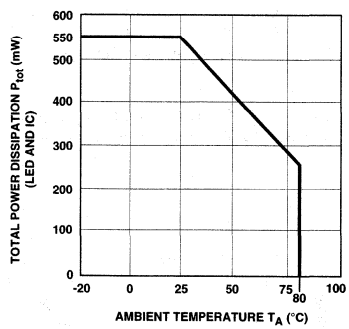


Figure 11. Maximum Total Power Dissipation vs. Ambient Temperature.

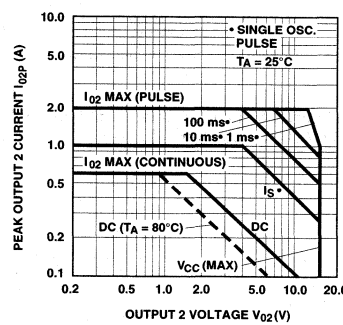


Figure 12. Typical Peak Output 2 Current vs. Output 2 Voltage (Safe Operating Area Q2).

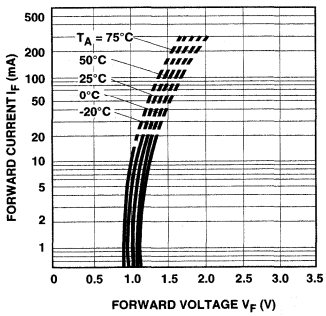


Figure 13. Typical Forward Current vs. Forward Voltage.

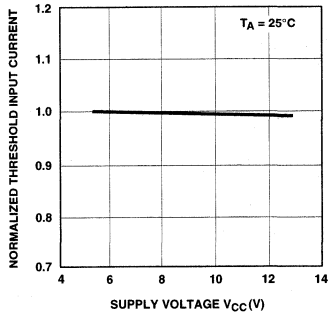


Figure 14. Normalized Low to High Threshold Input Current vs. Supply Voltage.

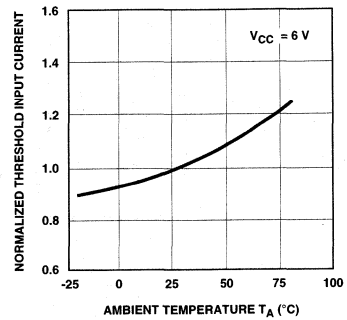


Figure 15. Normalized Low to High Threshold Input Current vs. Ambient Temperature.

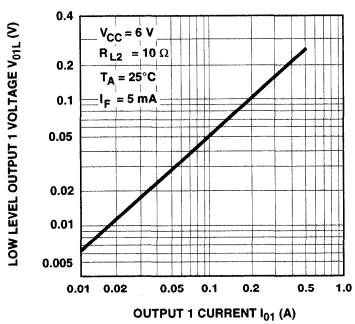


Figure 16. Typical Low Level Output 1 Voltage vs. Output 1 Current.

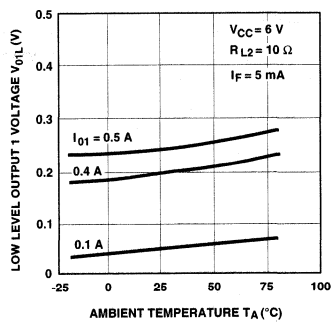


Figure 17. Typical Low Level Output 1 Voltage vs. Ambient Temperature.

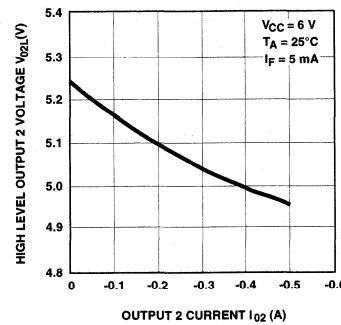


Figure 18. Typical High Level Output 2 Voltage vs. Output 2 Current.

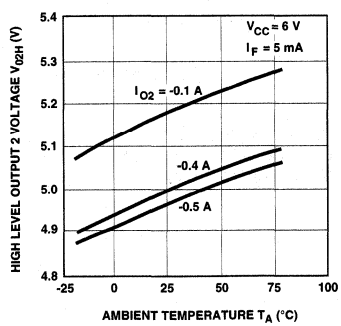


Figure 19. Typical High Level Output 2 Voltage vs. Ambient Temperature.

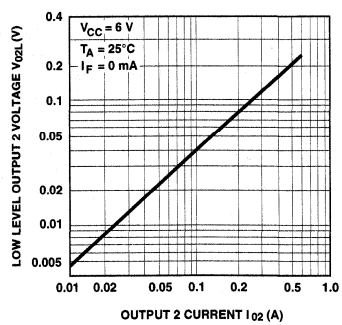


Figure 20. Typical Low Level Output 2 Voltage vs. Output 2 Current.

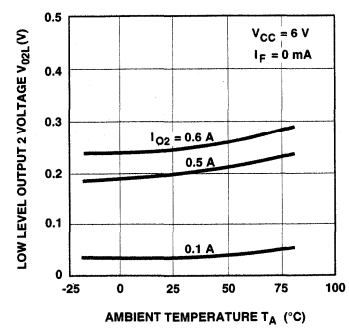


Figure 21. Typical Low Level Output 2 Voltage vs. Ambient Temperature.

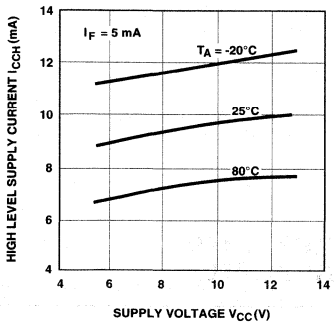


Figure 22. Typical High Level Supply Current vs. Supply Voltage.

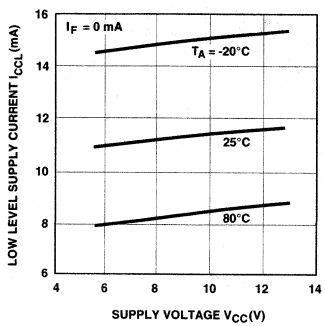


Figure 23. Typical Low Level Supply Current vs. Supply Voltage.

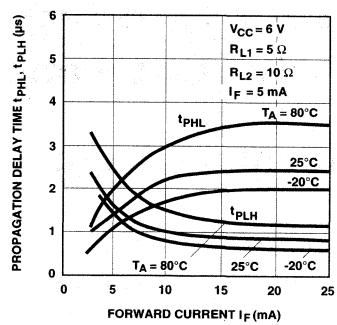


Figure 24. Typical Propagation Delay Time vs. Forward Current.

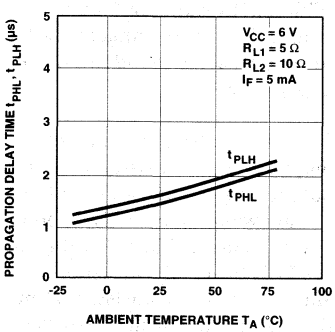


Figure 25. Typical Propagation Delay Time vs. Ambient Temperature.

HEWLETT® PACKARD

Power MOSFET/IGBT Gate Drive Optocouplers

Technical Data

HCPL-3100
HCPL-3101

Features

- **High Output Current**
  I_{O1} and I_{O2} (0.4 A Peak, 0.1 A Continuous)
- **1.5 kV/μs Minimum Common Mode Rejection (CMR) at V_{CM} = 600 V**
- **Wide Operating V_{CC} Range (15 to 30 Volts)**
- **High Speed**
  1 μs Typical Propagation Delay (HCPL-3100)
  0.3 μs Typical Propagation Delay (HCPL-3101)
- **Recognized under UL 1577 for Dielectric Withstand Proof Test Voltages of 5000 Vac, 1 Minute**

Applications

- **Isolated MOSFET/IGBT Gate Drive**
- **AC and DC Motor Drives**
- **General Purpose Industrial Inverters**
- **Uninterruptable Power Supply**

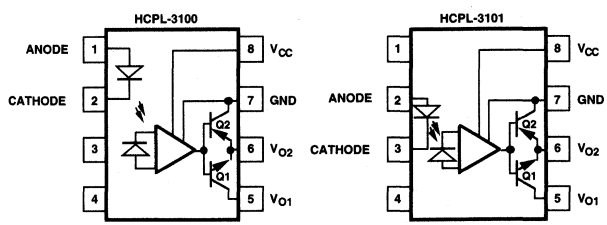
Description

The HCPL-3100/3101 consists of an LED* optically coupled to an integrated circuit with a power output stage. These optocouplers are suited for driving power MOSFETs and IGBTs used in motor control inverter applications. The high operating voltage range of the output stage provides the voltage drives required by gate controlled devices. The voltage and current supplied by these optocouplers allow for direct interfacing to the power device without the need for an intermediate amplifier stage.

The HCPL-3100 switches a 3000 pF load in 2 μs and the HCPL-3101, using a higher speed LED, switches a 3000 pF load in 0.5 μs. With a CMR rating of 5 kV/μs typical these optocouplers readily reject transients found in inverter applications.

The LED controls the state of the output stage. Transistor Q2 in the output stage is on with the LED off, allowing the gate of the power device to be held low. Turning on the LED turns off transistor Q2 and switches on transistor Q1 in the output stage which provides current and voltage to drive the gate of the power device.

Functional Diagram



TRUTH TABLE

LED	OUTPUT	Q1	Q2
ON	HIGH LEVEL	ON	OFF
OFF	LOW LEVEL	OFF	ON

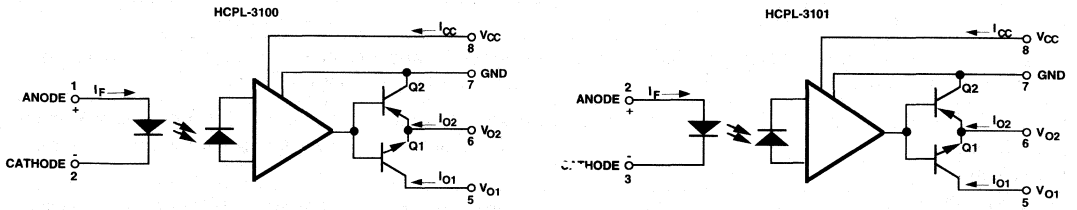
THE USE OF A 0.1 μF BYPASS CAPACITOR CONNECTED BETWEEN PINS 8 AND 7 IS RECOMMENDED. ALSO CURRENT LIMITING RESISTOR IS RECOMMENDED (SEE FIGURE 1, AND NOTE 2 AND NOTE 7).

*HCPL-3100 LED contains Silicon-doped GaAs and HCPL-3101 LED contains AlGaAs.

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

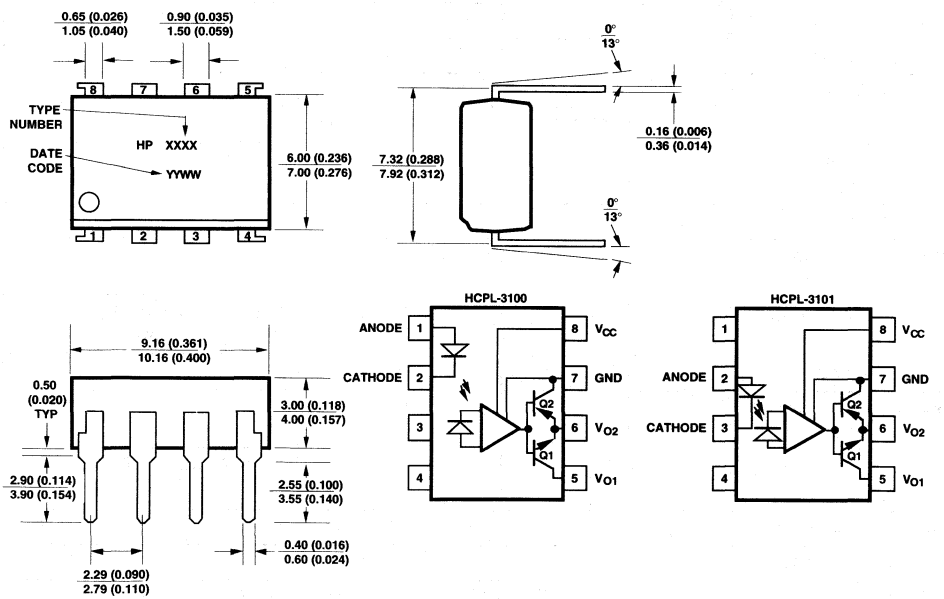
5965-3583E

Schematic



THE USE OF A 0.1 µF BYPASS CAPACITOR CONNECTED BETWEEN PINS 8 AND 7 IS RECOMMENDED. ALSO CURRENT LIMITING RESISTOR IS RECOMMENDED (SEE FIGURE 1, AND NOTE 2 AND NOTE 7).

Outline Drawing



Demonstrated ESD Performance

Human Body Model: MIL-STD-883 Method 3015.7: Class 2

Machine Model: EIAJ IC-121-1988 (1988.3.28 Version 2), Test Method 20, Condition C: 1200 V

Regulatory Information

The HCPL-3100/3101 has been approved by the following organization:

UL

Recognized under UL 1577, Component Recognition Program, File E55361.

Insulation and Safety Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min. External Air Gap (External Clearance)	L(IO1)	6.0	mm	Shortest distance measured through air, between two conductive leads, input to output
Min. External Tracking Path (External Creepage)	L(IO2)	6.0	mm	Shortest distance path measured along outside surface of optocoupler body between input and output leads
Min. Internal Plastic Gap (Internal Clearance)		0.15	mm	Through insulation distance conductor to conductor inside the optocoupler cavity

Absolute Maximum Ratings

Parameter		Symbol	Device	Min.	Max.	Unit	Conditions	Fig.	Note
Storage Temperature		T_S		-55	125	°C			
Operating Temperature		T_A		-25	80	°C			
Input	Continuous Current	I_F	HCPL-3100		25	mA		11	1
			HCPL-3101		20	mA		11	1
	Reverse Voltage	V_R			6	V	T_A = 25°C		
Supply Voltage		V_{CC}			35	V			
Output 1	Continuous Current	I_{O1}			0.1	A			1
	Peak Current				0.4	A	Pulse Width < 0.15 µs, Duty cycle = 1%		1
	Voltage	V_{O1}			35	V			
Output 2	Continuous Current	I_{O2}			0.1	A			1
	Peak Current				0.4	A	Pulse Width < 0.15 µs, Duty cycle = 1%		1
Output Power Dissipation		P_O			500	mW		12	1
Total Power Dissipation		P_T			550	mW		12	1
Lead Solder Temperature		260°C for 10 s, 1.0 mm below seating plane							

Recommended Operating Conditions

Parameter	Symbol	Device	Min.	Max.	Units
Power Supply Voltage	V_{CC}		15	30*	V
			15	24	V
Input Current (ON)	$I_{F(ON)}$	HCPL-3100	12**	24	mA
		HCPL-3101	8**	16	mA
Input Current (OFF)	$I_{F(OFF)}$	HCPL-3100	-	0.6	mA
		HCPL-3101	-	0.2	mA
Operating Temperature	T_A		-25	80	°C

*For T_A = -10°C to 60°C.
**The initial switching threshold is 10 mA or less for the HCPL-3100 and 5 mA or less for the HCPL-3101.

Recommended Protection for Output Transistors

During switching transitions, the output transistors Q1 and Q2 of the HCPL-3100/3101 can conduct large amounts of current. Figure 1 describes a recommended circuit design showing a current limiting resistor R_2 which is necessary in order to prevent damage to the output transistors Q1 and Q2. (See Note 7.) A bypass capacitor C_1 is also recommended to reduce power supply noise.

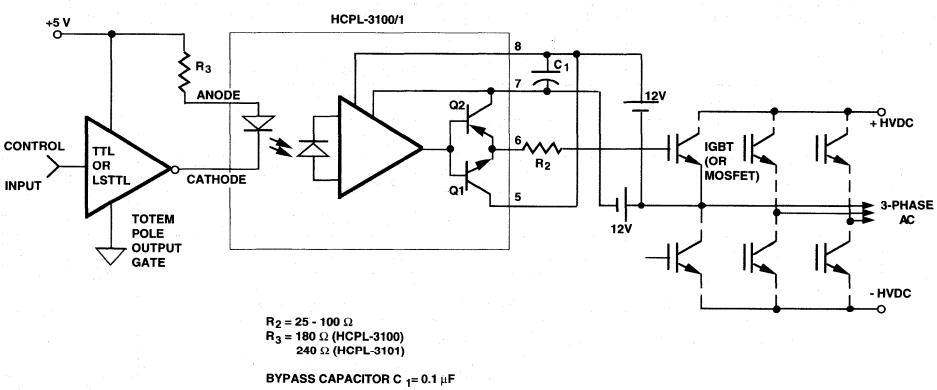


Figure 1. Recommended Output Transistor Protection and Typical Application Circuit.

Electrical Specifications

Over recommended temperature (T_A = -25°C to +80°C) unless otherwise specified.

Parameter		Sym.	Device	Min.	Typ.	Max.	Units	Test Conditions		Fig.	Note
Input Forward Voltage		V_F	HCPL-3100	-	1.2	1.4	V	I_F = 20 mA	T_A = 25°C	13	
				0.6	0.9	-	V	I_F = 0.2 mA			
			HCPL-3101	-	1.6	1.75	V	I_F = 10 mA		14	
				1.2	1.5	-	V	I_F = 0.2 mA			
Input Reverse Current		I_R	HCPL-3100	-	-	10	µA	V_R = 4 V	T_A = 25°C		
			HCPL-3101					V_F = 5 V			
Input Capacitance		C_{IN}		-	30	250	pF	V_F = 0 V, f = 1 kHz, T_A = 25°C			
Output 1	Low Level Voltage	V_{O1L}	HCPL-3100	-	0.2	0.4	V	I_F = 10 mA	V_{CC1} = 12 V, I_{O1} = 0.1 A, V_{CC2} = -12 V	2, 17, 18	2
			HCPL-3101					I_F = 5 mA			
	Leakage Current	I_{O1L}		-	-	500	µA	V_{CC} = V_{O1} = 35 V, V_{O2} = 0 V, I_F = 0 mA, T_A = 25°C		5	
Output 2	High Level Voltage	V_{O2H}	HCPL-3100	18	21	-	V	I_F = 10 mA	V_{CC} = 24 V, V_{O1} = 24 V, I_{O2} = -0.1 A	3, 19, 20	2
			HCPL-3101					I_F = 5 mA			
	Low Level Voltage	V_{O2L}		-	1.2	2.0	V	V_{CC} = V_{O1} = 24 V, I_{O2} = 0.1 A, I_F = 0 mA		4, 21, 22	
	Leakage Current	I_{O2L}	HCPL-3100	-	-	500	µA	I_F = 10 mA	V_{CC} = 35 V, V_{O2} = 35 V, T_A = 25°C	6	
			HCPL-3101					I_F = 5 mA			
Supply Current	High Level	I_{CCH}	HCPL-3100	-	6	10	mA	T_A = 25°C	V_{O1} = 24 V	7, 23	2
				-	-	14	mA	V_{CC} = 24 V, I_F = 10 mA			
			HCPL-3101	-	6	10	mA	T_A = 25°C	V_{O1} = 24 V		
				-	-	14	mA	V_{CC} = 24 V, I_F = 5 mA			
	Low Level	I_{CCL}		-	8	13	mA	T_A = 25°C	V_{O1} = 24 V	7, 24	
				-	-	17	mA	V_{CC} = 24 V, I_F = 0 mA			
Low to High Threshold Input		I_{FLH}	HCPL-3100	1.0	4.0	7.0	mA	T_A = 25°C		8, 15, 16	2, 3
				0.6	-	10.0	mA	V_{CC} = V_{O1} = 24 V			
			HCPL-3101	0.3	1.5	3.0	mA	T_A = 25°C			
				0.2	-	5.0	mA	V_{CC} = V_{O1} = 24 V			

Switching Specifications (T_A = 25°C)

Parameter	Sym.	Device	Min.	Typ.	Max.	Units	Test Conditions		Fig.	Note
Propagation Delay Time to High Output Level	t_{PLH}	HCPL-3100	-	1	2	µs	I_F = 10 mA	V_{CC} = 24 V, V_{O1} = 24 V, R_G = 47 Ω, C_G = 3000 pF	9, 25, 26, 27	2, 6
		HCPL-3101	-	0.3	0.5	µs	I_F = 5 mA			
Propagation Delay Time to Low Output Level	t_{PHL}	HCPL-3100	-	1	2	µs	I_F = 10 mA			
		HCPL-3101	-	0.3	0.5	µs	I_F = 5 mA			
Rise Time	t_r	HCPL-3100	-	0.2	0.5	µs	I_F = 10 mA			
		HCPL-3101					I_F = 5 mA			
Fall Time	t_f	HCPL-3100	-	0.2	0.5	µs	I_F = 10 mA			
		HCPL-3101					I_F = 5 mA			
Output High Level Common Mode Transient Immunity	$\|CM_H\|$	HCPL-3100	1500	5000	-	V/µs	I_F = 10 mA	V_{CM} = 600 V (peak), V_{CC} = 24 V V_{O1} = 24 V $\Delta V_{02H} = \Delta V_{02L}$ = 2.0 V	10	2
		HCPL-3101					I_F = 5mA			
Output Low Level Common Mode Transient Immunity	$\|CM_L\|$		1500	5000	-	V/µs	I_F = 0 mA			

Packaging Characteristics

Parameter	Sym.	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage*	V_{ISO}	5000			V rms	RH = 40% to 60% t = 1 min, T_A = 25°C		4, 5
Resistance (Input-Output)	R_{I-O}	$5x10^{10}$	10^{11}	–	Ω	V_{I-O} = 500 V, T_A = 25°C RH = 40% to 60%		4
Capacitance (Input-Output)	C_{I-O}	–	1.2	–	pF	f = 1 MHz		4

*The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the VDE 0884 Insulation Characteristics Table (if applicable), your equipment level safety specification, or HP Application Note 1074, "Optocoupler Input-Output Endurance Voltage."

Notes:

1. Derate absolute maximum ratings with ambient temperatures as shown in Figures 11 and 12.
2. A bypass capacitor of 0.01 µF or more is needed near the device between V_{CC} and GND when measuring output and transfer characteristics.
3. I_{FLH} represents the forward current when the output goes from low to high.
4. Device considered a two terminal device; pins 1-4 are shorted together and pins 5-8 are shorted together.
5. For devices with minimum V_{ISO} specified at 5000 V rms, in accordance with UL 1577, each optocoupler is proof-tested by applying an insulation test voltage ≥ 6000 V rms for one second (leakage current detection limit, $I_{I-O} \leq$ 200 µA).
6. The t_{PLH} and t_{PHL} propagation delays are measured from the 50% level of the input pulse to the 50% level of the output pulse.
7. R_2 limits the Q1 and Q2 peak currents. For more applications and circuit design information see Application Note "Power Transistor Gate/Base Drive Optocouplers."

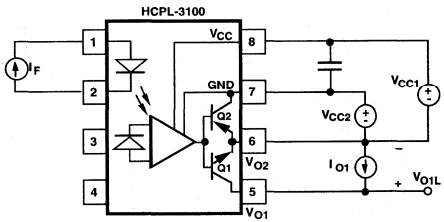


Figure 2. Test Circuit for Low Level Output Voltage V_{O1L}.

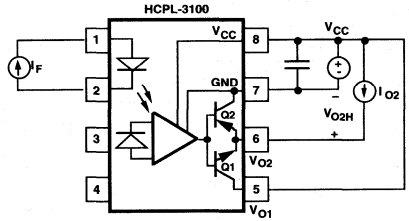


Figure 3. Test Circuit for High Level Output Voltage V_{O2H}.

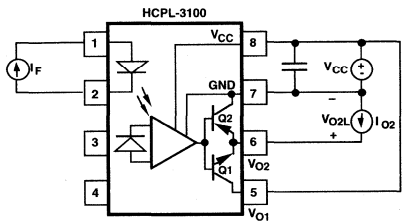


Figure 4. Test Circuit for Low Level Output Voltage V_{O2L}.

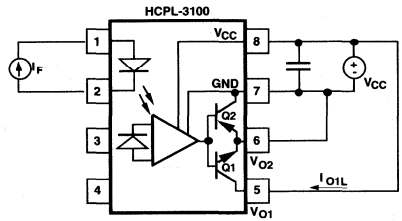


Figure 5. Test Circuit for Leakage Current I_{O1L}.

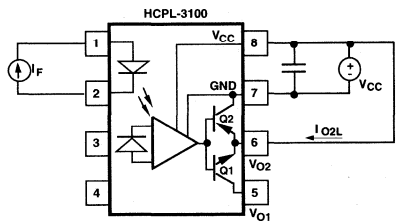


Figure 6. Test Circuit for Leakage Current I_{O2L}.

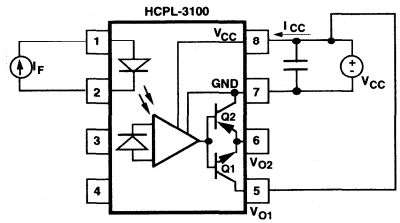


Figure 7. Test Circuit for I_{CCH} and I_{CCL}.

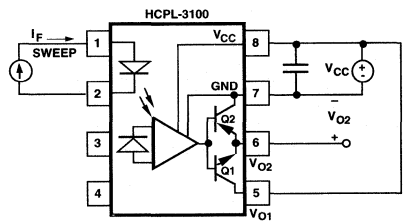


Figure 8. Test Circuit for Threshold Input Current I_{FLH}.

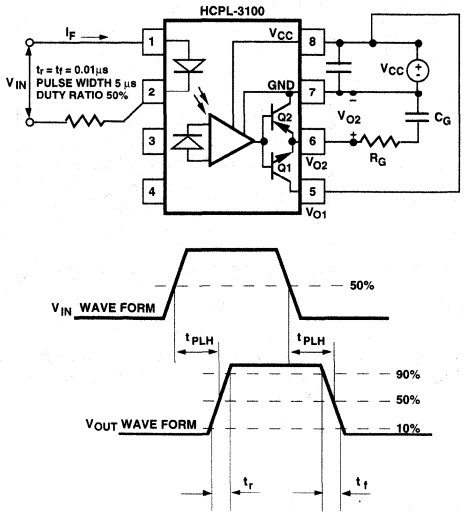


Figure 9. Test Circuit for t_{PLH}, t_{PHL}, t_r, and t_f.

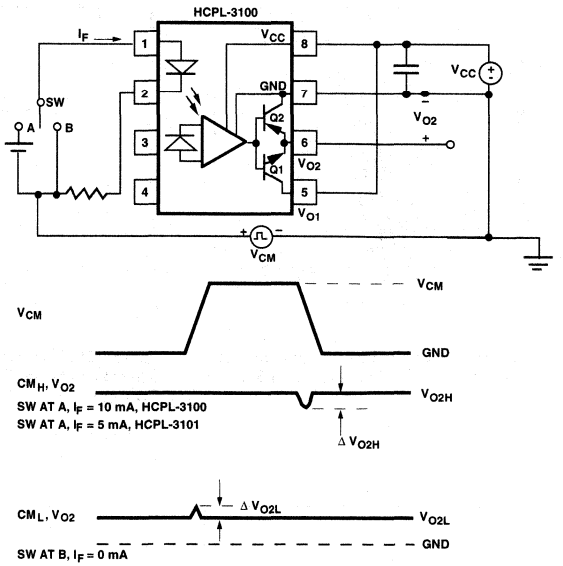


Figure 10. Test Circuit for CM_H and CM_L.

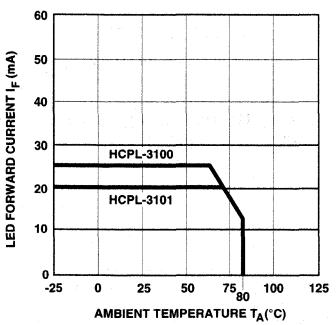


Figure 11. LED Forward Current vs. Ambient Temperature.

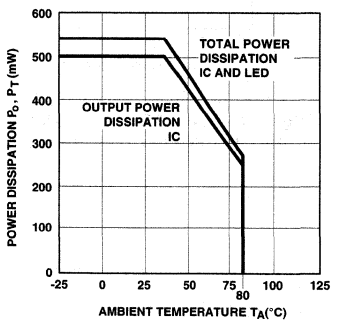


Figure 12. Maximum Power Dissipation vs. Ambient Temperature.

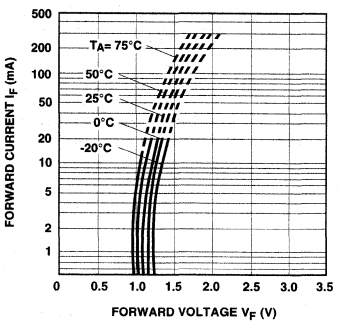


Figure 13. Typical Forward Current vs. Forward Voltage, HCPL-3100.

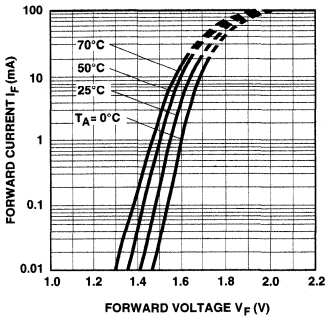


Figure 14. Typical Forward Current vs. Forward Voltage, HCPL-3101.

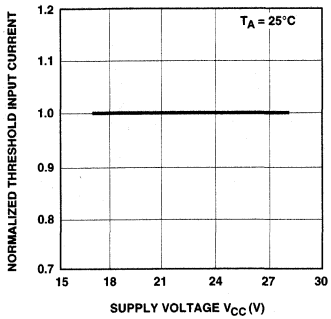


Figure 15. Normalized Low to High Threshold Input Current vs. Supply Voltage.

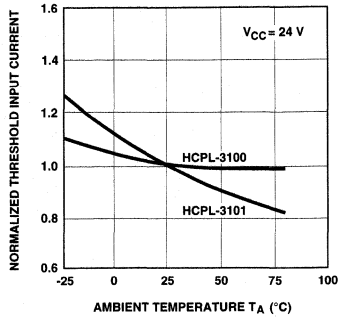


Figure 16. Normalized Low to High Threshold Input Current vs. Ambient Temperature.

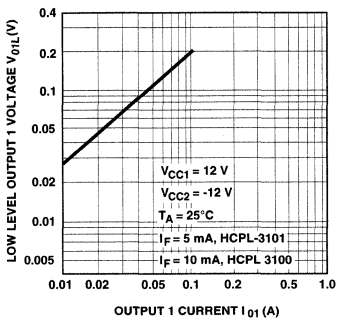


Figure 17. Typical Low Level Output 1 Voltage vs. Output 1 Current.

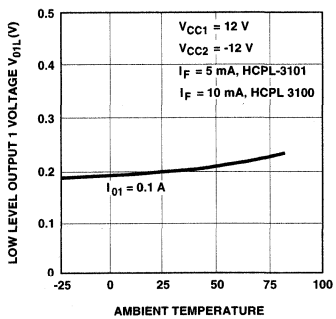


Figure 18. Typical Low Level Output 1 Voltage vs. Ambient Temperature.

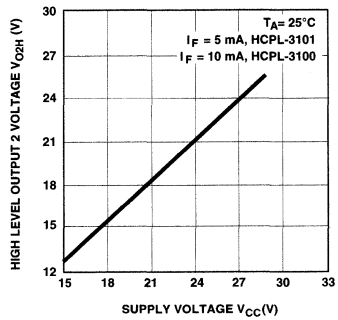


Figure 19. Typical High Level Output 2 Voltage vs. Supply Voltage.

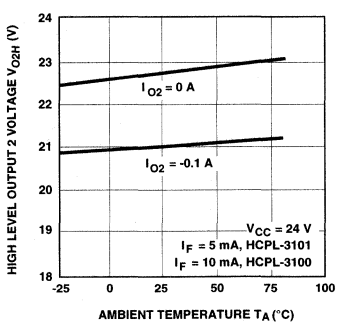


Figure 20. Typical High Level Output 2 Voltage vs. Ambient Temperature.

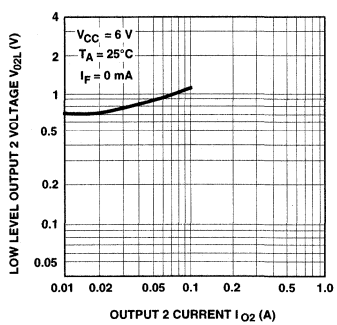


Figure 21. Typical Low Level Output 2 Voltage vs. Output 2 Current.

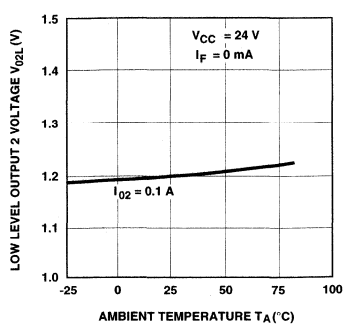


Figure 22. Typical Low Level Output 2 Voltage vs. Ambient Temperature.

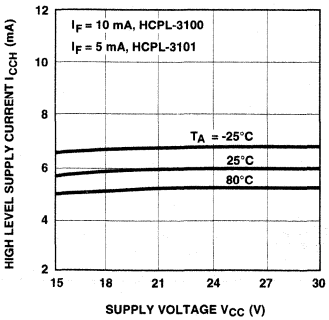


Figure 23. Typical High Level Supply Current vs. Supply Voltage.

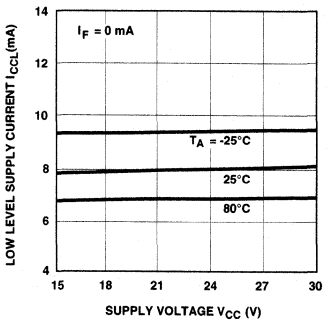


Figure 24. Typical Low Level Supply Current vs. Supply Voltage.

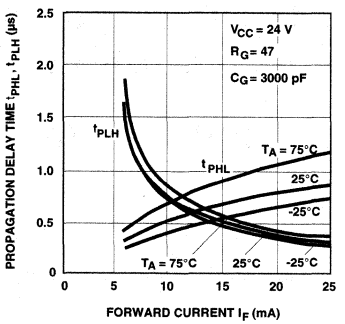


Figure 25. Typical Propagation Delay Time vs. Forward Current, HCPL-3100.

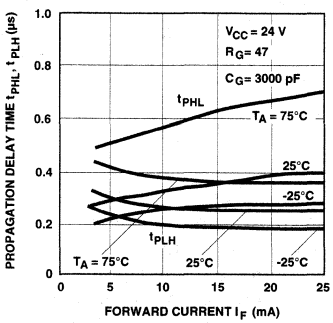


Figure 26. Typical Propagation Delay Time vs. Forward Current, HCPL-3101.

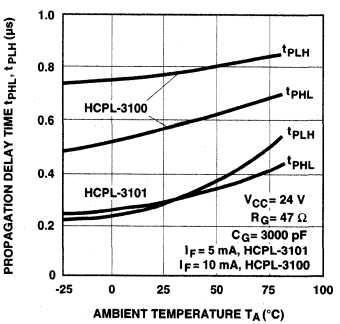


Figure 27. Typical Propagation Delay Time vs. Ambient Temperature.

HEWLETT® PACKARD

AC/DC to Logic Interface Optocouplers

Technical Data

HCPL-3700
HCPL-3760

Features

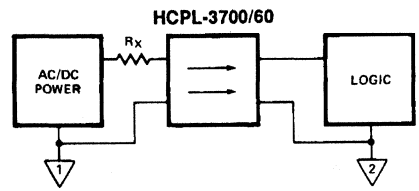
- **Standard (HCPL-3700) and Low Input Current (HCPL-3760) Versions**
- **AC or DC Input**
- **Programmable Sense Voltage**
- **Hysteresis**
- **Logic Compatible Output**
- **Thresholds Guaranteed over Temperature**
- **Thresholds Independent of LED Optical Parameters**
- **Recognized under UL 1577 and CSA Approved for Dielectric Withstand Proof Test Voltage of 2500 Vac, 1 Minute**

Applications

- **Limit Switch Sensing**
- **Low Voltage Detector**
- **5 V-240 V AC/DC Voltage Sensing**
- **Relay Contact Monitor**
- **Relay Coil Voltage Monitor**
- **Current Sensing**
- **Microprocessor Interfacing**

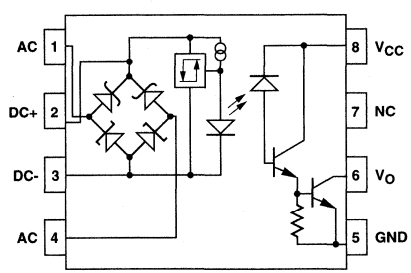
Description

The HCPL-3700 and HCPL-3760 are voltage/current threshold detection optocouplers. The HCPL-3760 is a low-current version of the HCPL-3700. To obtain lower current operation, the HCPL-3760 uses a high-efficiency AlGaAs LED which provides higher light output at lower drive currents. Both devices utilize threshold sensing input buffer ICs which permit control of threshold levels over a wide range of input voltages with a single external resistor.



The input buffer incorporates several features: hysteresis for extra noise immunity and switching immunity, a diode bridge for easy use with ac input signals, and internal clamping

Functional Diagram



TRUTH TABLE (POSITIVE LOGIC)

INPUT	OUTPUT
H	L
L	H

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

5965-3582E

diodes to protect the buffer and LED from a wide range of over-voltage and over-current transients. Because threshold sensing is done prior to driving the LED, variations in optical coupling from the LED to the detector will have no effect on the threshold levels.

The HCPL-3700's input buffer IC has a nominal turn on threshold of 2.5 mA (I_{TH} +) and 3.7 volts (V_{TH} +).

The buffer IC for the HCPL-3760 was redesigned to permit a lower input current. The nominal turn on threshold for the HCPL-3760 is 1.2 mA (I_{TH} +) and 3.7 volts (V_{TH} +).

The high gain output stage features an open collector output providing both TTL compatible saturation voltages and CMOS compatible breakdown voltages.

By combining several unique functions in a single package, the user is provided with an ideal component for industrial control computer input boards and other applications where a predetermined input threshold level is desirable.

Ordering Information

Specify Part Number followed by Option Number (if desired)

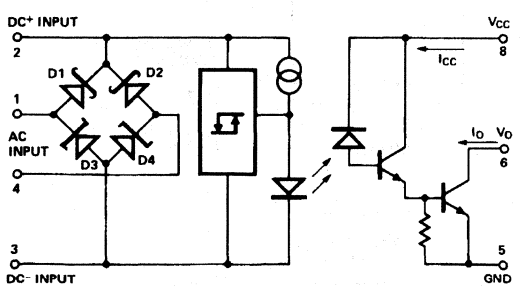
Example

HCPL-3700#XXX

- 300 = Gull Wing Surface Mount Option
- 500 = Tape/Reel Package Option (1 K min.)

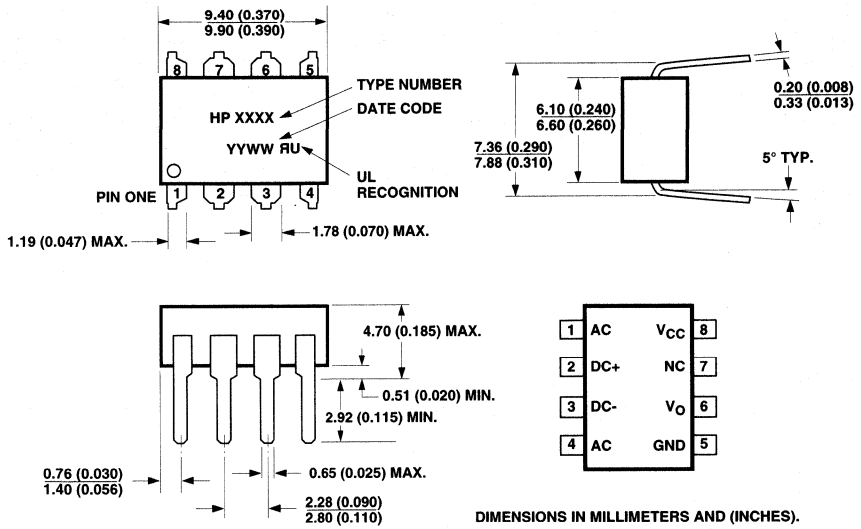
Option data sheets available. Contact your Hewlett-Packard sales representative or authorized distributor for information.

Schematic



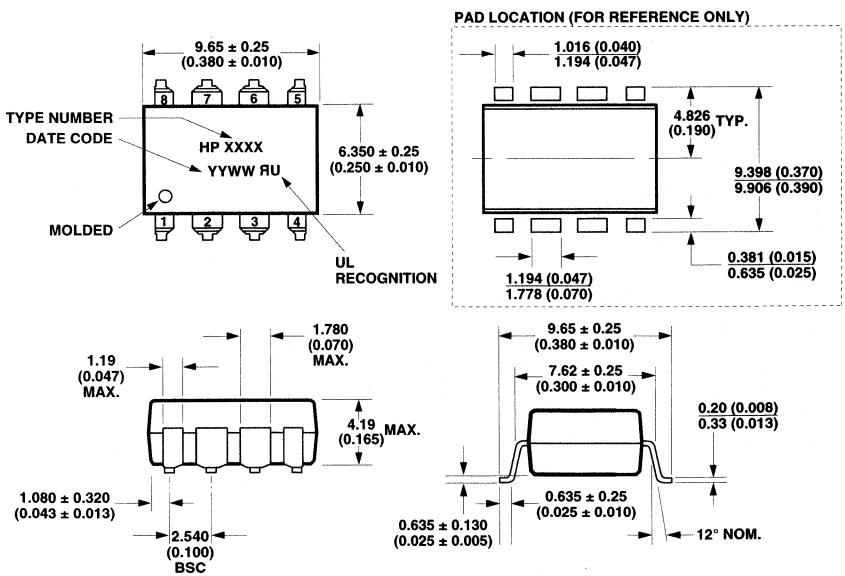
Package Outline Drawings

Standard DIP Package



DIMENSIONS IN MILLIMETERS AND (INCHES).

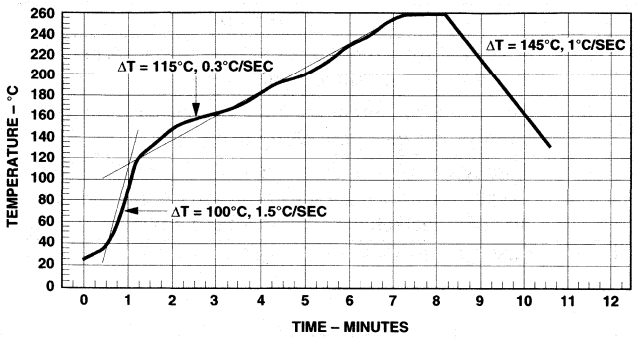
Gull Wing Surface Mount Option 300



DIMENSIONS IN MILLIMETERS (INCHES).
TOLERANCES (UNLESS OTHERWISE SPECIFIED): xx.xx = 0.01
xx.xxx = 0.005

LEAD COPLANARITY
MAXIMUM: 0.102 (0.004)

Maximum Solder Reflow Thermal Profile



(NOTE: USE OF NON-CHLORINE ACTIVATED FLUXES IS RECOMMENDED.)

Regulatory Information

The HCPL-3700/60 has been approved by the following organizations:

UL

Recognized under UL 1577, component recognition program, File E55361.

CSA

Approved under CSA Component Acceptance Notice #5, File CA 88324.

Insulation and Safety Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min. External Air Gap (External Clearance)	L(IO1)	7.1	mm	Measured from input terminals to output terminals, shortest distance through air
Min. External Tracking Path (External Creepage)	L(IO2)	7.4	mm	Measured from input terminals to output terminals, shortest distance path along body
Min. Internal Plastic Gap (Internal Clearance)		0.08	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity
Tracking Resistance (Comparative Tracking Index)	CTI	200	V	DIN IEC 112/VDE 0303 PART 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Option 300 – surface mount classification is Class A in accordance with CECC 00802.

Absolute Maximum Ratings (No derating required up to 70°C)

Parameter		Symbol	Min.	Max.	Units	Note
Storage Temperature		T_S	-55	125	°C	
Operating Temperature		T_A	-40	85	°C	
Lead Soldering Cycle	Temperature			260	°C	1
	Time			10	s	
Input Current	Average	I_{IN}		50	mA	2
	Surge			140		2, 3
	Transient			500		
Input Voltage (Pins 2-3)		V_{IN}	-0.5		V	
Input Power Dissipation		P_{IN}		230	mW	4
Total Package Power Dissipation		P_T		305	mW	5
Output Power Dissipation		P_O		210	mW	6
Output Current	Average	I_O		30	mA	7
Supply Voltage (Pins 8-5)		V_{CC}	-0.5	20	V	
Output Voltage (Pins 6-5)		V_O	-0.5	20	V	
Solder Reflow Temperature Profile		See Package Outline Drawings section				

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Note
Supply Voltage	V_{CC}	2	18	V	
Operating Temperature	T_A	0	70	°C	
Operating Frequency	f	0	4	kHz	8

Electrical Specifications

Over Recommended Temperature T_A = 0°C to 70°C, Unless Otherwise Specified.

Parameter		Sym.	Device	Min.	Typ.[9]	Max.	Units	Conditions	Fig.	Note
Input Threshold Current		I_{TH+}	HCPL-3700	1.96	2.5	3.11	mA	$V_{IN} = V_{TH+}$; V_{CC} = 4.5 V; V_O = 0.4 V; $I_O \geq$ 4.2 mA	2, 3	14
			HCPL-3760	0.87	1.2	1.56				
		I_{TH-}	HCPL-3700	1.00	1.3	1.62		$V_{IN} = V_{TH-}$; V_{CC} = 4.5 V; V_O = 2.4 V; $I_{OH} \leq$ 100 µA		
			HCPL-3760	0.43	0.6	0.80				
Input Threshold Voltage	DC (Pins 2, 3)	V_{TH+}		3.35	3.7	4.05	V	$V_{IN} = V_2 - V_3$; Pins 1 & 4 Open V_{CC} = 4.5 V; V_O = 0.4 V; $I_O \geq$ 4.2 mA		
		V_{TH-}		2.01	2.6	2.86	V	$V_{IN} = V_2 - V_3$; Pins 1 & 4 Open V_{CC} = 4.5 V; V_O = 2.4 V; $I_O \leq$ 100 µA		
	AC (Pins 1, 4)	V_{TH+}		4.23	4.9	5.50	V	$V_{IN} = \lvert V_1 - V_4 \rvert$; Pins 2 & 3 Open V_{CC} = 4.5 V; V_O = 0.4 V; $I_O \geq$ 4.2 mA		14, 15
		V_{TH-}		2.87	3.7	4.20	V	$V_{IN} = \lvert V_1 - V_4 \rvert$; Pins 2 & 3 Open V_{CC} = 4.5 V; V_O = 2.4 V; $I_O \leq$ 100 µA		
Hysteresis		I_{HYS}	HCPL-3700		1.2		mA	$I_{HYS} = I_{TH+} - I_{TH-}$	2	
			HCPL-3760		0.6					
		V_{HYS}			1.2		V	$V_{HYS} = V_{TH+} - V_{TH-}$		
Input Clamp Voltage		V_{IHC1}		5.4	6.0	6.6	V	$V_{IHC1} = V_2 - V_3$; V_3 = GND; I_{IN} = 10 mA; Pins 1 & 4 Connected to Pin 3	1	
		V_{IHC2}		6.1	6.7	7.3	V	$V_{IHC2} = \lvert V_1 - V_4 \rvert$; $\lvert I_{IN} \rvert$ = 10 mA; Pins 2 & 3 Open		
		V_{IHC3}			12.0	13.4	V	$V_{IHC3} = V_2 - V_3$; V_3 = GND; I_{IN} = 15 mA; Pins 1 & 4 Open		
		V_{ILC}			-0.76		V	$V_{ILC} = V_2 - V_3$; V_3 = GND; I_{IN} = -10 mA		
Input Current		I_{IN}	HCPL-3700	3.0	3.7	4.4	mA	$V_{IN} = V_2 - V_3$ = 5.0 V Pins 1 & 4 Open	5	
			HCPL-3760	1.5	1.8	2.2				
Bridge Diode Forward Voltage		$V_{D1,2}$	HCPL-3700		0.59		V	I_{IN} = 3 mA		
			HCPL-3760		0.51			I_{IN} = 1.5 mA		
		$V_{D3,4}$	HCPL-3700		0.74			I_{IN} = 3 mA		
			HCPL-3760		0.71			I_{IN} = 1.5 mA		
Logic Low Output Voltage		V_{OL}			0.1	0.4	V	V_{CC} = 4.5 V; I_{OL} = 4.2 mA	5	14
Logic High Output Current		I_{OH}				100	µA	$V_{OH} = V_{CC}$ = 18 V		14
Logic Low Supply Current		I_{CCL}	HCPL-3700		1.2	4	mA	$V_2 - V_3$ = 5.0 V; V_O = Open; V_{CC} = 5.0 V	6	
			HCPL-3760		0.7	3				
Logic High Supply Current		I_{CCH}			0.002	4	µA	V_{CC} = 18 V; V_O = Open	4	14
Input Capacitance		C_{IN}			50		pF	f = 1 MHz; V_{IN} = 0 V, Pins 2 & 3, Pins 1 & 4 Open		

Switching Specifications

T_A = 25°C, V_{CC} = 5.0 V, Unless Otherwise Specified.

Parameter	Sym.	Device	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to Logic Low at Output	t_{PHL}	HCPL-3700		4.0	15.0	µs	R_L = 4.7 kΩ, C_L = 30 pF	7, 10	10
		HCPL-3760		4.5					
Propagation Delay Time to Logic High at Output	t_{PLH}	HCPL-3700		10.0	40.0	µs	R_L = 4.7 kΩ, C_L = 30 pF		11
		HCPL-3760		8.0					
Output Rise Time (10-90%)	t_r	HCPL-3700		20		µs	R_L = 4.7 kΩ, C_L = 30 pF	8	
		HCPL-3760		14					
Output Fall Time (90-10%)	t_f	HCPL-3700		0.3		µs	R_L = 4.7 kΩ, C_L = 30 pF		
		HCPL-3760		0.4					
Common Mode Transient Immunity at Logic High Output	$\|CM_H\|$			4000		V/µs	I_{IN} = 0 mA, R_L = 4.7 kΩ, $V_{O\ min}$ = 2.0 V, V_{CM} = 1400 V	9, 11	12, 13
Common Mode Transient Immunity at Logic Low Output	$\|CM_L\|$	HCPL-3700		600		V/µs	I_{IN} = 3.11 mA; R_L = 4.7 kΩ, $V_{O\ max}$ = 0.8 V, V_{CM} = 140 V		
		HCPL-3760					I_{IN} = 1.56 mA; R_L = 4.7 kΩ, $V_{O\ max}$ = 0.8 V, V_{CM} = 140 V		

Package Characteristics

Over Recommended Temperature T_A = 0°C to 70°C, Unless Otherwise Specified.

Parameter	Sym.	Min.	Typ.[9]	Max.	Units	Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage*	V_{ISO}	2500			V rms	RH ≤ 50%, t = 1 min; T_A = 25°C		16, 17
Input-Output Resistance	R_{I-O}		10^{12}		Ω	V_{I-O} = 500 Vdc		16
Input-Output Capacitance	C_{I-O}		0.6		pF	f = 1 MHz; V_{I-O} = 0 Vdc		

*The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the VDE 0884 Insulation Characteristics Table (if applicable), your equipment level safety specification, or HP Application Note 1074, "Optocoupler Input-Output Endurance Voltage."

Notes:

1. Measured at a point 1.6 mm below seating plane.
2. Current into/out of any single lead.
3. Surge input current duration is 3 ms at 120 Hz pulse repetition rate. Transient input current duration is 10 μs at 120 Hz pulse repetition rate. Note that maximum input power, P_{IN}, must be observed.
4. Derate linearly above 70°C free-air temperature at a rate of 4.1 mW/°C. Maximum input power dissipation of 230 mW allows an input IC junction temperature of 125°C at an ambient temperature of T_A = 70°C with a typical thermal resistance from junction to ambient of θ_{JA1} = 240°C/W. Excessive P_{IN} and T_J may result in IC chip degradation.
5. Derate linearly above 70°C free-air temperature at a rate of 5.4 mW/°C.
6. Derate linearly above 70°C free-air temperature at a rate of 3.9 mW/°C. Maximum output power dissipation of 210 mW allows an output IC junction temperature of 125°C at an ambient temperature of T_A = 70°C with a typical thermal resistance from junction to ambient of θ_{JA0} = 265°C/W.
7. Derate linearly above 70°C free-air temperature at a rate of 0.6 mA/°C.
8. Maximum operating frequency is defined when output waveform Pin 6 obtains only 90% of V_{CC} with R_L = 4.7 kΩ, C_L = 30 pF using a 5 V square wave input signal.
9. All typical values are at T_A = 25°C, V_{CC} = 5.0 V unless otherwise stated.
10. The t_{PHL} propagation delay is measured from the 2.5 V level of the leading edge of a 5.0 V input pulse (1 μs rise time) to the 1.5 V level on the leading edge of the output pulse (see Figure 10).
11. The t_{PLH} propagation delay is measured from the 2.5 V level of the trailing edge of a 5.0 V input pulse (1 μs fall time) to the 1.5 V level on the trailing edge of the output pulse (see Figure 10).
12. Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, to insure that the output will remain in a Logic High state (i.e., V_O > 2.0 V). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to insure that the output will remain in a Logic Low state (i.e., V_O < 0.8 V). See Figure 11.
13. In applications where dV_{CM}/dt may exceed 50,000 V/μs (such as static discharge), a series resistor, R_{CC}, should be included to protect the detector IC from destructively high surge currents. The recommended value for R_{CC} is 240 Ω per volt of allowable drop in V_{CC} (between Pin 8 and V_{CC}) with a minimum value of 240 Ω.
14. Logic low output level at Pin 6 occurs under the conditions of $V_{IN} \geq V_{TH+}$ as well as the range of $V_{IN} > V_{TH-}$ once V_{IN} has exceeded V_{TH+}. Logic high output level at Pin 6 occurs under the conditions of $V_{IN} \leq V_{TH-}$ as well as the range of $V_{IN} < V_{TH+}$ once V_{IN} has decreased below V_{TH-}.
15. AC voltage is instantaneous voltage.
16. Device considered a two terminal device: Pins 1, 2, 3, 4 connected together, and Pins 5, 6, 7, 8 connected together.
17. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 3000 V rms for 1 second (leakage detection current limit, $I_{i-o} \leq$ 5 μA).

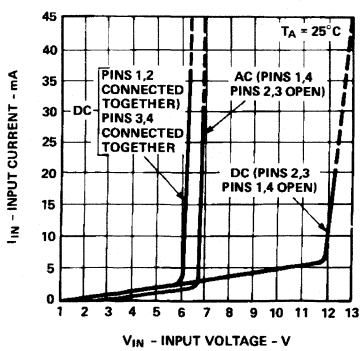
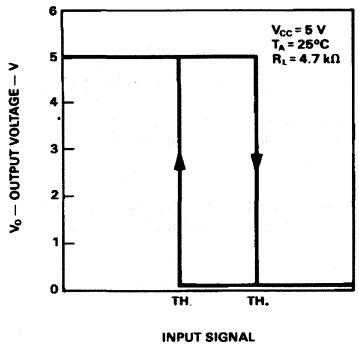
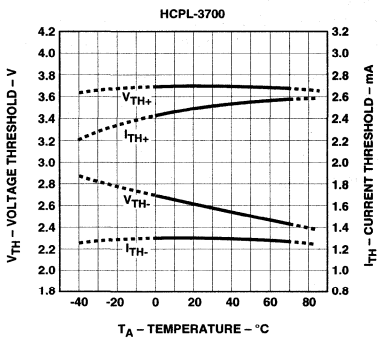


Figure 1. Typical Input Characteristics, I_{IN} vs. V_{IN} (AC Voltage is Instantaneous Value).



	DEVICE	TH_+	TH_-	INPUT CONNNECTION
I_{TH}	HCPL-3700	2.5 mA	1.3 mA	PINS 2, 3
	HCPL-3760	1.2 mA	0.6 mA	OR 1, 4
$V_{TH(dc)}$	BOTH	3.7 V	2.6 V	PINS 2, 3
$V_{TH(ac)}$	BOTH	4.9 V	3.7 V	PINS 1, 4

Figure 2. Typical Transfer Characteristics.



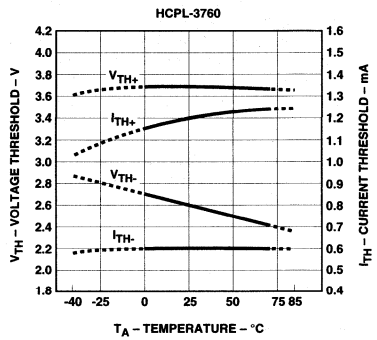


Figure 3. Typical DC Threshold Levels vs. Temperature.

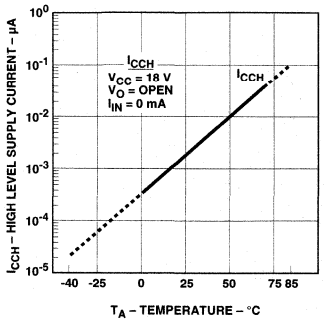


Figure 4. Typical High Level Supply Current, I_{CCH} vs. Temperature.

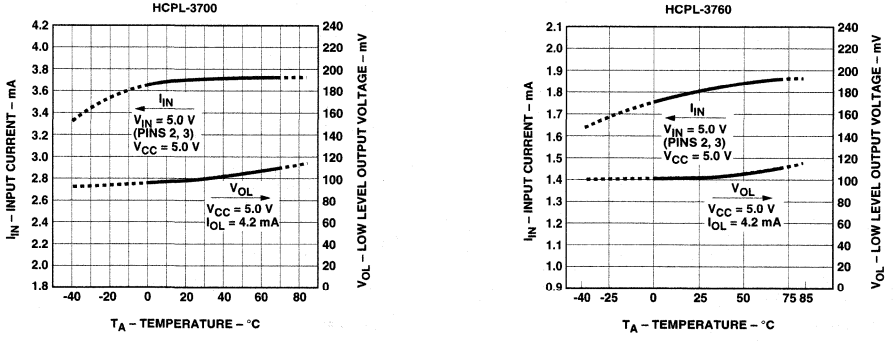


Figure 5. Typical Input Current, I_{IN}, and Low Level Output Voltage, V_{OL}, vs. Temperature.

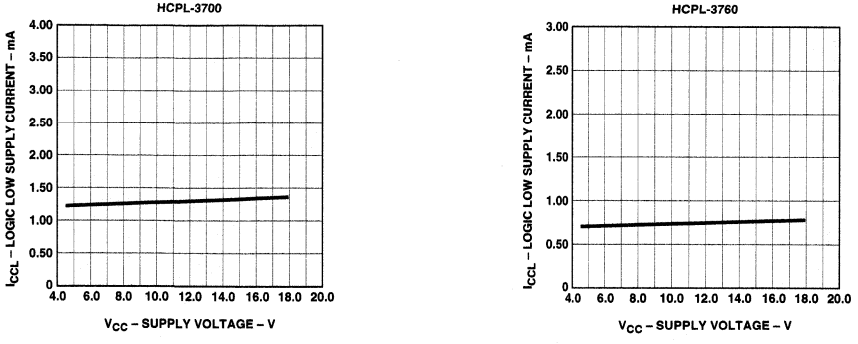


Figure 6. Typical Logic Low Supply Current vs. Supply Voltage.

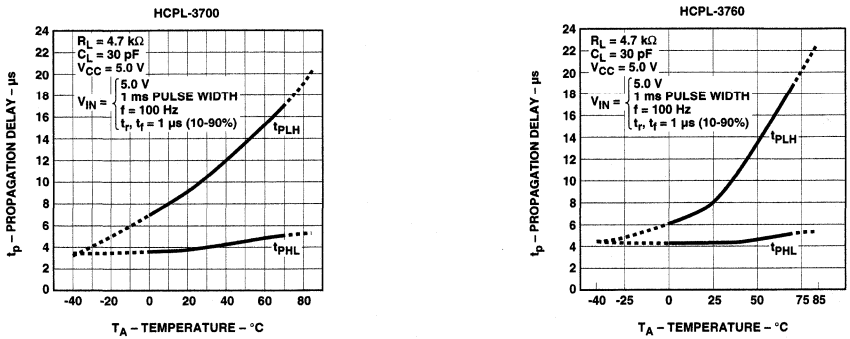


Figure 7. Typical Propagation Delay vs. Temperature.

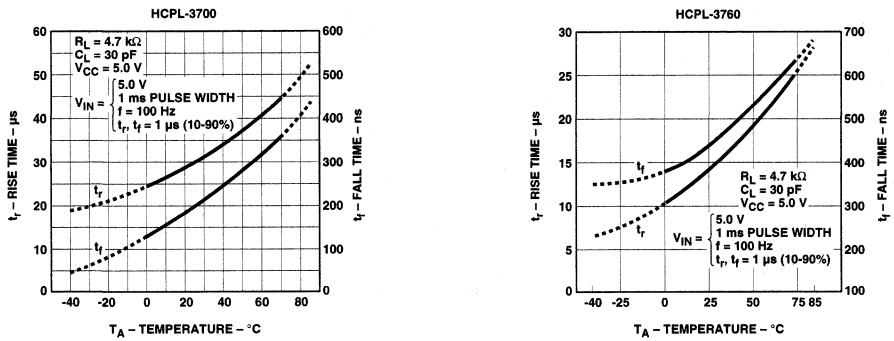


Figure 8. Typical Rise, Fall Times vs. Temperature.

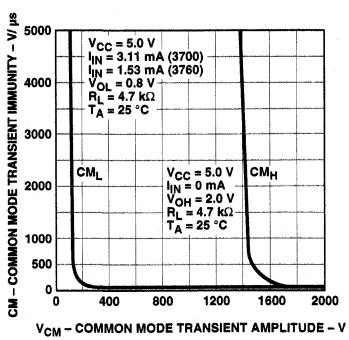


Figure 9. Common Mode Transient Immunity vs. Common Mode Transient Amplitude.

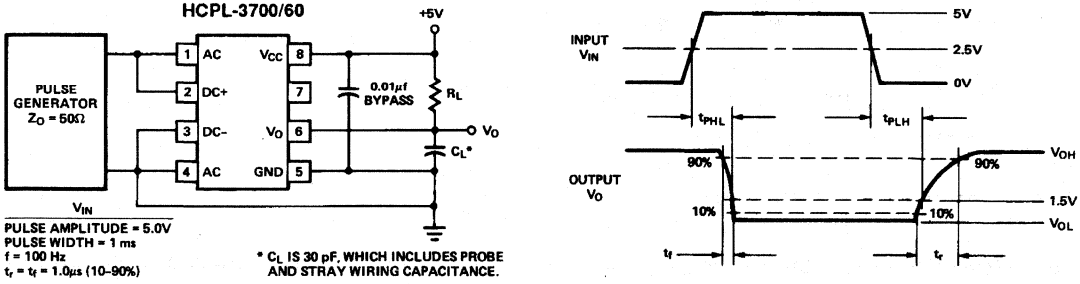


Figure 10. Switching Test Circuit.

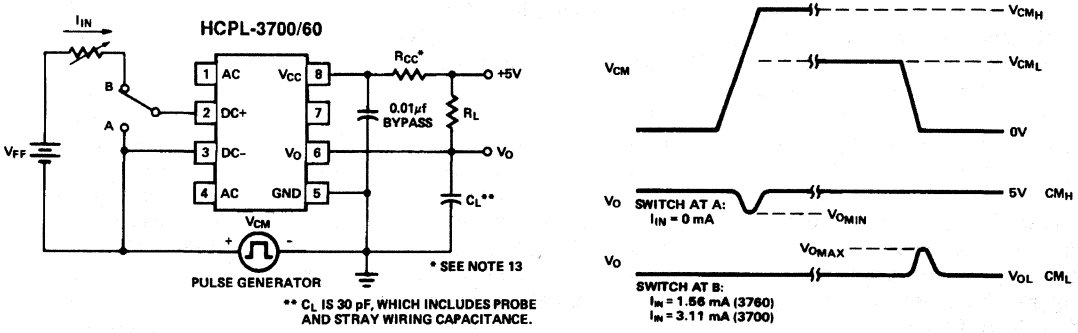


Figure 11. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

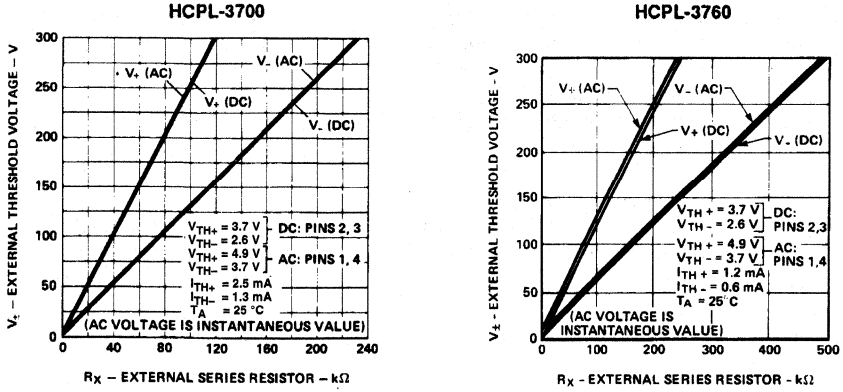


Figure 12. Typical External Threshold Characteristics, V± vs. R_x.

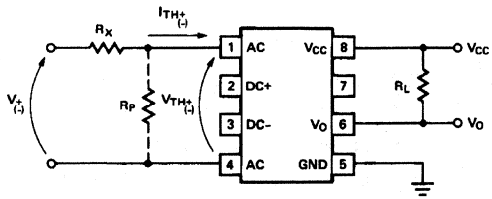


Figure 13. External Threshold Voltage Level Selection.

Electrical Considerations

The HCPL-3700/3760 optocouplers have internal temperature compensated, predictable voltage and current threshold points which allow selection of an external resistor, R_X, to determine larger external threshold voltage levels. For a desired external threshold voltage, $V_{\pm}$, a corresponding typical value of R_X can be obtained from Figure 12. Specific calculation of R_X can be obtained from Equation (1). Specification of both V_+ and V_- voltage threshold levels simultaneously can be obtained by the use of R_X and R_P as shown in Figure 13 and determined by Equations (2) and (3).

R_X can provide over-current transient protection by limiting input current during a transient condition. For monitoring contacts of a relay or switch, the HCPL-3700/3760 in combination with R_X and R_P can be used to allow a specific current to be conducted through the contacts for cleaning purposes (wetting current).

The choice of which input voltage clamp level to choose depends upon the application of this device (see Figure 1). It is recommended that the low clamp condition be used when possible. The low clamp condition in conjunction with the low input current feature will ensure extremely low input power dissipation.

In applications where dV_{CM}/dt may be extremely large (such as static discharge), a series resistor, R_{CC}, should be connected in series with V_{CC} and Pin 8 to protect the detector IC from destructively high surge currents. See Note 13 for determination of R_{CC}. In addition, it is recommended that a ceramic disc bypass capacitor of 0.01 µF be placed between Pins 8 and 5 to reduce the effect of power supply noise.

For interfacing ac signals to TTL systems, output low pass filtering can be performed with a pullup resistor of 1.5 kΩ and 20 µF capacitor. This application requires a Schmitt trigger gate to avoid slow rise time chatter problems. For ac input applications, a filter capacitor can be placed across the dc input terminals for either signal or transient filtering.

Either ac (Pins 1, 4) or dc (Pins 2, 3) input can be used to determine external threshold levels.

For one specifically selected external threshold voltage level V_+ or V_-, R_X can be determined without use of R_P via

$$R_X = \frac{V_{+(-)} - V_{TH+(-)}}{I_{TH+(-)}} \quad (1)$$

For two specifically selected external threshold voltage levels, V_+ and V_-, the use of R_X and R_P will permit this selection via equations (2), (3) provided the following conditions are met. If the denominator of equation (2) is positive, then

$$\frac{V_+}{V_-} \geq \frac{V_{TH+}}{V_{TH-}} \text{ and } \frac{V_+ - V_{TH+}}{V_- - V_{TH-}} < \frac{I_{TH+}}{I_{TH-}}$$

Conversely, if the denominator of equation (2) is negative, then

$$\frac{V_+}{V_-} \leq \frac{V_{TH+}}{V_{TH-}} \text{ and } \frac{V_+ - V_{TH+}}{V_- - V_{TH-}} > \frac{I_{TH+}}{I_{TH-}}$$

$$R_X = \frac{V_{TH-}(V_+) - V_{TH+}(V_-)}{I_{TH+}(V_{TH-}) - I_{TH-}(V_{TH+})} \quad (2)$$

$$R_P = \frac{V_{TH-}(V_+) - V_{TH+}(V_-)}{I_{TH+}(V_- - V_{TH-}) + I_{TH-}(V_{TH+} - V_+)} \quad (3)$$

Optically Coupled 20 mA Current Loop Transmitter

Technical Data

HCPL-4100

Features

- **Guaranteed 20 mA Loop Parameters**
- **Data Input Compatible with LSTTL, TTL and CMOS Logic**
- **Guaranteed Performance over Temperature (0°C to 70°C)**
- **Internal Shield for High Common Mode Rejection**
- **20 kBaud Data Rate at 400 Metres Line Length**
- **Guaranteed On and Off Output Current Levels**
- **Safety Approval**
  UL Recognized -2500 V rms for 1 minute
  CSA Approved
- **Optically Coupled 20 mA Current Loop Receiver, HCPL-4200, Also Available**

Applications

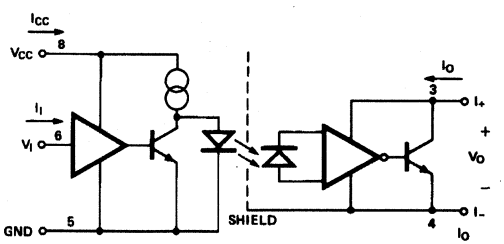
- **Isolated 20 mA Current Loop Transmitter in:**
  Computer Peripherals
  Industrial Control Equipment
  Data Communications Equipment

Description

The HCPL-4100 optocoupler is designed to operate as a transmitter in equipment using the 20 mA current loop. 20 mA current loop systems conventionally signal a logic high state by transmitting 20 mA of loop current (MARK), and signal a logic low state by allowing no more than a few milliamperes of loop current (SPACE). Optical coupling of the signal from the logic input to the 20 mA current loop breaks ground loops and provides very high immunity to common mode interference.

The HCPL-4100 data input is compatible with LSTTL, TTL, or CMOS logic gates. The input integrated circuit drives a GaAsP LED. The light emitted by the LED is sensed by a second integrated circuit that allows 20 mA to pass with a voltage drop of less than 2.7 volts when no light is emitted and allows less than 2 mA to pass when light is emitted. The transmitter output is capable of withstanding 27 volts. The input integrated circuit provides a controlled amount of LED drive current and takes into account any LED light output degradation. The internal shield allows a guaranteed 1000 V/μs common mode transient immunity.

Functional Diagram



TRUTH TABLE (POSITIVE LOGIC)*

V_I	V_{CC}	I_O
H	ON	H
L	ON	L
H	OFF	H
L	OFF	H

*CURRENT LOOP CONVENTION — H = MARK: $I_O \geq 12$ mA, L = SPACE: $I_O \leq 2$ mA.

A 0.1 μF bypass capacitor connected between pins 8 and 5 is recommended.

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Ordering Information

Specify part number followed by Option Number (if desired).

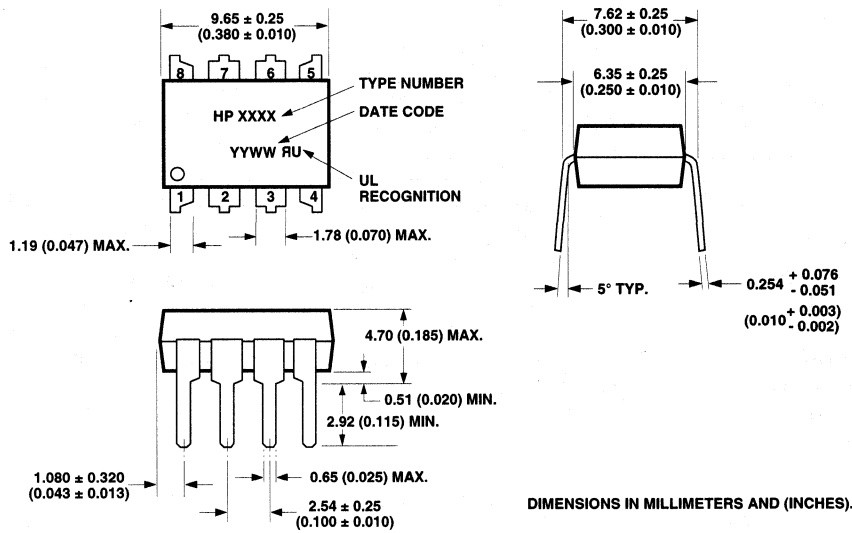
HCPL-4100# XXX

- 300 = Gull Wing Surface Mount Lead Option
- 500 = Tape/Reel Package Option (1 K min)

Option data sheets available. Contact your Hewlett-Packard sales representative or authorized distributor for information.

Package Outline Drawings

8-Pin DIP Package (HCPL-4100)



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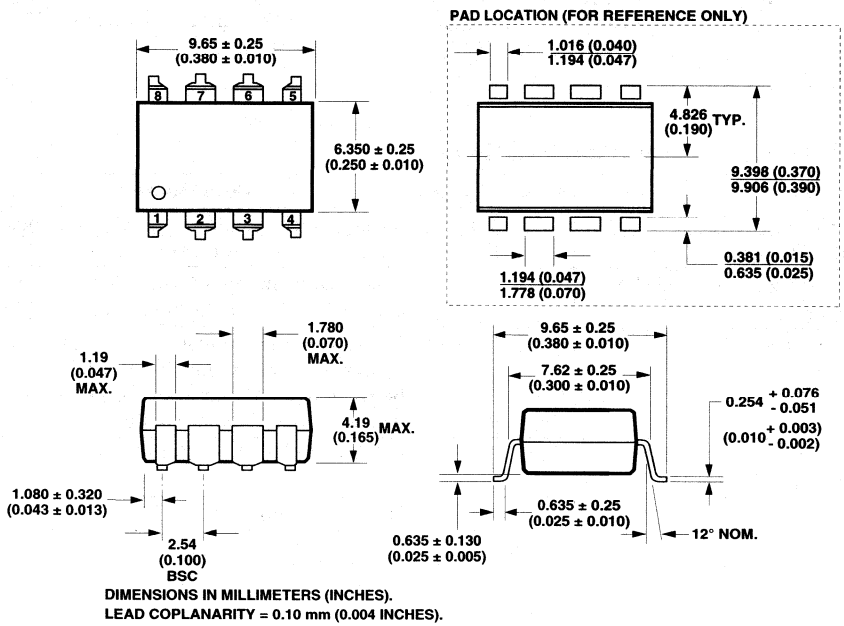
8-Pin DIP Package with Gull Wing Surface Mount Option 300 (HCPL-4100)



Thermal Profile (Option #300)

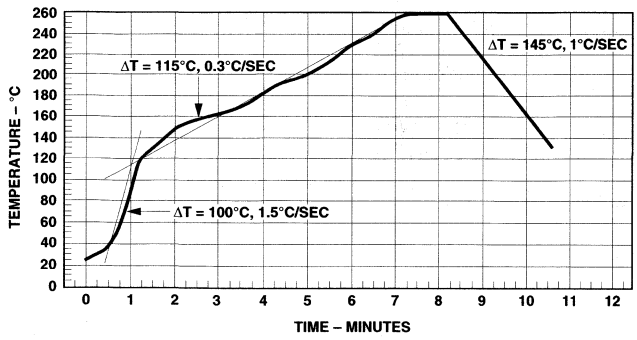


Figure 1. Maximum Solder Reflow Thermal Profile.
(Note: Use of non-chlorine activated fluxes is recommended.)

Regulatory Information

The HCPL-4100 has been approved by the following organizations:

UL

Recognized under UL 1577, Component Recognition Program, File E55361.

CSA

Approved under CSA Component Acceptance Notice #5, File CA 88324.

Insulation and Safety Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min. External Air Gap (External Clearance)	L(IO1)	7.1	mm	Measured from input terminals to output terminals, shortest distance through air
Min. External Tracking Path (External Creepage)	L(IO2)	7.4	mm	Measured from input terminals to output terminals, shortest distance path along body
Min. Internal Plastic Gap (Internal Clearance)		0.08	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity
Tracking Resistance (Comparative Tracking Index)	CTI	200	Volts	DIN IEC 112/VDE 0303 PART 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Option 300 – surface mount classification is Class A in accordance with CECC 00802.

Absolute Maximum Ratings

(No Derating Required up to 55°C)

Storage Temperature ..... -55°C to +125°C
Operating Temperature ..... -40°C to +85°C
Lead Solder Temperature .... 260°C for 10 s (1.6 mm below seating plane)
Supply Voltage – V_{CC} ..... 0 V to 20 V
Average Output Current - I_O ..... -30 mA to 30 mA
Peak Output Current - I_O ..... Internally Limited
Output Voltage – V_O ..... -0.4 V to 27 V
Input Voltage – V_I ..... -0.5 V to 20 V
Input Power Dissipation – P_I ..... 265 mW[1]
Output Power Dissipation – P_O ..... 125 mW[2]
Total Power Dissipation – P ..... 360 mW[3]
Infrared and Vapor Phase Reflow Temperature
(Option #300) ..... see Fig. 1, Thermal Profile

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage	V_{CC}	4.5	20	Volts
Input Voltage Low	V_{IL}	0	0.8	Volts
Input Voltage High	V_{IH}	2.0	20	Volts
Operating Temperature	T_A	0	70	°C
Output Voltage	V_O	0	27	Volts
Output Current	I_O	0	24	mA

DC Electrical Specifications

For 0°C ≤ T_A ≤ 70°C, 4.5 V ≤ V_{CC} ≤ 20 V, all typicals at T_A = 25°C and V_{CC} = 5 V unless otherwise noted. See note 12.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions		Fig.	Note
Mark State Output Current	V_{MO}		1.8 2.2 2.35	2.25 2.7	Volts Volts Volts	I_O = 2 mA I_O = 12 mA I_O = 20 mA	V_I = 2.0 V	2, 3	
Mark State Short Circuit Output Current	I_{SC}	30	85		mA	V_I = 2 V, V_O = 5 V to 27 V			4
Space State Input Current	I_{SO}	0.5	1.1	2.0	mA	V_I = 0.8 V, V_O = 27 V		4	
Low Level Input Current	I_{IL}		-0.12	-0.32	mA	V_{CC} = 20 V, V_I = 0.4 V			
Low Level Input Voltage	V_{IL}			0.8	Volts				
High Level Input Voltage	V_{IH}	2.0			Volts				
High Level Input Current	I_{IH}		 0.005	20 100 250	µA µA µA	V_I = 2.7 V V_I = 5.5 V V_I = 20 V			
Supply Current	I_{CC}		7.0 7.8	11.5 13	mA mA	V_{CC} = 5.5 V V_{CC} = 20 V	0 V ≤ V_I ≤ 20 V		

Switching Specifications

For $0°C \leq T_A \leq 70°C$, $4.5\ V \leq V_{CC} \leq 20\ V$, all typicals at $T_A = 25°C$ and $V_{CC} = 5\ V$ unless otherwise noted. See note 12.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to Logic High Output Level	t_{PLH}		0.3	1.6	µs	$C_O = 1000$ pF, $C_L = 15$ pF, $I_O = 20$ mA	5, 6, 7	6
Propagation Delay Time to Logic Low Output Level	t_{PHL}		0.2	1.0	µs	$C_O = 1000$ pF, $C_L = 15$ pF, $I_O = 20$ mA	5, 6, 7	7
Propagation Delay Time Skew	$t_{PLH} - t_{PHL}$		0.1		µs	$I_O = 20$ mA		
Output Rise Time (10-90%)	t_r		16		ns	$I_O = 20$ mA, $C_O = 1000$ pF, $C_L = 15$ pF	6, 8	8
Output Fall Time (90-10%)	t_f		23		ns	$I_O = 20$ mA, $C_O = 1000$ pF, $C_L = 15$ pF	6, 8	9
Common Mode Transient Immunity at Logic High Output Level	$\|CM_H\|$	1,000	10,000		V/µs	$V_I = 2$ V, $T_A = 25°C$ $V_{CM} = 50$ V (peak), $V_{CC} = 5$ V I_O (min.) = 12 mA	9, 10	10
Common Mode Transient Immunity at Logic Low Output Level	$\|CM_L\|$	1,000	10,000		V/µs	$V_I = 0.8$ V, $T_A = 25°C$ $V_{CM} = 50$ V (peak), $V_{CC} = 5$ V I_O (max.) = 3 mA	9, 10	11

Package Characteristics

For $0°C \leq T_A \leq 70°C$, unless otherwise specified. All typicals at $T_A = 25°C$.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Notes
Input-Output Momentary Withstand Voltage*	V_{ISO}	2500			V rms	RH ≤ 50%, t = 1 min, $T_A = 25°C$		5, 13
Resistance, Input-Output	R_{I-O}		10^{12}		ohms	$V_{I-O} = 500$ V dc		5
Capacitance, Input-Output	C_{I-O}		1		pF	f = 1 MHz, $V_{I-O} = 0$ V dc		5

*The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the VDE 0884 Insulation Characteristics Table (if applicable), your equipment level safety specification, or HP Application Note 1074, "Optocoupler Input-Output Endurance Voltage."

Notes:

1. Derate linearly above 55°C free air temperature at a rate of 3.8 mW/°C. Proper application of the derating factors will prevent IC junction temperatures from exceeding 125°C for ambient temperatures up to 85°C.
2. Derate linearly above a free-air temperature of 70°C at a rate of 2.3 mW/°C. A significant amount of power may be dissipated in the HCPL-4100 output circuit during the transition from the SPACE state to the MARK state when driving a data line or capacitive load (C_{OUT}). The average power dissipation during the transition can be estimated from the following equation which assumes a linear discharge of a capacitive load: $P = I_{SC} (V_{SO} + V_{MO})/2$, where V_{SO} is the output voltage in the SPACE state. The duration of this transition can be estimated as $t = C_{OUT} (V_{SO} - V_{MO})/I_{SC}$. For typical applications driving twisted pair data lines with NRZ data as shown in Figure 11, the transition time will be less than 10% of one bit time.
3. Derate linearly above 55°C free-air temperature at a rate of 5.1 mW/°C.
4. The maximum current that will flow into the output in the mark state (I_{SC}) is internally limited to protect the device. The duration of the output short circuit shall not exceed 10 ms.
5. The device is considered a two terminal device, pins 1, 2, 3, and 4 are connected together, and pins 5, 6, 7, and 8 are connected together.
6. The t_{PLH} propagation delay is measured from the 1.3 volt level on the leading edge of the input pulse to the 10 mA level on the leading edge of the output pulse.
7. The t_{PHL} propagation delay is measured from the 1.3 volt level on the trailing edge of the input pulse to the 10 mA level on the trailing edge of the output pulse.
8. The rise time, t_r, is measured from the 10% to the 90% level on the rising edge of the output current pulse.
9. The fall time, t_f, is measured from the 90% to the 10% level on the falling edge of the output current pulse.
10. Common mode transient immunity in the logic high level is the maximum (positive) dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, that can be sustained with the output in a Mark ("H") state (i.e., $I_O > 12$ mA).
11. Common mode transient immunity in the logic low level is the maximum (positive) dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, that can be sustained with the output in a Space ("L") state (i.e., $I_O < 3$ mA).
12. Use of a 0.1 µF bypass capacitor connected between pins 5 and 8 is recommended.
13. In accordance with UL 1577, each optocoupler is momentary withstand proof tested by applying an insulation test voltage ≥ 3000 V rms for 1 second (leakage detection current limit, $I_{i-o} \leq 5$ µA).

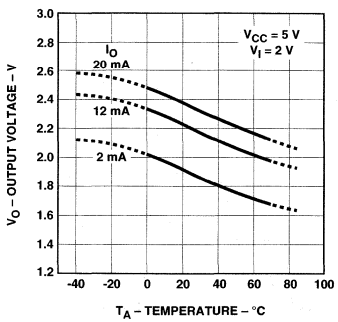


Figure 2. Typical Mark State Output Voltage vs. Temperature.

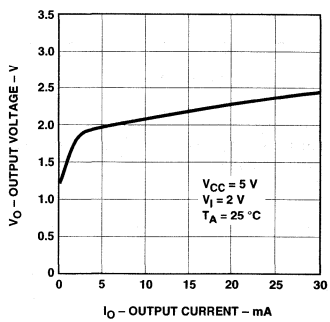


Figure 3. Typical Output Voltage vs. Loop Current.

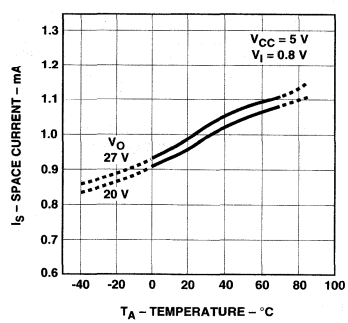


Figure 4. Typical Space State Output Current vs. Temperature.

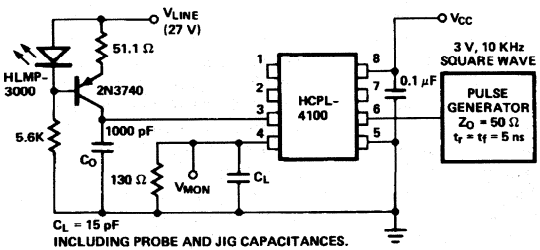


Figure 5. Test Circuit for t_{PLH}, t_{PHL}, t_r, and t_f.

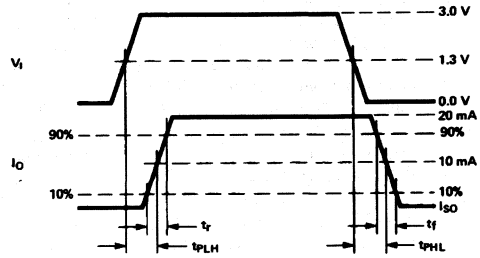


Figure 6. Waveforms for t_{PLH}, t_{PHL}, t_r, and t_f.

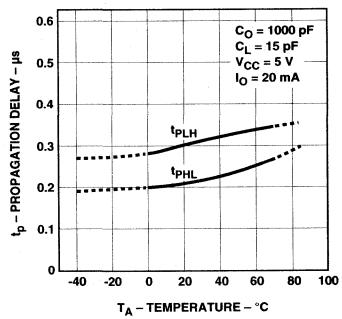


Figure 7. Typical Propagation Delay vs. Temperature.

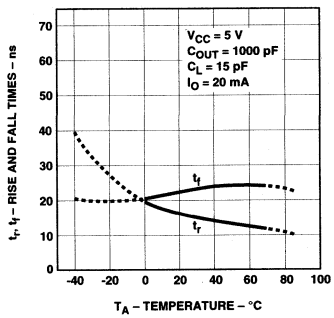


Figure 8. Typical Rise, Fall Times vs. Temperature.

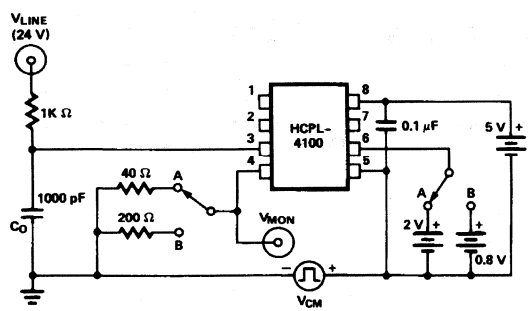


Figure 9. Test Circuit for Common Mode Transient Immunity.

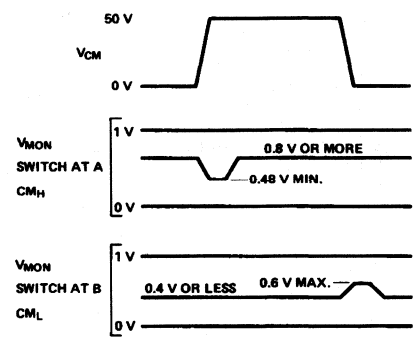


Figure 10. Typical Waveforms for Common Mode Transient Immunity.

Applications

Data transfer between equipment which employs current loop circuits can be accomplished via one of three configurations: simplex, half duplex or full duplex communication. With these configurations, point-to-point and multidrop arrangements are possible. The appropriate configuration to use depends upon data rate, number of stations, number and length of lines, direction of data flow, protocol, current source location and voltage compliance value, etc.

Simplex

The simplex configuration, whether point to point or multidrop, gives unidirectional data flow from transmitter to transmitter(s). This is the simplest configuration for use in long line length (two wire), moderate data rate, and low current source compliance level applications. A block diagram of simplex point to point arrangement is given in Figure 11 for the HCPL-4100 transmitter optocoupler.

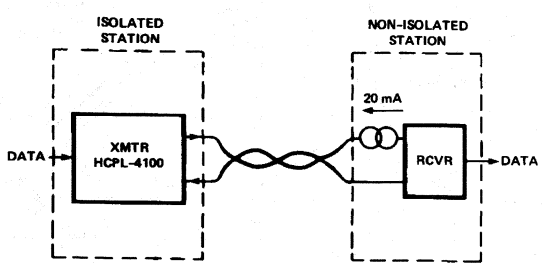


Figure 11. Simplex Point to Point Current Loop System Configuration.

Major factors which limit maximum data rate performance for a simplex loop are the location and compliance voltage of the loop current source as well as the total line capacitance. Application of the HCPL-4100 transmitter in a simplex loop necessitates thtat a non-isolated active receiver (containing current source) be used at the opposite end of the current loop. With long line length, large line capacitance will need to be charged to the compliance voltage level of the current source before the receiver loop current decreases to zero. This effect limits upper data rate performance. Slower data rates will occur with larger compliance voltage levels. The maximum compliance level is determined by the transmitter breakdown characteristic. In addition, adequate compliance of the current source must be available for voltage drops across station(s) during the MARK state in multidrop applications for long line lengths.

In a simplex multidrop application with multiple HCPL-4100 transmitters and one non-isolated active receiver, priority of transmitters must be established.

A recommended non-isolated active receiver circuit which can be used with the HCPL-4100 in point-to-point or in multidrop 20 mA current loop applications is given in Figure 12. This non-isolated active receiver current threshold must be chosen properly in order to provide adequate noise immunity as well as not to detect SPACE state current (bias current) of the HCPL-4100 transmitter. The receiver input threshold current is Vth/Rth ≈ 10 mA. A simple transistor current source provides a nominal 20 mA loop current over a V_{CC} compliance range of 6 V dc to 27 V dc. A resistor can be used in place of the constant current source for simple applications where the wire loop distance and number of stations on the loop are fixed. A minimum transmitter output load capacitance of 1000 pF is required between pins 3 and 4 to ensure absolute stability.

Length of current loop (one direction) versus minimum required DC supply voltage, V_{CC}, of the circuit in Figure 12 is graphically illustrated in Figure 13. Multidrop configurations will require larger V_{CC} than Figure 13 predicts in order to account for additional station terminal voltage drops.

Typical data rate performance versus distance is illustrated in Figure 14 for the combination of a non-isolated active receiver and HCPL-4100 optically coupled current loop transmitter shown in Figure 12. Curves are shown for

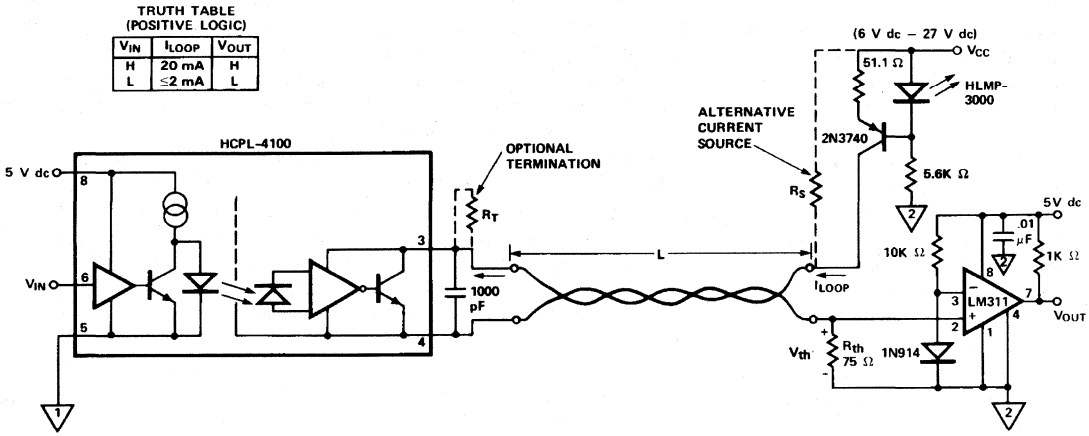


Figure 12. Recommended Non-Isolated Active Receiver with HCPL-4100 Isolated Transmitter for Simplex Point to Point 20 mA Current Loop.

25% distortion data rate at different V_{CC} values. 25% distortion data rate is defined as that rate at which 25% distortion occurs to output bit interval with respect to the input bit interval. Maximum data rate (dotted line) is restricted by device characteristics. An input Non-Return-to-Zero (NRZ) test waveform of 16 bits (0000001011111101) was used for data rate distortion measurements. Enhanced speed performance of the loop system can be obtained with lower V_{CC} supply levels, as illustrated in Figure 14. In addition, when loop current is supplied through a resistor instead of by a current source, an additional series termination resistance equal to the characteristic line impedance can be used at the HCPL-4100 transmitter end to enhance speed of response by approximately 20%.

The cable used contained five pairs of unshielded, twisted, 22 AWG wire (Dearborn #862205). Loop current is 20 mA nominal. Input and output logic supply voltages are 5 V dc.

Full Duplex

The full duplex point-to-point communication of Figure 15 uses a four wire system to provide simultaneous, bidirectional data communication between local and remote equipment. The basic application uses two simplex point-to-point loops which have two separate, active, non-isolated units at one common end of the loops. The other end of each loop is isolated.

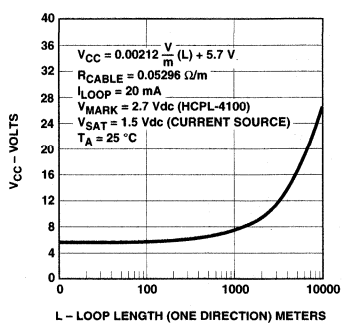


Figure 13. Minimum Required Supply Voltage, V_{CC}, vs. Loop Length for Current Loop Circuit of Figure 13.

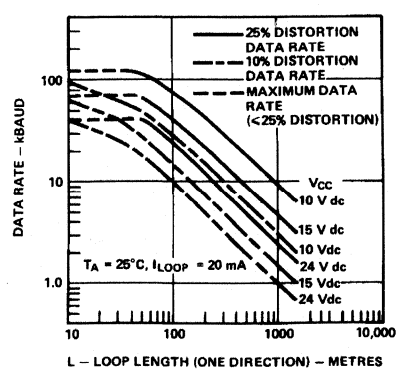


Figure 14. Typical Data Rate vs. Distance and Supply Voltage.

As Figure 15 illustrates, the combination of Hewlett-Packard current loop optocouplers, HCPL-4100 transmitter and HCPL-4200 receiver, can be used at the isolated end of current loops. Cross talk and common mode coupling are greatly reduced when optical isolation is implemented at the same end of both loops, as shown. Full duplex data rate is limited by the non-isolated active transmitter current loop. Comments mentioned under simplex configuration apply to the full duplex case. Consult the HCPL-4200 receiver optocoupler data sheet for specified device performance.

Half Duplex

The half duplex configuration, whether point to point or multi-drop, gives non-simultaneous bidirectional data flow from transmitters to transmitters shown in Figures 16a and 16b. This configuration allows the use of two wires to carry data back and forth between local and remote units. However, protocol must be used to determine which specific transmitter can operate at any given time. Maximum data rate for a half duplex system is limited by the loop current charging time. These considerations were explained in the Simplex configuration section.

Figures 16a and 16b illustrate half duplex application for the combination of HCPL-4100/-4200 optocouplers. The unique and complementary designs of the HCPL-4100 transmitter and HCPL-4200 receiver optocouplers provide many designed-in benefits. For example, total optical isolation at one end of the current loop is easily accomplished, which results in substantial removal of common mode influences, elimination of ground potential differences and reduction of power supply requirements. With this combination of IICPL-4100/-4200 optocouplers, specific current loop noise immunity is provided, i.e., minimum SPACE state current noise immunity is 1 mA, MARK state noise immunity is 8 mA.

Voltage compliance of the current source must be of an adequate level for operating all units in the loop while not exceeding 27 V dc, the maximum breakdown voltage for the HCPL-4100. Note that the HCPL-4100 transmitter will allow output loop current to conduct when input V_{CC} power is off. Consult the HCPL-4200 receiver optocoupler data sheet for specified device performance.

For more information about the HCPL-4100/-4200 optocouplers, consult Application Note 1018.

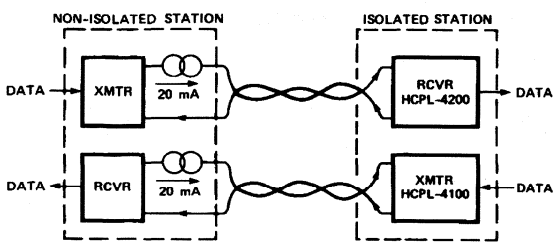
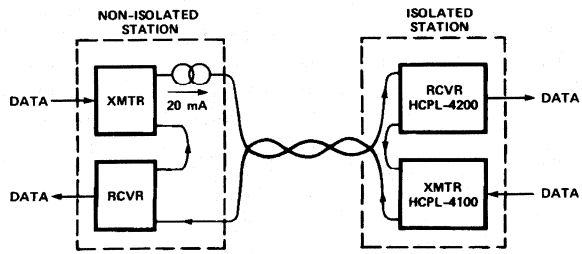
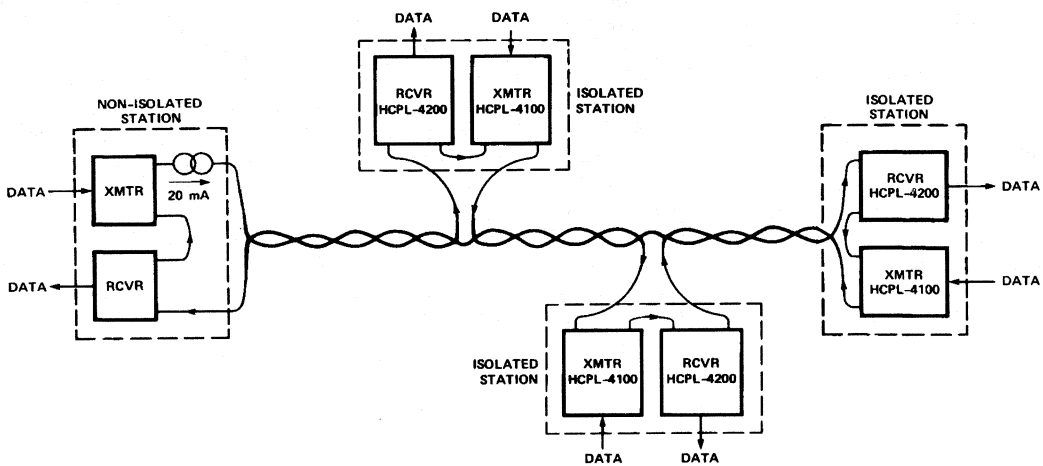


Figure 15. Full Duplex Point to Point Current Loop System Configuration.



(a) POINT TO POINT



(b) MULTIDROP

Figure 16. Half Duplex Current Loop System Configurations for (a) Point to Point, (b) Multidrop.

Optically Coupled 20 mA Current Loop Receiver

Technical Data

HCPL-4200

Features

- **Data Output Compatible with LSTTL, TTL and CMOS**
- **20 K Baud Data Rate at 1400 Metres Line Length**
- **Guaranteed Performance over Temperature (0°C to 70°C)**
- **Guaranteed On and Off Thresholds**
- **LED is Protected from Excess Current**
- **Input Threshold Hysteresis**
- **Three-State Output Compatible with Data Buses**
- **Internal Shield for High Common Mode Rejection**
- **Safety Approval**
  UL Recognized -2500 V rms, for 1 Minute
  CSA Approved
- **Optically Coupled 20 mA Current Loop Transmitter, HCPL-4100, Also Available**

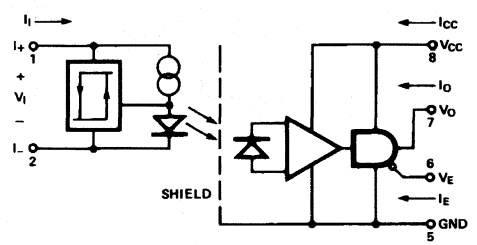
Applications

- **Isolated 20 mA Current**
- **Loop Receiver in:**
  Computer Peripherals
  Industrial Control Equipment
  Data Communications Equipment

Description

The HCPL-4200 optocoupler is designed to operate as a receiver in equipment using the 20 mA Current Loop. 20 mA current loop systems conventionally signal a logic high state by transmitting 20 mA of loop current (MARK), and signal a logic low state by allowing no more than a few milliamperes of loop current (SPACE). Optical coupling of the signal from the 20 mA current loop to the logic output breaks ground loops and provides for a very high common mode rejection. The HCPL-4200 aids in the design process by providing guaranteed thresholds for logic high state and logic low state for the current loop, providing an LSTTL, TTL, or CMOS compatible logic interface, and providing guaranteed common mode rejection. The buffer circuit on the current loop side of the HCPL-4200 provides typically 0.8 mA of hysteresis which increases the immunity to common mode and differential mode noise. The buffer also provides a controlled amount of LED drive current which takes into account any LED light output degradation. The internal shield allows a guaranteed 1000 V/µs common mode transient immunity.

Functional Diagram



TRUTH TABLE (POSITIVE LOGIC)*

I_I	V_E	V_O
H	H	Z
L	H	Z
H	L	H
L	L	L

*CURRENT LOOP CONVENTION —
H = MARK: $I_I \geq 12$ mA.
L = SPACE: $I_I \leq 3$ mA.
Z = OFF (HIGH IMPEDANCE) STATE.

A 0.1 µF bypass capacitor connected between pins 8 and 5 is recommended.

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Ordering Information

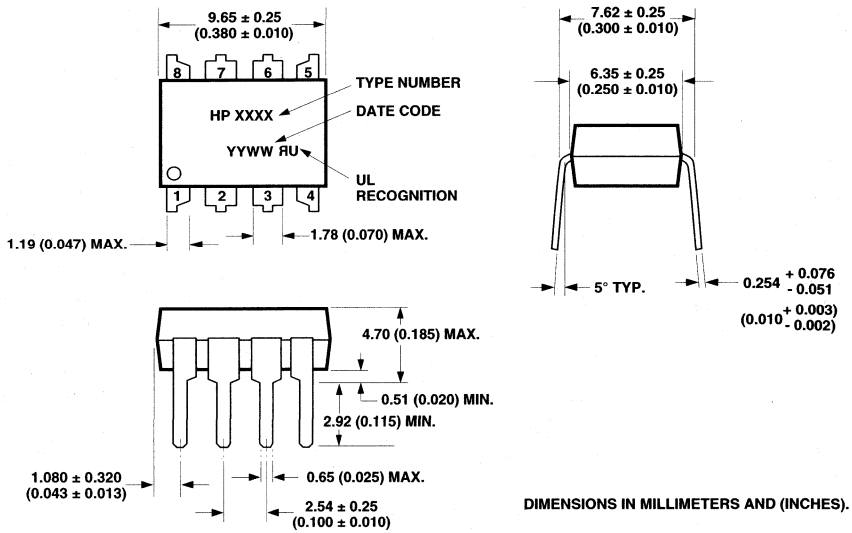
Specify part number followed by Option Number (if desired).

HCPL-4200# XXX

- 300 = Gull Wing Surface Mount Lead Option
- 500 = Tape/Reel Package Option (1 K min)

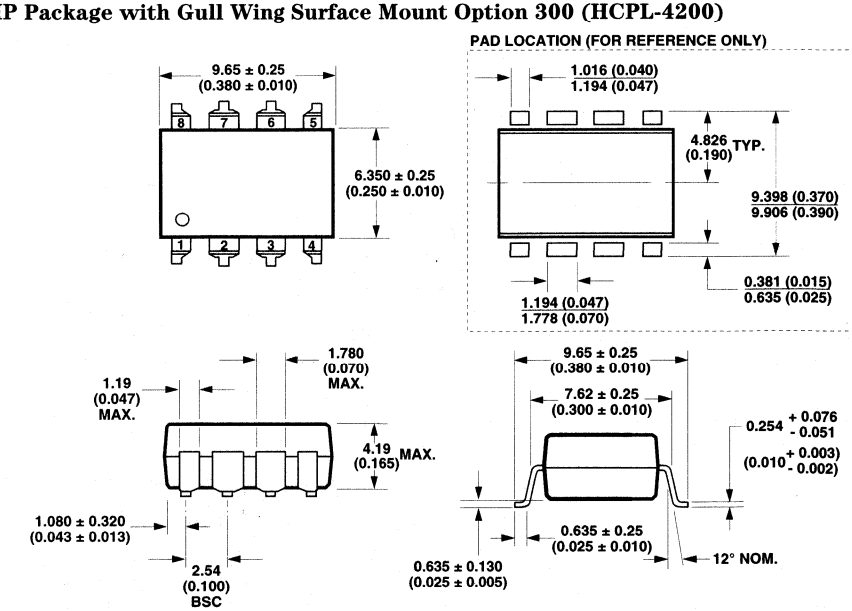
Option data sheets available. Contact your Hewlett-Packard sales representative or authorized distributor for information.

Package Outline Drawings – 8 Pin DIP Package (HCPL-4200)



DIMENSIONS IN MILLIMETERS AND (INCHES).

8 Pin DIP Package with Gull Wing Surface Mount Option 300 (HCPL-4200)



DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES).

Thermal Profile (Option #300)

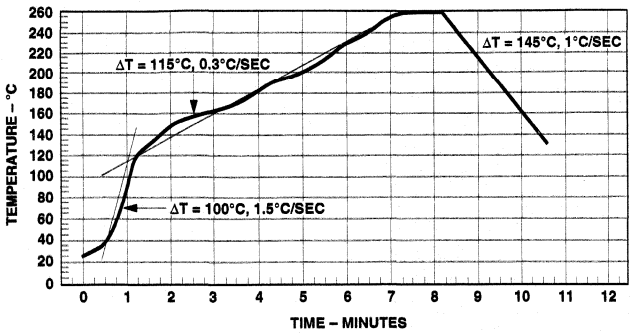


Figure 1. Maximum Solder Reflow Thermal Profile.
(Note: Use of non-chlorine activated fluxes is recommended.)

Regulatory Information

The HCPL-4200 has been approved by the following organizations:

UL

Recognized under UL 1577, Component Recognition Program, File E55361.

CSA

Approved under CSA Component Acceptance Notice #5, File CA 88324.

Insulation and Safety Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min. External Air Gap (External Clearance)	L(IO1)	7.1	mm	Measured from input terminals to output terminals, shortest distance through air
Min. External Tracking Path (External Creepage)	L(IO2)	7.4	mm	Measured from input terminals to output terminals, shortest distance path along body
Min. Internal Plastic Gap (Internal Clearance)		0.08	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity
Tracking Resistance (Comparative Tracking Index)	CTI	200	volts	DIN IEC 112/VDE 0303 PART 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Option 300 – surface mount classification is Class A in accordance with CECC 00802.

Absolute Maximum Ratings

(No Derating Required up to 70°C)

Storage Temperature ..... -55°C to +125°C
Operating Temperature ..... -40°C to +85°C
Lead Solder Temperature .... 260°C for 10 s (1.6 mm below seating plane)
Supply Voltage – V_{CC} ..... 0 V to 20 V
Average Input Current - I_I ..... -30 mA to 30 mA
Peak Transient Input Current - I_I ..... 0.5 A[1]
Enable Input Voltage – V_E ..... -0.5 V to 20 V
Output Voltage – V_O ..... -0.5 V to 20 V
Average Output Current – I_O ..... 25 mA
Input Power Dissipation – P_I ..... 90 mW[2]
Output Power Dissipation – P_O ..... 210 mW[3]
Total Power Dissipation – P ..... 255 mW[4]
Infrared and Vapor Phase Reflow Temperature
(Option #300) ..... see Fig. 1, Thermal Profile

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage	V_{CC}	4.5	20	Volts
Forward Input Current (SPACE)	I_{SI}	0	2.0	mA
Forward Input Current (MARK)	I_{MI}	14	24	mA
Operating Temperature	T_A	0	70	°C
Fan Out	N	0	4	TTL Loads
Logic Low Enable Voltage	V_{EL}	0	0.8	Volts
Logic High Enable Voltage	V_{EH}	2.0	20	Volts

DC Electrical Specifications

For 0°C ≤ T_A ≤ 70°C, 4.5 V ≤ V_{CC} ≤ 20 V, V_E = 0.8 V, all typicals at T_A = 25°C and V_{CC} = 5 V unless otherwise noted. See note 13.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Mark State Input Current	I_{MI}	12			mA		2, 3, 4	
Mark State Input Voltage	V_{MI}		2.52	2.75	Volts	I_I = 20 mA V_E = Don't Care	4, 5	
Space State Input Current	I_{SI}			3	mA		2, 3, 4	
Space State Input Voltage	V_{SI}		1.6	2.2	Volts	I_I = 0.5 to 2.0 mA V_E = Don't Care	2, 4	
Input Hysteresis Current	I_{HYS}	0.3	0.8		mA		2	
Logic Low Output Voltage	V_{OL}			0.5	Volts	I_{OL} = 6.4 mA I_I = 3 mA (4 TTL Loads)	6	
Logic High Output Voltage	V_{OH}	2.4			Volts	I_{OH} = -2.6 mA, I_I = 12 mA	7	
Output Leakage Current (V_{OUT} > V_{CC})	I_{OHH}			100	µA	V_O = 5.5 V I_I = 20 mA V_{CC} = 4.5 V		
				500	µA	V_O = 20 V		
Logic High Enable Voltage	V_{EH}	2.0			Volts			
Logic Low Enable Voltage	V_{EL}			0.8	Volts			
Logic High Enable Current	I_{EH}			20	µA	V_E = 2.7 V		
				100	µA	V_E = 5.5 V		
			0.004	250	µA	V_E = 20 V		
Logic Low Enable Current	I_{EL}			-0.32	mA	V_E = 0.4 V		
Logic Low Supply Current	I_{CCL}		4.5	6.0	mA	V_{CC} = 5.5 V I_I = 0 mA V_E = Don't Care		
			5.25	7.5	mA	V_{CC} = 20 V		
Logic High Supply Current	I_{CCH}		2.7	4.5	mA	V_{CC} = 5.5 V I_I = 20 mA V_E = Don't Care		
			3.1	6.0	mA	V_{CC} = 20 V		
High Impedance State Output Current	I_{OZL}			-20	µA	V_O = 0.4 V V_E = 2 V, I_I = 20 mA		
	I_{OZH}			20	µA	V_O = 2.4 V		
				100	µA	V_O = 5.5 V		
				500	µA	V_O = 20 V		
Logic Low Short Circuit Output Current	I_{OSL}	25			mA	V_O = V_{CC} = 5.5 V I_I = 0 mA		5
		40			mA	V_O = V_{CC} = 20 V		
Logic High Short Circuit Output Current	I_{OSH}	-10			mA	V_{CC} = 5.5 V I_I = 20 mA V_O = GND		5
		-25			mA	V_{CC} = 20 V		
Input Capacitance	C_{IN}		120		pF	f = 1 MHz, V_I = 0 V dc, Pins 1 and 2		

Switching Specifications

For $0°C \leq T_A \leq 70°C$, $4.5\ V \leq V_{CC} \leq 20\ V$, $V_E = 0.8\ V$, all typicals at $T_A = 25°C$ and $V_{CC} = 5\ V$ unless otherwise noted. See note 13.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to Logic High Output Level	t_{PLH}		0.23	1.6	µs	$V_E = 0\ V$, $C_L = 15\ pF$	8, 9, 10	7
Propagation Delay Time to Logic Low Output Level	t_{PHL}		0.17	1.0	µs	$V_E = 0\ V$, $C_L = 15\ pF$	8, 9, 10	8
Propagation Delay Time Skew	$t_{PLH} - t_{PHL}$		60		ns	$I_I = 20\ mA$, $C_L = 15\ pF$	8, 9, 10	
Output Enable Time to Logic Low Level	t_{PZL}		25		ns	$I_I = 0\ mA$, $C_L = 15\ pF$	12, 13, 15	
Output Enable Time to Logic High Level	t_{PZH}		28		ns	$I_I = 20\ mA$, $C_L = 15\ pF$	12, 13, 14	
Output Disable Time to Logic Low Level	t_{PLZ}		60		ns	$I_I = 0\ mA$, $C_L = 15\ pF$	12, 13, 15	
Output Disable Time to Logic High Level	t_{PHZ}		105		ns	$I_I = 20\ mA$, $C_L = 15\ pF$	12, 13, 14	
Output Rise Time (10-90%)	t_r		55		ns	$V_{CC} = 5\ V$, $C_L = 15\ pF$	8, 9, 11	9
Output Fall Time (90-10%)	t_f		15		ns	$V_{CC} = 5\ V$, $C_L = 15\ pF$	8, 9, 11	10
Common Mode Transient Immunity at Logic High Output Level	$\|CM_H\|$	1,000	10,000		V/µs	$V_{CM} = 50\ V$ (peak) $I_I = 12\ mA$, $T_A = 25°C$	16	11
Common Mode Transient Immunity at Logic Low Output Level	$\|CM_L\|$	1,000	10,000		V/µs	$V_{CM} = 50\ V$ (peak) $I_I = 3\ mA$, $T_A = 25°C$	16	12

Package Characteristics

For $0°C \leq T_A \leq 70°C$, unless otherwise specified. All typicals at $T_A = 25°C$.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Notes
Input-Output Momentary Withstand Voltage*	V_{ISO}	2500			V rms	RH ≤ 50%, t = 1 min, $T_A = 25°C$		6, 14
Resistance, Input-Output	R_{I-O}		10^{12}		ohms	$V_{I-O} = 500\ V$ dc		6
Capacitance, Input-Output	C_{I-O}		1.0		pF	f = 1 MHz, $V_{I-O} = 0\ V$		6

*The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the VDE 0884 Insulation Characteristics Table (if applicable), your equipment level safety specification, or HP Application Note 1074, "Optocoupler Input-Output Endurance Voltage."

Notes:

1. ≤ 1 μs pulse width, 300 pps.
2. Derate linearly above 70°C free air temperature at a rate of 1.6 mW/°C. Proper application of the derating factors will prevent IC junction temperatures from exceeding 125°C for ambient temperatures up to 85°C.
3. Derate linearly above 70°C free air temperature at a rate of 3.8 mW/°C.
4. Derate linearly above 70°C free air temperature at a rate of 4.6 mW/°C.
5. Duration of output short circuit time shall not exceed 10 ms.
6. The device is considered a two terminal device, pins 1, 2, 3, and 4 are connected together and pins 5, 6, 7, and 8 are connected together.
7. The t_{PLH} propagation delay is measured from the 10 mA level on the leading edge of the input pulse to the 1.3 V level on the leading edge of the output pulse.
8. The t_{PHL} propagation delay is measured from the 10 mA level on the trailing edge of the input pulse to the 1.3 V level on the trailing edge of the output pulse.
9. The rise time, t_r, is measured from the 10% to the 90% level on the rising edge of the output logic pulse.
10. The fall time, t_f, is measured from the 90% to the 10% level on the falling edge of the output logic pulse.
11. Common mode transient immunity in the logic high level is the maximum (negative) dV_{CM}/dt on the trailing edge of the common mode pulse, V_{CM}, which can be sustained with the output voltage in the logic high state (i.e., $V_O \geq 2$ V).
12. Common mode transient immunity in the logic low level is the maximum (positive) dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, which can be sustained with the output voltage in the logic low state (i.e., $V_O \leq 0.8$ V).
13. Use of a 0.1 μF bypass capacitor connected between pins 5 and 8 is recommended.
14. In accordance with UL 1577, each optocoupler momentary withstand is proof tested by applying an insulation test voltage ≥ 3000 V rms for 1 second (leakage detection current limit, $I_{i-o} \leq 5$ μA).

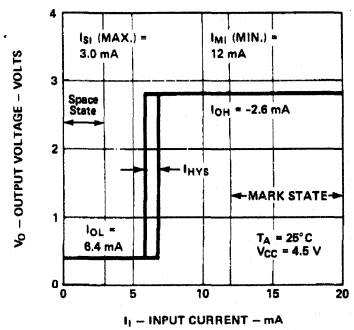


Figure 2. Typical Output Voltage vs. Loop Current.

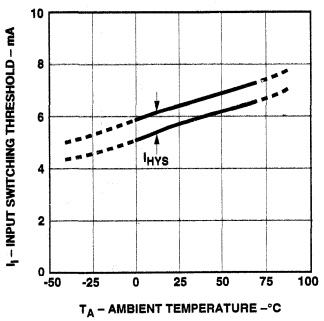


Figure 3. Typical Current Switching Threshold vs. Temperature.

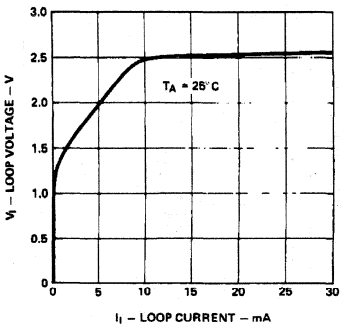


Figure 4. Typical Input Loop Voltage vs. Input Current.

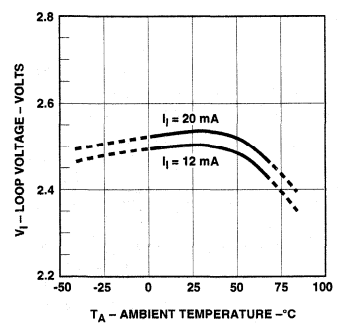


Figure 5. Typical Input Voltage vs. Temperature.

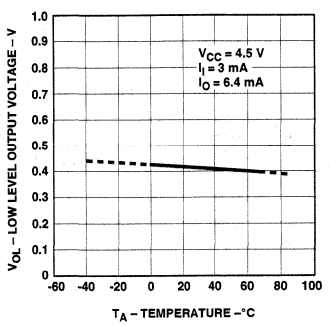


Figure 6. Typical Logic Low Output Voltage vs. Temperature.

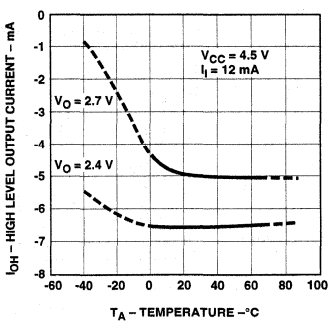


Figure 7. Typical Logic High Output Current vs. Temperature.

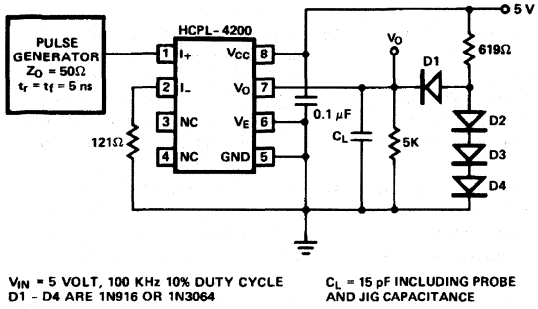


Figure 8. Test Circuit for t_{PHL}, t_{PLH}, t_r, and t_f.

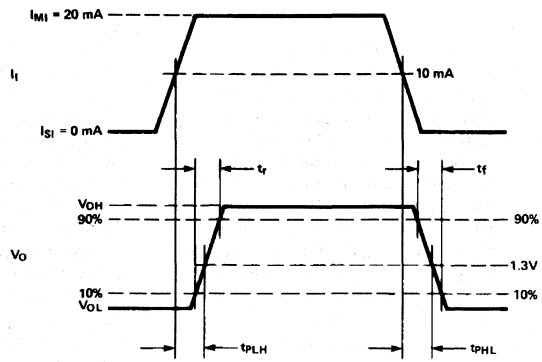


Figure 9. Waveforms for t_{PHL}, t_{PLH}, t_r, and t_f.

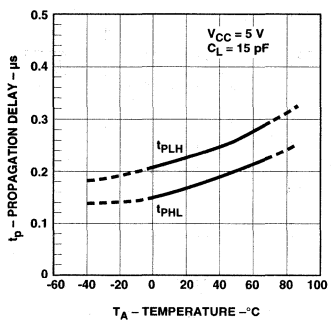


Figure 10. Typical Propagation Delay vs. Temperature.

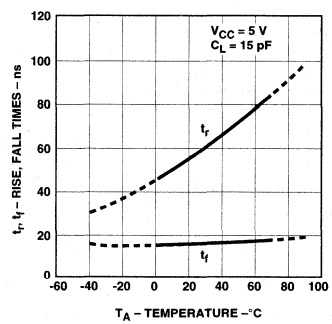


Figure 11. Typical Rise, Fall Time vs. Temperature.

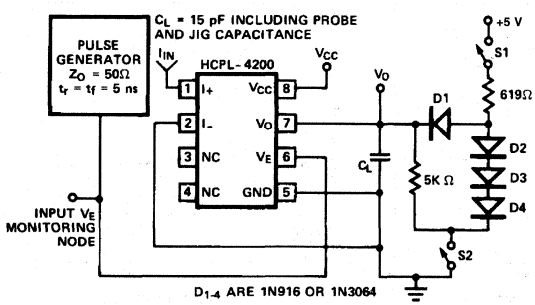


Figure 12. Test Circuit for t_{PZH}, t_{PZL}, t_{PHZ}, and t_{PLZ}.

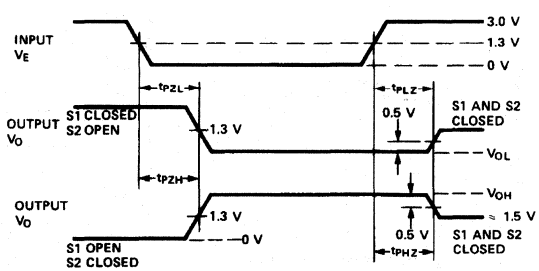


Figure 13. Waveforms for t_{PZH}, t_{PZL}, t_{PHZ}, and t_{PLZ}.

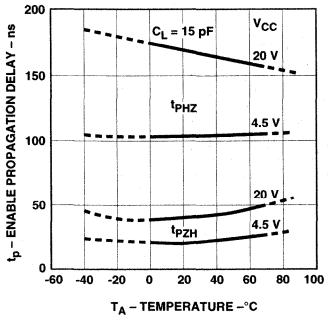


Figure 14. Typical Logic High Enable Propagation Delay vs. Temperature.

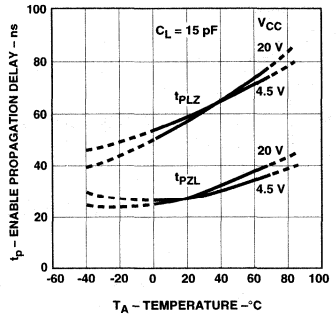


Figure 15. Typical Logic Low Enable Propagation Delay vs. Temperature.

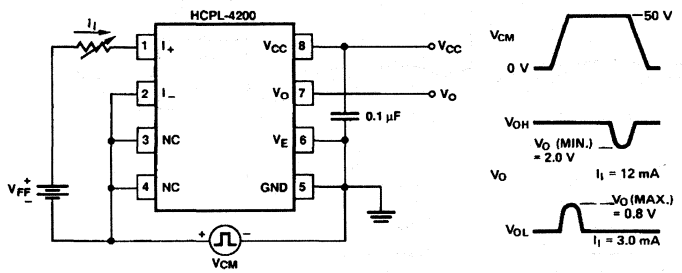


Figure 16. Test Circuit for Common Mode Transient Immunity.

Applications

Data transfer between equipment which employs current loop circuits can be accomplished via one of three configurations: simplex, half duplex or full duplex communication. With these configurations, point-to-point and multidrop arrangements are possible. The appropriate configuration to use depends upon data rate, number of stations, number and length of lines, direction of data flow, protocol, current source location and voltage compliance value, etc.

Simplex

The simplex configuration, whether point to point or multi-drop, gives unidirectional data flow from transmitter to receiver(s). This is the simplest configuration for use in long line length (two wire), for high data rate, and low current source compliance level applications. Block diagrams of simplex point-to-point and multidrop arrangements are given in Figures 17a and 17b respectively for the HCPL-4200 receiver optocoupler.

For the highest data rate performance in a current loop, the configuration of a non-isolated active transmitter (containing current source) transmitting data to a remote isolated receiver(s) should be used. When the current source is located at the transmitter end, the loop is charged approximately to V_{MI} (2.5 V). Alternatively, when the current source is located at the receiver end, the loop is charged to the full compliance voltage level. The lower the charged voltage level the faster the data rate will be. In the configurations of Figures 17a and 17b, data rate is independent of the current source voltage compliance level. An adequate compliance level of current source must be available for voltage drops across station(s) during the MARK state in multi-drop applications or for long line length. The maximum compliance level is determined by the transmitter breakdown characteristic.

A recommended non-isolated active transmitter circuit which can be used with the HCPL-4200 in point-to-point or in multidrop 20 mA current loop applications is given in Figure 18. The current source is controlled via a standard TTL 7407 buffer to provide high output impedance of current source in both the ON

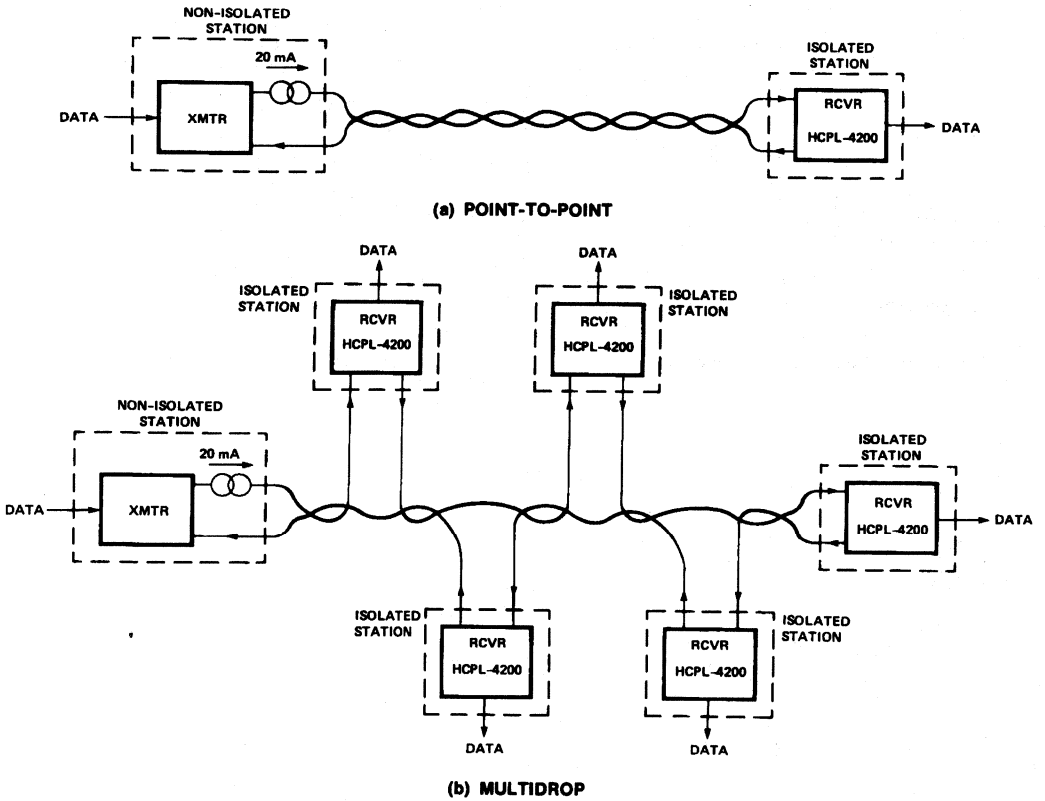


Figure 17. Simplex Current Loop System Configurations for (a) Point-to-Point, (b) Multidrop.

and OFF states. This non-isolated active transmitter provides a nominal 20 mA loop current for the listed values of V_{CC}, R2 and R3 in Figure 18.

Length of current loop (one direction) versus minimum required DC supply voltage, V_{CC}, of the circuit in Figure 18 is graphically illustrated in Figure 19. Multidrop configurations will require larger V_{CC} than Figure 19 predicts in order to account for additional station terminal voltage drops.

Typical data rate performance versus distance is illustrated in Figure 20 for the combination of a non-isolated active transmitter and HCPL-4200 optically coupled current loop receiver shown in Figure 18. Curves are shown for 10% and 25% distortion data rate. 10% (25%) distortion data rate is defined as that rate at which 10% (25%) distortion occurs to output bit interval with respect to input bit interval. An input Non-Return-to-Zero (NRZ) test waveform of 16 bits (0000001011111101) was used for data rate distortion measurements. Data rate is independent of current source supply voltage, V_{CC}.

The cable used contained five pairs of unshielded, twisted, 22 AWG wire (Dearborn #862205). Loop current is 20 mA nominal. Input and output logic supply voltages are 5 V dc.

Full Duplex

The full duplex point-to-point communication of Figure 21 uses a four wire system to provide simultaneous, bidirectional data communication between local and remote equipment. The basic application uses two simplex point-to-point loops which have two separate, active, non-isolated units at one common end of the loops. The other end of each loop is isolated.

As Figure 21 illustrates, the combination of Hewlett-Packard current loop optocouplers, HCPL-4100 transmitter and HCPL-4200

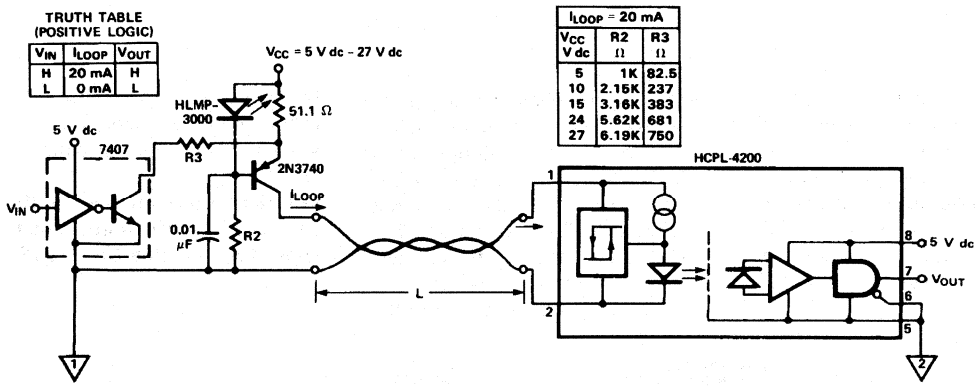


Figure 18. Recommended Non-Isolated Active Transmitter with HCPL-4200 Isolated Receiver for Simplex Point-to-Point 20 mA Current Loop.

receiver, can be used at the isolated end of current loops. Cross talk and common mode coupling are greatly reduced when optical isolation is implemented at the same end of both loops, as shown. The full duplex data rate is limited by the non-isolated active receiver current loop. Comments mentioned under simplex configuration apply to the full duplex case. Consult the HCPL-4100 transmitter optocoupler data sheet for specified device performance.

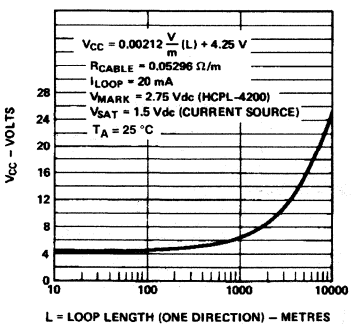


Figure 19. Minimum Required Supply Voltage, V_{CC}, vs. Loop Length for Current Loop Circuit of Figure 19.

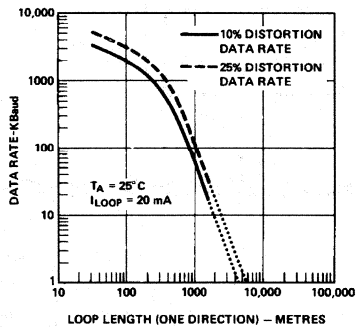


Figure 20. Typical Data Rate vs. Distance.

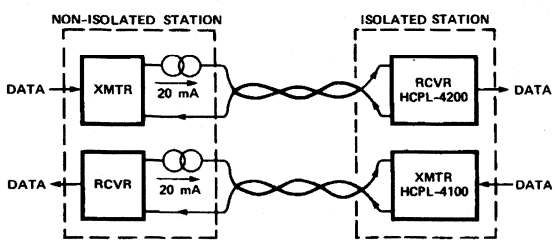


Figure 21. Full Duplex Point-to-Point Current Loop System Configuration.

Half Duplex

The half duplex configuration, whether point-to-point or multidrop, gives non-simultaneous bidirectional data flow from transmitters to receivers shown in Figures 22a and 22b. This configuration allows the use of two wires to carry data back and forth between local and remote units. However, protocol must be used to determine which specific transmitter can operate at any given time. Maximum data rate for a half duplex system is limited by the loop current charging time. These considerations were explained in the Simplex configuration section.

Figures 22a and 22b illustrate half duplex application for the combination of HCPL-4100/-4200 optocouplers. The unique and complementary designs of the HCPL-4100 transmitter and HCPL-4200 receiver optocouplers provide many designed-in benefits. For example, total optical isolation at one end of the current loop is easily accomplished, which results in substantial removal of common mode influences, elimination of ground potential

differences and reduction of power supply requirements. With this combination of HCPL-4100/ -4200 optocouplers, specific current loop noise immunity is provided, i.e., minimum SPACE state current noise immunity is 1 mA, MARK state noise immunity is 8 mA.

Voltage compliance of the current source must be of an adequate level for operating all units in the loop while not exceeding 27 V dc, the maximum breakdown voltage for the HCPL-4100. Note that the HCPL-4100 transmitter will allow loop current to conduct when input V_{CC} power is off. Consult the HCPL-4100 transmitter optocoupler data sheet for specified device performance.

For more information about the HCPL-4100/-4200 optocouplers, consult Application Note 1018.

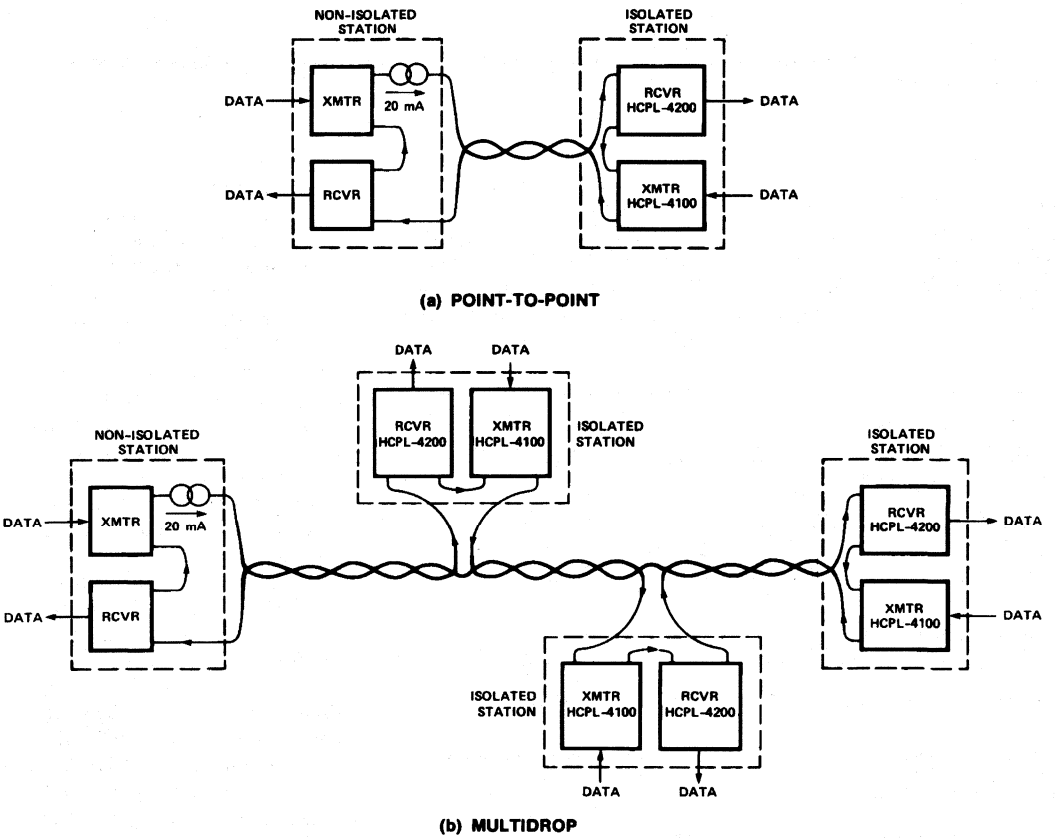


Figure 22. Half Duplex Current Loop System Configurations for (a) Point-to-Point, (b) Multidrop.

High Bandwidth, Analog/Video Optocouplers

Technical Data

HCPL-4562
HCNW4562

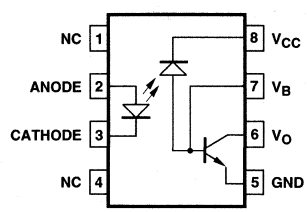
Features

- **Wide Bandwidth[1]:**
  17 MHz (HCPL-4562)
  9 MHz (HCNW4562)
- **High Voltage Gain[1]:**
  2.0 (HCPL-4562)
  3.0 (HCNW4562)
- **Low G_V Temperature Coefficient: -0.3%/°C**
- **Highly Linear at Low Drive Currents**
- **High-Speed AlGaAs Emitter**
- **Safety Approval**
  UL Recognized - 2500 V rms for 1 minute (5000 V rms for 1 minute for HCPL-4562#020 and HCNW4562) per UL 1577
  CSA Approved
  VDE 0884 Approved
  $-V_{IORM}$ = 1414 V peak for HCNW4562
  BSI Certified (HCNW4562)
- **Available in 8-Pin DIP and Widebody Packages**

Applications

- **Video Isolation for the Following Standards/ Formats: NTSC, PAL, SECAM, S-VHS, ANALOG RGB**
- **Low Drive Current Feedback Element in Switching Power Supplies, e.g., for ISDN Networks**
- **A/D Converter Signal Isolation**
- **Analog Signal Ground Isolation**
- **High Voltage Insulation**

Functional Diagram



Description

The HCPL-4562 and HCNW4562 optocouplers provide wide bandwidth isolation for analog signals. They are ideal for video isolation when combined with their application circuit (Figure 4). High linearity and low phase shift are achieved through an AlGaAs LED combined with a high speed detector. These single channel optocouplers are available in 8-Pin DIP and Widebody package configurations.

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Selection Guide

Single Channel Packages	
8-Pin DIP (300 Mil)	**Widebody (400 Mil)**
HCPL-4562	HCNW4562

Ordering Information

Specify Part Number followed by Option Number (if desired).

Example:

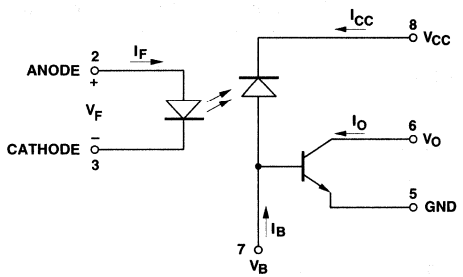
HCPL-4562#XXX

- 020 = UL 5000 V rms/1 Minute Option*
- 300 = Gull Wing Surface Mount Option†
- 500 = Tape and Reel Packaging Option

Option data sheets are available. Contact your Hewlett-Packard sales representative or authorized distributor for information.

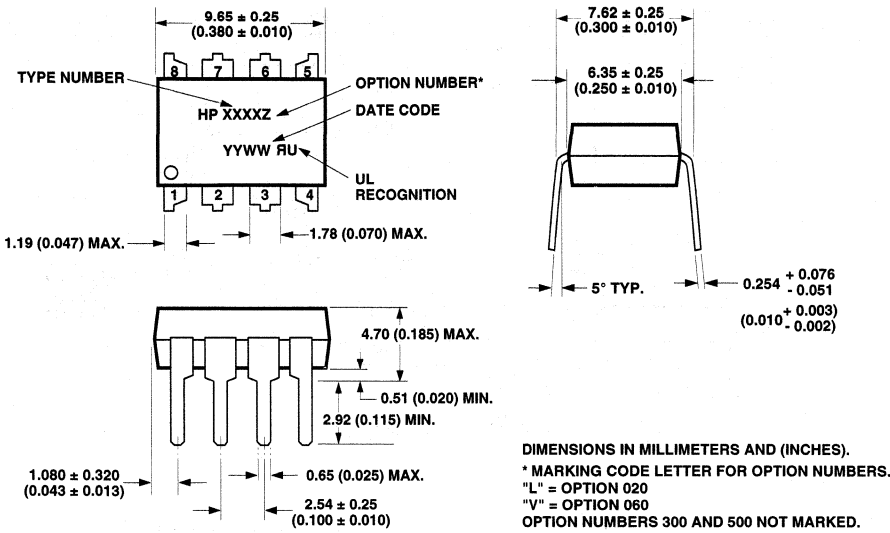
*For HCPL-4562 only.
†Gull wing surface mount option applies to through hole parts only.

Schematic



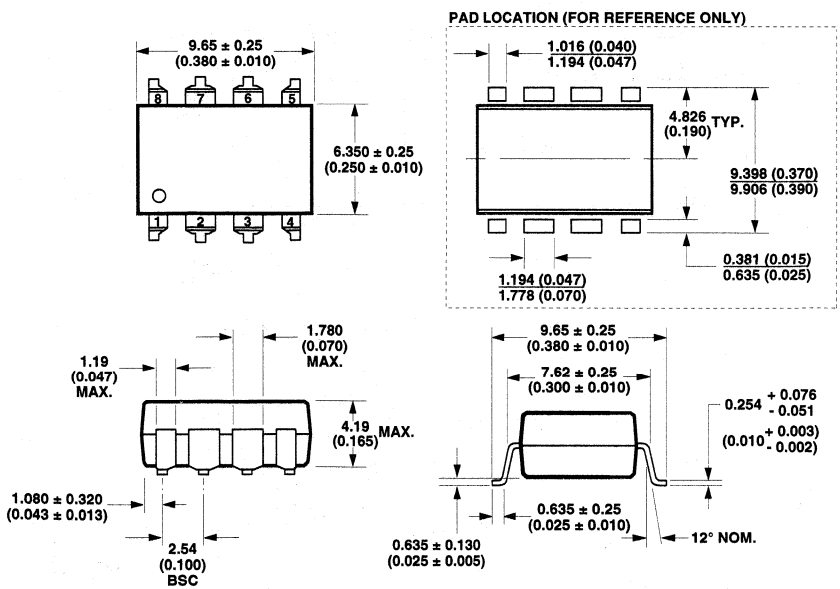
Package Outline Drawings

8-Pin DIP Package (HCPL-4562)



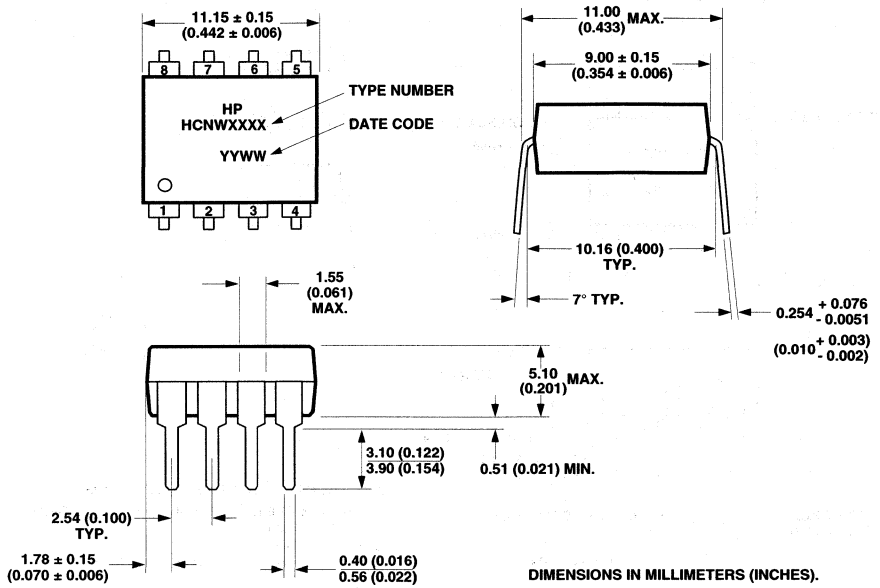
DIMENSIONS IN MILLIMETERS AND (INCHES).
* MARKING CODE LETTER FOR OPTION NUMBERS.
"L" = OPTION 020
"V" = OPTION 060
OPTION NUMBERS 300 AND 500 NOT MARKED.

8-Pin DIP Package with Gull Wing Surface Mount Option 300 (HCPL-4562)

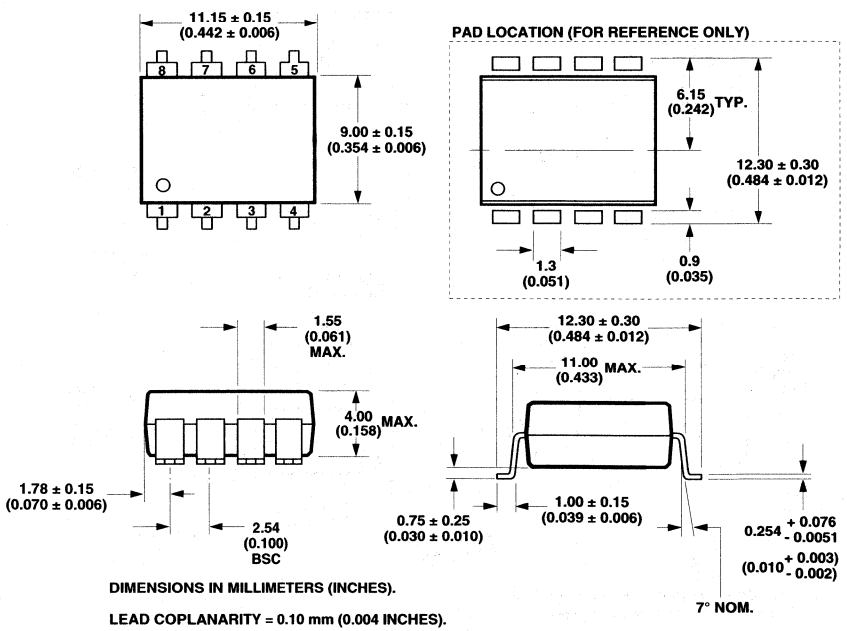


DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES).

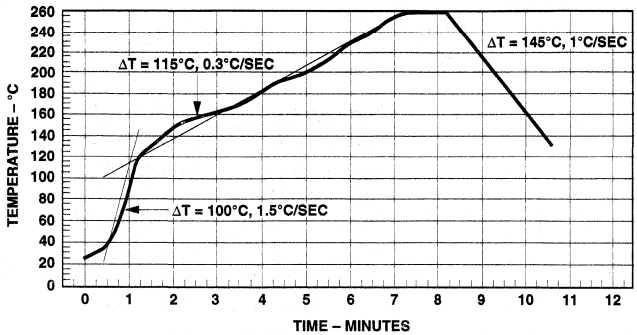
8-Pin Widebody DIP Package (HCNW4562)



8-Pin Widebody DIP Package with Gull Wing Surface Mount Option 300 (HCNW4562)



Solder Reflow Temperature Profile (Gull Wing Surface Mount Option Parts)



Note: Use of nonchlorine activated fluxes is highly recommended.

Regulatory Information

The devices contained in this data sheet have been approved by the following organizations:

UL

Recognized under UL 1577, Component Recognition Program, File E55361.

CSA

Approved under CSA Component Acceptance Notice #5, File CA 88324.

VDE

Approved according to VDE 0884/06.92 (HCNW4562 only).

BSI

Certification according to BS415:1994 (BS EN60065:1994); BS EN60950:1992 (BS7002:1992) and EN41003:1993 for Class II applications (HCNW4562 only).

Insulation and Safety Related Specifications

Parameter	Symbol	8-Pin DIP (300 Mil) Value	Widebody (400 Mil) Value	Units	Conditions
Minimum External Air Gap (External Clearance)	L(101)	7.1	9.6	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L(102)	7.4	10.0	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	1.0	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photo-emitter and photodetector inside the optocoupler cavity.
Minimum Internal Tracking (Internal Creepage)		NA	4.0	mm	Measured from input terminals to output terminals, along internal cavity.
Tracking Resistance (Comparative Tracking Index)	CTI	200	200	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa	IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Option 300 - surface mount classification is Class A in accordance with CECC 00802.

VDE 0884 Insulation Related Characteristics (HCNW4562 ONLY)

Description	Symbol	Characteristic	Units
Installation classification per DIN VDE 0110/1.89, Table 1 for rated mains voltage ≤ 600 V rms		I-IV	
for rated mains voltage ≤ 1000 V rms		I-III	
Climatic Classification		55/85/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	1414	V peak
Input to Output Test Voltage, Method b* V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial Discharge < 5 pC	V_{PR}	2652	V peak
Input to Output Test Voltage, Method a* V_{IORM} x 1.5 = V_{PR}, Type and sample test, t_m = 60 sec, Partial Discharge < 5 pC	V_{PR}	2121	V peak
Highest Allowable Overvoltage* (Transient Overvoltage, t_{ini} = 10 sec)	V_{IOTM}	8000	V peak
Safety Limiting Values (Maximum values allowed in the event of a failure, also see Figure 17, Thermal Derating curve.)			
Case Temperature	T_S	150	°C
Input Current	$I_{S,INPUT}$	400	mA
Output Power	$P_{S,OUTPUT}$	700	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	≥ 10^9	Ω

*Refer to the front of the optocoupler section of the current catalog, under Product Safety Regulations section (VDE 0884), for a detailed description.

Note: Isolation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuits in application.

Absolute Maximum Ratings

Parameter	Symbol	Device	Min.	Max.	Units	Note
Storage Temperature	T_S		-55	125	°C	
Operating Temperature	T_A		-40	85	°C	
Average Forward Input Current	$I_{F(avg)}$	HCPL-4562		12	mA	
		HCNW4562		25		
Peak Forward Input Current	$I_{F(PEAK)}$	HCPL-4562		18.6	mA	
		HCNW4562		40		
Effective Input Current	$I_{F(EFF)}$	HCPL-4562		12.9	mA rms	
Reverse LED Input Voltage (Pin 3-2)	V_R	HCPL-4562		1.8	V	
		HCNW4562		3		
Input Power Dissipation	P_{IN}	HCNW4562		40	mW	
Average Output Current (Pin 6)	$I_{O(AVG)}$			8	mA	
Peak Output Current (Pin 6)	$I_{O(PEAK)}$			16	mA	
Emitter-Base Reverse Voltage (Pin 5-7)	V_{EBR}			5	V	
Supply Voltage (Pin 8-5)	V_{CC}		-0.3	30	V	
Output Voltage (Pin 6-5)	V_O		-0.3	20	V	
Base Current (Pin 7)	I_B			5	mA	
Output Power Dissipation	P_O			100	mW	2
Lead Solder Temperature 1.6 mm Below Seating Plane, 10 Seconds up to Seating Plane, 10 Seconds	T_{LS}	HCPL-4562		260	°C	
		HCNW4562		260	°C	
Reflow Temperature Profile	T_{RP}	Option 300	See **Package Outline Drawings** Section			

Recommended Operating Conditions

Parameter	Symbol	Device	Min.	Max.	Units	Note
Operating Temperature	T_A	HCPL-4562	-10	70	°C	
Quiescent Input Current	I_{FQ}	HCPL-4562		6	mA	
		HCNW4562		10		
Peak Input Current	$I_{F(PEAK)}$	HCPL-4562		10	mA	
		HCNW4562		17		

Electrical Specifications (DC)

T_A = 25°C, I_F = 6 mA for HCPL-4562 and I_F = 10 mA for HCNW4562 (i.e., Recommended I_{FQ}) unless otherwise specified.

Parameter	Symbol	Device	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Base Photo Current	I_{PB}		13	31	65	µA	I_F = 10 mA, $V_{PB} \geq 5$ V	2, 6	
		HCPL-4562		19.2			I_F = 6 mA		
I_{PB} Temperature Coefficient	$\Delta I_{PB}/\Delta T$			-0.3		%/°C	2 mA < I_F < 10 mA, $V_{PB} \geq 5$ V	2	
I_{PB} Nonlinearity		HCPL-4562		0.25		%	2 mA < I_F < 10 mA	2, 6	3
		HCNW4562		0.15			6 mA < I_F < 14 mA		
Input Forward Voltage	V_F	HCPL-4562	1.1	1.3	1.6	V	I_F = 5 mA	5	
		HCNW4562	1.2	1.6	1.8		I_F = 10 mA		
Input Reverse Breakdown Voltage	BV_R	HCPL-4562	1.8	5		V	I_R = 10 µA		
		HCNW4562	3				I_R = 100 µA		
Transistor Current Gain	h_{FE}		60	160			I_C = 1 mA, V_{CE} = 1.25 V		
Current Transfer Ratio	CTR	HCPL-4562		45		%	V_{CE} = 1.25 V, $V_{PB} \geq 5$ V	8, 9	4
		HCNW4562		52					
DC Output Voltage	V_{OUT}	HCPL-4562		4.25		V	G_V = 2, V_{CC} = 9 V	4, 15	
		HCNW4562		5.0					

Small Signal Characteristics (AC)

T_A = 25°C, I_F = 6 mA for HCPL-4562 and I_F = 10 mA for HCNW4562 (i.e., Recommended I_{FO}) unless otherwise specified.

Parameter	Symbol	Device	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Voltage Gain	G_V (0.1 MHz)	HCPL-4562	0.8	2.0	4.2		V_{IN} = 1 V_{P-P}	1	6
		HCNW4562		3.0					
G_V Temperature Coefficient	$\Delta G_V/\Delta T$			-0.3		%/°C	V_{IN} = 1 V_{P-P}, f_{REF} = 0.1 MHz	1, 11	
Base Photo Current Variation	Δi_{PB} (6 MHz)	HCPL-4562		1.1	3.0	-dB	V_{IN} = 1 V_{P-P}, f_{REF} = 0.1 MHz	3, 10, 12	
		HCNW4562		0.36					
-3 dB Frequency (i_{PB})	i_{PB} (-3 dB)	HCPL-4562	6	15		MHz	V_{IN} = 1 V_{P-P}, f_{REF} = 0.1 MHz	3, 10, 12	7
		HCNW4562		13					
-3 dB Frequency (G_V)	G_V (-3 dB)	HCPL-4562	6	17		MHz	V_{IN} = 1 V_{P-P}, f_{REF} = 0.1 MHz	1, 11	7
		HCNW4562		9					
Gain Variation	ΔG_V (6 MHz)	HCPL-4562		1.1	3.0	-dB	T_A = 25°C, V_{IN} = 1 V_{P-P}, f_{REF} = 0.1 MHz	1, 11	
		HCNW4562		0.54					
		HCPL-4562		0.8			T_A = -10°C		
				1.5			T_A = 70°C		
	ΔG_V (10 MHz)	HCPL-4562		1.15		-dB	V_{IN} = 1 V_{P-P}, f_{REF} = 0.1 MHz		
		HCNW4562		2.27					
Differential Gain at f = 3.58 MHz		HCPL-4562		± 1.0		%	I_{Fac} = 0.7 mA p-p, I_{Fdc} = 3 to 9 mA	3, 7	8
		HCNW4562		± 0.9			I_{Fac} = 1 mA p-p, I_{Fdc} = 7 to 13 mA		
Differential Phase at f = 3.58 MHz		HCPL-4562		± 1		deg.	I_{Fac} = 0.7 mA p-p, I_{Fdc} = 3 to 9 mA	3, 7	9
		HCNW4562		± 0.6			I_{Fac} = 1 mA p-p, I_{Fdc} = 7 to 13 mA		
Total Harmonic Distortion	THD	HCPL-4562		2.5		%	V_{IN} = 1 V_{P-P}, f = 3.58 MHz, G_V = 2	4	10
		HCNW4562		0.75					
Output Noise Voltage	V_O(noise)			950		µVrms	10 Hz to 10 MHz	1	
Isolation Mode Rejection Ratio	IMRR	HCPL-4562		122		dB	f = 120 Hz, G_V = 2	14	11
		HCNW4562		119					

Package Characteristics

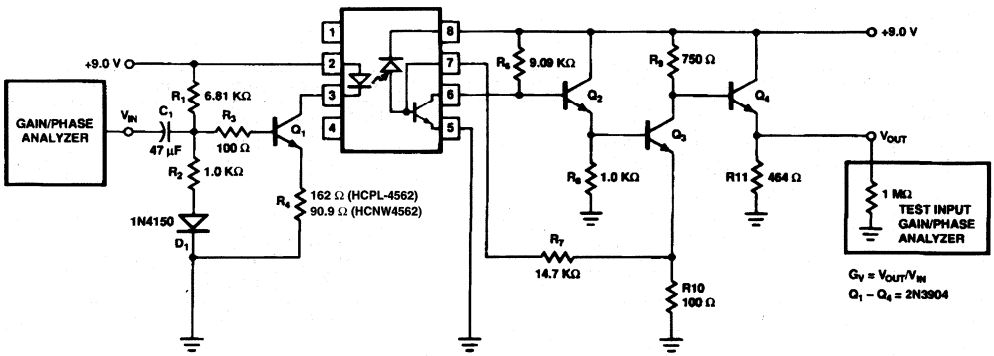
All Typicals at $T_A = 25°C$

Parameter	Sym.	Device	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage*	V_{ISO}	HCPL-4562	2500			V rms	RH ≤ 50%, t = 1 min., T_A = 25°C		5, 12
		HCNW4562	5000						5, 13
		HCPL-4562 (Option 020)	5000						5, 13
Input-Output Resistance	R_{I-O}	HCPL-4562		10^{12}		Ω	V_{I-O} = 500 Vdc		5
		HCNW4562	10^{12}	10^{13}			T_A = 25°C		
			10^{11}				T_A = 100°C		
Input-Output Capacitance	C_{I-O}	HCPL-4562		0.6		pF	f = 1 MHz		5
		HCNW4562		0.5	0.6				

*The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the VDE 0884 Insulation Related Characteristics Table (if applicable), your equipment level safety specification or HP Application Note 1074 entitled "Optocoupler Input-Output Endurance Voltage," publication number 5963-2203E.

Notes:

1. When used in the circuit of Figure 1 or Figure 4; $G_V = V_{OUT}/V_{IN}$; I_{FQ} = 6 mA (HCPL-4562), I_{FQ} = 10 mA (HCNW4562).
2. Derate linearly above 70°C free-air temperature at a rate of 2.0 mW/°C (HCPL-4562).
3. Maximum variation from the best fit line of I_{PB} vs. I_F expressed as a percentage of the peak-to-peak full scale output.
4. CURRENT TRANSFER RATIO (CTR) is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
5. Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.
6. Flat-band, small-signal voltage gain.
7. The frequency at which the gain is 3 dB below the flat-band gain.
8. Differential gain is the change in the small-signal gain of the optocoupler at 3.58 MHz as the bias level is varied over a given range.
9. Differential phase is the change in the small-signal phase response of the optocoupler at 3.58 MHz as the bias level is varied over a given range.
10. TOTAL HARMONIC DISTORTION (THD) is defined as the square root of the sum of the square of each harmonic distortion component. The THD of the isolated video circuit is measured using a 2.6 kΩ load in series with the 50 Ω input impedance of the spectrum analyzer.
11. ISOLATION MODE REJECTION RATIO (IMRR), a measure of the optocoupler's ability to reject signals or noise that may exist between input and output terminals, is defined by $20 \log_{10} [(V_{OUT}/V_{IN})/(V_{OUT}/V_{IM})]$, where V_{IM} is the isolation mode voltage signal.
12. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 3000 V rms for 1 second (leakage detection current limit, $I_{I-O} \leq 5$ μA). This test is performed before the 100% Production test shown in the VDE 0884 Insulation Related Characteristics Table, if applicable.
13. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 6000 V rms for 1 second (leakage detection current limit, $I_{I-O} \leq 5$ μA). This test is performed before the 100% Production test shown in the VDE 0884 Insulation Related Characteristics Table, if applicable.



NOTE: ALL RESISTORS ARE 1% TOLERANCE

Figure 1. Gain and Bandwidth Test Circuit.

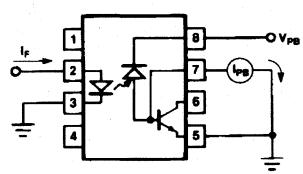


Figure 2. Base Photo Current Test Circuit.

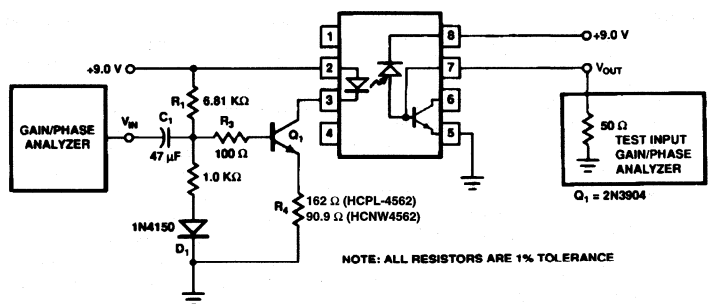


Figure 3. Base Photo Current Frequency Response Test Circuit.

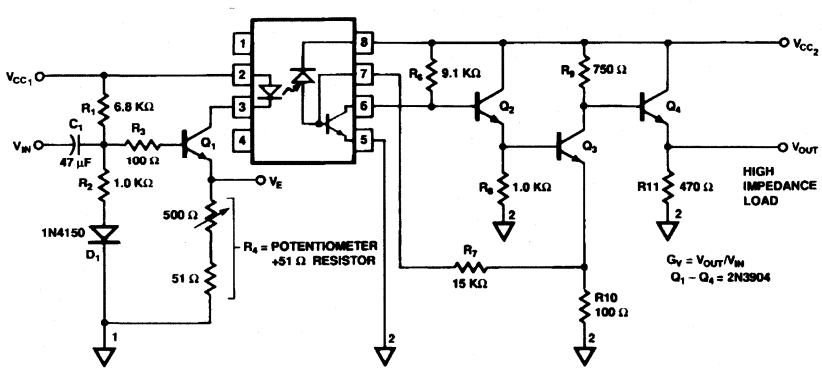


Figure 4. Recommended Isolated Video Interface Circuit.

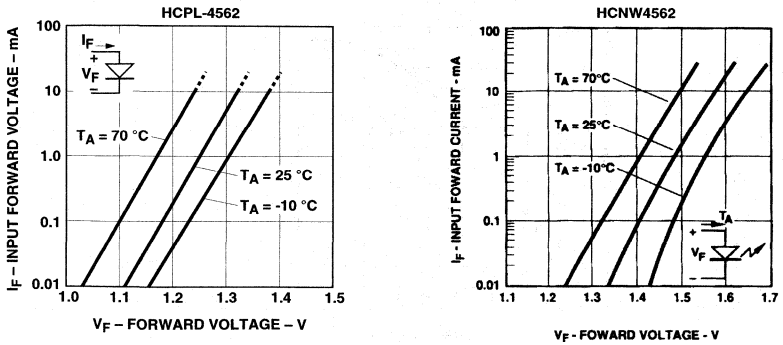


Figure 5. Input Current vs. Forward Voltage.

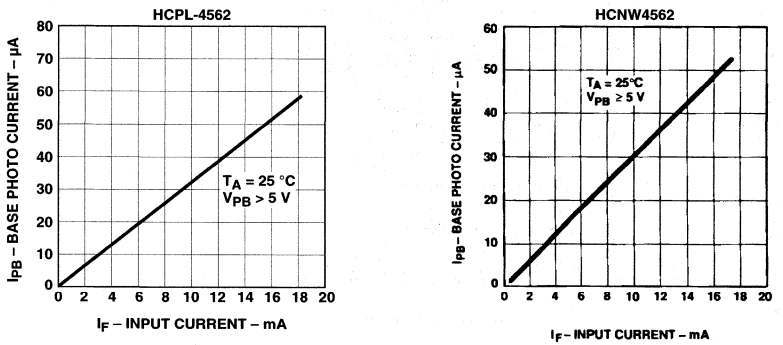


Figure 6. Base Photo Current vs. Input Current.

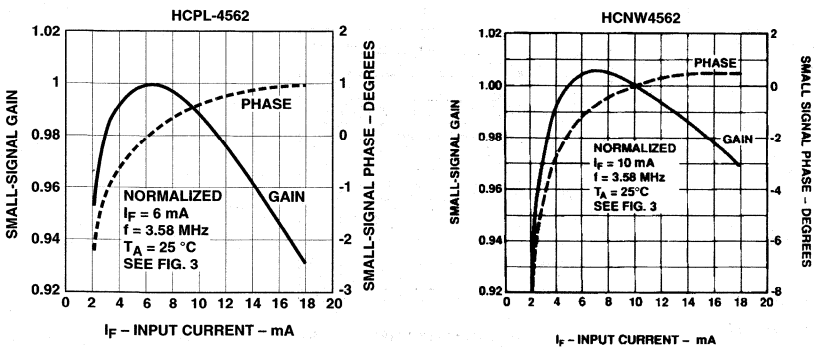


Figure 7. Small-Signal Response vs. Input Current.

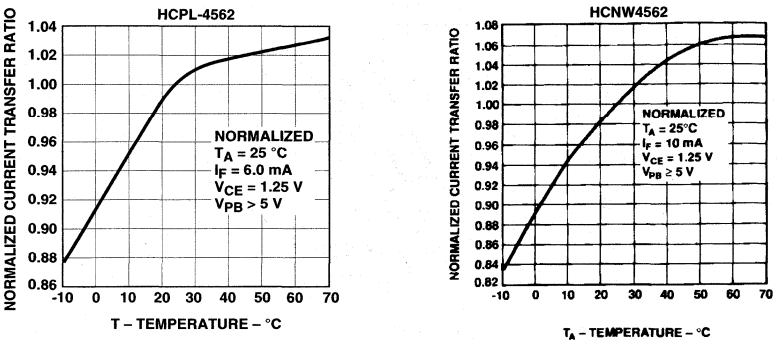


Figure 8. Current Transfer Ratio vs. Temperature.

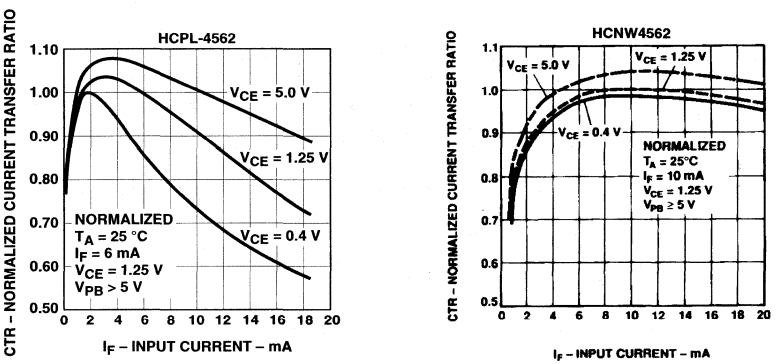


Figure 9. Current Transfer Ratio vs. Input Current.

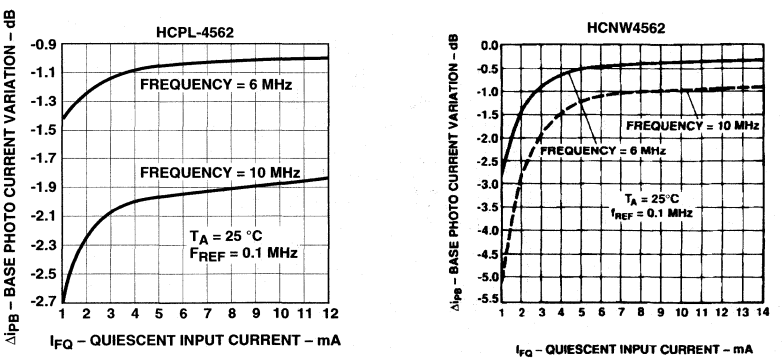


Figure 10. Base Photo Current Variation vs. Bias Conditions.

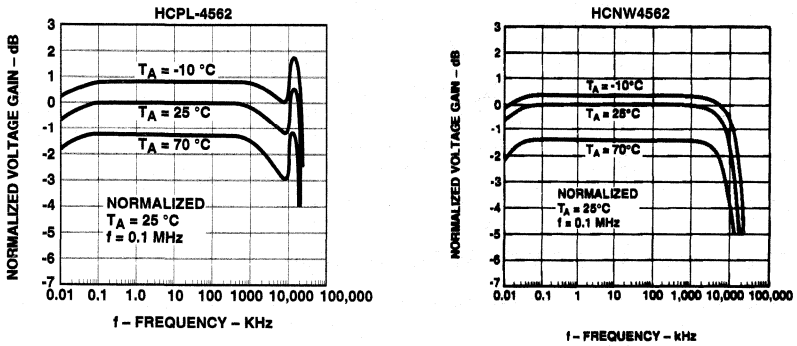


Figure 11. Normalized Voltage Gain vs. Frequency.

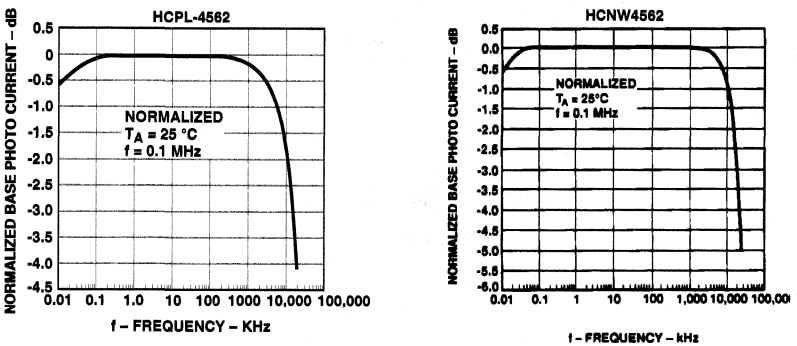


Figure 12. Normalized Base Photo Current vs. Frequency.

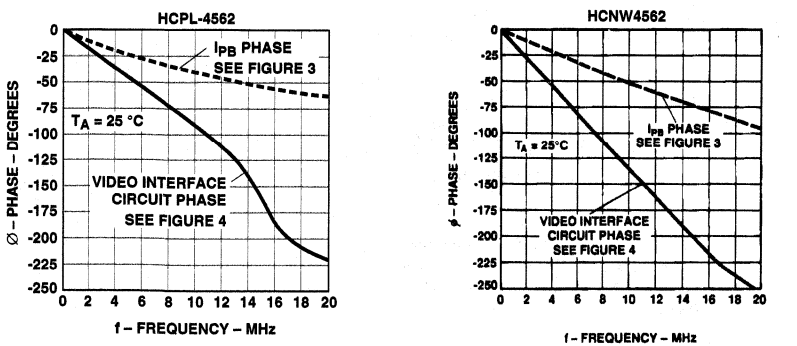


Figure 13. Phase vs. Frequency.

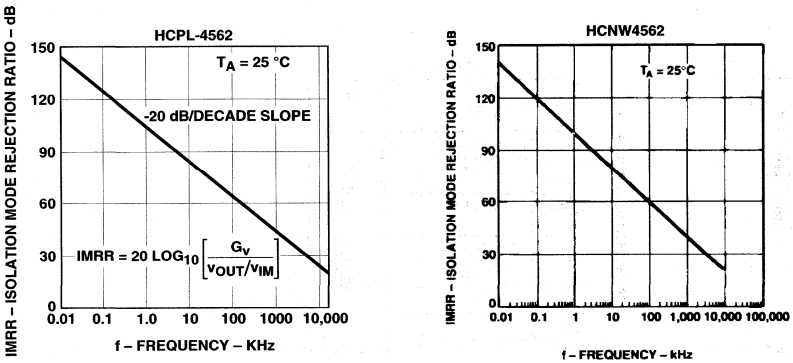


Figure 14. Isolation Mode Rejection Ratio vs. Frequency.

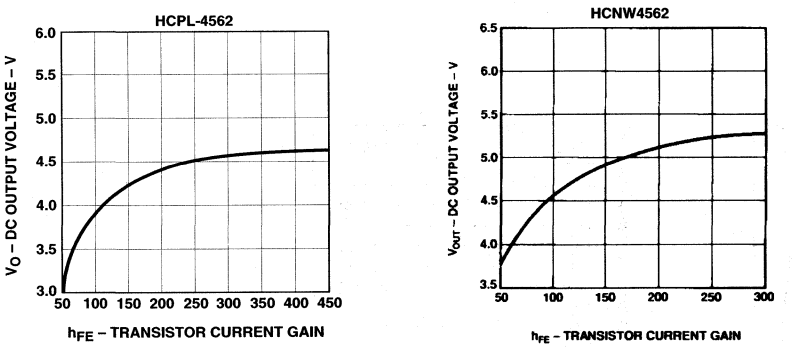


Figure 15. DC Output Voltage vs. Transistor Current Gain.

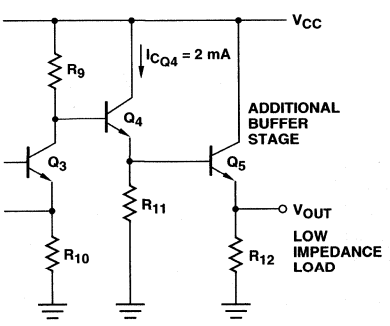


Figure 16. Output Buffer Stage for Low Impedance Loads.

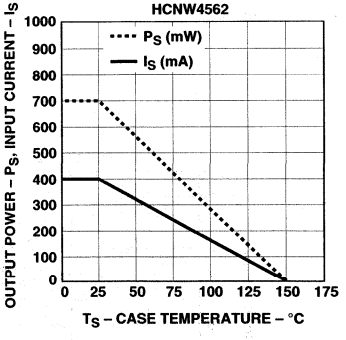


Figure 17. Thermal Derating Curve, Dependence of Safety Limiting Value with Case Temperature per VDE 0884.

Conversion from HCPL-4562 to HCNW4562

In order to obtain similar circuit performance when converting from the HCPL-4562 to the HCNW4562, it is recommended to increase the Quiescent Input Current, I_{FQ}, from 6 mA to 10 mA. If the application circuit in Figure 4 is used, then potentiometer R4 should be adjusted appropriately.

Design Considerations of the Application Circuit

The application circuit in Figure 4 incorporates several features that help maximize the bandwidth performance of the HCPL-4562/HCNW4562. Most important of these features is peaked response of the detector circuit that helps extend the frequency range over which the voltage gain is relatively constant. The number of gain stages, the overall circuit topology, and the choice of DC bias points are all consequences of the desire to maximize bandwidth performance.

To use the circuit, first select R_1 to set V_E for the desired LED quiescent current by:

$$I_{FQ} = \frac{V_E}{R_4} \cong \frac{G_V V_E R_{10}}{(\partial I_{PB}/\partial I_F) R_7 R_9} \quad (1)$$

For a constant value V_{INp-p}, the circuit topology (adjusting the gain with R_4) preserves linearity by keeping the modulation factor (MF) dependent only on V_E.

$$i_{F_{p-p}} \cong V_{IN}/R_4 \quad (2)$$

$$\frac{i_{Fp-p}}{I_{FQ}} \cong \frac{i_{PBp-p}}{I_{PBQ}} = \frac{V_{INp-p}}{V_E} \quad (3)$$

Modulation Factor (MF): $$\frac{i_{F(p-p)}}{2\ I_{FQ}} = \frac{V_{INp-p}}{2\ V_E} \quad (4)$$

For a given G_V, V_E, and V_{CC}, DC output voltage will vary only with h_{FEX}.

$$V_O = V_{CC} - V_{BE_4} - \frac{R_9}{R_{10}} [V_{BEX} - (I_{PBQ} - I_{BXQ}) R_7] \quad (5)$$

Where:

$$I_{PBQ} \cong \frac{G_V V_E R_{10}}{R_7 R_9} \quad (6)$$

and,

$$I_{BXQ} \cong \frac{V_{CC} - 2\ V_{BE}}{R_6\ h_{FEX}} \quad (7)$$

Figure 15 shows the dependency of the DC output voltage on h_{FEX}.

For 9 V < V_{CC} < 12 V, select the value of R_{11} such that

$$I_{CQ4} \cong \frac{V_O}{R_{11}} \leq \frac{4.25\ V}{470\ \Omega} \leq 9.0\ mA \quad (8)$$

The voltage gain of the second stage (Q_3) is approximately equal to:

$$\frac{R_9}{R_{10}} * \frac{1}{1 + s\ R_9 \left[C_{CQ_3} + \frac{1}{2\pi\ R'_{11}\ f_{T_4}}\right]} \quad (9)$$

Increasing R'_{11} (R'_{11} includes the parallel combination of R_{11} and the load impedance) or reducing R_9 (keeping R_9/R_{10} ratio constant) will improve the bandwidth.

If it is necessary to drive a low impedance load, bandwidth may also be preserved by adding an additional emitter following the buffer stage (Q_5 in Figure 16), in which case R_{11} can be increased to set $I_{CQ4} \cong 2$ mA.

Finally, adjust R_4 to achieve the desired voltage gain.

$$G_V \cong \frac{V_{OUT}}{V_{IN}} \cong \frac{\partial I_{PB}}{\partial I_F} \left[\frac{R_7 R_9}{R_4 R_{10}}\right] \quad (10)$$

where typically $\frac{\partial I_{PB}}{\partial I_F} = 0.0032$

Definition:

G_V = Voltage Gain
I_{FQ} = Quiescent LED forward current
i_{Fp-p} = Peak-to-peak small signal LED forward current
V_{INp-p} = Peak-to-peak small signal input voltage
i_{PBp-p} = Peak-to-peak small signal base photo current
I_{PBQ} = Quiescent base photo current
V_{BEX} = Base-Emitter voltage of HCPL-4562/HCNW4562 transistor
I_{BXQ} = Quiescent base current of HCPL-4562/HCNW4562 transistor
h_{FEX} = Current Gain (I_C/I_B) of HCPL-4562/HCNW4562 transistor
V_E = Voltage across emitter degeneration resistor R_4
f_{T_4} = Unity gain frequency of Q_5
C_{CQ_3} = Effective capacitance from collector of Q_3 to ground

HEWLETT® PACKARD

High Speed CMOS Optocouplers

Technical Data

HCPL-7100
HCPL-7101

Features

- **1 μm CMOS IC Technology**
- **Compatibility with All +5 V CMOS and TTL Logic Families**
- **No External Components Required for Logic Interface**
- **High Speed: 15 MBd (HCPL-7100) and 50 MBd (HCPL-7101) Guaranteed**
- **Low Power Consumption**
- **Safety Approvals**
  UL 1577 (3750 Vac/1 Min)
  VDE 0884 (V_{IORM} = 848 V peak)
  CSA
- **3-State Output**
- **3750 Vac/1 Minute Dielectric Withstand**
- **High Common Mode Transient Immunity**

Applications

- **Multiplexed Data Transmission**
- **Computer-Peripheral Interface**
- **Microprocessor System Interface**
- **Digital Isolation for A/D, D/A Conversion**
- **Instrument Input/Output Isolation**
- **Motor Control**
- **Power Inverter**

Description

The HCPL-7100/7101 optocoupler combines the latest CMOS IC technology, a new high-speed high-efficiency AlGaAs LED, and an optimized light coupling system to achieve outstanding performance with very low power consumption. It requires only two bypass capacitors for complete CMOS/TTL compatibility.

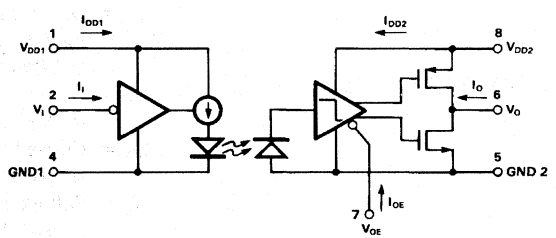
Basic building blocks of the HCPL-7100/7101 are a CMOS LED driver IC, an AlGaAs LED, and a CMOS detector IC. A CMOS or TTL logic input signal controls the LED driver IC which supplies current to the LED. The detector IC incorporates an integrated photodiode, a high-speed transimpedance amplifier and a voltage comparator with hysteresis. The 3-state output is CMOS and TTL compatible and is controlled by the output enable pin, V_{OE}.

The HCPL-7100/7101 consumes very little power, due to the CMOS IC technology and the light coupling system. The entire optocoupler typically uses only 10 mA of supply current, including the LED current.

World-wide safety approval and 3750 Vac/1 minute dielectric withstand is achieved with our patented "light-pipe" optocoupler packaging technology.

The HCPL-7100/7101 provides he user with an easy-to-use CMOS or TTL compatible optocoupler ideally suited for a variety of applications where high speed and low power consumption are desired.

Schematic



TRUTH TABLE (POSITIVE LOGIC)

INPUT	ENABLE	OUTPUT
H	H	Z
L	H	Z
H	L	H
L	L	L

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

5965-3578E

Ordering Information

HCPL-710x

- 0 = 15 MBd Minimum Data Rate
- 1 = 50 MBd Minimum Data Rate

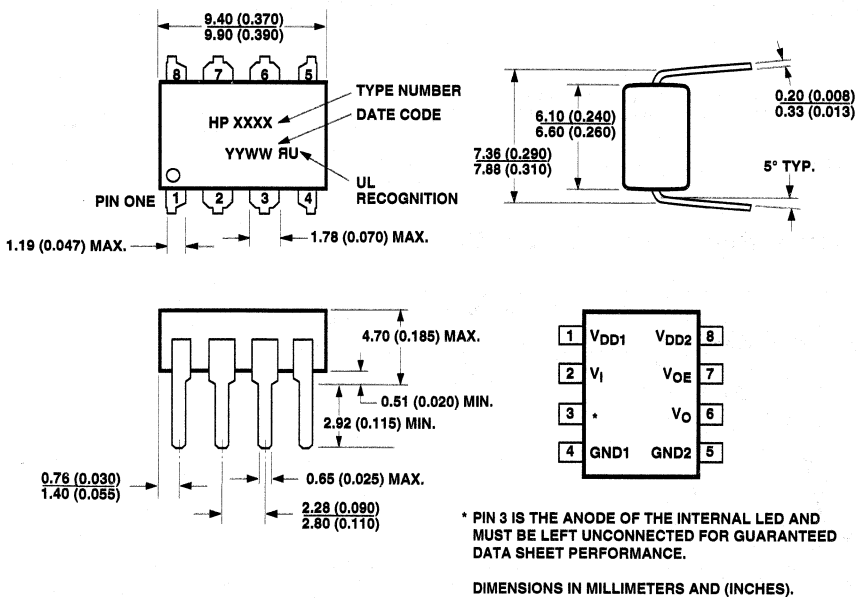
Option yyy

- 300 = Gull Wing Surface Mount Lead Option
- 500 = Tape/Reel Package Option (1 k min.)

Option data sheets available. Contact your Hewlett-Packard sales representative or authorized distributor for information.

Package Outline Drawings

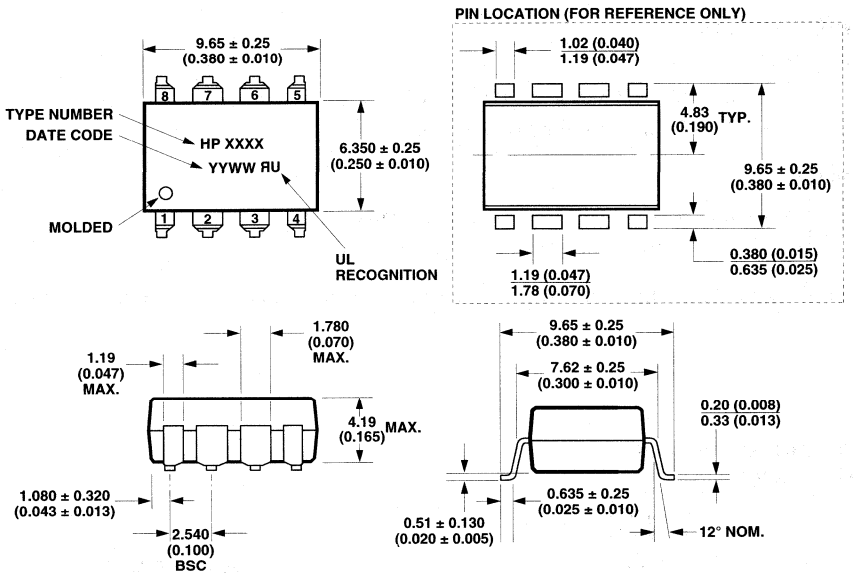
Standard DIP Package



* PIN 3 IS THE ANODE OF THE INTERNAL LED AND MUST BE LEFT UNCONNECTED FOR GUARANTEED DATA SHEET PERFORMANCE.

DIMENSIONS IN MILLIMETERS AND (INCHES).

Gull Wing Surface Mount Option 300*

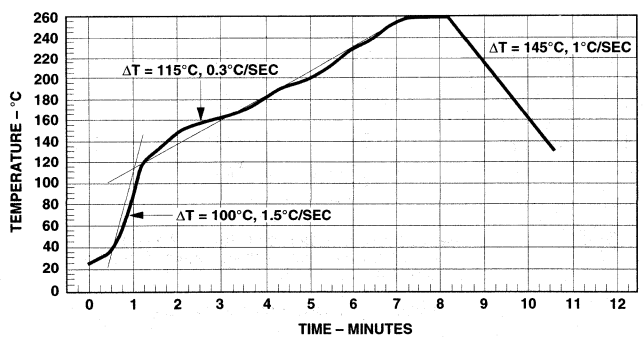


DIMENSIONS IN MILLIMETERS (INCHES).
TOLERANCES (UNLESS OTHERWISE SPECIFIED): xx.xx = 0.01
xx.xxx = 0.005

LEAD COPLANARITY
MAXIMUM: 0.102 (0.004)

*Refer to Option 300 data sheet for more information.

Maximum Solder Reflow Thermal Profile



(NOTE: USE OF NON-CHLORINE ACTIVATED FLUXES IS RECOMMENDED.)

Regulatory Information

The HCPL-7100/1 has been approved by the following organizations:

UL
Recognized under UL 1577, Component Recognition Program, File E55361.

CSA
Approved under CSA Component Acceptance Notice #5, File CA 88324.

VDE
Approved according to VDE 0884/06.92

Insulation and Safety Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min. External Air Gap (External Clearance)	L(IO1)	7.4	mm	Measured from input terminals to output terminals, shortest distance through air
Min. External Tracking Path (External Creepage)	L(IO2)	8.0	mm	Measured from input terminals to output terminals, shortest distance path along body
Min. Internal Plastic Gap (Internal Clearance)		0.5	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity
Tracking Resistance (Comparative Tracking Index)	CTI	175	V	DIN IEC 112/VDE 0303 PART 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Option 300 – surface mount classification is Class A in accordance with CECC 00802.

VDE 0884 (06.92) Insulation Characteristics

Description	Symbol	Characteristic	Unit
Installation classification per DIN VDE 0110, Table 1 for rated mains voltage ≤ 300 V rms for rated mains voltage ≤ 600 V rms		 I-IV I-III	
Climatic Classification		40/85/21	
Pollution Degree (DIN VDE 0110, Table 1)*		2	
Maximum Working Insulation Voltage	V_{IORM}	848	V peak
Input to Output Test Voltage, Method b** V_{PR} = 1.875 x V_{IORM}, Production test with t_p = 1 sec, Partial discharge < 5 pC	V_{PR}	1591	V peak
Input to Output Test Voltage, Method a** V_{PR} = 1.5 x V_{IORM}, Type and sample test, t_p = 60 sec, Partial discharge < 5 pC	V_{PR}	1273	V peak
Highest Allowable Overvoltage** (Transient Overvoltage, t_{TR} = 10 sec)	V_{TR}	6000	V peak
Safety-limiting values (Maximum values allowed in the event of a failure, also see Figure 15) Case Temperature Input Power Output Power	 T_S $P_{S,INPUT}$ $P_{S,OUTPUT}$	 175 80 250	 °C mW mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	≥ 1 x 10^{12}	Ω

*This part may also be used in Pollution Degree 3 environments where the rated mains voltage is ≤ 300 V rms (per DIN VDE 0110).
**Refer to the front of the optocoupler section in the current catalog for a more detailed description of VDE 0884 and other product safety requirements.

Note: Optocouplers providing safe electrical separation per VDE 0884 do so only within the safety-limiting values to which they are qualified. Protective cut-out switches must be used to ensure that the safety limits are not exceeded.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	T_S	-55	125	°C
Ambient Operating Temperature	T_A	-40	85	°C
Supply Voltages	$V_{DD1,2}$	0.0	5.5	V
Input Voltage	V_I	-0.5	V_{DD1} + 0.5	V
Output Voltage	V_O	-0.5	V_{DD2} + 0.5	V
Output Enable Voltage	V_{OE}	-0.5	V_{DD2} + 0.5	V
Average Output Current	I_O		25	mA
Package Power Dissipation	P_{PD}		220	mW
Lead Solder Temperature (1.6 mm Below Seating Plane, 10 sec.)	T_{LS}		260	°C
Reflow Temperature Profile	See **Package Outline Drawings** Section			

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit	Test Conditions
Operating Temperature	T_A	-40	85	°C	
Supply Voltages	$V_{DD1,2}$	4.5	5.5	V	
Logic High Input Voltage	V_{IH}	2.0	V_{DD1}	V	
Logic Low Input Voltage	V_{IL}	0.0	0.8	V	
Logic High Output Enable Voltage	V_{OEH}	2.0	V_{DD2}	V	Output in high impedance state
Logic Low Output Enable Voltage	V_{OEL}	0.0	0.8	V	Output enabled
Input Signal Rise and Fall Times	t_r, t_f		1	ms	
TTL Fanout	N		6		Standard Loads

Electrical Specifications

Guaranteed across recommended operating conditions. Test conditions represent worst case values for the parameter under test. Test conditions that are not specified can be anywhere within their operating range. All typicals are at 25°C and 5 V supplies unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions		Fig.	Note
Logic Low Input Supply Current	I_{DD1L}		5.2	10.0	mA	V_{DD1} = 5.5 V $V_I = V_{IL}$			1
Logic High Input Supply Current	I_{DD1H}		0.3	0.6	mA	V_I = 4.5 V	V_{DD1} = 5.5 V		1
			0.9	1.6		V_I = 2.0 V			
Logic Low Output Supply Current	I_{DD2L}		5.0	9.0	mA	V_{DD2} = 5.5 V $V_{OE} = V_{OEL}$ $V_I = V_{IL}$			
Logic High Output Supply Current	I_{DD2H}		5.2	9.0	mA	V_{DD2} = 5.5 V $V_{OE} = V_{OEL}$ I_O = 0 mA $V_I = V_{IH}$			
Tri-State Output Supply Current	I_{DD2Z}		5.1	9.0	mA	V_{OE} = 4.5 V	V_{DD2} = 5.5 V		
			5.6	10.0		V_{OE} = 2.0 V			
Input Current	I_I	-1		1	µA	$V_I = V_{DD1}$ or GND V_{DD1} = 5.5 V			
Output Enable Current	I_{OE}	-1		1	µA	$V_{OE} = V_{DD2}$ or GND V_{DD2} = 5.5 V			
Logic High Output Voltage	V_{OH}	4.4	5.0		V	I_O = -20 µA	V_{DD2} = 4.5 V $V_I = V_{IH}$ $V_{OE} = V_{OEL}$	6	
		4.0	4.8			I_O = -4.0 mA			
		3.7	4.7			I_O = -6.0 mA			
Logic High Output Current	I_{OH}	-7.5	-25		mA	V_{DD2} = 4.5 V V_O = 3.6 V $V_I = V_{IH}$ $V_{OE} = V_{OEL}$		6	
Logic Low Output Voltage	V_{OL}		0.0	0.1	V	I_O = 20 µA	V_{DD2} = 4.5 V $V_I = V_{IL}$ $V_{OE} = V_{OEL}$	5	
			0.1	0.3		I_O = 4.0 mA			
			0.15	0.4		I_O = 6.0 mA			
Logic Low Output Current	I_{OL}	10.5	23		mA	V_{DD2} = 4.5 V V_O = 0.6 V $V_I = V_{IL}$ $V_{OE} = V_{OEL}$		5	
High Impedance State Output Current	I_{OZ}	-5		5	µA	V_{DD2} = 5.5 V $V_{OE} = V_{OEH}$ $V_O = V_{DD2}$ or GND			
Input Capacitance	C_I		4.3		pF	f = 1 MHz			4

Switching Specifications

Guaranteed across recommended operating conditions. Test conditions represent worst case values for the parameter under test. Test conditions that are not specified can be anywhere within their operating range. All typicals are at 25°C and 5 V supplies unless otherwise noted.

Parameter	Symbol	Device	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Note
Propagation Delay Time to Logic Low Output	t_{PHL}	HCPL-7100			70	ns	C_L = 50 pF CMOS Signal Levels	7, 8	5, 6
		HCPL-7101		28	40				
		HCPL-7100			70	ns	C_L = 15 pF TTL Signal Levels		
		HCPL-7101			40				
Propagation Delay Time to Logic High Output	t_{PLH}	HCPL-7100			70	ns	C_L = 50 pF CMOS Signal Levels	7, 8	5, 6
		HCPL-7101		27	40				
		HCPL-7100			70	ns	C_L = 15 pF TTL Signal Levels		
		HCPL-7101			40				
Pulse Width Distortion $\lvert t_{PHL}-t_{PLH} \rvert$	PWD	HCPL-7100			20	ns	C_L = 50 pF CMOS Signal Levels	7, 9	6, 7
		HCPL-7101		2	6				
		HCPL-7100			20	ns	C_L = 15 pF TTL Signal Levels		
		HCPL-7101			6				
Data Rate		HCPL-7100	15			MBd	% PWD < 30%		8
		HCPL-7101	50	65					
Propagation Delay Skew	t_{PSK}	HCPL-7101			10	ns		10	9
Output Rise Time (10-90%)	t_R	HCPL-7100		12		ns	C_L = 50 pF CMOS Signal Levels	7	
		HCPL-7101		10					
Output Fall Time (90-10%)	t_F	HCPL-7100		8		ns	C_L = 50 pF CMOS Signal Levels	7	
		HCPL-7101		7					
Random Jitter	RJ	HCPL-7101		50		ps rms	V_I = 0-5 V square wave, f = 25 MHz, input rise/ fall time = 5 ns. R_L = 10 kΩ, C_L = 5 pF. TTL Threshold Levels.		
Propagation Delay Time From Output Enabled to Logic High Output	t_{PZH}			13		ns	C_L = 50 pF CMOS Signal Levels	12	6
				12		ns	C_L = 15 pF TTL Signal Levels		
Propagation Delay Time From Output Enabled to Logic Low Output	t_{PZL}			11		ns	C_L = 50 pF CMOS Signal Levels	12	6
				10		ns	C_L = 15 pF TTL Signal Levels		

Switching Specifications (cont.)

Guaranteed across recommended operating conditions. Test conditions represent worst case values for the parameter under test. Test conditions that are not specified can be anywhere within their operating range. All typicals are at 25°C and 5 V supplies unless otherwise noted.

Parameter	Symbol	Device	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Note
Propagation Delay Time from Logic High to Output Disabled	t_{PHZ}			12		ns	C_L = 50 pF CMOS Signal Levels	12	6
				12		ns	C_L = 15 pF TTL Signal Levels		
Propagation Delay Time from Logic Low to Output Disabled	t_{PLZ}			9		ns	C_L = 50 pF CMOS Signal Levels	12	6
				11		ns	C_L = 15 pF TTL Signal Levels		
Common Mode Transient Immunity at Logic High Output	$\|CM_H\|$	HCPL-7100	1000			V/μs	V_{CM} = 50 V; $V_I = V_{IH}$, $V_D > 3.2$ V	13, 14	10
		HCPL-7101	2000				V_{CM} = 200 V		
Common Mode Transient Immunity at Logic Low Output	$\|CM_L\|$	HCPL-7100	1000			V/μs	V_{CM} = 50 V; $V_I = V_{IL}$, $V_D < 0.8$ V	13, 14	10
		HCPL-7101	2000				V_{CM} = 200 V		
Input Dynamic Power Dissipation Capacitance	C_{PD1}			68		pF			11
Output Dynamic Power Dissipation Capacitance	C_{PD2}			10		pF			11

Package Characteristics

Guaranteed across recommended operating conditions. Test conditions represent worst case value for the parameter under test. Test conditions that are not specified can be anywhere within their operating range. All typicals are at T_A = 25°C and 5 V supplies unless otherwise noted.

Parameter	Sym.	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage*	V_{ISO}	3750			V rms	t = 1 min., RH < 50%, T_A = 25°C		2, 3
Input-Output Resistance	R_{I-O}	10^{12}	10^{13}		Ω	T_A = 25°C; V_{I-O} = 500 Vdc		2
		10^{11}				T_A = 100°C		
Input-Output Capacitance	C_{I-O}		0.7		pF	f = 1 MHz		2

*The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the VDE 0884 Insulation Characteristics Table (if applicable), your equipment level safety specification or HP Application Note 1074 entitled "Optocoupler Input-Output Endurance Voltage."

Notes:

1. The LED is OFF when the V_I is high and ON when V_I is low.
2. Device considered a two terminal device; pins 1-4 shorted together and pins 5-8 shorted together.
3. In accordance with UL 1577, for devices with minimum V_{ISO} specified at 3750 V rms, each optocoupler is proof-tested by applying an insulation test voltage greater than 4500 V rms for one second (leakage current detection limit $I_{I-O} < 5$ μA). This test is performed before the method b, 100% production test for partial discharge shown in the VDE 0884 Insulation Characteristics Table.
4. C_I is the capacitance measured at pin 2 (V_I).
5. t_{PHL} propagation delay is measured from the 50% level on the falling edge of the V_I signal to the logic switching level of the V_O signal. t_{PLH} propagation delay is measured from the 50% level on the rising edge of the V_I signal to the logic switching level of the V_O signal.
6. The logic switching levels are 1.5 V for TTL signals (0-3 V) and 2.5 V for CMOS signals (0-5 V).
7. PWD is defined as $|t_{PHL} - t_{PLH}|$. %PWD (percent pulse width distortion) is equal to PWD in ns divided by symbol duration (bit length) in ns.
8. Minimum data rate is calculated as follows: %PWD/PWD where %PWD is typically chosen by the design engineer (30% is common).
9. t_{PSK} is equal to the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between units at the same temperature, supply voltage, and output load within the recommended operating condition range.
10. CM_H is the maximum common mode voltage slew rate that can be sustained while maintaining $V_O > 3.2$ V. CM_L is the maximum common mode voltage slew rate that can be sustained while maintaining $V_O < 0.8$ V. The common mode voltage slew rates apply to both rising and falling common mode voltage edges.
11. Unloaded dynamic power dissipation is calculated as follows: $C_{PD} \cdot V_{DD}^2 \cdot f + I_{DD} \cdot V_{DD}$ where f is switching frequency in MHz.

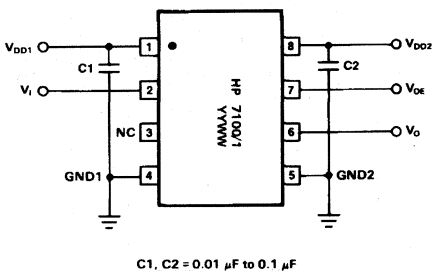


Figure 1. Recommended Application Circuit.

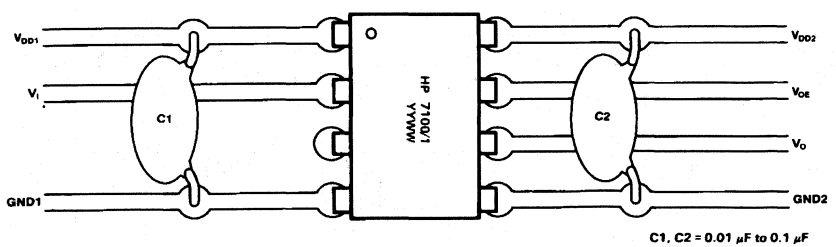


Figure 2. Recommended Printed Circuit Board Layout.

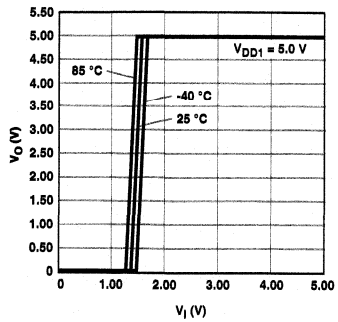


Figure 3. Typical Output Voltage vs. Input Voltage.

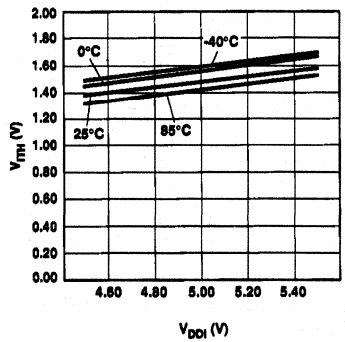


Figure 4. Typical Input Voltage Switching Threshold vs. Input Supply Voltage.

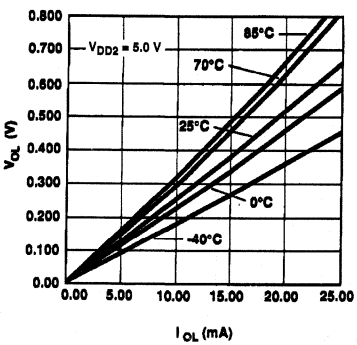


Figure 5. Typical Logic Low Output Voltage vs. Logic Low Output Current.

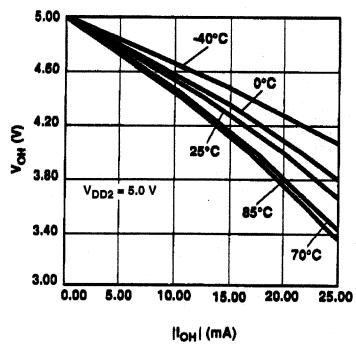


Figure 6. Typical Logic High Output Voltage vs. Logic High Output Current.

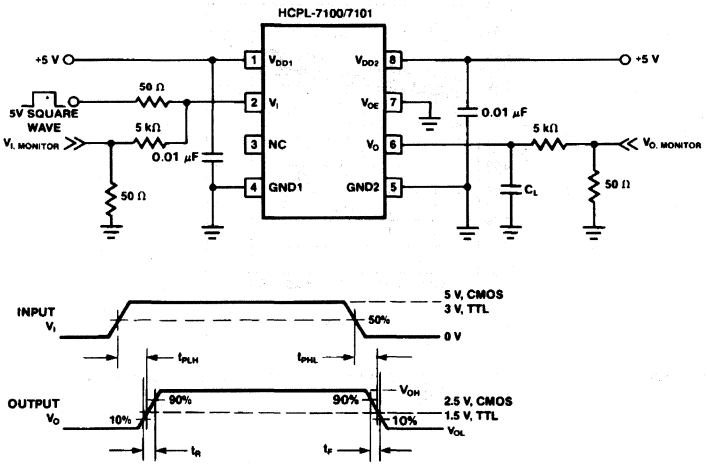


Figure 7. Test Circuit for Propagation Delay, Rise Time and Fall Time.

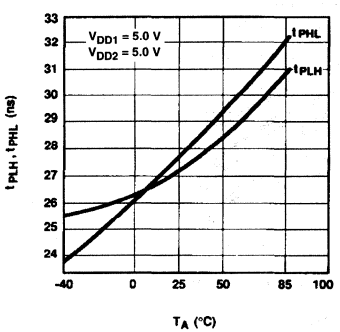


Figure 8. HCPL-7101 Typical Propagation Delay vs. Temperature.

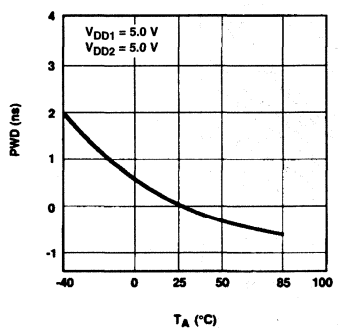


Figure 9. HCPL-7101 Typical Pulse Width Distortion vs. Temperature.

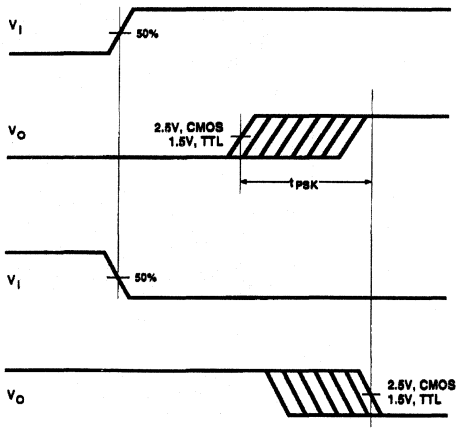


Figure 10. Propagation Delay Skew Waveform.

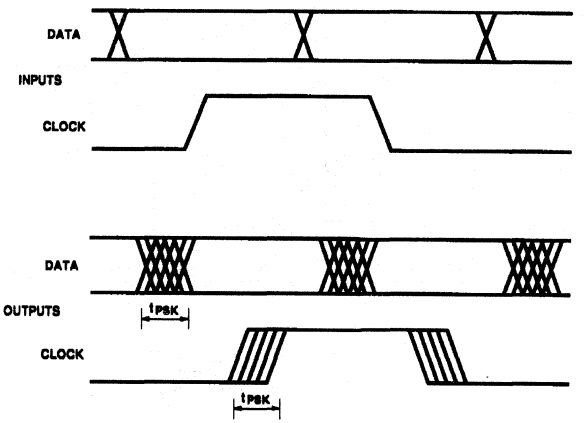
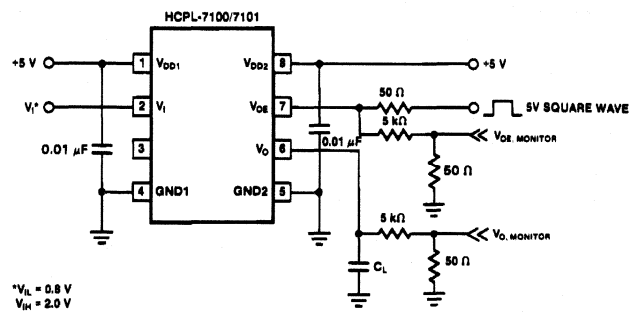


Figure 11. Parallel Data Transmission Example.



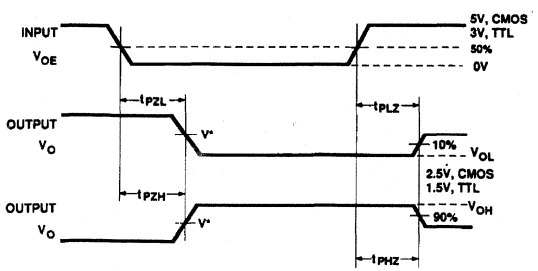


Figure 12. Test Circuit for 3-State Output Enable and Disable Propagation Delays.

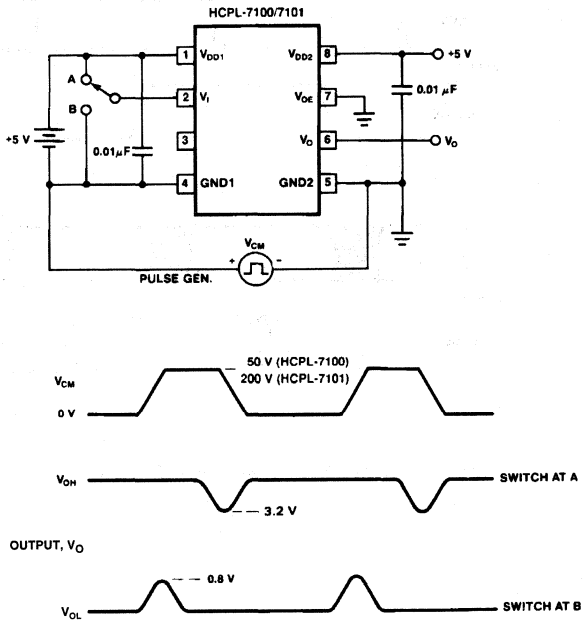


Figure 13. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

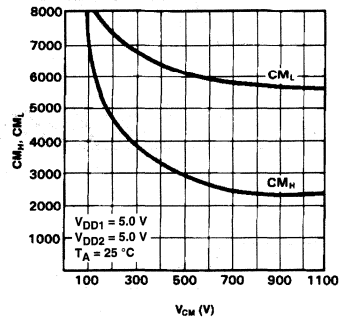


Figure 14. Typical Common Mode Transient Immunity vs. Common Mode Transient Voltage.

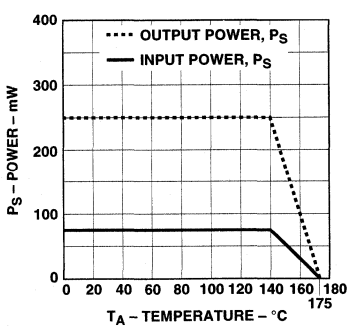


Figure 15. Dependence of Safety-Limiting Data on Ambient Temperature.

HCPL-7100/7101 Application Information

The HCPL-7100/7101 is extremely easy to use. Because the optocoupler uses high-speed CMOS IC technology, the inputs and output are fully compatible with all +5 V TTL and CMOS logic. TTL or CMOS logic can be connected directly to the inputs and output; no external interface circuitry is required.

As shown in Figure 1, the only external components required for proper operation are two ceramic bypass capacitors. Capacitor values should be between 0.01 μF and 0.1 μF. For each capacitor, the total lead length between both ends of the capacitor and the power-supply pins should not exceed 20 mm. Figure 2 illustrates the recommended printed circuit board layout for the HCPL-7100/7101.

Propagation Delay, Pulse-Width Distortion, and Propagation Delay Skew

Propagation delay is a figure of merit which describes how quickly a logic signal propagates through a system. The propagation delay from low to high (t_{PLH}) is the amount of time required for an input signal to propagate to the output, causing the output to change from low to high. Similarly, the propagation delay from high to low (t_{PHL}) is the amount of time required for the input signal to propagate to the output, causing the output to change from high to low (see Figure 7).

Pulse-width distortion (PWD) results when t_{PLH} and t_{PHL} differ in value. PWD is defined as the difference between t_{PLH} and t_{PHL} and often determines the maximum data rate capability of a transmission system. PWD can be expressed in percent by dividing the PWD (in ns) by the minimum pulse width (in ns) being transmitted. Typically, PWD on the order of 20-30% of the minimum pulse width is tolerable; the exact figure depends on the particular application (RS232, RS422, T-1, etc.).

Propagation delay skew, t_{PSK}, is an important parameter to consider in parallel data applications where synchronization of signals on parallel data lines is a concern. If the parallel data is being sent through a group of optocouplers, differences in propagation delays will cause the data to arrive at the outputs of the optocouplers at different times. If this difference in propagation delays is large enough, it will determine the maximum rate at which parallel data can be sent through the optocouplers.

Propagation delay skew is defined as the difference between the minimum and maximum propagation delays, either t_{PLH} or t_{PHL}, for any given group of optocouplers which are operating under the same conditions (i.e., the same supply voltage, output load, and operating temperature). As illustrated in Figure 10, if the inputs of a group of optocouplers are switched either ON or OFF at the same time, t_{PSK} is the difference between the shortest propagation delay, either t_{PLH} or t_{PHL}, and the longest propagation delay, either t_{PLH} or t_{PHL}.

As mentioned earlier, t_{PSK} can determine the maximum parallel data transmission rate. Figure 11 is the timing diagram of a typical parallel data application with both the clock and the data lines being sent through optocouplers. The figure shows data and clock signals at the inputs and outputs of the optocouplers. To obtain the maximum data transmission rate, both edges of the clock signal are being used to clock the data; if only one edge were used, the clock signal would need to be twice as fast.

Propagation delay skew represents the uncertainty of where an edge might be after being sent through an optocoupler. Figure 11 shows that there will be uncertainty in both the data and the clock lines. It is important that these two areas of uncertainty not overlap, otherwise the clock signal might arrive before all of the data outputs have settled, or some of the data outputs may start to change before the clock signal has arrived. From these considerations, the absolute minimum pulse width that can be sent through optocouplers in a parallel application is twice t_{PSK}. A cautious design should use a slightly longer pulse width to ensure that any additional uncertainty in the rest of the circuit does not cause a problem.

The HCPL-7101 optocoupler offers the advantages of guaranteed specifications for propagation delays, pulse-width distortion and propagation delay skew over the recommended temperature, and power supply ranges.

HEWLETT® PACKARD

40 ns Prop. Delay, SO-8 Optocoupler

Preliminary Technical Data

HCPL-0710

Features

- **+5 V CMOS Compatibility**
- **8 ns Pulse Width Distortion**
- **High Speed: 12 Mbd**
- **10 kV/μs Minimum Common Mode Rejection**
- **Industrial Temperature Range: 0°C to 85°C**
- **Safety and Regulatory Approvals**
  UL Recognized 2500 V rms for 1 min. per UL 1577
  CSA Component Acceptance Notice #5

Applications

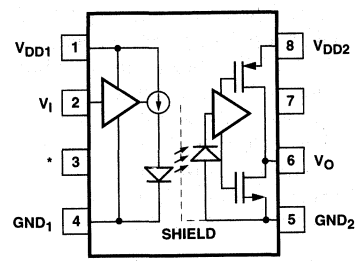
- **Digital Fieldbus Isolation: DeviceNet, SDS, PROFIBUS**
- **Multiplexed Data Transmission**
- **Computer Peripheral Interface**
- **Microprocessor System Interface**

Description

Available in the SO-8 package style, the HCPL-0710 optocoupler utilizes the latest CMOS IC technology to achieve outstanding performance with very low power consumption. The HCPL-0710 requires only two bypass capacitors for complete CMOS compatibility.

Basic building blocks of the HCPL-0710 are a CMOS LED driver IC and a CMOS detector IC. A CMOS logic input signal controls the LED driver IC which supplies current to the LED. The detector IC incorporates an integrated photodiode, a high-speed transimpedance amplifier, and a voltage comparator with an output driver.

Functional Diagram



TRUTH TABLE

V_I, INPUT	V_O, OUTPUT
H	H
L	L

*Pin 3 is the anode of the internal LED and must be left unconnected for guaranteed data sheet performance. Pin 7 is not connected internally. External connections to pin 7 are not recommended.
**A 0.1 μF bypass capacitor must be connected between pins 1 and 4, and 5 and 8.*

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

This data sheet represents the latest information at the time of publication of this catalog. All specifications subject to change. Samples available Fall 1996.

Electrical Specifications

Unless otherwise noted, all specifications are guaranteed across recommended operating conditions. All Typical specifications are at T_A = +25°C, V_{DD1} = V_{DD2} = +5 V. Test conditions that are not specified can be anywhere within the recommended operating range.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
DC Specifications						
Logic Low Input Supply Current	I_{DDIL}		1.5	3.0	mA	V_{DD1} = 5.5 V, V_I = 0 V
Logic High Input Supply Current	I_{DDIH}		6.0	10.0	mA	V_{DD1} = 5.5 V, V_I = V_{DDI}
Input Supply Current	I_{DDI}			13.0	mA	V_{DD1} = 5.5 V
Output Supply Current	I_{DD2}		5.5	10.0	mA	V_{DD2} = 5.5 V
Input Current	I_I	-10		10	µA	
Logic High Output Voltage	V_{OH}	V_{DD2} - 0.1	V_{DD2}		V	I_O = -20 µA, V_I = V_{IH}
		0.8 *V_{DD2}	4.5			I_O = -4 mA, V_I = V_{IH}
Logic Low Output Voltage	V_{OL}		0	0.1	V	I_O = 20 µA, V_I = V_{IL}
			0.2	0.8		I_O = 4 mA, V_I = V_{IL}
Switching Specifications						
Propagation Delay Time to Logic Low Output	t_{PHL}		20	40	ns	C_L = 15 pF CMOS Signal Levels
Propagation Delay Time to Logic High Output	t_{PLH}		23	40		
Pulse Width	PW	80				
Data Rate				12.5	MBd	
Pulse Width Distortion $\lvert t_{PHL} - t_{PLH} \rvert$	PWD		3	8	ns	C_L = 15 pF CMOS Signal Levels
Propagation Delay Skew	t_{PSK}			20		
Output Rise Time (10 - 90%)	t_R		13			C_L = 15 pF CMOS Signal Levels
Output Fall Time (90 - 10%)	t_F		5			
Common Mode Transient Immunity at Logic High Output	$\lvert CM_H \rvert$	10	20		kV/µs	V_I = V_{DDI}, V_O > 0.8 V_{DDI}, V_{CM} = 1000 V
Common Mode Transient Immunity at Logic Low Output	$\lvert CM_L \rvert$	10	20			V_I = 0 V, V_O > 0.8 V, V_{CM} = 1000 V
Input Dynamic Power Dissipation Capacitance	C_{PD1}		60		pF	
Output Dynamic Power Dissipation Capacitance	C_{PD2}		10			

HEWLETT® PACKARD

High-Linearity Analog Optocouplers

Technical Data

HCNR200
HCNR201

Features

- **Low Nonlinearity: 0.01%**
- **K_3 (I_{PD2}/I_{PD1}) Transfer Gain**
  HCNR200: ± 15%
  HCNR201: ± 5%
- **Low Gain Temperature Coefficient: -65 ppm/°C**
- **Wide Bandwidth – DC to >1 MHz**
- **Worldwide Safety Approval**
  - UL 1577 Recognized (5 kV rms/1 min Rating)
  - CSA Approved
  - BSI Certified
  - VDE 0884 Approved
    V_{IORM} = 1414 V peak
    (Option #050)
- **Surface Mount Option Available**
  (Option #300)
- **8-Pin DIP Package - 0.400" Spacing**
- **Allows Flexible Circuit Design**
- **Special Selection for HCNR201: Tighter K_1, K_3 and Lower Nonlinearity Available**

Applications

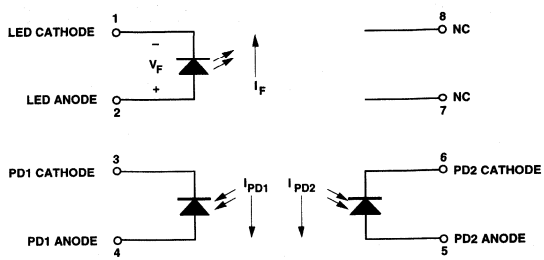
- **Low Cost Analog Isolation**
- **Telecom: Modem, PBX**
- **Industrial Process Control:**
  Transducer Isolator
  Isolator for Thermocouples
  4 mA to 20 mA Loop Isolation
- **SMPS Feedback Loop, SMPS Feedforward**
- **Monitor Motor Supply Voltage**
- **Medical**

Description

The HCNR200/201 high-linearity analog optocoupler consists of a high-performance AlGaAs LED that illuminates two closely matched photodiodes. The input photodiode can be used to monitor, and therefore stabilize, the light output of the LED. As a result, the nonlinearity and drift characteristics of the LED can be virtually eliminated. The output photodiode produces a photocurrent that is linearly related to the light output of the LED. The close matching of the photodiodes and advanced design of the package ensure the high linearity and stable gain characteristics of the optocoupler.

The HCNR200/201 can be used to isolate analog signals in a wide variety of applications that require good stability, linearity, bandwidth and low cost. The HCNR200/201 is very flexible and, by appropriate design of the application circuit, is capable of operating in many different modes, including: unipolar/bipolar, ac/dc and inverting/non-inverting. The HCNR200/201 is an excellent solution for many analog isolation problems.

Schematic



CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

5965-3577E

Ordering Information:

HCNR20x

- 0 = ± 15% Transfer Gain, 0.25% Maximum Nonlinearity
- 1 = ± 5% Transfer Gain, 0.05% Maximum Nonlinearity

Option yyy

- 050 = VDE 0884 V_{IORM} = 1414 V peak Option
- 300 = Gull Wing Surface Mount Lead Option
- 500 = Tape/Reel Package Option (1 k min.)

Option data sheets available. Contact your Hewlett-Packard sales representative or authorized distributor for information.

Package Outline Drawings

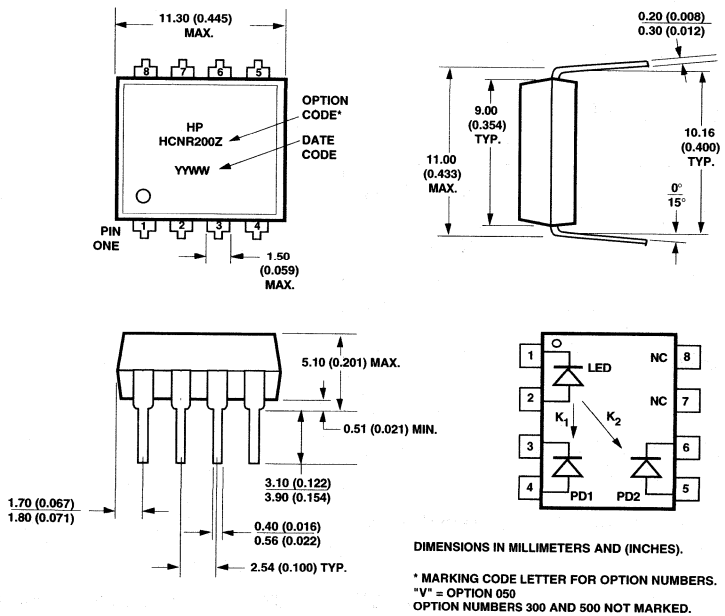
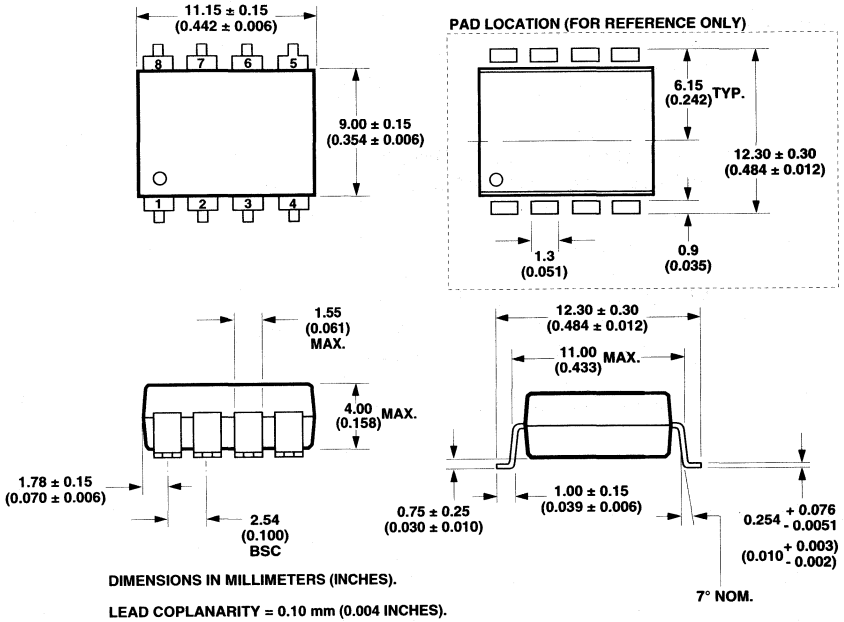
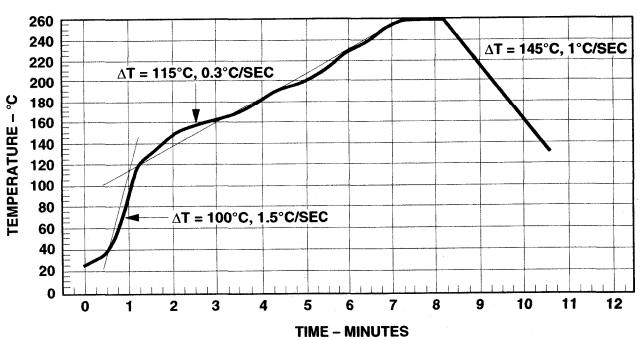


Figure 1.

Gull Wing Surface Mount Option #300



Maximum Solder Reflow Thermal Profile



(NOTE: USE OF NON-CHLORINE ACTIVATED FLUXES IS RECOMMENDED.)

Regulatory Information

The HCNR200/201 optocoupler features a 0.400" wide, eight pin DIP package. This package was specifically designed to meet worldwide regulatory requirements. The HCNR200/201 has been approved by the following organizations:

UL	Recognized under UL 1577, Component Recognition Program, FILE E55361
CSA	Approved under CSA Component Acceptance Notice #5, File CA 88324
BSI	Certification according to BS415:1994; (BS EN60065:1994); BS EN60950:1992 (BS7002:1992) and EN41003:1993 for Class II applications
VDE	Approved according to VDE 0884/06.92 (Available Option #050 only)

Insulation and Safety Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min. External Clearance (External Air Gap)	L(IO1)	9.6	mm	Measured from input terminals to output terminals, shortest distance through air
Min. External Creepage (External Tracking Path)	L(IO2)	10.0	mm	Measured from input terminals to output terminals, shortest distance path along body
Min. Internal Clearance (Internal Plastic Gap)		1.0	mm	Through insulation distance conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity
Min. Internal Creepage (Internal Tracking Path)		4.0	mm	The shortest distance around the border between two different insulating materials measured between the emitter and detector
Comparative Tracking Index	CTI	200	V	DIN IEC 112/VDE 0303 PART 1
Isolation Group		IIIa		Material group (DIN VDE 0110)

Option 300 – surface mount classification is Class A in accordance with CECC 00802.

VDE 0884 (06.92) Insulation Characteristics (Option #050 Only)

Description	Symbol	Characteristic	Unit
Installation classification per DIN VDE 0110/1.89, Table 1			
For rated mains voltage ≤ 600 V rms		I-IV	
For rated mains voltage ≤ 1000 V rms		I-III	
Climatic Classification (DIN IEC 68 part 1)		55/100/21	
Pollution Degree (DIN VDE 0110 Part 1/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	1414	V peak
Input to Output Test Voltage, Method b* V_{PR} = 1.875 x V_{IORM}, 100% Production Test with t_m = 1 sec, Partial Discharge < 5 pC	V_{PR}	2651	V peak
Input to Output Test Voltage, Method a* V_{PR} = 1.5 x V_{IORM}, Type and sample test, t_m = 60 sec, Partial Discharge < 5 pC	V_{PR}	2121	V peak
Highest Allowable Overvoltage* (Transient Overvoltage, t_{ini} = 10 sec)	V_{IOTM}	8000	V peak
Safety-Limiting Values (Maximum values allowed in the event of a failure, also see Figure 11)			
Case Temperature	T_S	150	°C
Current (Input Current I_F, P_S = 0)	I_S	400	mA
Output Power	$P_{S,OUTPUT}$	700	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	$>10^9$	Ω

*Refer to the front of the Optocoupler section of the current catalog for a more detailed description of VDE 0884 and other product safety regulations.

Note: Optocouplers providing safe electrical separation per VDE 0884 do so only within the safety-limiting values to which they are qualified. Protective cut-out switches must be used to ensure that the safety limits are not exceeded.

Absolute Maximum Ratings

Storage Temperature ..... -55°C to +125°C
Operating Temperature (T_A) ..... -55°C to +100°C
Junction Temperature (T_J) ..... 125°C
Reflow Temperature Profile ... See **Package Outline Drawings** Section
Lead Solder Temperature ..... 260°C for 10s
(up to seating plane)
Average Input Current - I_F ..... 25 mA
Peak Input Current - I_F ..... 40 mA
(50 ns maximum pulse width)
Reverse Input Voltage - V_R ..... 2.5 V
(I_R = 100 µA, Pin 1-2)
Input Power Dissipation ..... 60 mW @ T_A = 85°C
(Derate at 2.2 mW/°C for operating temperatures above 85°C)
Reverse Output Photodiode Voltage ..... 30 V
(Pin 6-5)
Reverse Input Photodiode Voltage ..... 30 V
(Pin 3-4)

Recommended Operating Conditions

Storage Temperature ..... -40°C to +85°C
Operating Temperature ..... -40°C to +85°C
Average Input Current - I_F ..... 1 - 20 mA
Peak Input Current - I_F ..... 35 mA
(50% duty cycle, 1 ms pulse width)
Reverse Output Photodiode Voltage ..... 0 - 15 V
(Pin 6-5)
Reverse Input Photodiode Voltage ..... 0 - 15 V
(Pin 3-4)

Electrical Specifications

T_A = 25°C unless otherwise specified.

Parameter	Symbol	Device	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Transfer Gain	K_3	HCNR200	0.85	1.00	1.15		5 nA < I_{PD} < 50 µA, 0 V < V_{PD} < 15 V	2,3	1
		HCNR201	0.95	1.00	1.05		5 nA < I_{PD} < 50 µA, 0 V < V_{PD} < 15 V		1,2
		HCNR201	0.93	1.00	1.07		-40°C < T_A < 85°C, 5 nA < I_{PD} < 50 µA, 0 V < V_{PD} < 15 V		1,2
Temperature Coefficient of Transfer Gain	$\Delta K_3/\Delta T_A$			-65		ppm/°C	-40°C < T_A < 85°C, 5 nA < I_{PD} < 50 µA, 0 V < V_{PD} < 15 V	2,3	
DC NonLinearity (Best Fit)	NL_{BF}	HCNR200		0.01	0.25	%	5 nA < I_{PD} < 50 µA, 0 V < V_{PD} < 15 V	4,5, 6	3
		HCNR201		0.01	0.05		5 nA < I_{PD} < 50 µA, 0 V < V_{PD} < 15 V		2,3
		HCNR201		0.01	0.07		-40°C < T_A < 85°C, 5 nA < I_{PD} < 50 µA, 0 V < V_{PD} < 15 V		2,3
DC Nonlinearity (Ends Fit)	NL_{EF}			0.016			5 nA < I_{PD} < 50 µA, 0 V < V_{PD} < 15 V		4
Input Photodiode Current Transfer Ratio (I_{PD1}/I_F)	K_1	HCNR200	0.25	0.50	0.75	%	I_F = 10 mA, 0 V < V_{PD1} < 15 V	7	2
		HCNR201	0.36	0.48	0.72				
Temperature Coefficient of K_1	$\Delta K_1/\Delta T_A$			-0.3		%/°C	-40°C < T_A < 85°C, I_F = 10 mA 0 V < V_{PD1} < 15 V	7	
Photodiode Leakage Current	I_{LK}			0.5	25	nA	I_F = 0 mA, 0 V < V_{PD} < 15 V	8	
Photodiode Reverse Breakdown Voltage	BV_{RPD}		30	150		V	I_R = 100 µA		
Photodiode Capacitance	C_{PD}			22		pF	V_{PD} = 0 V		
LED Forward Voltage	V_F		1.3	1.6	1.85	V	I_F = 10 mA	9, 10	
			1.2	1.6	1.95		I_F = 10 mA, -40°C < T_A < 85°C		
LED Reverse Breakdown Voltage	BV_R		2.5	9		V	I_F = 100 µA		
Temperature Coefficient of Forward Voltage	$\Delta V_F/\Delta T_A$			-1.7		mV/°C	I_F = 10 mA		
LED Junction Capacitance	C_{LED}			80		pF	f = 1 MHz, V_F = 0 V		

AC Electrical Specifications

T_A = 25°C unless otherwise specified.

Parameter	Symbol	Device	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
LED Bandwidth	f -3dB			9		MHz	I_F = 10 mA		
Application Circuit Bandwidth:									
High Speed				1.5		MHz		16	7
High Precision				10		kHz		17	7
Application Circuit: IMRR									
High Speed				95		dB	freq = 60 Hz	16	7, 8

Package Characteristics

T_A = 25°C unless otherwise specified.

Parameter	Symbol	Device	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary-Withstand Voltage*	V_{ISO}		5000			V rms	RH ≤ 50%, t = 1 min.		5, 6
Resistance (Input-Output)	R_{I-O}		10^{12}	10^{13}		Ω	V_O = 500 VDC		5
			10^{11}				TA = 100°C, V_{IO} = 500 VDC		5
Capacitance (Input-Output)	C_{I-O}			0.4	0.6	pF	f = 1 MHz		5

*The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the VDE 0884 Insulation Characteristics Table (if applicable), your equipment level safety specification, or HP Application Note 1074, "Optocoupler Input-Output Endurance Voltage."

Notes:

1. K_3 is calculated from the slope of the best fit line of I_{PD2} vs. I_{PD1} with eleven equally distributed data points from 5 nA to 50 µA. This is approximately equal to I_{PD2}/I_{PD1} at I_F = 10 mA.
2. Special selection for tighter K_1, K_3 and lower Nonlinearity available.
3. BEST FIT DC NONLINEARITY (NL_{BF}) is the maximum deviation expressed as a percentage of the full scale output of a "best fit" straight line from a graph of I_{PD2} vs. I_{PD1} with eleven equally distributed data points from 5 nA to 50 µA. I_{PD2} error to best fit line is the deviation below and above the best fit line, expressed as a percentage of the full scale output.
4. ENDS FIT DC NONLINEARITY (NL_{EF}) is the maximum deviation expressed as a percentage of full scale output of a straight line from the 5 nA to the 50 µA data point on the graph of I_{PD2} vs. I_{PD1}.
5. Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and pins 5, 6, 7, and 8 shorted together.
6. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage of ≥ 6000 V rms for ≥ 1 second (leakage detection current limit, I_{I-O} of 5 µA max.). This test is performed before the 100% production test for partial discharge (method b) shown in the VDE 0884 Insulation Characteristics Table (for Option #050 only).
7. Specific performance will depend on circuit topology and components.
8. IMRR is defined as the ratio of the signal gain (with signal applied to V_{IN} of Figure 16) to the isolation mode gain (with V_{IN} connected to input common and the signal applied between the input and output commons) at 60 Hz, expressed in dB.

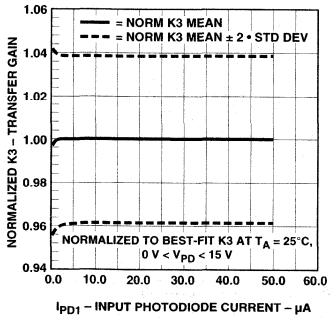


Figure 2. Normalized K3 vs. Input I_{PD}.

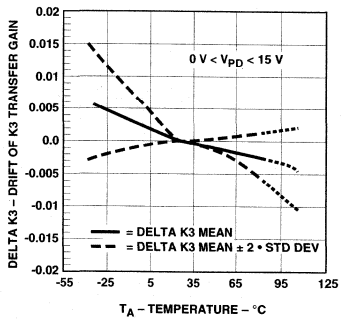


Figure 3. K3 Drift vs. Temperature.

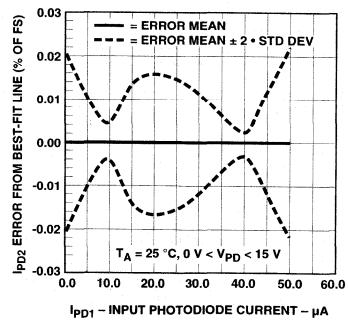


Figure 4. I_{PD2} Error vs. Input I_{PD} (See Note 4).

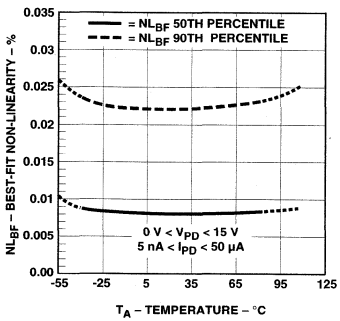


Figure 5. NL_{BF} vs. Temperature.

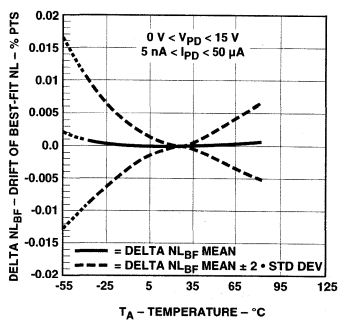


Figure 6. NL_{BF} Drift vs. Temperature.

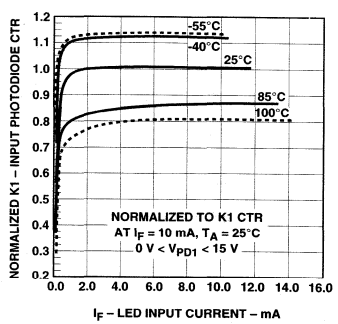


Figure 7. Input Photodiode CTR vs. LED Input Current.

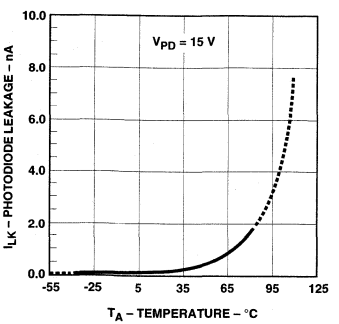


Figure 8. Typical Photodiode Leakage vs. Temperature.

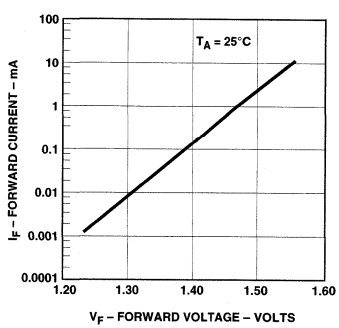


Figure 9. LED Input Current vs. Forward Voltage.

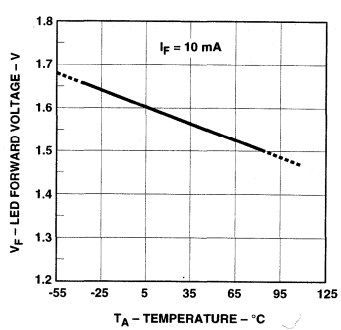


Figure 10. LED Forward Voltage vs. Temperature.

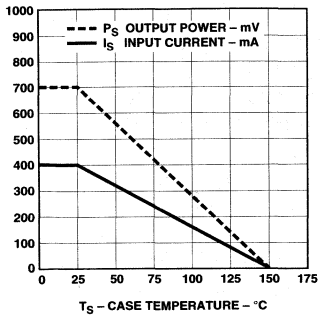


Figure 11. Thermal Derating Curve Dependence of Safety Limiting Value with Case Temperature per VDE 0884.

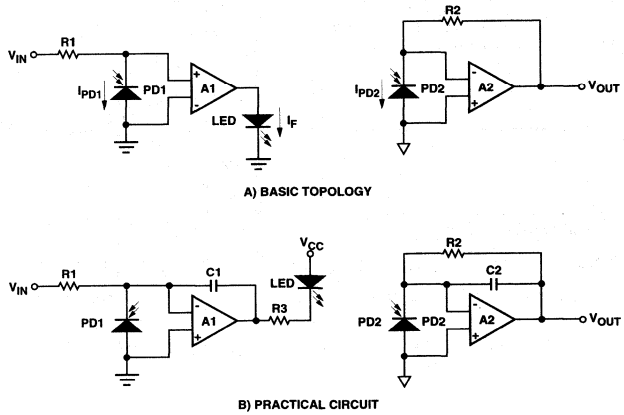


Figure 12. Basic Isolation Amplifier.

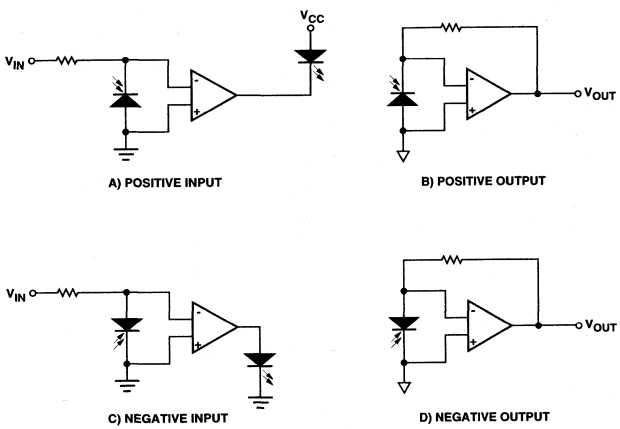


Figure 13. Unipolar Circuit Topologies.

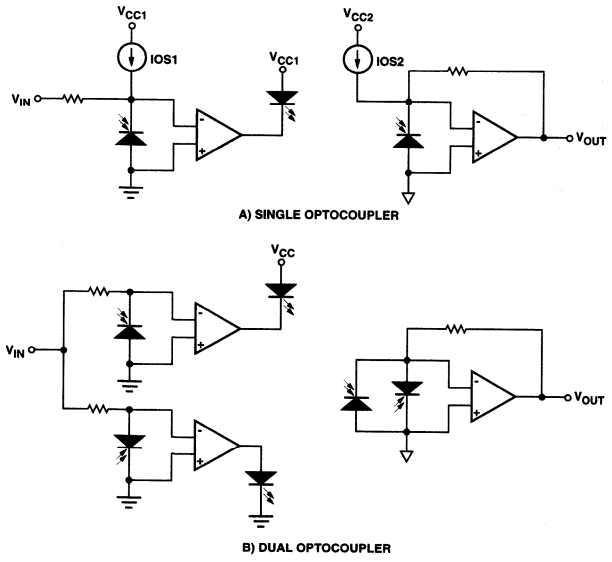


Figure 14. Bipolar Circuit Topologies.

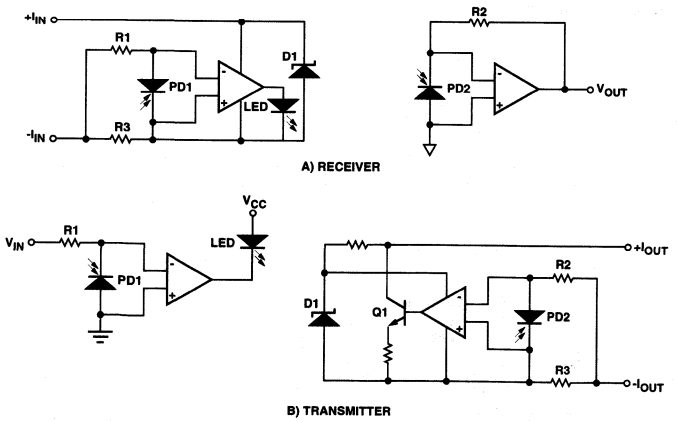


Figure 15. Loop-Powered 4-20 mA Current Loop Circuits.

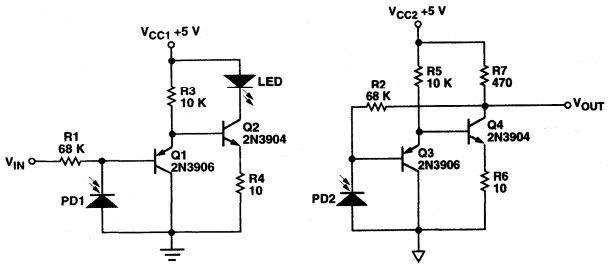


Figure 16. High-Speed Low-Cost Analog Isolator.

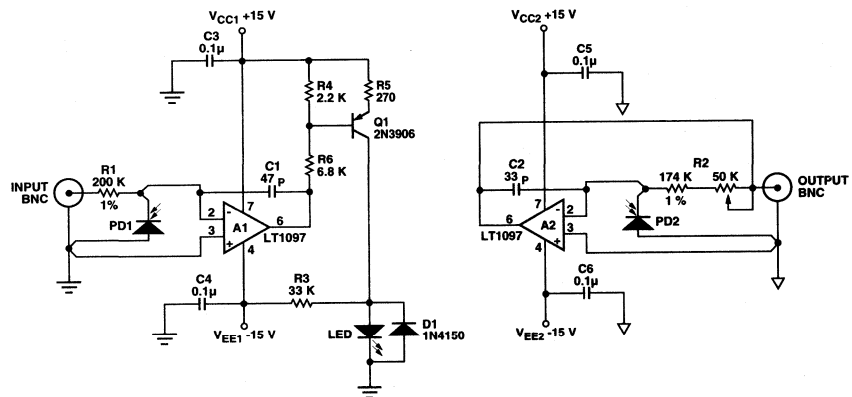


Figure 17. Precision Analog Isolation Amplifier.

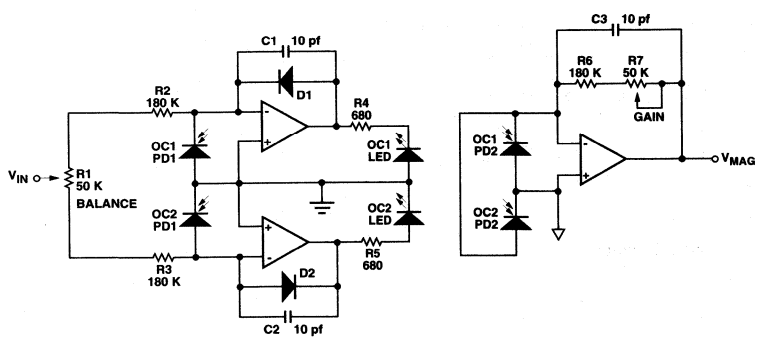


Figure 18. Bipolar Isolation Amplifier.

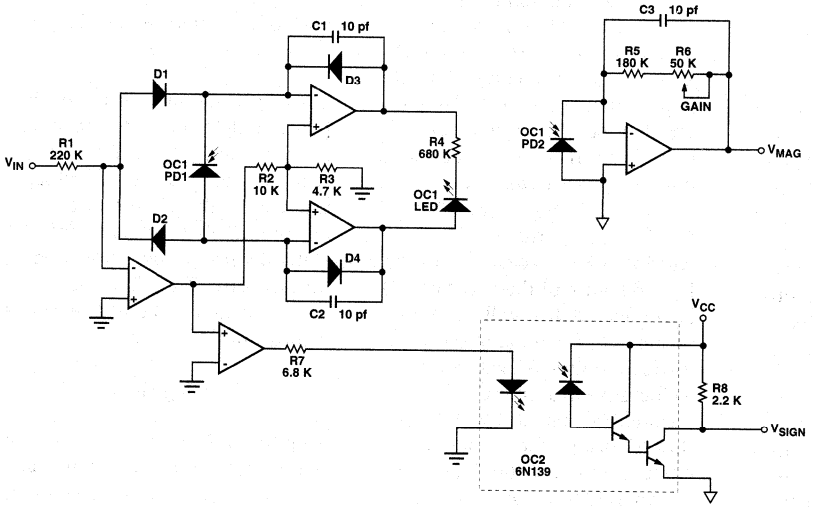


Figure 19. Magnitude/Sign Isolation Amplifier.

```
*HCNR200 Linear Optocoupler SPICE Model
*                LED Cathode
*                | LED Anode
*                | | PD1 Cathode
*                | | | PD1 Anode
*                | | | | PD2 Anode
*                | | | | | PD2 Cathode
*                | | | | | |
.SUBCKT HCNR200  1 2 3 4 5 6

* LED circuit
QLED1 8 2 7 QCPL .5
QLED2 9 2 7 QCPL .5
VLED 7 1 DC .685
VPD1 8 1 DC 2
VPD2 9 1 DC 2

* Input photodiode circuit
DPD1 4 3 DPHOTO
FPD1 3 4 VPD1 -1
CPD1 4 3 8P

* Output photodiode circuit
DPD2 5 6 DPHOTO
FPD2 6 5 VPD2 -1
CPD2 5 6 8P

* Photodiode model
.MODEL DPHOTO D(IS=4.5E-12 RS=150 N=1.3 XTI=4 EG=1.11
+  CJO=14P M=1.96 VJ=1.9)

* LED/Optical-coupling transistor model
.model QCPL NPN(IS=2.214E-19 BF=10m NF=1.010 IKF=11.00m ISE=1.167P
+  NE=1.737 RB=3.469 VAF=100 TF=1.77U CJE=80P)

.ENDS
```

Figure 20. SPICE Model Listing.

Theory of Operation

Figure 1 illustrates how the HCNR200/201 high-linearity optocoupler is configured. The basic optocoupler consists of an LED and two photodiodes. The LED and one of the photodiodes (PD1) is on the input leadframe and the other photodiode (PD2) is on the output leadframe. The package of the optocoupler is constructed so that each photodiode receives approximately the same amount of light from the LED.

An external feedback amplifier can be used with PD1 to monitor the light output of the LED and automatically adjust the LED current to compensate for any non-linearities or changes in light output of the LED. The feedback amplifier acts to stabilize and linearize the light output of the LED. The output photodiode then converts the stable, linear light output of the LED into a current, which can then be converted back into a voltage by another amplifier.

Figure 12a illustrates the basic circuit topology for implementing a simple isolation amplifier using the HCNR200/201 optocoupler. Besides the optocoupler, two external op-amps and two resistors are required. This simple circuit is actually a bit too simple to function properly in an actual circuit, but it is quite useful for explaining how the basic isolation amplifier circuit works (a few more components and a circuit change are required to make a practical circuit, like the one shown in Figure 12b).

The operation of the basic circuit may not be immediately obvious just from inspecting Figure 12a, particularly the input part of the circuit. Stated briefly, amplifier A1 adjusts the LED current (I_F), and therefore the current in PD1 (I_{PD1}), to maintain its "+" input terminal at 0 V. For example, increasing the input voltage would tend to increase the voltage of the "+" input terminal of A1 above 0 V. A1 amplifies that increase, causing I_F to increase, as well as I_{PD1}. Because of the way that PD1 is connected, I_{PD1} will pull the "+" terminal of the op-amp back toward ground. A1 will continue to increase I_F until its "+" terminal is back at 0 V. Assuming that A1 is a perfect op-amp, no current flows into the inputs of A1; therefore, all of the current flowing through R1 will flow through PD1. Since the "+" input of A1 is at 0 V, the current through R1, and therefore I_{PD1} as well, is equal to $V_{IN}/R1$.

Essentially, amplifier A1 adjusts I_F so that

$$I_{PD1} = V_{IN}/R1.$$

Notice that I_{PD1} depends ONLY on the input voltage and the value of R1 and is independent of the light output characteristics of the LED. As the light output of the LED changes with temperature, amplifier A1 adjusts I_F to compensate and maintain a constant current in PD1. Also notice that I_{PD1} is exactly proportional to V_{IN}, giving a very linear relationship between the input voltage and the photodiode current.

The relationship between the input optical power and the output current of a photodiode is very linear. Therefore, by stabilizing and linearizing I_{PD1}, the light output of the LED is also stabilized and linearized. And since light from the LED falls on both of the photodiodes, I_{PD2} will be stabilized as well.

The physical construction of the package determines the relative amounts of light that fall on the two photodiodes and, therefore, the ratio of the photodiode currents. This results in very stable operation over time and temperature. The photodiode current ratio can be expressed as a constant, K, where

$$K = I_{PD2}/I_{PD1}.$$

Amplifier A2 and resistor R2 form a trans-resistance amplifier that converts I_{PD2} back into a voltage, V_{OUT}, where

$$V_{OUT} = I_{PD2}*R2.$$

Combining the above three equations yields an overall expression relating the output voltage to the input voltage,

$$V_{OUT}/V_{IN} = K*(R2/R1).$$

Therefore the relationship between V_{IN} and V_{OUT} is constant, linear, and independent of the light output characteristics of the LED. The gain of the basic isolation amplifier circuit can be adjusted simply by adjusting the ratio of R2 to R1. The parameter K (called K_3 in the electrical specifications) can be thought of as the gain of the optocoupler and is specified in the data sheet.

Remember, the circuit in Figure 12a is simplified in order to explain the basic circuit operation. A practical circuit, more like Figure 12b, will require a few additional components to stabilize the input part of the circuit, to limit the LED current, or to

optimize circuit performance. Example application circuits will be discussed later in the data sheet.

Circuit Design Flexibility

Circuit design with the HCNR200/201 is very flexible because the LED and both photodiodes are accessible to the designer. This allows the designer to make performance trade-offs that would otherwise be difficult to make with commercially available isolation amplifiers (e.g., bandwidth vs. accuracy vs. cost). Analog isolation circuits can be designed for applications that have either unipolar (e.g., 0-10 V) or bipolar (e.g., ± 10 V) signals, with positive or negative input or output voltages. Several simplified circuit topologies illustrating the design flexibility of the HCNR200/201 are discussed below.

The circuit in Figure 12a is configured to be non-inverting with positive input and output voltages. By simply changing the polarity of one or both of the photodiodes, the LED, or the op-amp inputs, it is possible to implement other circuit configurations as well. Figure 13 illustrates how to change the basic circuit to accommodate both positive and negative input and output voltages. The input and output circuits can be matched to achieve any combination of positive and negative voltages, allowing for both inverting and non-inverting circuits.

All of the configurations described above are unipolar (single polarity); the circuits cannot accommodate a signal that might swing both positive and negative. It is possible, however, to use the HCNR200/201 optocoupler to implement a bipolar isolation amplifier. Two topologies that allow for bipolar operation are shown in Figure 14.

The circuit in Figure 14a uses two current sources to offset the signal so that it appears to be unipolar to the optocoupler. Current source I_{OS1} provides enough offset to ensure that I_{PD1} is always positive. The second current source, I_{OS2}, provides an offset of opposite polarity to obtain a net circuit offset of zero. Current sources I_{OS1} and I_{OS2} can be implemented simply as resistors connected to suitable voltage sources.

The circuit in Figure 14b uses two optocouplers to obtain bipolar operation. The first optocoupler handles the positive voltage excursions, while the second optocoupler handles the negative ones. The output photodiodes are connected in an antiparallel configuration so that they produce output signals of opposite polarity.

The first circuit has the obvious advantage of requiring only one optocoupler; however, the offset performance of the circuit is dependent on the matching of I_{OS1} and I_{OS2} and is also dependent on the gain of the optocoupler. Changes in the gain of the optocoupler will directly affect the offset of the circuit.

The offset performance of the second circuit, on the other hand, is much more stable; it is independent of optocoupler gain and has no matched current sources to worry about. However, the second circuit requires two optocouplers, separate gain adjustments for the positive and negative portions of the signal, and can exhibit crossover distortion near zero volts. The correct circuit to choose for an application would depend on the requirements of that particular application. As with the basic isolation amplifier circuit in Figure 12a, the circuits in Figure 14 are simplified and would require a few additional components to function properly. Two example circuits that operate with bipolar input signals are discussed in the next section.

As a final example of circuit design flexibility, the simplified schematics in Figure 15 illustrate how to implement 4-20 mA analog current-loop transmitter and receiver circuits using the HCNR200/201 optocoupler. An important feature of these circuits is that the loop side of the circuit is powered entirely by the loop current, eliminating the need for an isolated power supply.

The input and output circuits in Figure 15a are the same as the negative input and positive output circuits shown in Figures 13c and 13b, except for the addition of R3 and zener diode D1 on the input side of the circuit. D1 regulates the supply voltage for the input amplifier, while R3 forms a current divider with R1 to scale the loop current down from 20 mA to an appropriate level for the input circuit (<50 μA).

As in the simpler circuits, the input amplifier adjusts the LED current so that both of its input terminals are at the same voltage. The loop current is then divided

between R1 and R3. I_{PD1} is equal to the current in R1 and is given by the following equation:

$$I_{PD1} = I_{LOOP}*R3/(R1+R3).$$

Combining the above equation with the equations used for Figure 12a yields an overall expression relating the output voltage to the loop current,

$$V_{OUT}/I_{LOOP} = K*(R2*R3)/(R1+R3).$$

Again, you can see that the relationship is constant, linear, and independent of the characteristics of the LED.

The 4-20 mA transmitter circuit in Figure 15b is a little different from the previous circuits, particularly the output circuit. The output circuit does not directly generate an output voltage which is sensed by R2, it instead uses Q1 to generate an output current which flows through R3. This output current generates a voltage across R3, which is then sensed by R2. An analysis similar to the one above yields the following expression relating output current to input voltage:

$$I_{LOOP}/V_{IN} = K*(R2+R3)/(R1*R3).$$

The preceding circuits were presented to illustrate the flexibility in designing analog isolation circuits using the HCNR200/201. The next section presents several complete schematics to illustrate practical applications of the HCNR200/201.

Example Application Circuits

The circuit shown in Figure 16 is a high-speed low-cost circuit designed for use in the feedback path of switch-mode power supplies. This application requires good bandwidth, low cost and stable gain, but does not require very high accuracy. This circuit is a good example of how a designer can trade off accuracy to achieve improvements in bandwidth and cost. The circuit has a bandwidth of about 1.5 MHz with stable gain characteristics and requires few external components.

Although it may not appear so at first glance, the circuit in Figure 16 is essentially the same as the circuit in Figure 12a. Amplifier A1 is comprised of Q1, Q2, R3 and R4, while amplifier A2 is comprised of Q3, Q4, R5, R6 and R7. The circuit operates in the same manner as well; the only difference is the performance of amplifiers A1 and A2. The lower gains, higher input currents and higher offset voltages affect the accuracy of the circuit, but not the way it operates. Because the basic circuit operation has not changed, the circuit still has good gain stability. The use of discrete transistors instead of op-amps allowed the design to trade off accuracy to achieve good bandwidth and gain stability at low cost.

To get into a little more detail about the circuit, R1 is selected to achieve an LED current of about 7-10 mA at the nominal input operating voltage according to the following equation:

$$I_F = (V_{IN}/R1)/K1,$$

where K_1 (i.e., I_{PD1}/I_F) of the optocoupler is typically about 0.5%. R2 is then selected to achieve the desired output voltage according to the equation,

$$V_{OUT}/V_{IN} = R2/R1.$$

The purpose of R4 and R6 is to improve the dynamic response (i.e., stability) of the input and output circuits by lowering the local loop gains. R3 and R5 are selected to provide enough current to drive the bases of Q2 and Q4. And R7 is selected so that Q4 operates at about the same collector current as Q2.

The next circuit, shown in Figure 17, is designed to achieve the highest possible accuracy at a reasonable cost. The high accuracy and wide dynamic range of the circuit is achieved by using low-cost precision op-amps with very low input bias currents and offset voltages and is limited by the performance of the opto-coupler. The circuit is designed to operate with input and output voltages from 1 mV to 10 V.

The circuit operates in the same way as the others. The only major differences are the two compensation capacitors and additional LED drive circuitry. In the high-speed circuit discussed above, the input and output circuits are stabilized by reducing the local loop gains of the input and output circuits. Because reducing the loop gains would decrease the accuracy of the circuit, two compensation capacitors, C1 and C2, are instead used to improve circuit stability. These capacitors also limit the bandwidth of the circuit to about 10 kHz and can be used to reduce the output noise of the circuit by reducing its bandwidth even further.

The additional LED drive circuitry (Q1 and R3 through R6) helps to maintain the accuracy and bandwidth of the circuit over the entire range of input voltages. Without these components, the transconductance of the LED driver would

decrease at low input voltages and LED currents. This would reduce the loop gain of the input circuit, reducing circuit accuracy and bandwidth. D1 prevents excessive reverse voltage from being applied to the LED when the LED turns off completely.

No offset adjustment of the circuit is necessary; the gain can be adjusted to unity by simply adjusting the 50 kohm potentiometer that is part of R2. Any OP-97 type of op-amp can be used in the circuit, such as the LT1097 from Linear Technology or the AD705 from Analog Devices, both of which offer pA bias currents, μV offset voltages and are low cost. The input terminals of the op-amps and the photodiodes are connected in the circuit using Kelvin connections to help ensure the accuracy of the circuit.

The next two circuits illustrate how the HCNR200/201 can be used with bipolar input signals. The isolation amplifier in Figure 18 is a practical implementation of the circuit shown in Figure 14b. It uses two optocouplers, OC1 and OC2; OC1 handles the positive portions of the input signal and OC2 handles the negative portions.

Diodes D1 and D2 help reduce crossover distortion by keeping both amplifiers active during both positive and negative portions of the input signal. For example, when the input signal positive, optocoupler OC1 is active while OC2 is turned off. However, the amplifier controlling OC2 is kept active by D2, allowing it to turn on OC2 more rapidly when the input signal goes negative, thereby reducing crossover distortion.

Balance control R1 adjusts the relative gain for the positive and negative portions of the input signal, gain control R7 adjusts the overall gain of the isolation amplifier, and capacitors C1-C3 provide compensation to stabilize the amplifiers.

The final circuit shown in Figure 19 isolates a bipolar analog signal using only one optocoupler and generates two output signals: an analog signal proportional to the magnitude of the input signal and a digital signal corresponding to the sign of the input signal. This circuit is especially useful for applications where the output of the circuit is going to be applied to an analog-to-digital converter. The primary advantages of this circuit are very good linearity and offset, with only a single gain adjustment and no offset or balance adjustments.

To achieve very high linearity for bipolar signals, the gain should be exactly the same for both positive and negative input polarities. This circuit achieves excellent linearity by using a single optocoupler and a single input resistor, which guarantees identical gain for both positive and negative polarities of the input signal. This precise matching of gain for both polarities is much more difficult to obtain when separate components are used for the different input polarities, such as is the previous circuit.

The circuit in Figure 19 is actually very similar to the previous circuit. As mentioned above, only one optocoupler is used. Because a photodiode can conduct current in only one direction, two diodes (D1 and D2) are used to steer the input current to the appropriate terminal of input photodiode PD1 to allow bipolar input currents. Normally the forward voltage drops of the diodes would cause a serious linearity or accuracy problem. However, an additional amplifier is used to provide an appropriate offset voltage to the other amplifiers that exactly cancels the diode voltage drops to maintain circuit accuracy.

Diodes D3 and D4 perform two different functions; the diodes keep their respective amplifiers active independent of the input signal polarity (as in the previous circuit), and they also provide the feedback signal to PD1 that cancels the voltage drops of diodes D1 and D2.

Either a comparator or an extra op-amp can be used to sense the polarity of the input signal and drive an inexpensive digital optocoupler, like a 6N139.

It is also possible to convert this circuit into a fully bipolar circuit (with a bipolar output signal) by using the output of the 6N139 to drive some CMOS switches to switch the polarity of PD2 depending on the polarity of the input signal, obtaining a bipolar output voltage swing.

HCNR200/201 SPICE Model

Figure 20 is the net list of a SPICE macro-model for the HCNR200/201 high-linearity optocoupler. The macro-model accurately reflects the primary characteristics of the HCNR200/201 and should facilitate the design and understanding of circuits using the HCNR200/201 optocoupler.

HEWLETT® PACKARD

High Gain Darlington Output Optocouplers

Technical Data

4N45
4N46

Features

- **High Current Transfer Ratio–1500% Typical**
- **Low Input Current Requirement–0.5 mA**
- **Performance Guaranteed over 0°C to 70°C Temperature Range**
- **Internal Base-Emitter Resistor Minimizes Output Leakage**
- **Gain-Bandwidth Adjustment Pin**
- **Safety Approval**
  UL Recognized -2500 V rms for 1 Minute
  CSA Approved

Applications

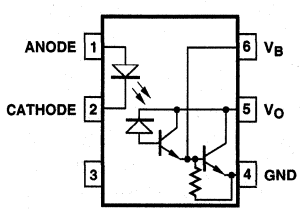
- **Telephone Ring Detector**
- **Digital Logic Ground Isolation**
- **Low Input Current Line Receiver**
- **Line Voltage Status Indicator–Low Input Power Dissipation**
- **Logic to Reed Relay Interface**
- **Level Shifting**
- **Interface Between Logic Families**

Description

The 4N45/46 optocouplers contain a GaAsP light emitting diode optically coupled to a high gain photodetector IC.

The excellent performance over temperature results from the inclusion of an integrated emitter-base bypass resistor which shunts photodiode and first stage leakage currents as well as bleeding off excess base drive to ground. External access to the second stage base provides the capability for better noise rejection than a conventional photodarlington detector. An external resistor or capacitor at the base can be added to make a gain-bandwidth or input current threshold adjustment. The base lead can also be used for feedback.

Functional Diagram



The high current transfer ratio at very low input currents permits circuit designs in which adequate margin can be allowed for the effects of optical coupling variations.

The 4N46 has a 350% minimum CTR at an input current of only 0.5 mA making it ideal for use in low input current applications such as MOS, CMOS and low power logic interfacing. Compatibility with high voltage CMOS logic systems is assured by the 20 V minimum breakdown voltage of the output transistor and by the guaranteed maximum output leakage (I_{OH}) at 18 V.

The 4N45 has a 250% minimum CTR at 1.0 mA input current and a 7 V minimum breakdown voltage rating.

Selection for lower input current down to 250 μA is available upon request.

TRUTH TABLE (POSITIVE LOGIC)

LED	OUTPUT
ON	L
OFF	H

*JEDEC Registered Data
**JEDEC Registered up to 70°C.

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Ordering Information

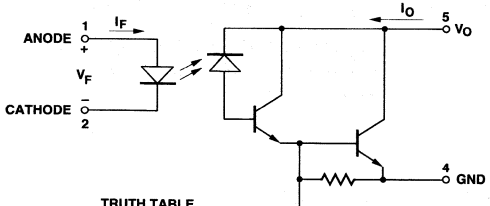
Specify part number followed by Option Number (if desired).

4N45#XXX

- 300 = Gull Wing Surface Mount Lead Option
- 500 = Tape/Reel Package Option (1 K min)

Option data sheets available. Contact your Hewlett-Packard sales representative or authorized distributor for information.

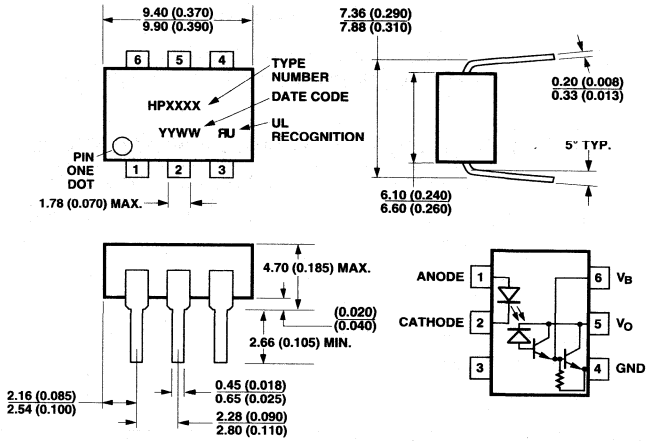
Schematic



TRUTH TABLE (POSITIVE LOGIC)

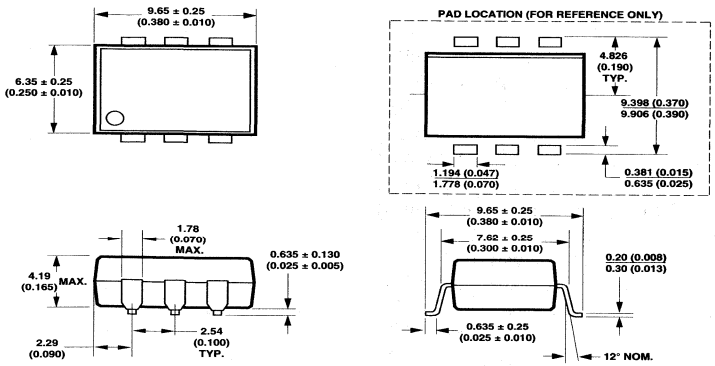
LED	OUTPUT
ON	L
OFF	H

Outline Drawing



DIMENSIONS IN MILLIMETERS AND (INCHES).

Outline Drawing – Option 300



DIMENSIONS IN mm (INCHES)
TOLERANCES: xx.xx = 0.01
xx.xxx = 0.001
(unless otherwise specified)

LEAD COPLANARITY [3] [5]
MAXIMUM: 0.102 (0.004)

Thermal Profile (Option #300)

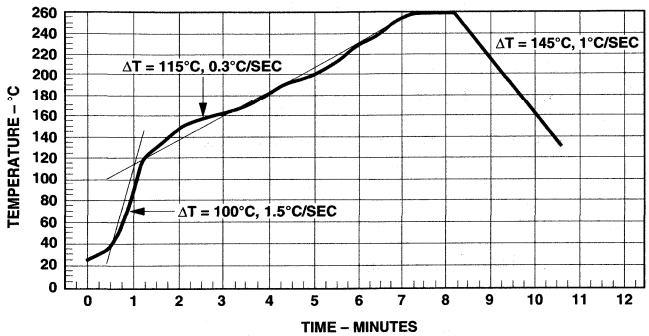


Figure 1. Maximum Solder Reflow Thermal Profile.
(Note: Use of non-chlorine activated fluxes is recommended.)

Regulatory Information

The 4N45 and 4N46 have been approved by the following regulatory organizations:

UL

Recognized under UL 1577, Component Recognition Program, File E55361.

CSA

Approved under CSA Component Acceptance Notice #5, File CA 88324.

Insulation and Safety Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min. External Air Gap (External Clearance)	L(IO1)	7.1	mm	Measured from input terminals to output terminals, shortest distance through air
Min. External Tracking Path (External Creepage)	L(IO2)	7.4	mm	Measured from input terminals to output terminals, shortest distance path along body
Min. Internal Plastic Gap (Internal Clearance)		0.08	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity
Tracking Resistance (Comparative Tracking Index)	CTI	200	Volts	DIN IEC 112/VDE 0303 PART 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Option 300 – surface mount classification is Class A in accordance with CECC 00802.

Absolute Maximum Ratings

Storage Temperature, T_S ..... -55°C to +125°C
Operating Temperature, T_A ..... -40°C to +85°C
Lead Solder Temperature, max ..... 260°C for 10 s
(1.6 mm below seating plane)
Average Input Current, I_F ..... 20 mA[1]
Peak Input Current, I_F ..... 40 mA
(50% duty cycle, 1 ms pulse width)
Peak Transient Input Current, I_F ..... 1.0 A
(≤ 1 µs pulse width, 300 pps)
Reverse Input Voltage, V_R ..... 5 V
Input Power Dissipation, P_I ..... 35 mW[2]
Output Current, I_O (Pin 5) ..... 60 mA[3]
Emitter-Base Reverse Voltage (Pins 4-6) ..... 0.5 V
Output Voltage, V_O (Pin 5-4)
4N45 ..... -0.5 to 7 V
4N46 ..... -0.5 to 20 V
Output Power Dissipation ..... 100 mW[4]
Infrared and Vapor Phase Reflow Temperature
(Option #300) ..... see Fig. 1, Thermal Profile

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Output Voltage (4N46)	V_O	4.5	20	V
Output Voltage (4N45)		4.5	7	V
Input Current (High)	$I_{F(ON)}$	0.5	10	mA
Input Voltage (Low)	$V_{F(OFF)}$	0	0.8	V
Operating Temperature	T_A	0	70	°C

DC Electrical Specifications

Over recommended temperature (T_A = 0°C to 70°C), unless otherwise specified.

Parameter	Device	Symbol	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	4N46	CTR	350*	1500	3200	%	I_F = 0.5 mA, V_O = 1.0 V	3, 4, 5, 11, 12	5, 6, 8
			500*	1500	2000		I_F = 1.0 mA, V_O = 1.0 V		
			200*	600	1000		I_F = 10 mA, V_O = 1.2 V		
	4N45		250*	1200	2000	%	I_F = 1.0 mA, V_O = 1.0 V		
			200*	500	1000		I_F = 10 mA, V_O = 1.2 V		
Logic Low Output Voltage	4N46	V_{OL}		0.90	1.0	V	I_F = 0.5 mA, I_{OL} = 1.75 mA	3	6
				0.92	1.0		I_F = 1.0 mA, I_{OL} = 5.0 mA		
				0.95	1.2		I_F = 10 mA, I_{OL} = 20 mA		
	4N45			0.90	1.0	V	I_F = 1.0 mA, I_{OL} = 2.5 mA		
				0.95	1.2		I_F = 10 mA, I_{OL} = 20 mA		
Logic High Output Current	4N46	I_{OH}*		0.001	100	µA	I_F = 0 mA, V_O = 18 V		6
	4N45			0.001	250	µA	I_F = 0 mA, V_O = 5 V		
Input Forward Voltage		V_F		1.4	1.7*	V	T_A = 25°C | I_F = 1.0 mA	2	
					1.75				
Temperature Coefficient of Forward Voltage		$\frac{\Delta V_F}{\Delta T_A}$		-1.8		mV/°C	I_F = 1.0 mA		
Input Reverse Breakdown Voltage		BV_R*	5			V	I_R = 10 µA		
Input Capacitance		C_{IN}		60		pF	f = 1 MHz, V_F = 0		

Switching Specifications

(Over recommended temperature T_A = 0°C to 70°C unless otherwise specified. V_{CC} = 5.0 V.

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to Logic Low at Output	t_{PHL}		80		µs	T_A = 25°C | I_F = 0.5 mA, R_L = 10 kΩ	6, 7, 8, 9, 11, 13	6, 8
	t_{PHL}		5	50*		T_A = 25°C | I_F = 10 mA, R_L = 2.2 kΩ		
				60				
Propagation Delay Time to Logic High at Output	t_{PLH}		1500		µs	T_A = 25°C | I_F = 10 mA, R_L = 10 kΩ	6, 7, 8, 9, 11, 13	6, 8
	t_{PLH}		150	500*		T_A = 25°C | I_F = 10 mA, R_L = 220 kΩ		
				600				
Common Mode Transient Immunity at High Output Level	$\|CM_H\|$		500		V/µs	I_F = 0 mA, R_L = 10 kΩ, $\|V_{CM}\|$ = 10 V_{P-P}	10	9
Common Mode Transient Immunity at Low Output Level	$\|CM_L\|$		500		V/µs	I_F = 1.0 mA, R_L = 10 kΩ, $\|V_{CM}\|$ = 10 V_{P-P}	10	9

*JEDEC Registered Data.
**All typicals at T_A = 25°C, unless otherwise noted.

Package Characteristics

For 0°C ≤ T_A ≤ 70°C, unless otherwise specified. All typicals at T_A = 25°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Notes
Input-Output Momentary Withstand Voltage*	V_{ISO}	2500			V rms	RH ≤ 50%, t = 1 min, T_A = 25°C		7, 10
Resistance, Input-Output	R_{I-O}		10^{12}		Ω	V_{I-O} = 500 Vdc		7
Capacitance, Input-Output	C_{I-O}		0.6		pF	f = 1 MHz		7

*The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the VDE 0884 Insulation Characteristics Table (if applicable), your equipment level safety specification, or HP Application Note 1074, "Optocoupler Input-Output Endurance Voltage."

Notes:

1. Derate linearly above 50°C free-air temperature at a rate of 0.4 mA/°C.
2. Derate linearly above 50°C free-air temperature at a rate of 0.7 mW/°C.
3. Derate linearly above 25°C free-air temperature at a rate of 0.8 mA/°C.
4. Derate linearly above 25°C free-air temperature at a rate of 1.5 mW/°C.
5. DC CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
6. Pin 6 Open.
7. Device considered a two-terminal device: Pins 1, 2, 3 shorted together and Pins 4, 5, and 6 shorted together.
8. Use of a resistor between pin 4 and 6 will decrease gain and delay time. (See Figures 11, 12, and 13.)
9. Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{cm}/dt on the leading edge of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (i.e., V_O > 2.5 V). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{cm}/dt on the trailing edge of the common mode pulse signal, V_{cm}, to assure that the output will remain in a Logic Low state (i.e., V_O < 2.5 V).
10. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 3000 V rms for 1 second (leakage detection current limit, I_{I-O} ≤ 5 μA).

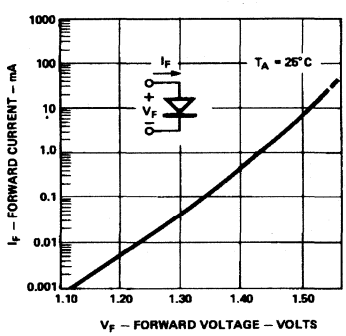


Figure 2. Input Diode Forward Current vs. Forward Voltage.

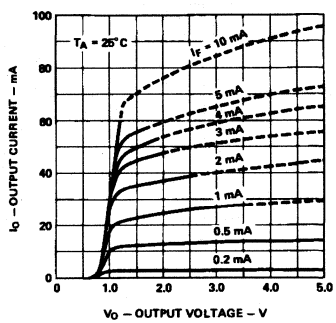


Figure 3. Typical DC Transfer Characteristics.

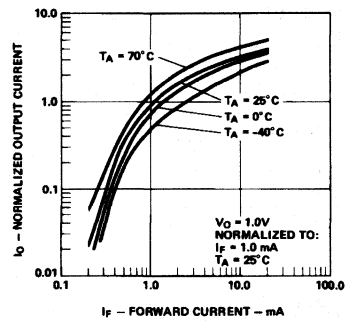


Figure 4. Output Current vs. Input Current.

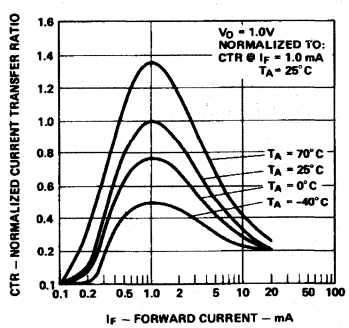


Figure 5. Current Transfer Ratio vs. Input Current.

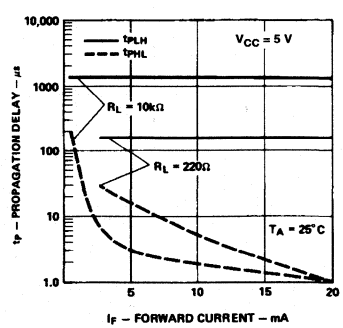


Figure 6. Propagation Delay vs. Forward Current.

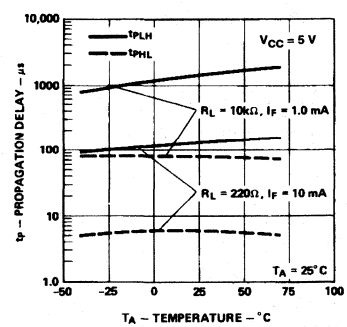


Figure 7. Propagation Delay vs. Temperature.

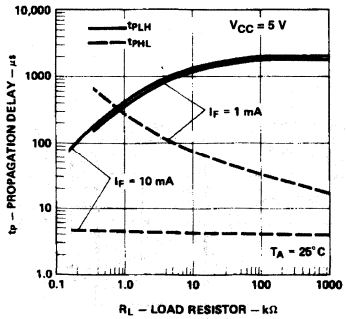


Figure 8. Propagation Delay vs. Load Resistor.

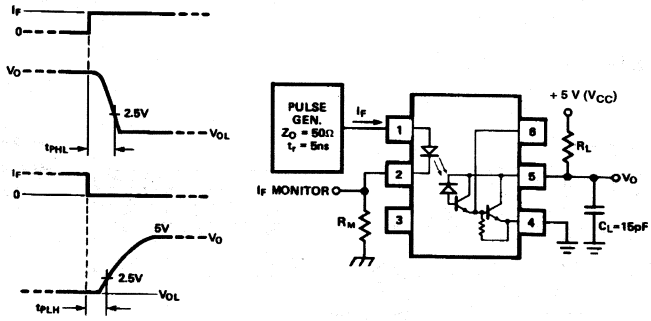
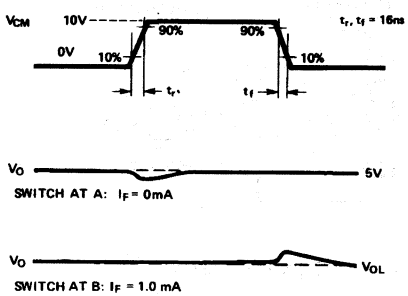


Figure 9. Switching Test Circuit.



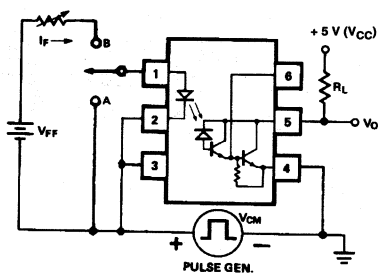


Figure 10. Test Circuit for Transient Immunity and Typical Waveforms.

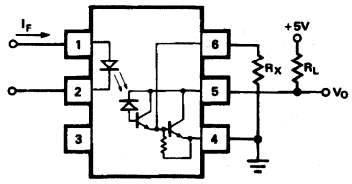


Figure 11. External Base Resistor, R_X.

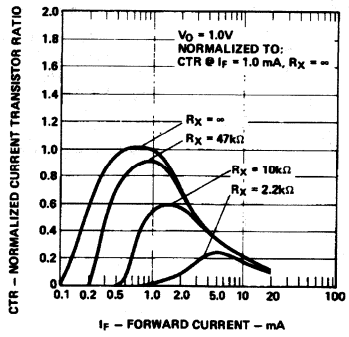


Figure 12. Effect of R_X On Current Transfer Ratio.

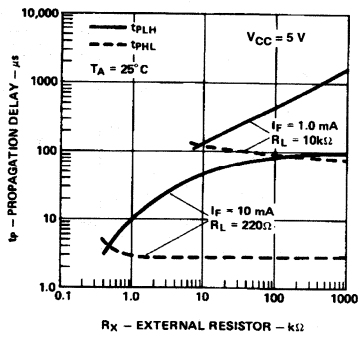
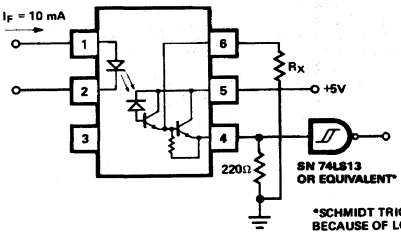


Figure 13. Effect of R_X On Propagation Delay.

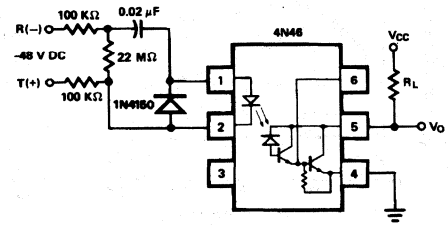
Applications



R_X (kΩ)	t_{PHL} (μs)	t_{PLH} (μs)
∞	5	320
100	5	200
47	5	140
20	6	80
10	6	45

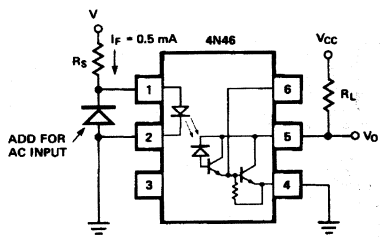
*SCHMIDT TRIGGER RECOMMENDED BECAUSE OF LONG t_r, t_f.

TTL Interface



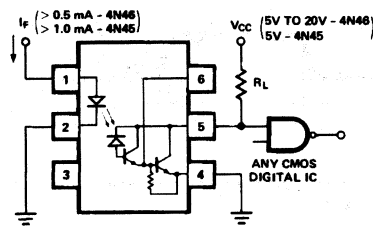
NOTE: AN INTEGRATOR MAY BE REQUIRED AT THE OUTPUT TO ELIMINATE DIALING PULSES AND LINE TRANSIENTS.

Telephone Ring Detector

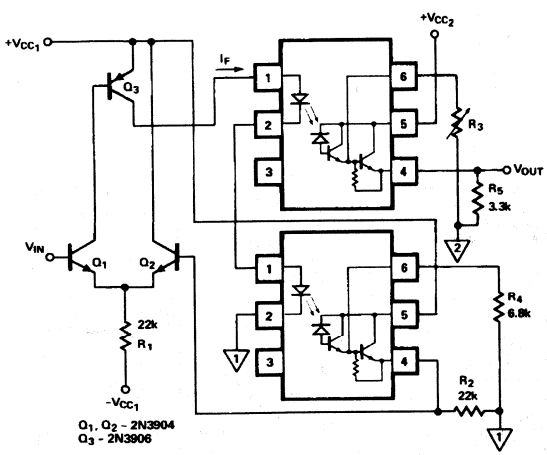


V (Vdc or Vrms)	R_S	V • I_F (mW)
24	47kΩ	11
48	100kΩ	22
115	220kΩ	62
230	470kΩ	113

Line Voltage Monitor



CMOS Interface



CHARACTERISTICS

$R_{IN} \approx 30M\Omega$, $R_{OUT} \approx 50\Omega$
$V_{IN\,(MAX.)} = V_{CC_1} - 1V$, LINEARITY BETTER THAN 5%

DESIGN COMMENTS

R_1 - NOT CRITICAL $\left(<< \frac{V_{IN\,(MAX.)} - (-V_{CC_1}) - V_{BE}}{I_{F\,(MAX.)}}\right) h_{FE}\ Q_3$

R_2 - NOT CRITICAL (OMIT IF 0.2 TO 0.3V OFFSET IS TOLERABLE)

$R_4 > \frac{V_{IN\,(MAX.)} + V_{BE}}{1\ mA}$

$R_5 > \frac{V_{IN\,(MAX.)}}{2.5\ mA}$

NOTE: ADJUST R_3 SO $V_{OUT} = V_{IN}$ AT $V_{IN} = \frac{V_{IN\,(MAX.)}}{2}$

Analog Signal Isolation

60 V/0.7 Ohm, General Purpose, 1 Form A, Solid State Relay

Technical Data

HSSR-8060

Features

- **Compact Solid-State Bidirectional Switch**
- **Normally-Off Single-Pole Relay Function (1 Form A)**
- **60 V Output Withstand Voltage in Both Polarities at 25°C**
- **0.75/1.5 Amp Current Ratings (See Schematic for Connections A & B)**
- **Low Input Current; CMOS Compatibility**
- **Very Low On-resistance: 0.4 Ω Typical at 25°C**
- **ac/dc Signal and Power Switching**
- **Input-to-Output Momentary Withstand Insulation Voltage: 2500 Vac, 1 Minute**
- **16-kV ESD Immunity: MIL-STD-883, Method 3015**
- **IEEE Surge Withstand Capability (IEEE STD 472-1974)**
- **CSA Approved**
- **UL 508 Approved**

Applications

- **Programmable Logic Controllers**
- **Telecommunication Switching Equipment**
- **Reed Relay Replacement**
- **28 Vdc, 24 Vac, 48 Vdc Load Driver**
- **Industrial Relay Coil Driver**

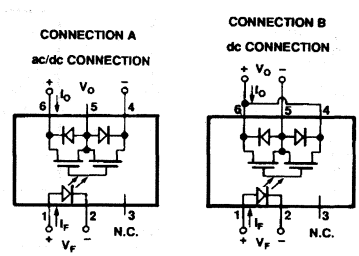
Description

The HSSR-8060 consists of a high-voltage circuit, optically coupled with a light emitting diode (LED). This device is a solid-state replacement for single-pole, normally-open (1 Form A) electromechanical relays used for general purpose switching of signals and low-power loads. The relay turns on (contact closes) with a minimum input current, I_F, of 5 mA through the input LED. The relay turns off (contact opens) with an input voltage, V_F, of 0.8 V or less. The detector contains a high speed photosensitive FET driver circuit and two high voltage MOSFETs.

This relay's logic level input control and very low typical output on-resistance of 0.4 Ω makes it suitable for both ac and dc loads. Connection A, as shown in the schematic, allows the relay to switch either ac or dc loads. Connection B, with the polarity and pin configuration as indicated in the schematic, allows the relay to switch dc loads only. The advantage of Connection B is that the on-resistance is significantly reduced, and the output current capability increases by a factor of two.

The electrical and switching characteristics of the HSSR-8060 are specified from -40°C to +85°C.

Functional Diagram



TRUTH TABLE (POSITIVE LOGIC)

LED	OUTPUT
ON	L
OFF	H

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Selection Guide

6-Pin DIP (300 Mil) Single Channel Package	4-Pin DIP (300 Mil) Dual Channel Package	Maximum Speed t(ON) msec 25°C	Maximum ON Resistance R(ON) Ω 25°C	Maximum Output Voltage VO(off) V 25°C	Maximum Output Current Io(ON) mA 25°C	Minimum Input Current mA	Hermetic 8-Pin Single Channel Packages
HSSR-8400[1]		0.95	10	400	150	5	
HSSR-8060		1.4	0.7	60	750	5	
	HSSR-8200[1]	1.5	200	200	40	1	
		6	1	90	800	5	HSSR-7110[1]

Note:
1. Technical data are on separate HP publication.

Ordering Information

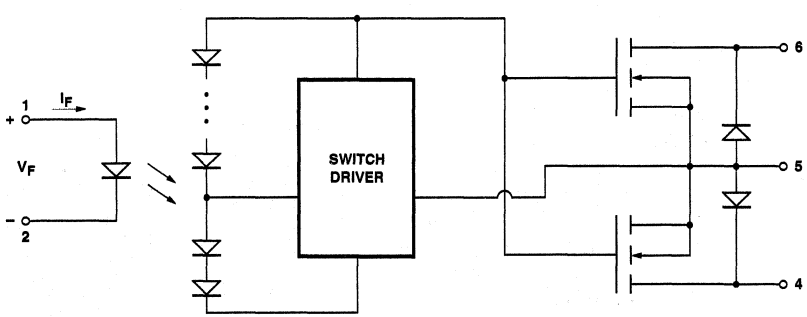
Specify part number followed by Option Number (if desired).

HSSR-8060#XXX

- 300 = Gull Wing Surface Mount Lead Option
- 500 = Tape/Reel Package Option (1 k min.)

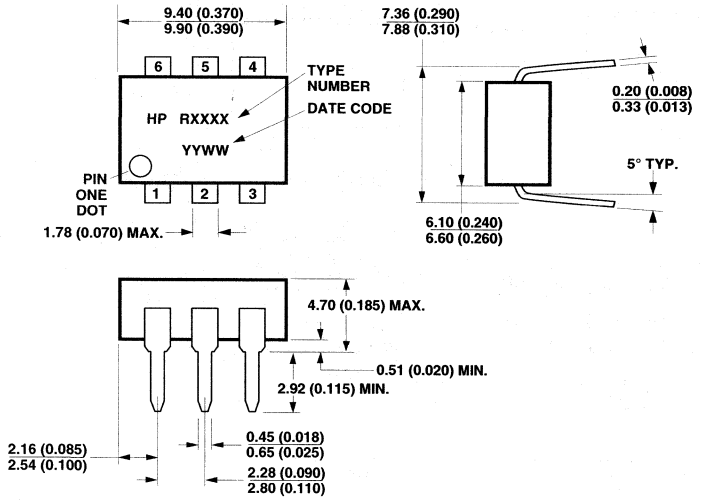
Option data sheets available. Contact your Hewlett-Packard sales representative or authorized distributor for information.

Schematic



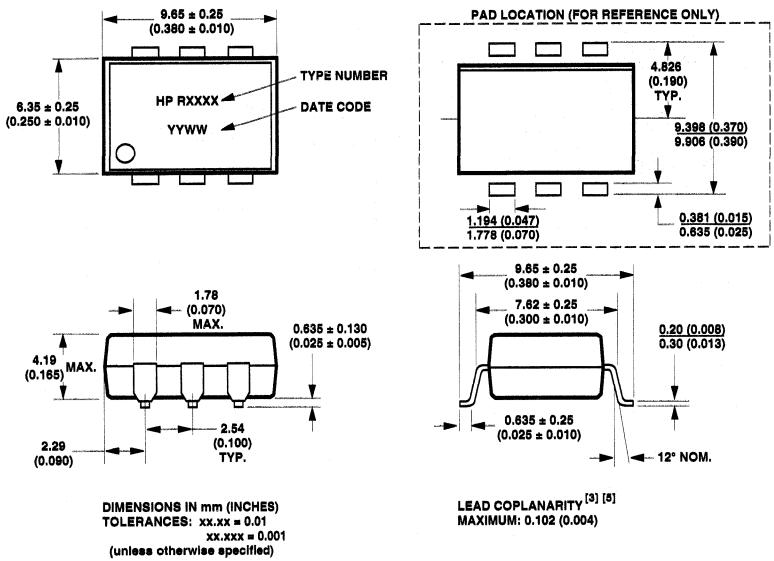
Outline Drawing

6-pin DIP Package (HSSR-8060)



DIMENSIONS IN MILLIMETERS AND (INCHES).

6-Pin Device Outline Drawing Option #300 (Gull Wing Surface Mount)



Thermal Profile (Option #300)

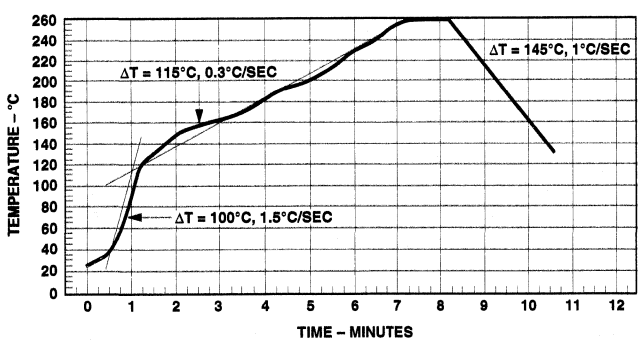


Figure 1. Maximum Solder Reflow Thermal Profile.
(Note: Use of non-chlorine activated fluxes is recommended.)

Regulatory Information

The HSSR-8060 has been approved by the following organizations:

UL

Recognized under UL 508, Component Recognition Program, Industrial Control Switches, File E142465.

CSA

Approved under CAN/CSA-C22.2 No. 14-95, Industrial Control Equipment, File LR 87683.

Insulation and Safety Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min. External Air Gap (External Clearance)	L(IO1)	7.0	mm	Measured from input terminals to output terminals, shortest distance through air
Min. External Tracking Path (External Creepage)	L(IO2)	8.5	mm	Measured from input terminals to output terminals, shortest distance path along body
Min. Internal Plastic Gap (Internal Clearance)		0.5	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity
Tracking Resistance (Comparative Tracking Index)	CTI	200	V	DIN IEC 112/VDE 0303 PART 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Option 300 – surface mount classification is Class A in accordance with CECC 00802.

Absolute Maximum Ratings

Storage Temperature ..... -55°C to+125°C
Operating Temperature - T_A ..... -40°C to +85°C
Case Temperature - T_C ..... +105°C[1]
Average Input Current - I_F ..... 20 mA
Repetitive Peak Input Current - I_F ..... 40 mA
(Pulse Width ≤ 1 ms; duty cycle ≤ 50%)
Transient Peak Input Current - I_F ..... 100 mA
(Pulse Width ≤ 200 µs; duty cycle ≤ 1%)
Reverse Input Voltage - V_R ..... 3 V
Input Power Dissipation ..... 40 mW
Output Voltage (T_A = 25°C)
Connection A - V_O ..... -60 to +60 V
Connection B - V_O ..... 0 to +60 V
Average Output Current - Figure 3 (T_A = 25°C, T_C ≤ 70°C)
Connection A - I_O ..... 0.75 A
Connection B - I_O ..... 1.50 A
Single Shot Peak Output Current
(100 ms pulse width, T_A = 25°C, I_F = 10 mA)
Connection A - I_O ..... 3.75 A
Connection B - I_O ..... 7.0 A
Output Power Dissipation ..... 750 mW[2]
Lead Solder Temperature .... 260°C for 10 S (1.6 mm below seating plane)
Infrared and Vapor Phase Reflow Temperature
(Option #300) ..... See Fig. 1, Thermal Profile

Thermal Resistance

Typical Output MOSFET Junction to Case – θ_{JC} = 55°C/W

Demonstrated ESD Performance

Human Body Model: MIL-STD-883 Method 3015.7 - 16 kV
Machine Model: EIAJ 1988.3.28 Version 2), Test Method 20, Condition C – 1200 V

Surge Withstand Capability

IEEE STD 472-1974

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Input Current (ON)	$I_{F(ON)}$	5	20	mA
Input Voltage (OFF)	$V_{F(OFF)}$	0	0.8	Volt
Operating Temperature	T_A	-40	+85	°C
Output Voltage				
Connection A	$V_{O(OFF)}$	-55	55	Volt
Connection B		0	55	
Output Current				
Connection A	$I_{O(ON)}$	-0.75	0.75	A
Connection B		-1.5	1.5	

DC Electrical Specifications

For -40°C ≤ T_A ≤ +85°C unless otherwise specified. All Typicals at T_A = 25°C.

Parameter	Connection	Sym.	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Notes
Output Withstand Voltage	A	$\|V_{O(OFF)}\|$	60			V	V_F = 0.8 V, I_O = 250 µA, T_A = 25°C	5	
			55				V_F = 0.8 V, I_O = 250 µA		
Output On-Resistance	A	$R_{(ON)}$		0.4	0.7	Ω	I_F = 10 mA, I_O = 750 mA (pulse duration ≤ 30 ms), T_A = 25°C	6,7	3
	B			0.1	0.2				
	A				1.6		I_F = 10 mA, I_O = 750 mA (pulse duration ≤ 30 ms)		
	B				0.4				
Output Leakage Current	A	$I_{O(OFF)}$		10^{-4}	1.0	µA	V_F = 0.8 V, V_O = 60 V, T_A = 25°C	13	
Output Off-Capacitance	A	$C_{(OFF)}$		135		pF	V_F = 0.8 V, V_O = 25 V, f = 1 MHz	14	
Output Off-set Voltage	A	$\|V_{OS}\|$		1		µV	I_F = 5 mA, I_O = 0 mA	18	4
Input Reverse Breakdown Voltage		V_R	3			V	I_R = 100 µA		
Input Forward Voltage		V_F	1.3	1.6	1.85	V	I_F = 10 mA, T_A = 25°C	15	
Input Diode Temperature Coefficient		$\Delta V_F/\Delta T_A$		-1.3		mV/°C	I_F = 10 mA		
Input Capacitance		C_{IN}		72		pF	V_F = 0 V, f = 1 MHz		

Switching Specifications

For -40°C ≤ T_A ≤ +85°C with Connection A, unless otherwise specified. All Typicals at T_A = 25°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Notes
Turn On Time	t_{ON}		0.93	1.4	ms	I_F = 10 mA, V_{DD} = 60 V, I_O = 750 mA, T_A = 25°C	2,8, 9,10, 20,21	7
				1.8	ms	I_F = 10 mA, V_{DD} = 55 V, I_O = 750 mA		
Turn Off Time	t_{OFF}		0.013	0.1	ms	I_F = 10 mA, V_{DD} = 60 V, I_O = 750 mA, T_A = 25°C	2,8, 11,12, 20,21	
				0.1	ms	I_F = 10 mA, V_{DD} = 55 V, I_O = 750 mA		
Output Transient Rejection	$\|dV_O/dt\|$	1000			V/µs	$V_{(peak)}$ = 60 V, $R_M \geq$ 1 MΩ, C_M = 1000 pF, T_A = 25°C	16	
Input-Output Transient Rejection	$\|dV_{I-O}/dt\|$	2500			V/µs	V_{DD} = 5 V, $V_{I-O(peak)}$ = 1000 V, R_L = 1 kΩ, C_L = 25 pF, T_A = 25°C	17	

Package Characteristics

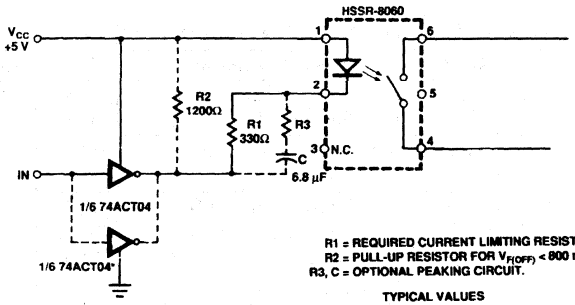
For 0°C ≤ T_A ≤ 70°C, unless otherwise specified. All typicals at T_A = 25°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Notes
Input-Output Momentary Withstand Voltage*	V_{ISO}	2500			V rms	RH ≤ 50%, t = 1 min, T_A = 25°C		5,6
Resistance Input-Output	R_{I-O}		100		GΩ	V_{I-O} = 500 Vdc, t = 1 min, RH = 45%		5
Capacitance Input-Output	C_{I-O}		1.0		pF	V_{I-O} = 0 V, f = 1 MHz		5

*The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the VDE 0884 Insulation Characteristics Table (if applicable), your equipment level safety specification, or HP Application Note 1074, "Optocoupler Input-Output Endurance Voltage."

Notes:

1. The case temperature, T_C, is measured at the center of the bottom of the package.
2. For derating, see Figure 4. The output power P_O derating curve is obtained when the part is handling the maximum average output current I_O as shown in Figure 3.
3. During the pulsed R_{ON} measurement (I_O duration ≤ 30 ms), ambient (T_A) and case temperature (T_C) are equal.
4. V_{OS} is a function of I_F, and is defined between pins 4 and 6, with pin 4 as the reference. V_{OS} must be measured in a stable ambient (free of temperature gradients).
5. Device considered a two terminal device: pins 1, 2, and 3 shorted together and pins 4, 5, and 6 shorted together.
6. This is a momentary withstand proof test. These parts are 100% tested in production at 3000 V rms, one second.
7. For a faster turn-on time, the optional peaking circuit shown in Figure 2 may be implemented.



*USE SECOND GATE IF $I_{F(PK)}$ > 50 mA.

TYPICAL VALUES

R_3 (Ω)	$I_{F(PK)}$ (mA)	HSSR-8060 t_{ON} (ms)
–	10 (no pk)	0.93
330	20	0.53
100	40	0.32
33	100	0.17

Figure 2. Recommended Input Circuit.

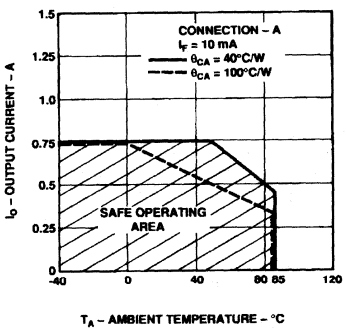


Figure 3A. Maximum Average Output Current Rating vs. Ambient Temperature.

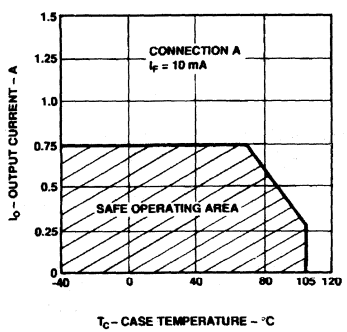


Figure 3B. Maximum Average Output Current Rating vs. Case Temperature.

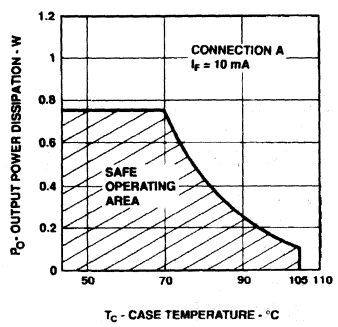


Figure 4. Output Power Derating vs. Case Temperature.

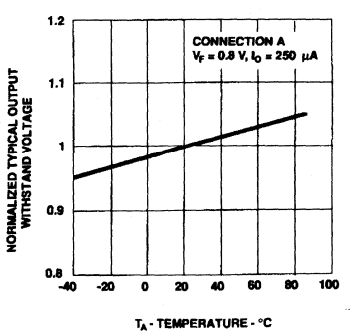


Figure 5. Normalized Typical Output Withstand Voltage vs. Temperature.

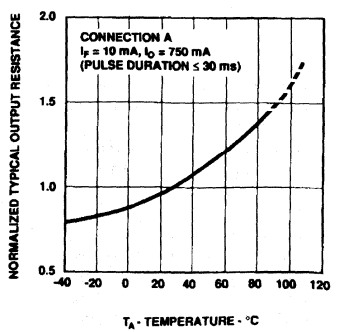


Figure 6. Normalized Typical Output Resistance vs. Temperature.

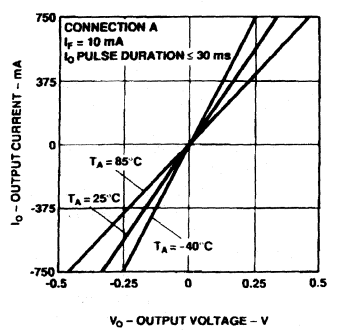


Figure 7. Typical On State Output I-V Characteristics.

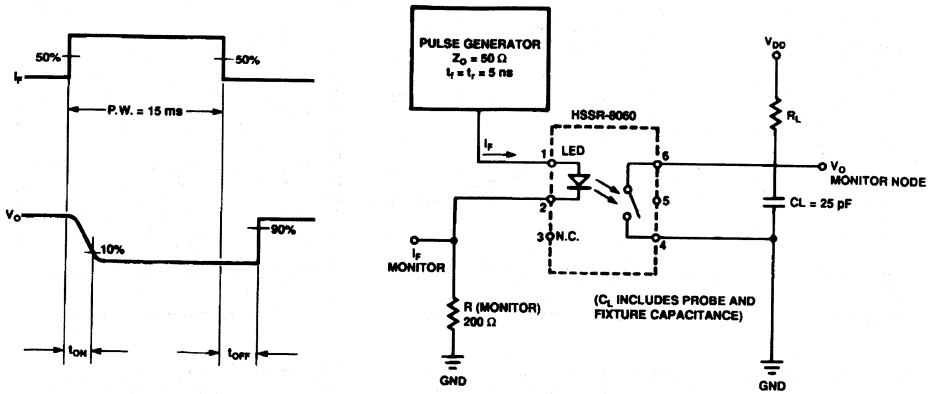


Figure 8. Switching Test Circuit for t_{ON}, t_{OFF}.

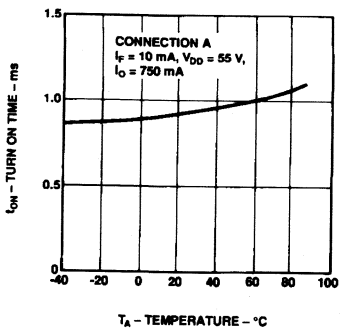


Figure 9. Typical Turn On Time vs. Temperature.

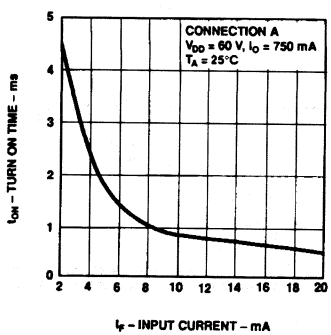


Figure 10. Typical Turn On Time vs. Input Current.

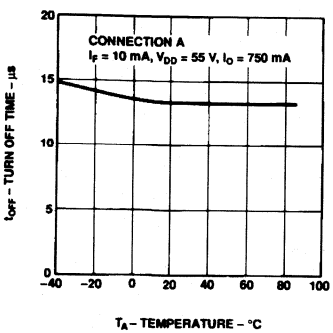


Figure 11. Typical Turn Off Time vs. Temperature.

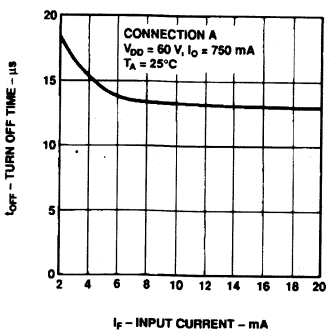


Figure 12. Typical Turn Off Time vs. Input Current.

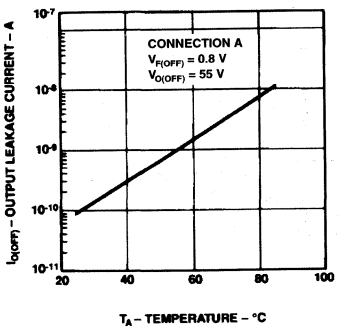


Figure 13. Typical Output Leakage vs. Temperature.

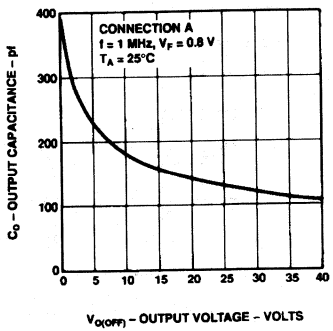


Figure 14. Typical Output Capacitance vs. Output Voltage.

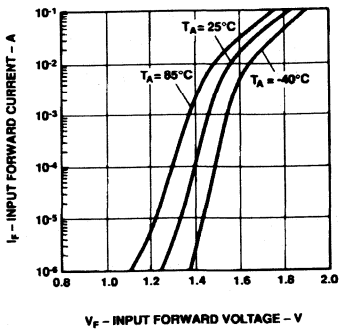


Figure 15. Typical Input Forward Current vs. Input Forward Voltage.

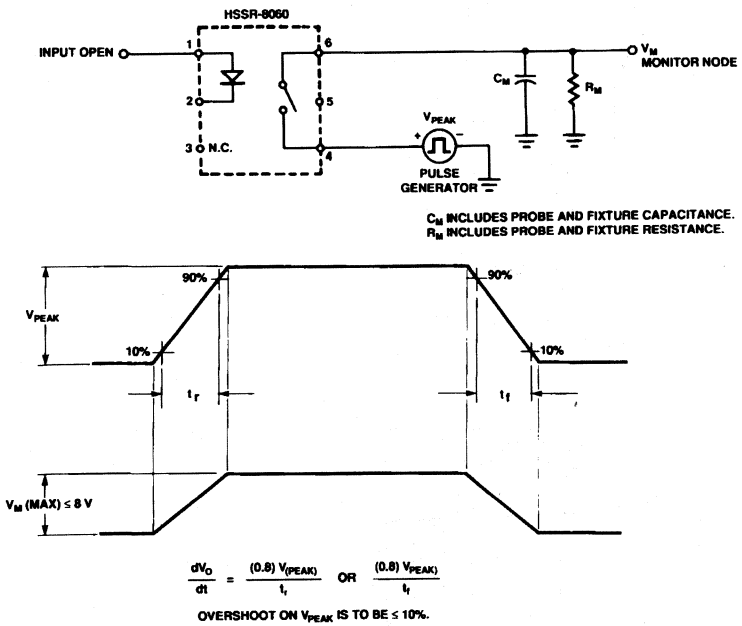


Figure 16. Output Transient Rejection Test Circuit.

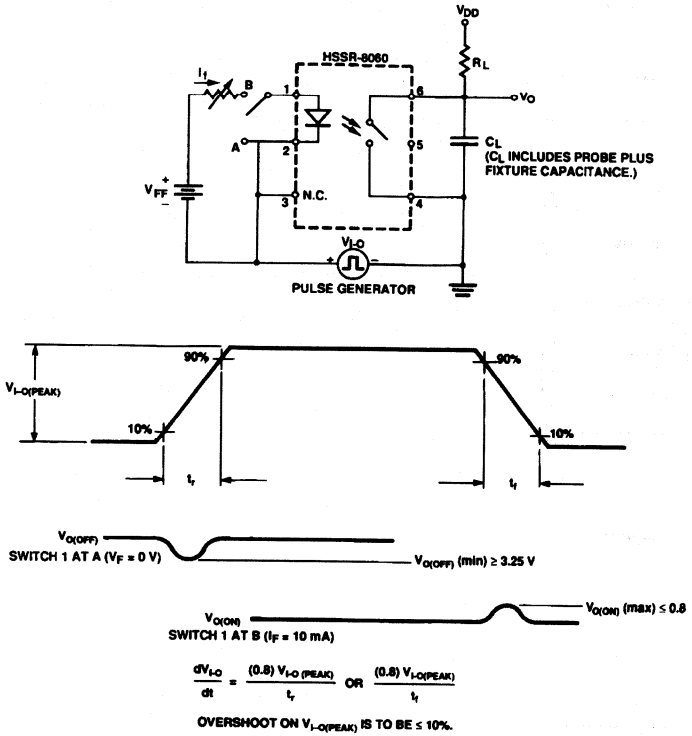


Figure 17. Input-Output Transient Rejection Test Circuit.

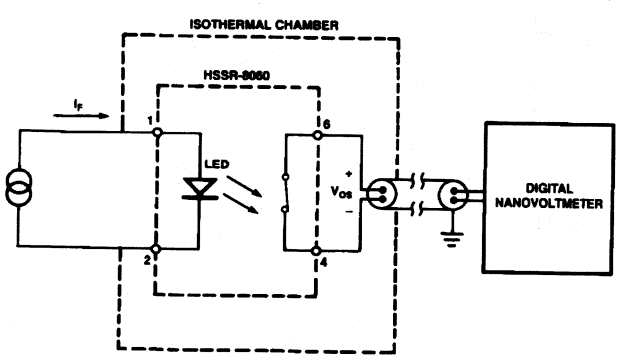


Figure 18. Voltage Offset Test Setup.

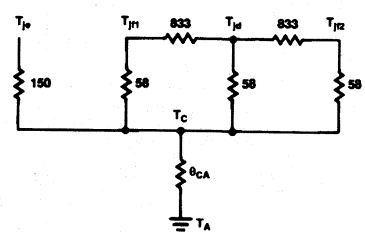


Figure 19. Thermal Model.

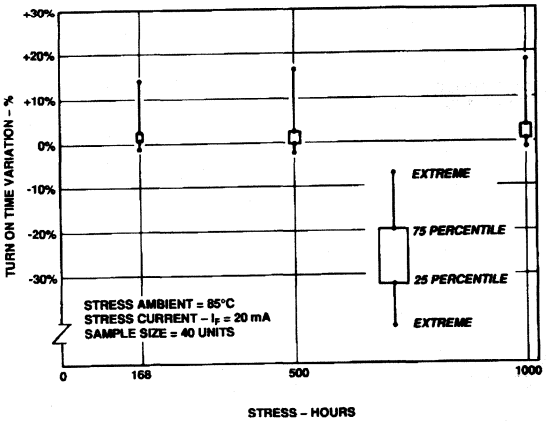


Figure 20. Turn On Time Variation with High Temperature Operating Life.

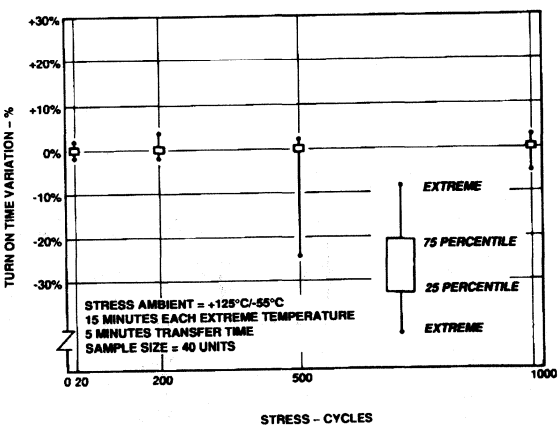


Figure 21. Turn On Time Variation with Temperature Cycling.

Applications Information

Thermal Model

The steady state thermal model for the HSSR-8400 is shown in Figure 19. The thermal resistance values given in this model can be used to calculate the temperatures at each node for a given operating condition. The thermal resistances between the LED and other internal nodes are very large in comparison with the other terms and are omitted for simplicity. The components do, however, interact indirectly through θ_{CA}, the case-to-ambient thermal resistance. All heat generated flows through θ_{CA}, which raises the case temperature T_C accordingly. The value of θ_{CA} depends on the conditions of the board design and is, therefore, determined by the designer.

The typical value for each output MOSFET junction-to-case thermal resistance is specified as 55°C/W. This is the thermal resistance from one MOSFET junction to the case when power is dissipated equally in the MOSFETs. The power dissipation in the FET Driver is negligible in comparison to the MOSFETs.

On-Resistance and Derating Curves

The output on-resistance, R_{ON}, specified in this data sheet, is the resistance measured across the output contact when a pulsed current signal (I_O = 150 mA) is applied to the output pins. The use of a pulsed signal (≤ 30 ms) implies that each junction temperature is equal to the ambient and case temperatures. The steady-state resistance, R_{SS}, on the other hand, is the value of the resistance measured across the output contact when a DC current signal is applied to the output pins for a duration sufficient to reach thermal equilibrium. R_{SS} includes the effects of the temperature rise of each element in the thermal model.

Derating curves are shown in Figures 3 and 4. Figure 3 specifies the maximum average output current allowable for a given ambient or case temperature. Figure 4 specifies the output power dissipation allowable for a given case temperature. Above a case temperature of 93°C, the maximum allowable output current and power dissipation are related by the expression $R_{SS} = P_O(max)/(I_O(max))^2$ from which R_{SS} can be calculated. Staying within the safe area assures that the steady state junction temperatures remain less than 125°C. As an example, for a case temperature of 100°C, Figure 4 shows that the output power dissipation should be limited to less than 0.5 watts. A check with Figure 3B shows that the output current should be limited to less than 150 mA. This yields an R_{SS} of 22 Ω.

Turn On Time Variation

For applications which are sensitive to turn on time, the designer should refer to Figures 20 and 21. These figures show that although there is very little variation in t_{ON} within most of the population, a portion of the distribution will vary with use. The optional peaking circuit shown in Figure 2 can be used to reduce the total turn on time and, consequently, any associated variation.

HEWLETT® PACKARD

200-V/160 Ohm, 1 Form A, Small-Signal Solid State Relay

Technical Data

HSSR-8200

Features

- **Compact Solid-State Bidirectional Signal Switch**
- **Normally-Off Single-Pole Relay Function (1 Form A)**
- **Very High Output Off-Impedance: 10,000 Gigaohms Typical at 25°C**
- **Very Low Output Offset Voltage: < 0.5 μV at I_F = 1 mA**
- **200-Volt Output Withstand Voltage at 25°C**
- **High-Transient Immunity: > 2000 V/μs**
- **Monolithic High-Voltage IC**
- **Operating Range: -40°C to +85°C**
- **Very Low Input Current (1 mA); CMOS Compatibility**
- **High-Speed Switching: 50 μs Typical**
- **160-Ohm Maximum On-Resistance at 25°C**
- **Surface Mount Option**
- **8-kV ESD Immunity: MIL-STD-883 Method 3015**
- **Input-to-Output Insulation Voltage: 2500 Vac, 1 Minute**
- **UL 508 Recognized**
- **CSA Approved**

Applications

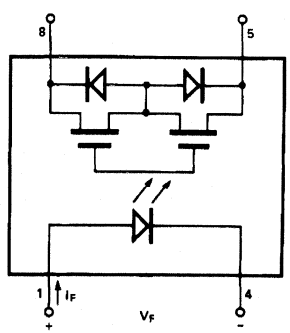
- **Relay Scanners & Analog Input Modules of Data Acquisition Systems**
- **Analog Input Modules of Programmable Logic Controllers**
- **Relay Multiplexers of High-Performance Voltmeters**
- **Telecommunication Test Instruments**
- **Functional Tester of Board Test Equipment**
- **Analog Signal Multiplexer**
- **Flying Capacitor Multiplexer**
- **Reed Relay Replacement**

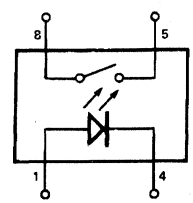
Description

The HSSR-8200 consists of a high-voltage integrated circuit optically coupled with a light emitting diode. This device is a solid-state replacement for single-pole, normally-open electromechanical relays used for general purpose switching of analog signals.

The light-emitting diode controls the ON/OFF function of the solid-state relay. The detector contains high voltage MOS transistors and a high speed photosensitive drive circuit. This relay has superior OFF impedance, very low output offset voltage and input drive current.

Functional Diagram





EQUIVALENT RELAY DIAGRAM

TRUTH TABLE (POSITIVE LOGIC)

LED	OUTPUT
ON	L
OFF	H

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

5965-3574E

The electrical and switching characteristics of the HSSR-8200 are specified from –40°C to +85°C. The low I_F allows compatibility with TTL, LSTTL, and CMOS logic resulting in low power consumption compared to other solid state and mechanical relays.

Selection Guide

6-Pin DIP (300 Mil) Single Channel Package	4-Pin DIP (300 Mil) Dual Channel Package	Maximum Speed t(ON) msec 25°C	Maximum ON Resistance R(ON) Ω 25°C	Maximum Output Voltage VO(off) V 25°C	Maximum Output Current Io(ON) mA 25°C	Minimum Input Current mA	Hermetic 8-Pin Single Channel Packages
HSSR-8400[1]		0.95	10	400	150	5	
HSSR-8060[1]		1.4	0.7	60	750	5	
	HSSR-8200	1.5	200	200	40	1	
		6	1	90	800	5	HSSR-7110[1]

Note:
1. Technical data are on separate HP publication.

Ordering Information

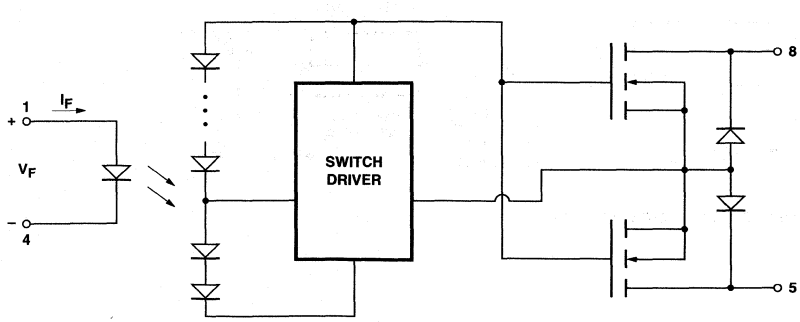
Specify part number followed by Option Number (if desired).

HSSR-8200#XXX

- 300 = Gull Wing Surface Mount Lead Option
- 500 = Tape/Reel Package Option (1 K min)

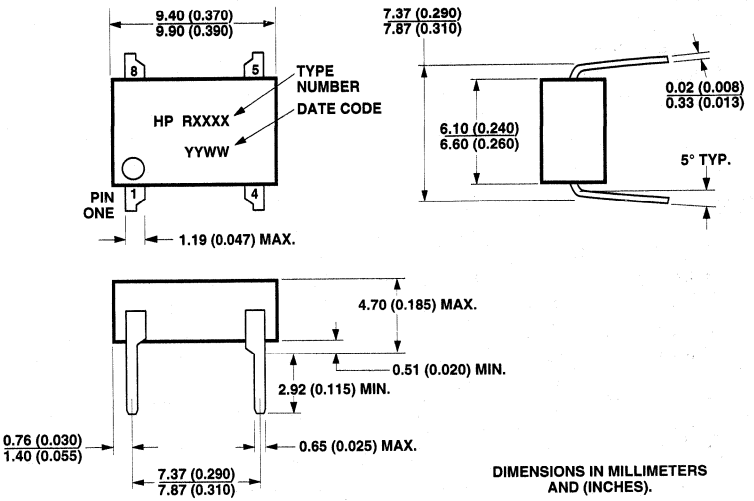
Option data sheets available. Contact your Hewlett-Packard sales representative or authorized distributor for information.

Schematic

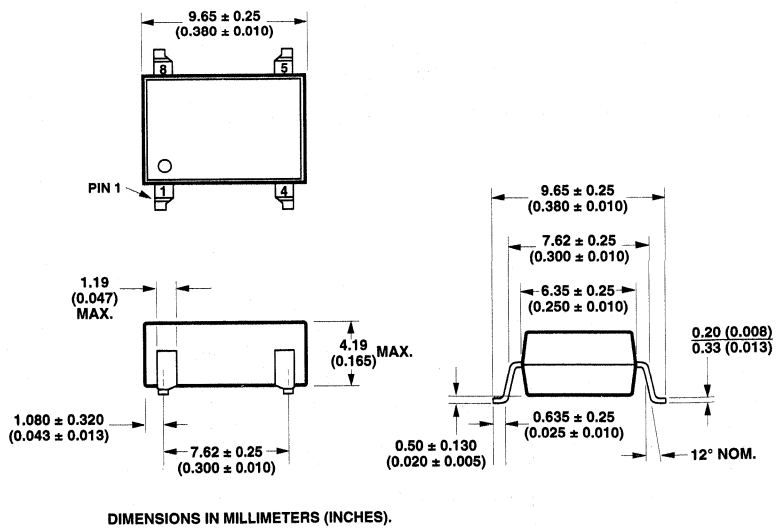


Package Outline Drawings

4-Pin DIP Package (HSSR-8200)



4-Pin DIP Package with Gull Wing Surface Mount Option 300



Thermal Profile (Option #300)

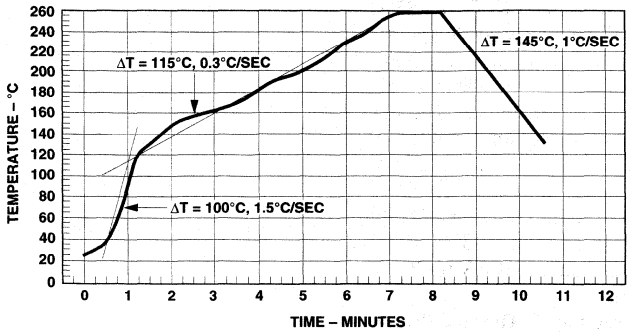


Figure 1. Maximum Solder Reflow Thermal Profile.
(Note: Use of non-chlorine activated fluxes is recommended.)

Regulatory Information

The HSSR-8200 has been approved by the following organizations:

UL

Recognized under UL 508, Component Recognition Program, Industrial Control Switches, File E142465.

CSA

Approved under CAN/CSA-C22.2 No. 14-95, Industrial Control Equipment, File LR 87683.

Insulation and Safety Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min. External Air Gap (External Clearance)	L(IO1)	7.0	mm	Measured from input terminals to output terminals, shortest distance through air
Min. External Tracking Path (External Creepage)	L(IO2)	7.5	mm	Measured from input terminals to output terminals, shortest distance path along body
Min. Internal Plastic Gap (Internal Clearance)		0.5	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity
Tracking Resistance (Comparative Tracking Index)	CTI	200	Volts	DIN IEC 112/VDE 0303 PART 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Option 300 – surface mount classification is Class A in accordance with CECC 00802.

Absolute Maximum Ratings

Storage Temperature ..... -55°C to+125°C
Operating Temperature ..... -40°C to +85°C
Lead Solder Temperature .... 260°C for 10 s (1.6 mm below seating plane)
Average Input Current - I_F ..... 10 mA
Repetitive Peak Input Current - I_F ..... 20 mA; 50% Duty Cycle
Transient Peak Input Current - I_F ..... 100 mA
(≤ 1 µs pulse width; 1 kHz Pulse Repetition Rate)
Reverse Input Voltage ..... 5 V
Average Output Current – I_O ..... 40 mA[1]
Input Output Insulation Voltage ..... 2500 VAC[6]
Output Power Dissipation ..... 320 mW[2]
Output Voltage – V_O ..... -200 V to 200 V
Infrared and Vapor Phase Reflow Temperature
(Option #300) ..... see Fig. 1, Thermal Profile

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Input Current (ON)	$I_{F(ON)}$	1	5	mA
Input Voltage (OFF)	$V_{F(OFF)}$	0	0.6	Volt
Operating Temperature	T_A	-40	+85	°C
Output Voltage	$V_{O(OFF)}$	-200	200	Volt
Output Current	$I_{O(ON)}$	-40	40	mA

DC Electrical Specifications

$-40°C \le T_A \le +85°C$, 1 mA $\le I_{F(ON)} \le$ 5 mA, 0 V $\le V_{F(OFF)} \le$ 0.6 V, and all Typicals at T_A = 25°C unless otherwise specified.

Parameter	Sym.	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Notes
Output Withstand Voltage	$\|V_{O(OFF)}\|$	200	245		V	I_O = 1 µA		
Output On-Resistance	$R_{(ON)}$	70	125	160	Ω	T_A = 25°C, I_O = 1 MA	3, 4, 5	
		40	125	250		I_O = 1 MA		
		30	100	200		I_O = 40 mA		
Output On-Current Rating	$\|I_{O(ON)}\|$			40	mA	$V_O \le$ 8 V, $T_A \le$ 40°C		1
Output Off-Resistance	$R_{(OFF)}$	50	10,000		GΩ	V_O = 200 V	6	6
Output Off-Leakage Current	$I_{O(OFF)}$		0.02	4.0	nA	V_O = 200 V	6	
Output Off-Capacitance	$C_{(OFF)}$			4.5	pF	V_O = 0 V, f = 1 MHz	7	
Output Offset Voltage	$V_{O(OS)}$	Note 3	-0.2	Note 3	µV	I_O = 0 A; I_F = 1 mA	8, 17, 18	3
			-1.3			I_O = 0 A; I_F = 5 mA		
Input Reverse Breakdown Voltage	V_R	3	10		V	I_R = 10 µA		
Input Diode Temperature Coefficient	dV_F/dT		-1.75		mV/°C	I_F = 1 mA		
Input Forward Voltage	V_F		1.5	2.0	V	I_F = 5 mA	9	
Input Capacitance	C_{IN}		21		pF	V_F = 0 V; f = 1 MHz		

Switching Specifications

$-40°C \le T_A \le +85°C$, 1 mA $\le I_{F(ON)} \le$ 5 mA, 0 V $\le V_{F(OFF)} \le$ 0.6 V, and all Typicals at T_A = 25°C unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions		Fig.	Notes
Turn On Time	t_{ON}		50	200	µs	I_F = 5 mA	V_O = 50 V	10, 11, 12, 13	
			300	1500		I_F = 1 mA			
Turn Off Time	t_{OFF}		45	250	µs	I_F = 5 mA	V_O = 50 V	10, 11, 12, 13	
			75	350		I_F = 1 mA			
Output Transient Rejection	dV_O/dt		≥ 7000		V/µs	ΔV_O = 200 V	T_A = 25°C	14	
		2000				ΔV_O = 50 V			
Input-Output Transient Rejection	dV_{I-O}/dt		≥ 7000		V/µs	ΔV_{I-O} = 300 V	T_A = 25°C	15	
		2000				ΔV_{I-O} = 50 V			

Package Characteristics

For -40°C ≤ T_A ≤ +85°C, unless otherwise specified. All Typicals at T_A = 25°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Notes
Input-Output Momentary Withstand Voltage*	V_{ISO}	2500			V rms	RH = 45%, t = 1 min, T_A = 25°C		4, 5
Resistance Input-Output	R_{I-O}	100	100,000		GΩ	V_{I-O} = 500 VDC, t = 1 min, RH = 45%		4
Capacitance Input-Output	C_{I-O}		0.6	1.0	pF	V_{I-O} = 0 V, f = 1 MHz, T_A = 25°C		4

*The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the VDE 0884 Insulation Characteristics Table (if applicable), your equipment level safety specification, or HP Application Note 1074, "Optocoupler Input-Output Endurance Voltage."

Notes:

1. Derate linearly above 40°C at a rate of 0.3 mA/°C.
2. Derate linearly above 60°C at a rate of 5 mW/°C.
3. $V_{O(OS)}$ is a function of $I_{F(ON)}$, and is defined between pins 8 and 5 with pin 5 as reference. $V_{O(OS)}$ must be measured in a stable ambient. See Figure 8 for variation of $V_{O(OS)}$ around the typical value.
4. Device considered a two terminal device: pins 1 and 4 shorted together, and pins 5 and 8 shorted together.
5. This is a momentary withstand proof test. These parts are 100% tested in production at 3000 Vrms, one second.
6. $R_{(OFF)}$ is defined as $V_{O(OFF)}/I_{O(OFF)}$.

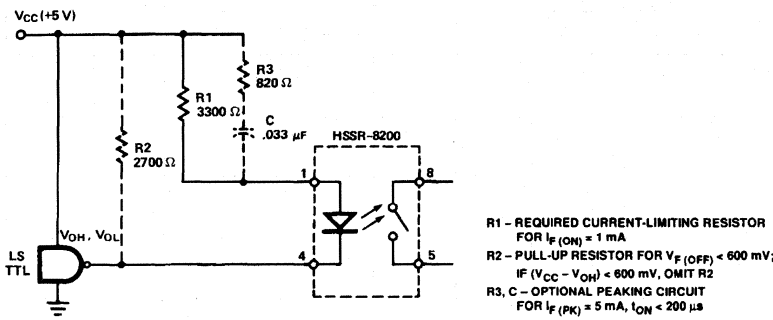


Figure 2. Recommended Input Circuit.

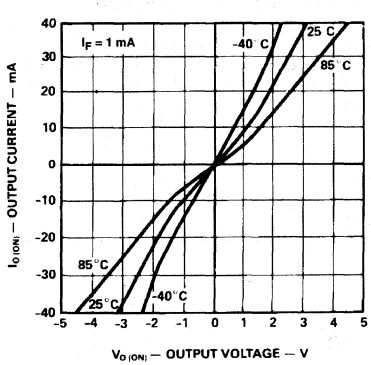


Figure 3. Typical On State I-V Characteristics.

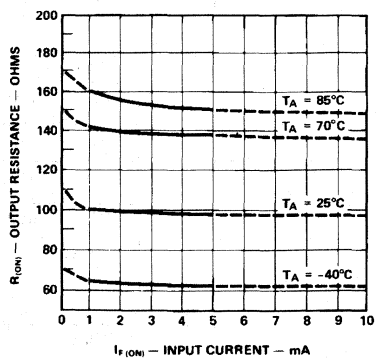


Figure 4. Typical Output Resistance vs. Input Current.

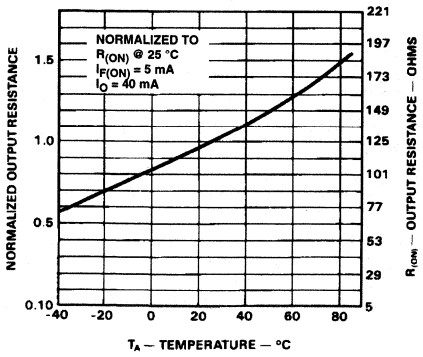


Figure 5. Typical Output Resistance vs. Temperature.

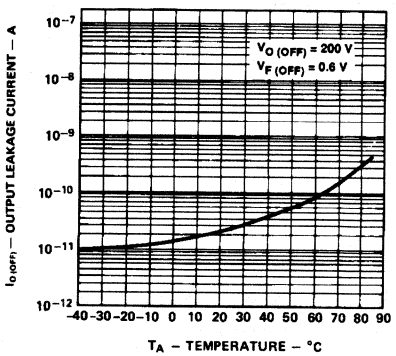


Figure 6. Typical Output Leakage vs. Temperature.

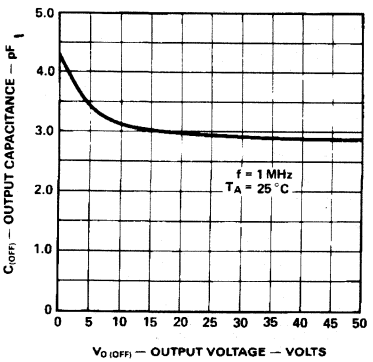


Figure 7. Typical Output Capacitance vs. Output Voltage.

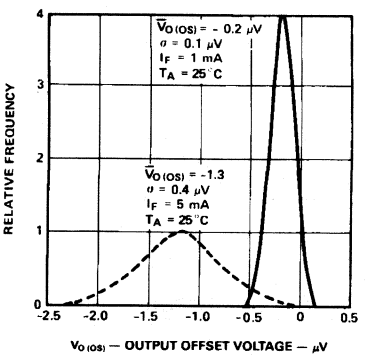


Figure 8. Output Offset Voltage Distribution.

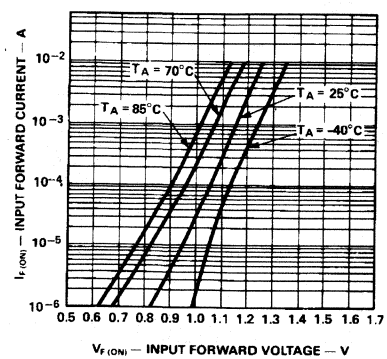


Figure 9. Typical Input Forward Current vs. Forward Voltage.

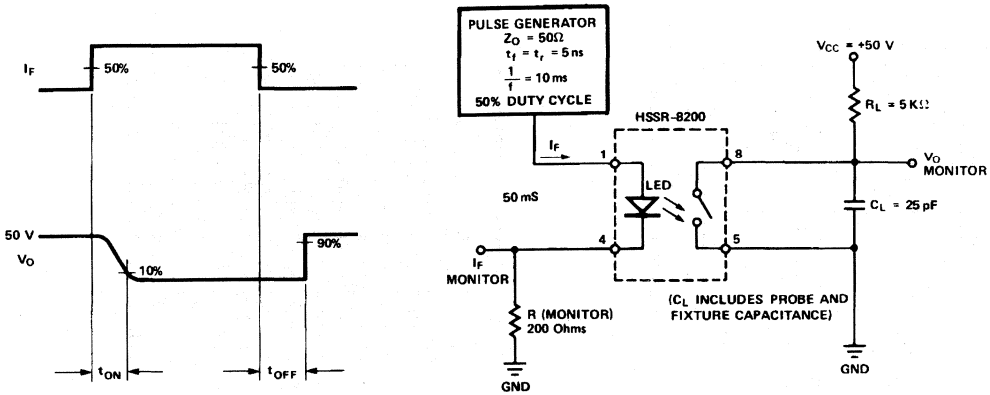


Figure 10. Switching Test Circuit for t_{ON}, t_{OFF}.

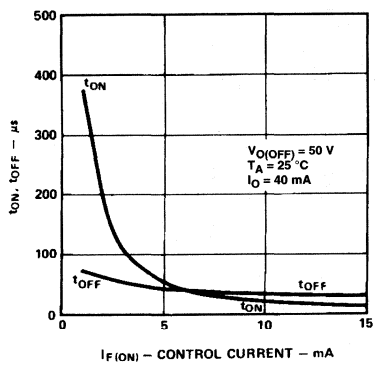


Figure 11. Typical t_{ON} and t_{OFF} vs. Input Current.

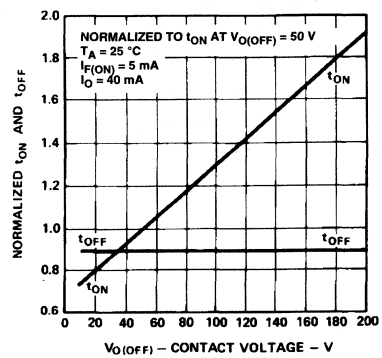


Figure 12. t_{ON} and t_{OFF} vs. Output Voltage.

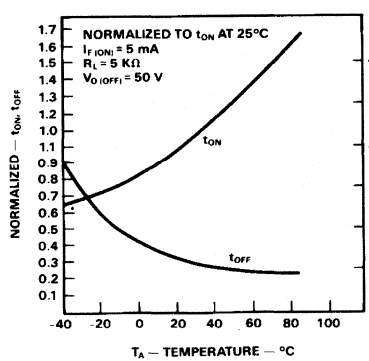


Figure 13. Normalized t_{ON} and t_{OFF} vs. Temperature.

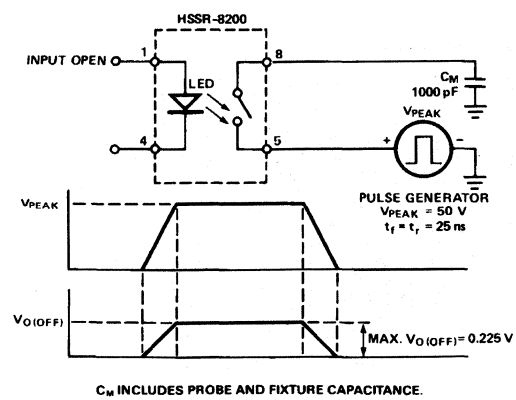


Figure 14. Output Transient Rejection Test Circuit.

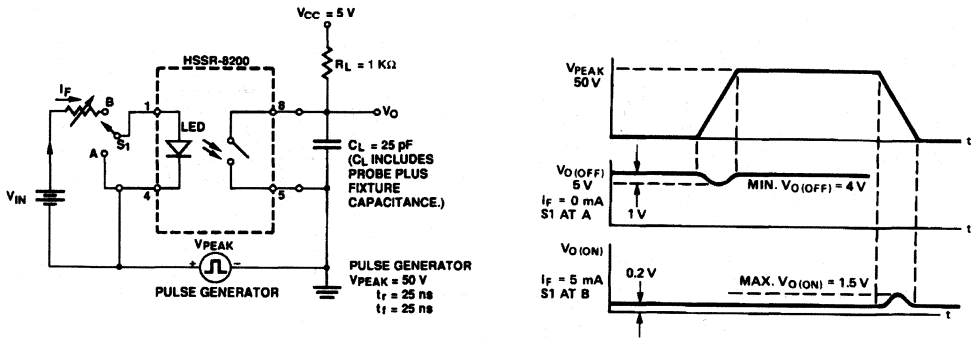


Figure 15. Input-Output Transient Rejection.

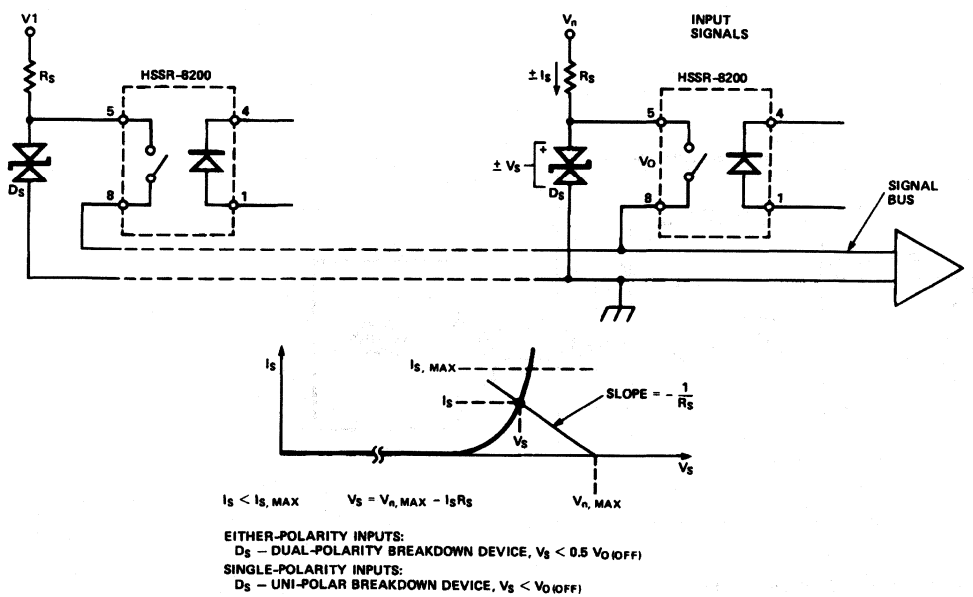


Figure 16. Over-Voltage Protection in Multiplexer Applications.

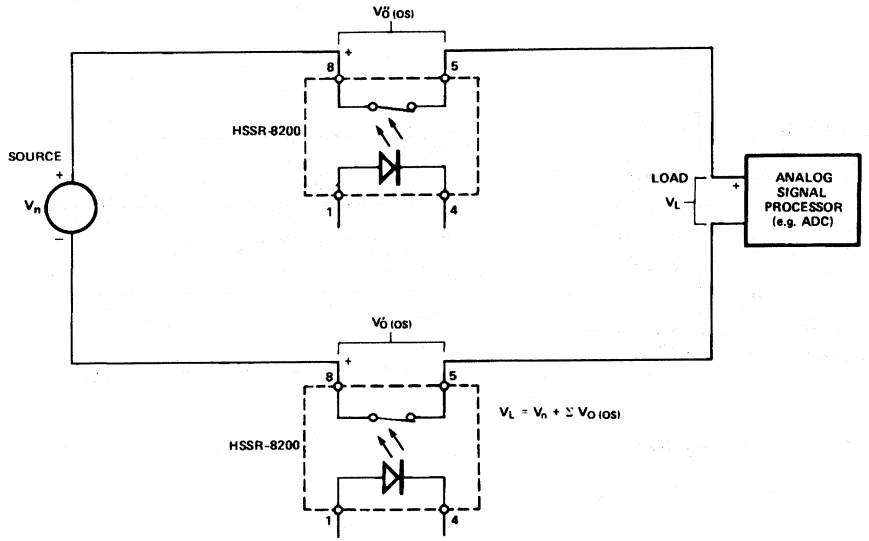


Figure 17. Differential Output Connections to Minimize Offset Voltage Effects.

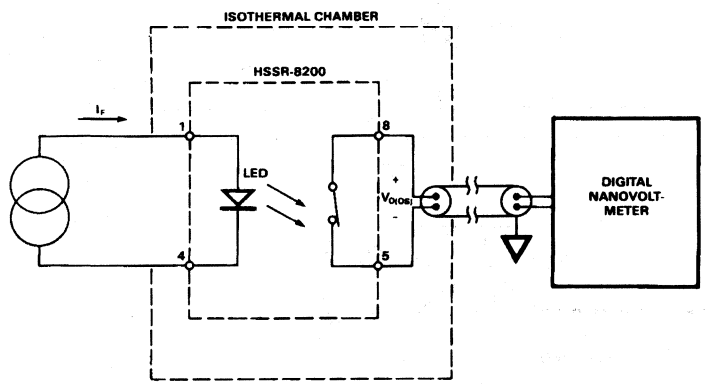


Figure 18. Voltage Offset Test Setup.

400 V/10 Ohm, General Purpose, 1 Form A, Solid State Relay

Technical Data

HSSR-8400

Features

- **Compact Solid-State Bidirectional Switch**
- **Normally-Off Single-Pole Relay Function (1 Form-A)**
- **400 V Output Withstand Voltage in Both Polarities at 25°C**
- **150/300 mA Current Ratings (See Schematic for Connection A & B)**
- **Low Input Current; CMOS Compatibility**
- **Very Low On-Resistance: 6 Ω Typical at 25°C**
- **ac/dc Signal & Power Switching**
- **Input-to-Output Momentary Withstand Insulation Voltage: 2500 Vac, 1 Minute**
- **16-kV ESD Immunity: MIL-STD-883, Method 3015**
- **CSA Approved**
- **UL 508 Recognized**

Applications

- **Modems**
- **Telecommunication Switching Equipment**
- **Telecommunication Test Instruments**
- **Reed Relay Replacement**
- **110/220 Vac Load Driver**
- **Industrial Relay Coil Driver**

Description

The HSSR-8400 consists of a high-voltage circuit, optically coupled with a Light-Emitting Diode (LED). This device is a solid-state replacement for single-pole, normally-open (1 Form A) electromechanical relays used for general purpose switching of signals and low-power ac/dc loads. The relay turns on (contact closes) with a minimum input current, I_F, of 5 mA through the input LED. The relay turns off (contact opens) with an input voltage, V_F, of 0.8 V or less. The detector contains a high speed photosensitive FET driver circuit and two high voltage MOSFETs.

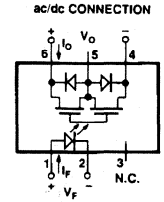
This relay's logic-level input control and very low typical output on-resistance of 6 Ω make it suitable for switching of audio frequency signals in telecom applications. Connection A, as shown in the schematic, allows the relay to switch either ac or dc loads. In this configuration, the 150 mA output current rating allows it to switch small loads that are driven from 110 Vac and 220 Vac power lines. Connection B, with the polarity and pin configuration as indicated in the schematic, allows the relay to switch dc loads only. The advantage of Connection B is that the on-resistance is significantly reduced and the output current capability increases by a factor of two.

The electrical and switching characteristics of the HSSR-8400 are specified from -40°C to +85°C.

Functional Diagram

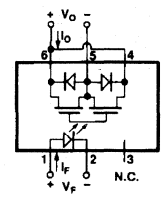
CONNECTION A

ac/dc CONNECTION



CONNECTION B

dc CONNECTION



TRUTH TABLE (POSITIVE LOGIC)

LED	OUTPUT
ON	L
OFF	H

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Selection Guide

6-Pin DIP (300 Mil) Single Channel Package	4-Pin DIP (300 Mil) Dual Channel Package	Maximum Speed t(ON) msec 25°C	Maximum ON Resistance R(ON) Ω 25°C	Maximum Output Voltage VO(off) V 25°C	Maximum Output Current Io(ON) mA 25°C	Minimum Input Current mA	Hermetic 8-Pin Single Channel Packages
HSSR-8400		0.95	10	400	150	5	
HSSR-8060[1]		1.4	0.7	60	750	5	
	HSSR-8200[1]	1.5	200	200	40	1	
		6	1	90	800	5	HSSR-7110[1]

Note:
1. Technical data are on separate HP publication.

Ordering Information:

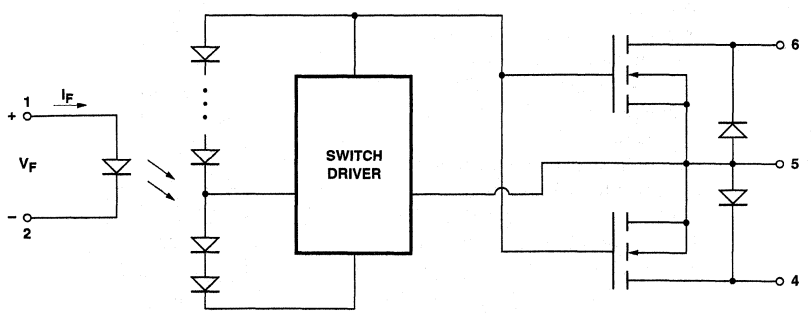
Specify part number followed by Option Number (if desired).

HSSR-8400#XXX

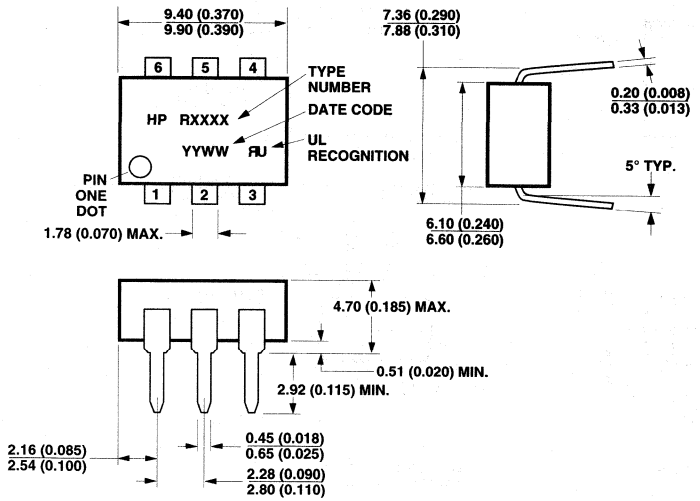
300 = Gull Wing Surface Mount Lead Option
500 = Tape/Reel Package Option (1 Kmin.)

Option data sheets available. Contact your Hewlett-Packard sales representative or authorized distributor for information.

Schematic

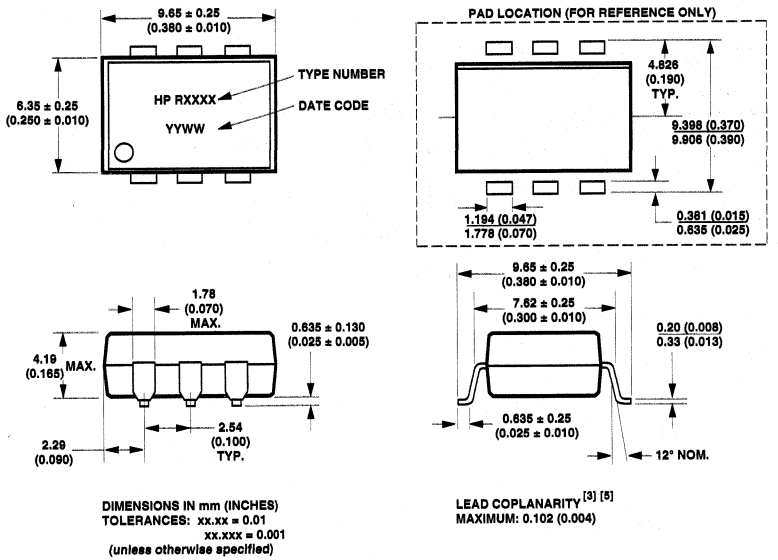


Outline Drawing
6-Pin DIP Package



DIMENSIONS IN MILLIMETERS AND (INCHES).

6-Pin Device Outline Drawing Option #300 (Gull Wing Surface Mount)



HSSR-8400 Outline – Option 300

Thermal Profile (Option #300)

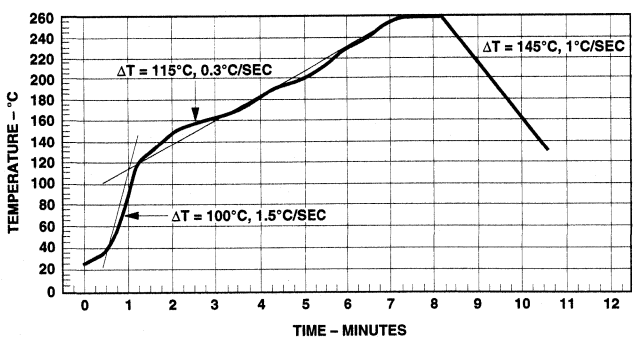


Figure 1. Maximum Solder Reflow Thermal Profile.
(Note: Use of non-chlorine activated fluxes is recommended.)

Regulatory Information

The HSSR-8400 has been approved by the following organizations:

UL

Recognized under UL 508, Component Recognition Program, Industrial Control Switches, File E142465.

CSA

Approved under CAN/CSA-C22.2 No. 14-95, Industrial Control Equipment, File LR 87683.

Insulation and Safety Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min. External Air Gap (External Clearance)	L(IO1)	7.0	mm	Measured from input terminals to output terminals, shortest distance through air
Min. External Tracking Path (External Creepage)	L(IO2)	8.5	mm	Measured from input terminals to output terminals, shortest distance path along body
Min. Internal Plastic Gap (Internal Clearance)		0.5	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity
Tracking Resistance (Comparative Tracking Index)	CTI	200	volts	DIN IEC 112/VDE 0303 PART 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Option 300 – surface mount classification is Class A in accordance with CECC 00802.

Absolute Maximum Ratings

Storage Temperature ..... -55°C to+125°C
Operating Temperature - T_A ..... -40°C to +85°C
Case Temperature - T_C ..... +105°C[1]
Lead Solder Temperature .... 260°C for 10 S (1.6 mm below seating plane)
Average Input Current - I_F ..... 20 mA
Repetitive Peak Input Current - I_F ..... 40 mA
(Pulse Width ≤ 1 ms; duty cycle ≤ 50%)
Transient Peak Input Current - I_F ..... 100 mA
(Pulse Width ≤ 200 µs; duty cycle ≤ 1%)
Reverse Input Voltage - V_R ..... 3 V
Input Power Dissipation ..... 40 mW
Output Voltage (T_A = 25°C)
Connection A - V_O ..... -400 to +400 V
Connection B - V_O ..... 0 to +400 V
Average Output Current - Figure 3 (T_A = 25°C, T_C ≤ 70°C)
Connection A - I_O ..... 0.15 A
Connection B - I_O ..... 0.3 A
Single Shot Peak Output Current
(100 ms pulse width, T_A = 25°C, I_F = 10 mA)
Connection A - I_O ..... 1.0 A
Connection B - I_O ..... 2.0 A
Output Power Dissipation ..... 750 mW[2]
Infrared and Vapor Phase Reflow Temperature
(Option #300) ..... See Fig. 1, Thermal Profile

Thermal Resistance

Typical Output MOSFET Junction to Case – θ_{JC} = 55°C/W

Demonstrated ESD Performance

Human Body Model: MIL-STD-883 Method 3015.7 - 16 kV
Machine Model: EIAJ 1988.3.28 Version 2), Test Method 20, Condition C – 1200 V

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Input Current (ON)	$I_{F(ON)}$	5	20	mA
Input Voltage (OFF)	$V_{F(OFF)}$	0	0.8	Volt
Operating Temperature	T_A	-40	+85	°C
Output Voltage				
Connection A	$V_{O(OFF)}$	-370	370	Volt
Connection B		0	370	
Output Current				
Connection A	$I_{O(ON)}$	-150	150	mA
Connection B		-300	300	

DC Electrical Specifications

For -40°C ≤ T_A ≤ +85°C unless otherwise specified. All Typicals at T_A = 25°C.

Parameter	Connection	Sym.	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Notes
Output Withstand Voltage	A	$\|V_{O(OFF)}\|$	400			V	V_F = 0.8 V, I_O = 250 µA, T_A = 25°C	5	
			370				V_F = 0.8 V, I_O = 250 µA		
Output On-Resistance	A	$R_{(ON)}$		6	10	Ω	I_F = 10 mA, I_O = 150 mA (pulse duration ≤ 30 ms), T_A = 25°C	6,7	3
	B			1.5	2.5				
	A				15		I_F = 10 mA, I_O = 150 mA (pulse duration ≤ 30 ms)		
	B				3.8				
Output Leakage Current	A	$I_{O(OFF)}$		6×10^{-4}	1.0	µA	V_F = 0.8 V, V_O = 400 V, T_A = 25°C	13	
Output Off-Capacitance	A	$C_{(OFF)}$		60		pF	V_F = 0.8 V, V_O = 25 V, f = 1 MHz	14	
Output Off-set Voltage	A	$\|V_{OS}\|$		1		µV	I_F = 5 mA, I_O = 0 mA	18	4
Input Reverse Breakdown Voltage		V_R	3			V	I_R = 100 µA		
Input Forward Voltage		V_F	1.3	1.6	1.85	V	I_F = 10 mA, T_A = 25°C	15	
Input Diode Temperature Coefficient		$\Delta V_F/\Delta T_A$		-1.3		mV/°C	I_F = 10 mA		
Input Capacitance		C_{IN}		72		pF	V_F = 0 V, f = 1 MHz		

Switching Specifications

For -40°C ≤ T_A ≤ +85°C with Connection A, unless otherwise specified. All Typicals at T_A = 25°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Notes
Turn On Time	t_{ON}		0.5	0.95	ms	I_F = 10 mA, V_{DD} = 400 V, I_O = 150 mA, T_A = 25°C	2,8, 9,10, 20,21	7
				1.2	ms	I_F = 10 mA, V_{DD} = 370 V, I_O = 150 mA		
Turn Off Time	t_{OFF}		0.013	0.1	ms	I_F = 10 mA, V_{DD} = 400 V, I_O = 150 mA, T_A = 25°C	2,8, 11,12, 20,21	
				0.1		I_F = 10 mA, V_{DD} = 370 V, I_O = 150 mA		
Output Transient Rejection	$\|dV_O/dt\|$	1000			V/µs	$V_{(peak)}$ = 100 V, R_M ≥ 1 MΩ, C_M = 1000 pF, T_A = 25°C	16	
Input-Output Transient Rejection	$\|dV_{I-O}/dt\|$	2500			V/µs	V_{DD} = 5 V, $V_{I-O(peak)}$ = 1000 V, R_L = 1 kΩ, C_L = 25 pF, T_A = 25°C	17	

Package Characteristics

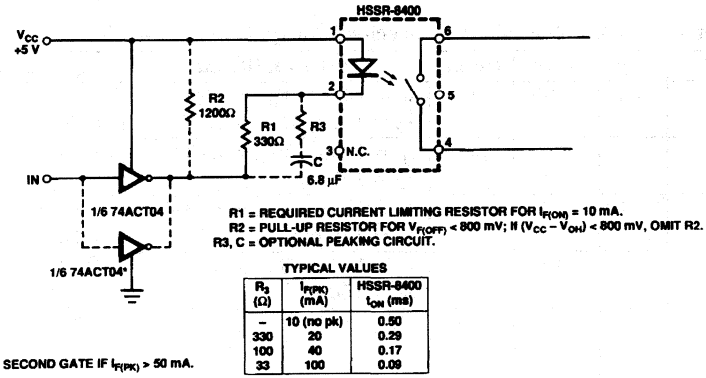
For 0°C ≤ T_A ≤ +70°C with Connection A, unless otherwise specified. All Typicals at T_A = 25°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Notes
Input-Output Momentary Withstand Voltage*	V_{ISO}	2500			V rms	RH ≤ 50%, t = 1 min, T_A = 25°C		5,6
Resistance Input-Output	R_{I-O}		100		GΩ	V_{I-O} = 500 Vdc, t = 1 min, RH = 45%		5
Capacitance Input-Output	C_{I-O}		1.0		pF	V_{I-O} = 0 V, f = 1 MHz		5

*The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the VDE 0884 Insulation Characteristics Table (if applicable), your equipment level safety specification, or HP Application Note 1074, "Optocoupler Input-Output Endurance Voltage."

Notes:

1. The case temperature, T_C, is measured at the center of the bottom of the package.
2. For derating, see Figure 4. The output power P_O derating curve is obtained when the part is handling the maximum average output current I_O as shown in Figure 3.
3. During the pulsed R_{ON} measurement (I_O duration ≤ 30 ms), ambient (T_A) and case temperature (T_C) are equal.
4. V_{OS} is a function of I_F, and is defined between pins 4 and 6, with pin 4 as the reference. V_{OS} must be measured in a stable ambient (free of temperature gradients).
5. Device considered a two terminal device: pins 1, 2, and 3 shorted together and pins 4, 5, and 6 shorted together.
6. This is a momentary withstand proof test. These parts are 100% tested in production at 3000 V rms, one second.
7. For a faster turn-on time, the optional peaking circuit shown in Figure 2 may be implemented.



R_3 (Ω)	$I_{F(PK)}$ (mA)	HSSR-8400 t_{ON} (ms)
–	10 (no pk)	0.50
330	20	0.29
100	40	0.17
33	100	0.09

Figure 2. Recommended Input Circuit.

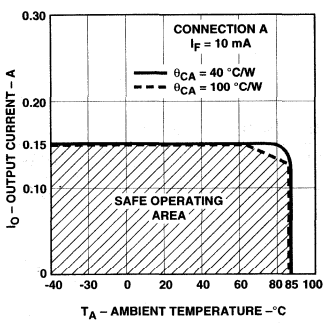


Figure 3A. Maximum Average Output Current Rating vs. Ambient Temperature.

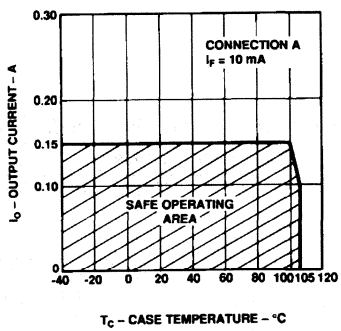


Figure 3B. Maximum Average Output Current Rating vs. Case Temperature.

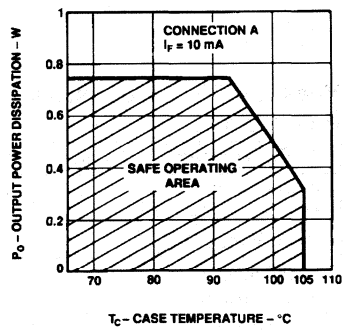


Figure 4. Output Power Derating vs. Case Temperature.

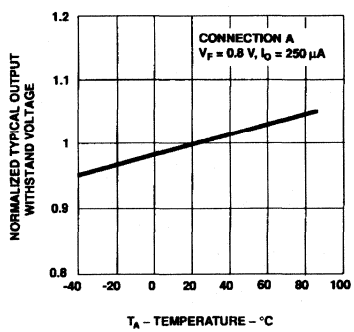


Figure 5. Normalized Typical Output Withstand Voltage vs. Temperature.

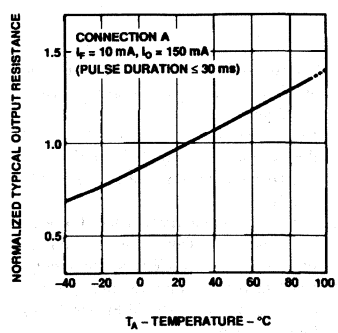


Figure 6. Normalized Typical Output Resistance vs. Temperature.

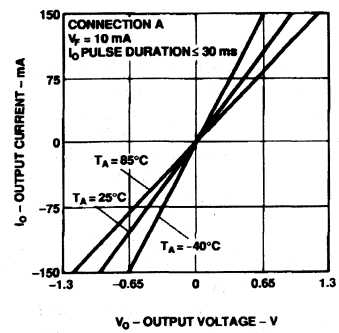


Figure 7. Typical On State Output I-V Characteristics.

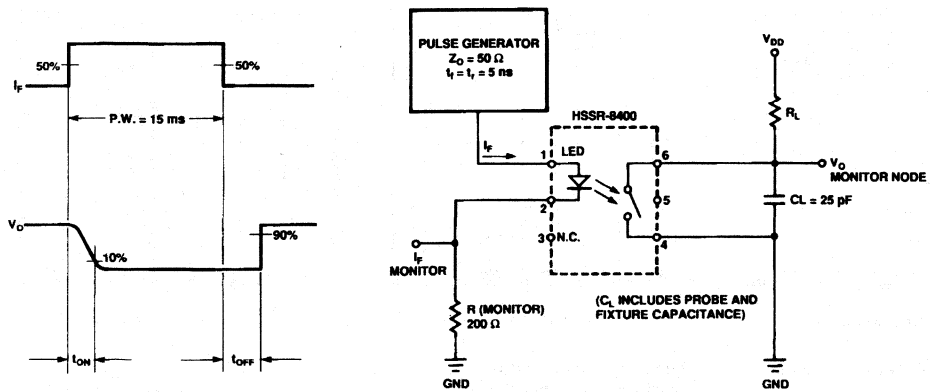


Figure 8. Switching Test Circuit for t_{ON}, t_{OFF}.

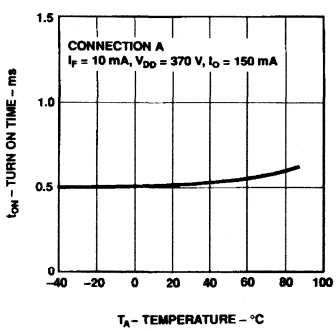


Figure 9. Typical Turn On Time vs. Temperature.

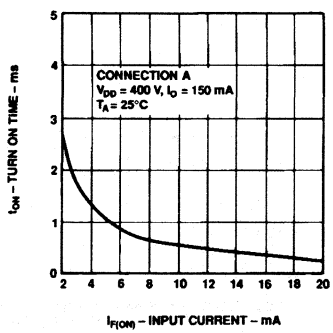


Figure 10. Typical Turn On Time vs. Input Current.

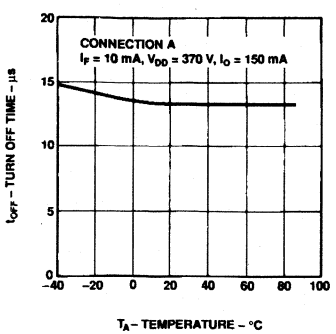


Figure 11. Typical Turn Off Time vs. Temperature.

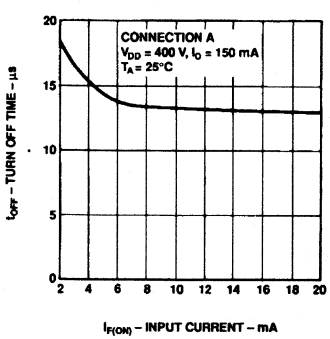


Figure 12. Typical Turn Off Time vs. Input Current.

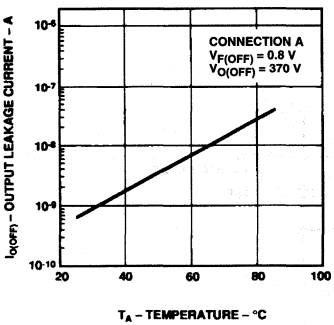


Figure 13. Typical Output Leakage vs. Temperature.

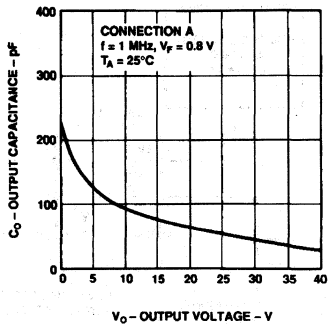


Figure 14. Typical Output Capacitance vs. Output Voltage.

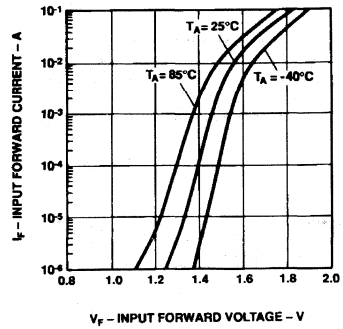


Figure 15. Typical Input Forward Current vs. Input Forward Voltage.

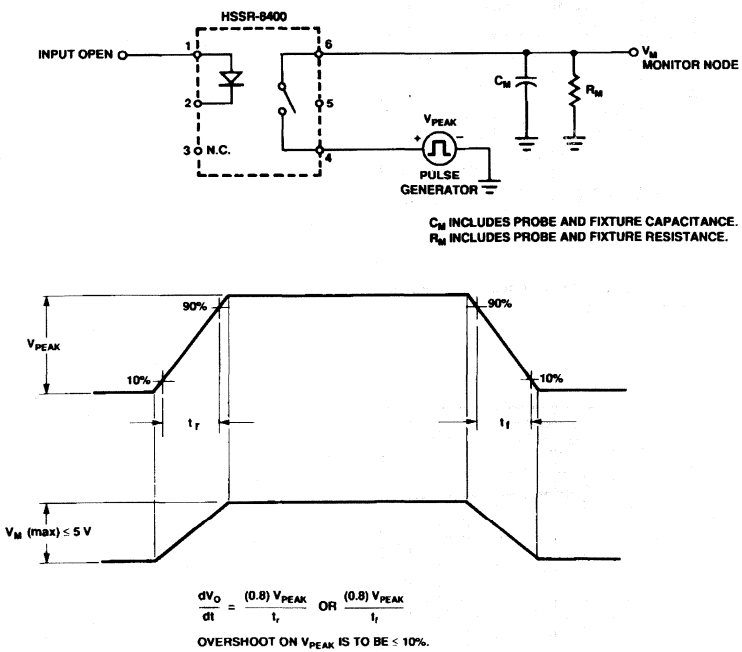


Figure 16. Output Transient Rejection Test Circuit.

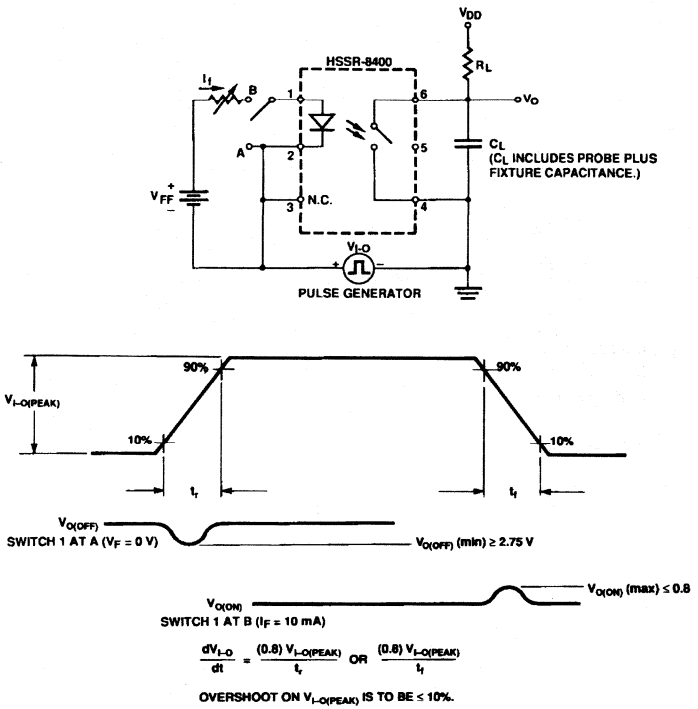


Figure 17. Input-Output Transient Rejection Test Circuit.

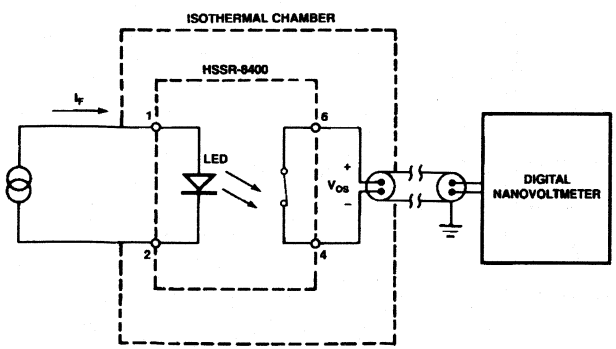
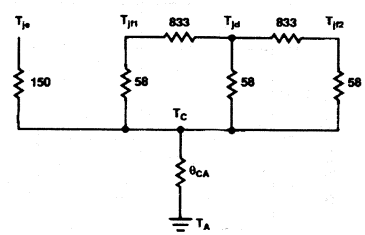


Figure 18. Voltage Offset Test Setup.



T_{jo} = LED JUNCTION TEMPERATURE
T_{j1} = FET 1 JUNCTION TEMPERATURE
T_{j2} = FET 2 JUNCTION TEMPERATURE
T_{jd} = FET DRIVER JUNCTION TEMPERATURE
T_C = CASE TEMPERATURE (MEASURED AT CENTER OF PACKAGE BOTTOM)
T_A = AMBIENT TEMPERATURE (MEASURED 15 cm AWAY FROM THE PACKAGE)
θ_{CA} = CASE-TO-AMBIENT THERMAL RESISTANCE

ALL THERMAL RESISTANCE VALUES ARE IN °C/W.

Figure 19. Thermal Model.

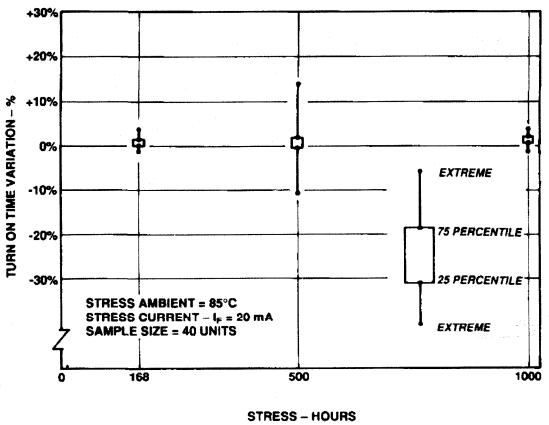


Figure 20. Turn On Time Variation with High Temperature Operating Life.

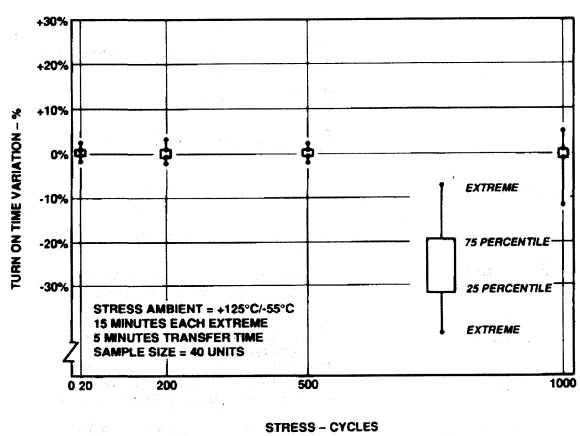


Figure 21. Turn On Time Variation with Temperature Cycling.

Applications Information

Thermal Model

The steady state thermal model for the HSSR-8400 is shown in Figure 19. The thermal resistance values given in this model can be used to calculate the temperatures at each node for a given operating condition. The thermal resistances between the LED and other internal nodes are very large in comparison with the other terms and are omitted for simplicity. The components do, however, interact indirectly through θ_{CA}, the case-to-ambient thermal resistance. All heat generated flows through θ_{CA}, which raises the case temperature T_C accordingly. The value of θ_{CA} depends on the conditions of the board design and is, therefore, determined by the designer.

The typical value for each output MOSFET junction-to-case thermal resistance is specified as 55°C/W. This is the thermal resistance from one MOSFET junction to the case when power is dissipated equally in the MOSFETs. The power dissipation in the FET Driver is negligible in comparison to the MOSFETs.

On-Resistance and Derating Curves

The output on-resistance, R_{ON}, specified in this data sheet, is the resistance measured across the output contact when a pulsed current signal (I_O = 150 mA) is applied to the output pins. The use of a pulsed signal (≤ 30 ms) implies that each junction temperature is equal to the ambient and case temperatures. The steady-state resistance, R_{SS}, on the other hand, is the value of the resistance measured across the output contact when a DC current signal is applied to the output pins for a duration sufficient to reach thermal equilibrium. R_{SS} includes the effects of the temperature rise of each element in the thermal model.

Derating curves are shown in Figures 3 and 4. Figure 3 specifies the maximum average output current allowable for a given ambient or case temperature. Figure 4 specifies the output power dissipation allowable for a given case temperature. Above a case temperature of 93°C, the maximum allowable output current and power dissipation are related by the expression $R_{SS} = P_O(max)/(I_O(max))^2$ from which R_{SS} can be calculated. Staying within the safe area assures that the steady state junction temperatures remain less than 125°C. As an example, for a case temperature of 100°C, Figure 4 shows that the output power dissipation should be limited to less than 0.5 watts. A check with Figure 3B shows that the output current should be limited to less than 150 mA. This yields an R_{SS} of 22 Ω.

Turn On Time Variation

For applications which are sensitive to turn on time, the designer should refer to Figures 20 and 21. These figures show that although there is very little variation in t_{ON} within most of the population, a portion of the distribution will vary with use. The optional peaking circuit shown in Figure 2 can be used to reduce the total turn on time and, consequently, any associated variation.

HEWLETT® PACKARD

Optocoupler Option for 5000 V rms/1 Minute Requirement

Technical Data

OPTION 020

Features

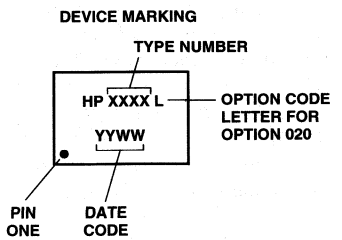
- **Special Construction and Testing**
- **UL Recognition for 5000 V rms/1 Minute Requirement (File No. E55361)**

Description

Option 020 consists of special construction on a wide range of Hewlett-Packard plastic optocouplers. After assembly, each unit is subjected to an equivalent electrical performance test to ensure its capability to withstand 5000 V rms input to output for one minute. This test is recognized by Underwriters Laboratory as proof that these components may be used in many high voltage applications.

Applications

Dielectric withstand voltage ratings are required by Underwriters Laboratory when components are used in certain types of electronic equipment. The voltage rating depends on the type of electronic equipment and the specific application within the equipment. The 5000 V rms/1 Minute dielectric withstand voltage rating provided by Option 020 offers excellent high voltage input to output protection. Some applicable UL documents are listed below.



UL Spec Number	Specification Title
114	Appliance and Business Equipment
347	High Voltage Industrial Control Equipment
508	Industrial Control Equipment
544	Medical and Dental Equipment
773	Plug-in, Locking Type Photocontrols
916	Standard for Energy Management Equipment
1012	Power Supplies
1244	Electrical and Electronic Measuring and Testing Equipment
1410	Television and Video Products
1950	Information Technology Equipment Including Electrical Business Equipment

Specifications

All specifications for optocouplers remain unchanged when this option is ordered. The 5000 V rms/1 Minute capability is validated by a factory 6200 VAC/1 Second dielectric voltage withstand test.

Ordering Information

To obtain this high voltage capability on plastic optocouplers order the standard part number and Option 020.

Examples:

6N135#020
HCPL-2001#020

This option may also be combined with option #300 (gullwing surface mount) or #500 (gullwing in tape & reel).

To obtain these combinations order option #320 or #520 respectively.

Examples:

6N135#320 (gullwing surface mount and 5000 VAC/1 min)
HCPL-2601#520 (gullwing surface mount and 5000 VAC/1 min) in tape & reel

This option is currently available on the following plastic optocouplers.

6N135/6
6N137
6N138/9
HCPL-2502/3
HCPL-2601/11
HCPL-261A/N
HCPL-4562
HCPL-4502/3/4
HCPL-4504/6
HCPL-2530/1/3, -4534
HCPL-2630/1, -4661
HCPL-263A/N
HCPL-2730/1

Contact your local HP Sales Representative concerning availability of this option for optocouplers not listed.

HEWLETT® PACKARD

VDE 0884 V_{IORM} = 630 V peak Option for Plastic Optocouplers

Technical Data

Option 060

Description

Optocouplers are frequently used to provide high voltage insulation. Because optocouplers perform this safety function, they are regulated by many country safety agencies, both at the component level and the equipment level. With Option 060, the products are tested according to VDE 0884 (June 1992 Revision) at V_{IORM} = 630 V peak. HP also offers other various VDE 0884 approved products at different levels of V_{IORM} such as V_{IORM} = 1414 kV peak (HCNWXXXX series) and V_{IORM} = 891 V peak (HCPL-JXXX series).

Refer to the front of the optocoupler section of the current catalog, under Product Safety Regulations section, for a detailed description of VDE 0884 and the partial discharge tests for production and type testing.

Option 060 is available on the following products.

HCPL-2211	**HCPL-2212**
HCPL-2219	**HCPL-2300**
HCPL-2400	**HCPL-261A**
HCPL-261N	**HCPL-2611**
HCPL-3120	**HCPL-3150**
HCPL-4503	**HCPL-4504**
HCPL-4506	**HCPL-4701**

Contact your local HP Sales Representative concerning availablility of this option for optocouplers not listed.

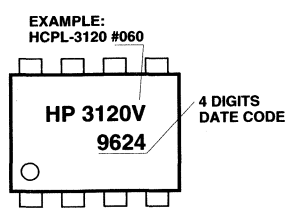
Ordering Information

Specify Part Number followed by Option Number.

Example

HCPL-3120#060

Marketing Information



Insulation Related Specifications

Parameter	Symbol	Value	Units	Conditions
Minimum External Air Gap (External Clearance)	L(101)	7.1	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L(102)	7.4	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity.
Tracking Resistance (Comparative Tracking Index)	CTI	200	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

VDE 0884 Insulation Related Characteristics (Option 060)

***85°C**

HCPL-2211, HCPL-2212, HCPL-2219, HCPL-2300, HCPL-2400, HCPL-2611, HCPL-261A, HCPL-261N, HCPL-4701.

****100°C**

HCPL-3120, HCPL-3150, HCPL-4503 HCPL-4504, HCPL-4506.

Description	Symbol	Characteristic	Units
Installation classification per DIN VDE 0110/1.89, Table 1 for rated mains voltage ≤ 300 V rms		I-IV	
for rated mains voltage ≤ 450 V rms		I-III	
Climatic Classification		55/85/21* 55/100/21**	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	630	V peak
Input to Output Test Voltage, Method b† V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial Discharge < 5 pC	V_{PR}	1181	V peak
Input to Output Test Voltage, Method a† V_{IORM} x 1.5 = V_{PR}, Type and Sample Test, t_m = 60 sec, Partial Discharge < 5 pC	V_{PR}	945	V peak
Highest Allowable Overvoltage† (Transient Overvoltage, t_{ini} = 10 sec)	V_{IOTM}	6000	V peak
Safety Limiting Values (Maximum values allowed in the event of a failure, also see Thermal Derating curve, Figure 1.)			
Case Temperature	T_S	175	°C
Input Current	$I_{S,INPUT}$	230	mA
Output Power	$P_{S,OUTPUT}$	600	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	≥ 10^9	Ω

†Refer to the front of the optocoupler section of the current catalog, under Product Safety Regulations section (VDE 0884), for a detailed description.

Note: Isolation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuits in application.

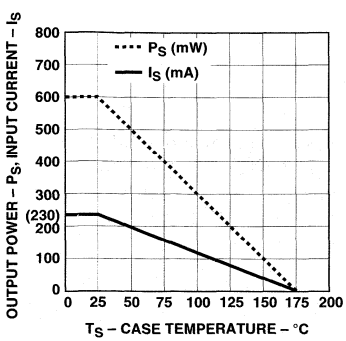


Figure 1. Thermal Derating Curve, Dependence of Safety Limiting Value with Case Temperature per VDE 0884.

Gull Wing Surface Mount Option for Optocouplers and Solid State Relays

Technical Data

Option 300

Description

Option 300 is available on most optocouplers and solid state relays. It consists of standard dual-in-line package devices with gull wing leads. The lead profile is designed to be compatible with standard surface mount processes.

Option 300 enables electronic component assemblers to include Hewlett-Packard optocouplers and solid state relays on a PCB that utilizes surface mount processes. These options do not require "through holes" in a PCB. This reduces board costs, while potentially increasing assembly rates and component density per board. For the maximum solder reflow thermal profile, refer to Figure 3.

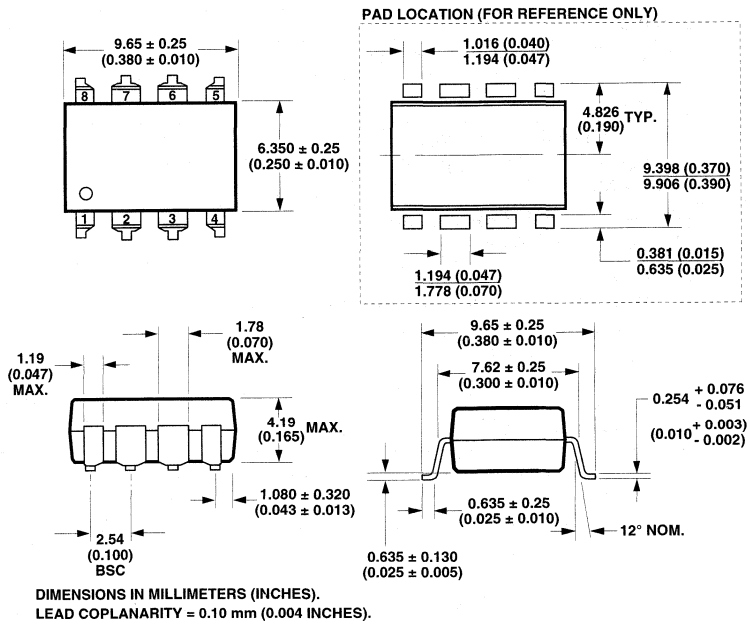


Figure 1. 8-Pin 300 Mil Package.

Ordering Information

To obtain optocouplers and solid state relays with gull wing leads, order the standard part number and Option 300.

Example:

HCPL-2630#300

Option 300 (300 mil package) is shipped in tubes, with 50 units per tube. Option 300 (400 mil package) is shipped in tubes with 42 units per tube. To obtain optocouplers and solid state relays with gull wing leads shipped in tape and reel, order Option 500[1] instead of Option 300.

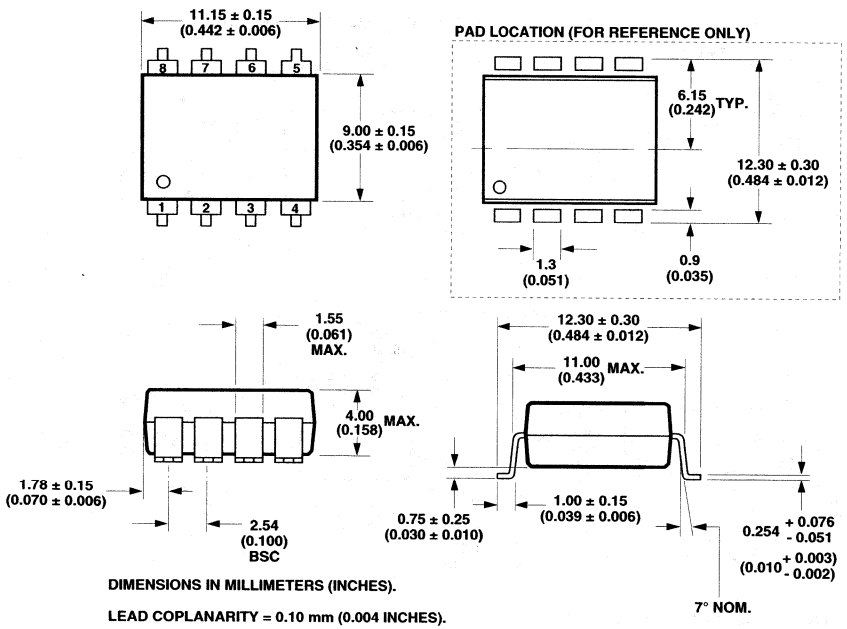


Figure 2. 8 Pin 400 Mil Package.

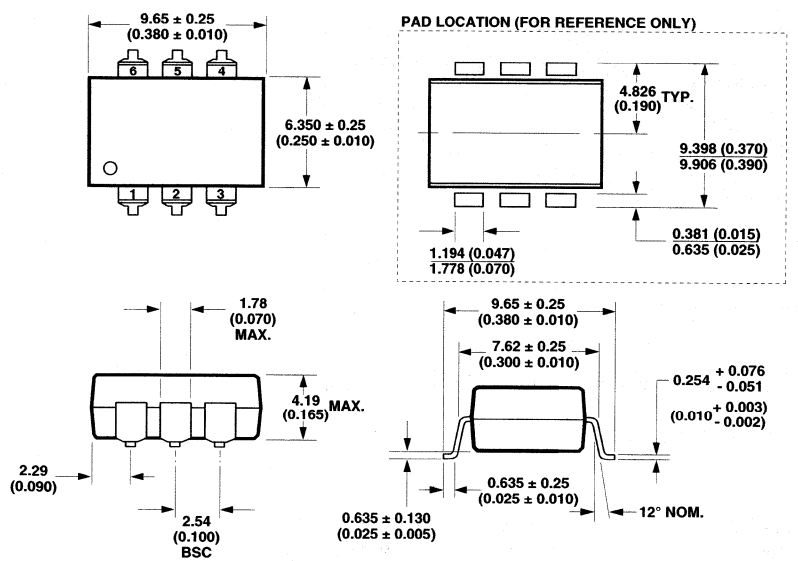


Figure 3. 6 Pin 300 Mil Package.

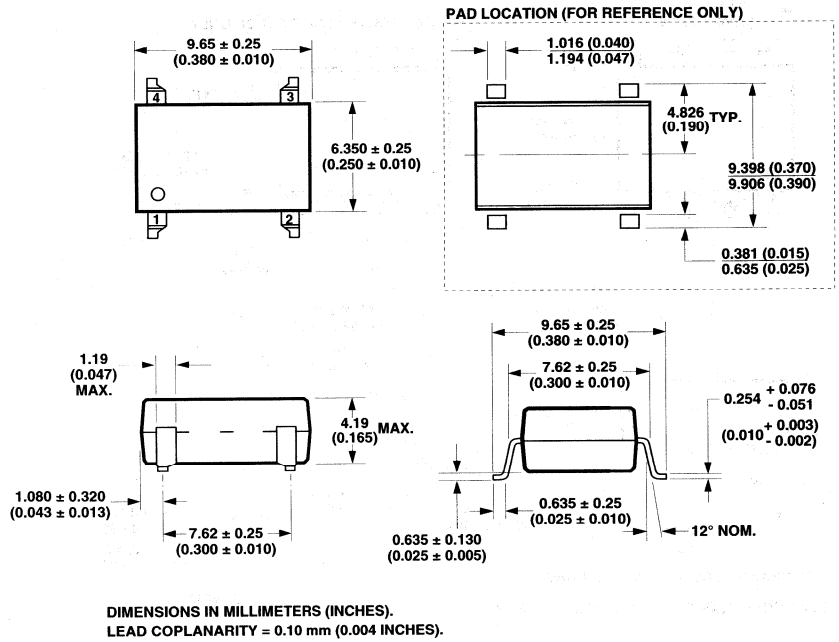
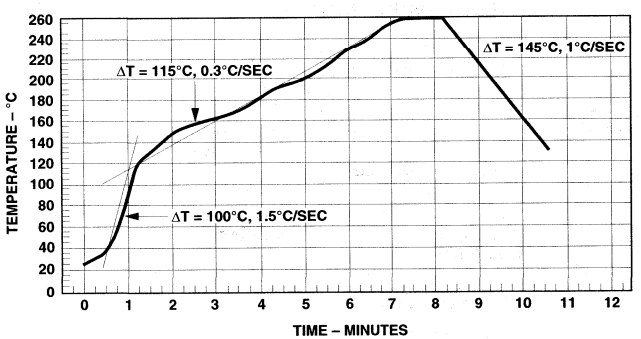


Figure 4. 4 Pin 300 Mil Package.



NOTE: USE OF NON-CHLORINE ACTIVATED FLUXES IS HIGHLY RECOMMENDED.

Figure 5. Maximum Solder Reflow Thermal Profile.[4]

Notes:

1. Tape and Reel Option 500 can also be obtained for small outline SOIC-8 optocouplers.
2. Dimensions in mm (INCHES)
   TOLERANCES: xx.xx = .01
   xx.xxx = .001
   (unless otherwise specified)
3. Lead coplanarity for Option 300 product is 0.10 mm (0.004").
4. Lead coplanarity definition: The maximum distance between the lowest and the highest pin when the package rests on a perfectly flat surface.

Tape and Reel Packaging Option for Optocouplers and Solid State Relays

Technical Data

Option 500

Description

Option 500 is available on most optocouplers and solid-state relays. It consists of devices with gull wing leads, shipped in a tape and reel. The following package styles and their corresponding tape and reel are available.

Style A: Small outline optocouplers with the SOIC-8 footprint, which are supplied in 12 mm wide tape on 33 cm diameter reels with 1500 units per reel.

Style B: 300 mil gull wing package which are supplied in 16 mm wide tape on 33 cm diameter reels with 1000 units per reel.

Style C: 400 mil gull wing packages which are supplied in 24 mm wide tape on 33 cm diameter reels with 750 units per reel.

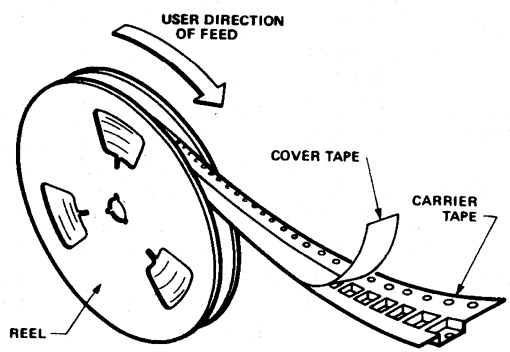
The above tape and reels conform to the EIA standard RS 481 Rev. A specifications.

Ordering Information

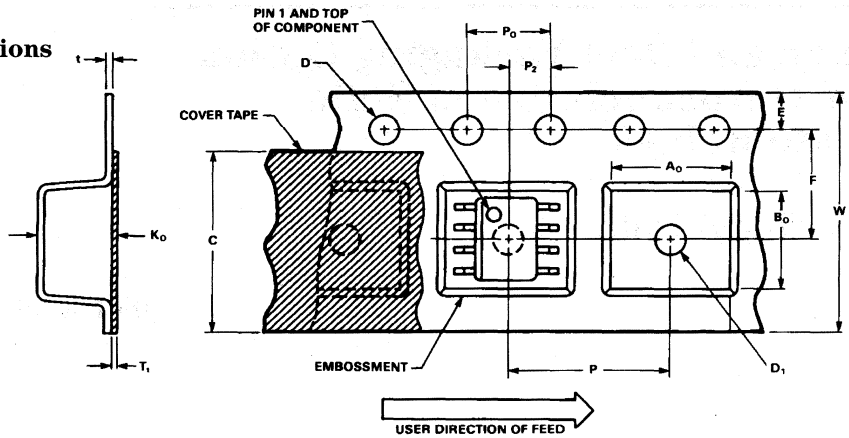
To obtain this tape and reel option for optocouplers and solid-state relays, order the standard part number with Option 500. All Option 500 units are supplied with the gull wing leads. Hence, there is no need to order Gull Wing Option 300 along with Option 500.

Example:
HCPL-2601
Option 500

The minimum order quantities are 1500 for Style A, 1000 for Style B, and 750 for Style C.



Tape Dimensions



Item		Symbol	Size (mm) Style A (SOIC-8)	Style B (300 mil Gull Wing)	Style C (400 mil Gull Wing)
Cavity	Length	A_0	6.30 ± 0.10	10.30 ± 0.10	12.80 ± 0.10
	Width	B_0	5.35 ± 0.10	10.30 ± 0.10	11.50 ± 0.10
	Depth	K_0	3.50 ± 0.10	4.90 ± 0.10	5.20 ± 0.10
	Pitch	P	8.00 ± 0.10	12.00 ± 0.10	16.00 ± 0.10
	Bottom Hole Diameter	D_1	1.50 min.	1.50 min.	2.00 min.
	Component Rotation in Cavity (See Fig. 1).		15° max.	15° max.	15° max.
Perforation	Diameter of Sprocket Holes	D	1.55 ± 0.05	1.55 ± 0.05	1.55 ± 0.05
	Pitch	P_0	4.00 ± 0.10	4.00 ± 0.10	4.00 ± 0.10
	Position	E	1.75 ± 0.10	1.75 ± 0.10	1.75 ± 0.10
Cover Tape	Width	C	9.05 ± 0.10	13.05 ± 0.10	21.05 ± 0.10
	Tape Thickness	T_t	0.065 ± 0.01	0.065 ± 0.01	0.066 ± 0.01
Carrier Tape	Width	W	12.00 ± 0.30	16.00 ± 0.30	24.00 ± 0.30
	Thickness	t	0.30 ± 0.05	0.30 ± 0.05	0.30 ± 0.05
Distance Between Centerline	Cavity to Perforation (Width Direction)	F	5.50 ± 0.05	7.50 ± 0.10	11.50 ± 0.10
	Cavity to Perforation (Length Direction)	P_2	2.00 ± 0.05	2.00 ± 0.10	2.00 ± 0.10

Note:
1. Drawing is not to scale.

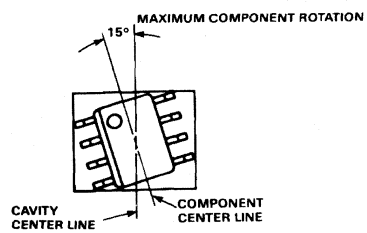
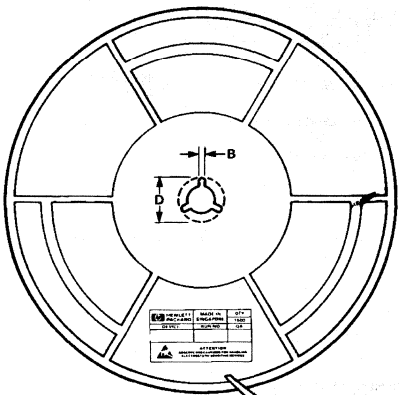
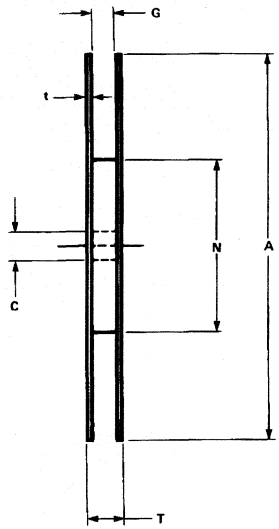


Figure 1.

Reel Dimensions



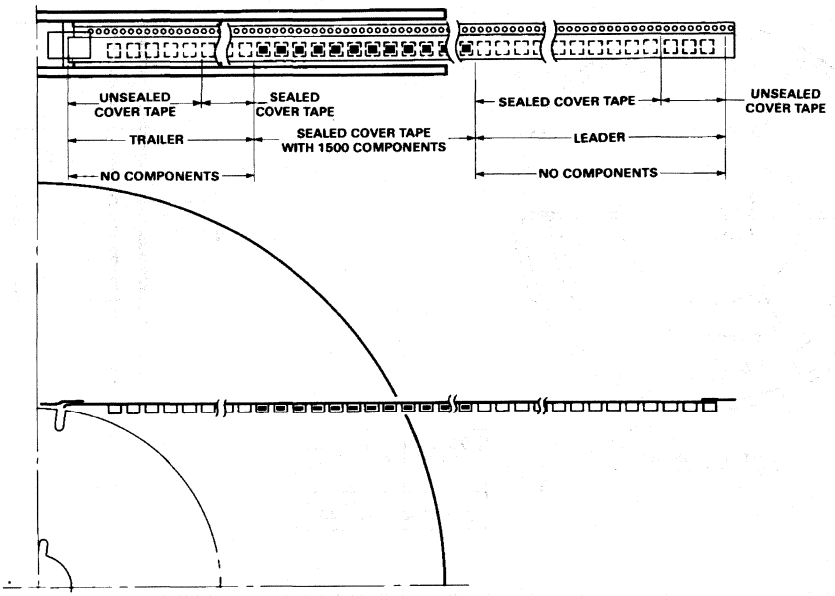


HEWLETT PACKARD	MADE IN SINGAPORE	QTY 1500
DEVICE	RUN NO.	QA
ATTENTION OBSERVE PRECAUTIONS FOR HANDLING ELECTROSTATIC SENSITIVE DEVICES		

Item			Symbol	Size (mm) Style A (SOIC-8)	Style B (8-pin Gull Wing)	Style C (400 mil Gull Wing)
Flange	Diameter		A	$330^{+0.0}_{-0.2}$	$330^{+0.0}_{-0.2}$	$330^{+0.0}_{-0.2}$
	Thickness (see note 2)		t	2.00	2.00	2.00
	Internal Width		G	$12.4^{+2.0}_{-0.0}$	$16.4^{+2.0}_{-0.0}$	$24.4^{+2.0}_{-0.0}$
	External Width		T	$16.4^{+2.0}_{-0.0}$	$20.4^{+2.0}_{-0.0}$	$28.4^{+2.0}_{-0.0}$
Hub	Outer Diameter		N	178.0 ± 0.1	100.0 ± 0.1	100.0 ± 0.1
	Spindle Hole Diameter		C	13.0 ± 0.2	13.0 ± 0.2	13.0 ± 0.2
	Key Slit	Width	B	1.9 ± 0.4	1.9 ± 0.4	1.9 ± 0.4
		Diameter	D	$21.0^{+1.0}_{-0.0}$	$21.0^{+1.0}_{-0.0}$	$21.0^{+1.0}_{-0.0}$

Notes:
1. Drawing is not to scale.
2. Typical value only.

Packing – Leader and Trailer



Item		Size (mm)		
		Style A (SOIC-8)	**Style B (300 mil Gull Wing)**	**Style C (400 mil Gull Wing)**
Leader	Unsealed Cover Tape	24 (3 pockets)	24 (2 pockets)	80 (5 pockets)
	Sealed Cover Tape with Empty Cavities	504 (63 pockets)	480 (40 pockets)	480 (30 pockets)
Trailer	Unsealed Cover Tape	40 (5 pockets)	24 (2 pockets)	80 (5 pockets)
	Sealed Cover Tape with Empty Cavities	304 (38 pockets)	240 (20 pockets)	480 (30 pockets)

Materials

A. Carrier Tape:

Material: Carbon coating on both sides of polyvinyl chloride sheet.
Color: Black
Tensile strength: 530 Kgf/cm^2
Resistivity: $R_S = 10^6\ \Omega/cm^2$
$R_V = 10^{11}\ \Omega/cm^3$

B. Cover Tape:

Material: Cohesive failure type consisting of olephine-type resin. Static dissipative agent treated.
Color: Transparent
Tensile strength: 500 Kgf/cm^2
Peel-off strength: 40 ± 30 g
Resistivity: $R_S = 10^{11}\ \Omega/cm^2$

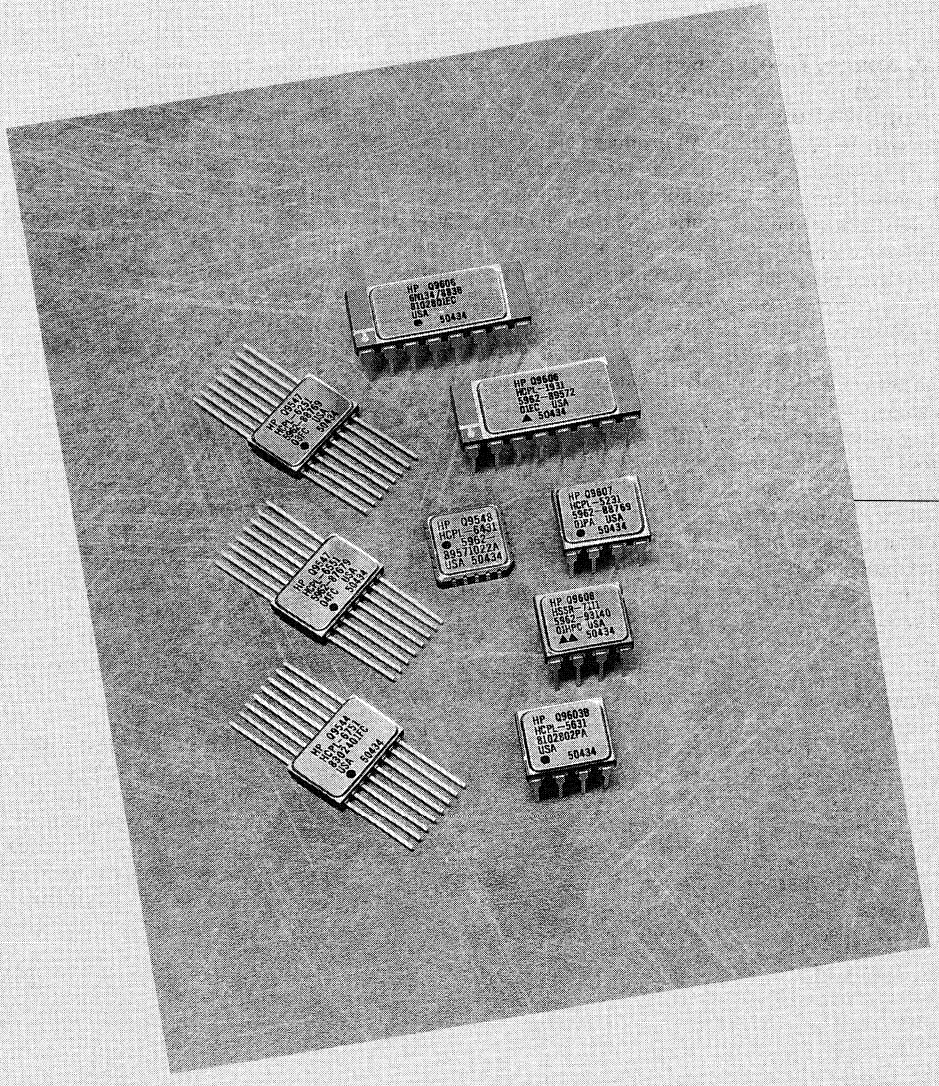
C. Reel:

Material: Plastic

HEWLETT® PACKARD

Hermetic and Hi-Rel Optocouplers

Data Sheet Index 1-492
Product Selection Guide 1-493
Applications 1-606



Hermetic and Hi-Rel Optocouplers

For Military, Space, Life Critical and High Reliability Applications

Choose from Hewlett-Packard's broad line of high performance optocouplers to meet your military, space, life critical and high reliability applications. There are four ceramic package styles to choose from: 8 and 16 pin dual-in-line packages, 20 terminal leadless chip carriers (LCC), and, our newest offering, 16 pin flat packages. Available in most package styles are six basic families of optocouplers: the new Power Transistor Interface, High Speed Logic Gate Optocouplers, High Speed Transistor Optocouplers, High Gain Optocouplers, AC/DC to Logic Interface, and the Power MOSFET.

Hewlett-Packard's Class H (military approved) and Class K (space approved) hermetic optocouplers are classified by the Department of Defense as hybrid microcircuits and are manufactured in the United States on a MIL-PRF-38534 certified and qualified line. Hewlett-Packard is listed as a qualified supplier for both Class H and Class K product on QML-38534.

All product families are represented by commercial grade units and by high reliability tested units. All high reliability Class H products are also offered with recognized DESC part numbers either from DESC Drawings, Standard Military Drawings (SMD's), or from DESC's "One Part, One Part Numbering System." All high reliability devices are tested and guaranteed over the full military temperature range of -55°C to +125°C.

To give maximum opportunity to utilize recognized DESC parts, all 26 hermetic products are under DESC drawings. Dual part marking of the HP part number and the DESC Drawing is standard on all Class H product.

New this year is our standard line of Class K devices which extend over the entire isolation product presentation with the exception of the MOSFET device. We're very excited about this new offering which may allow "off-the-shelf" Class K devices to be procured that require no source control drawing to be generated. Note that while we are not currently able to supply a certified Class K MOSFET device, we can provide upscreening to the Class K requirements of MIL-PRF-38534.

Hewlett-Packard is both DESC certified and qualified to manufacture Class H (military approved) and Class K (space approved) hermetic optocouplers per the requirements of MIL-PRF-38534 Option 1 QCI (in-line inspection) *or* Option 2 QCI (end-of-line inspection). All catalog Class H and Class K devices are processed per Option 1 QCI. Custom devices are available processed to either option.

Option 1 Screening and Quality Conformance Inspection is outlined on the following page. Custom Option 2 programs may include full Group A, B, C, and D inspections. Screening is identical for both options.

Screening per MIL-PRF-38534

Procedure	Method	Conditions	Class H	Class K
Nondestruct bond pull	2023		100%	100%
Internal visual	2017		100%	100%
Temperature Cycle	1010	Condition C, -65°C to +125°C, 10 cycles	100%	100%
Constant Acceleration	2001	Condition A, 5 Kg's, Y1 and Y2	100%	100%
Visual Inspection		Internal requirements	100%	100%
PIND	2020	Condition A	N/A	100%
Serialization			N/A	100%
Pre-Burn-In Elec. Test		Group A, subgroup 1 (except I_{I-O}) (DC @ +25°C)	100%	100%
Burn-In	1015	Condition B, +125°C, 160 hours Condition B, +125°C, 320 hours	100%	 100%
Interim Elec. Test		Group A, subgroup 1 (except I_{I-O}) (DC @ +25°C)	N/A	100%
Post Burn-In Elec. Test		Group A, subgroup 1, (DC @ +25°C), 10% PDA Group A, subgroup 1, (DC @ +25°C), 2% PDA	100%	 100%
Final Elec. Test		Group A, subgroup 2 (DC @ +125°C) Group A, subgroup 3 (DC @ -55°C) Group A, subgroup 9 (AC @ +25°C)	100% 100% 100%	100% 100% 100%
Fine Leak	1014	Condition A	100%	100%
Gross Leak	1014	Condition C	100%	100%
Radiographics	2012		N/A	100%
External Visual	2009		100%	100%

Option 1 Quality Conformance Inspection

Group A Testing

Group A testing is satisfied per the in-line verification testing requirements of MIL-PRF-38534 for Class H devices.

Group A testing is performed via in-line sample testing requirements of MIL-PRF-38534 for Class K devices.

Group B Testing

Group B testing is satisfied by performing in-line inspection sample monitoring as required by MIL-PRF-38534.

Group C Testing

Group C testing is performed only on the first inspection lot and as required to evaluate or qualify changes per the requirements of MIL-PRF-38534.

Group D Testing

Group D testing is not performed. Note that Group D requirements are performed during incoming inspection element evaluation.

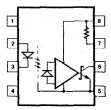
Please be advised that Class H and Class K devices have very similar Screening and Quality Conformance Inspection requirements as shown above. Class K devices, however, have substantially more stringent element evaluation and assembly criteria. The quality and reliability of a Class K device must be built in, not tested out.

HEWLETT® PACKARD

Hermetic and Hi-Rel Optocouplers Data Sheet Index

- Intelligent Power Modules and Gate Drive Interface Optocouplers 1-498
- Hermetically Sealed, Low I_F, Wide V_{CC}, Logic Gate Optocouplers 1-512
- Hermetically Sealed, Very High Speed Logic Gate Optocouplers 1-524
- Hermetically Sealed, High Speed, High CMR, Logic Gate Optcouplers 1-536
- Dual Channel Line Receiver Hermetic Optocoupler 1-548
- Hermetically Sealed, Transistor Output Optocouplers for Analog and Digital Applications 1-559
- Hermetically Sealed, Low I_F, Wide V_{CC}, High Gain Optocouplers 1-571
- AC/DC to Logic Interface Hermetically Sealed Optocouplers 1-583
- 90 V/1.0 Ω, Hermetically Sealed, Power MOSFET Optocoupler 1-593

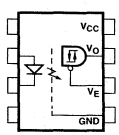
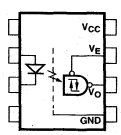
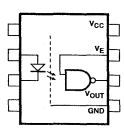
Power Transistor Interface Optocoupler

Functional Diagram	Device Part No.	Config-uration	Description	Application	Max. t(prop)	Max. PWD	Min. CTR	CMR	With-stand Test Voltage	Page No.
	**HCPL-5300** 1/	8-Pin DIP	Intelligent Power Module and Gate Drive Interface	IPM isolation, Isolated IGBT/ MOSFET gate drive, AC and brushless DC motor drives, Industrial inverters	0.65 µs	0.45 µs	30% at I_F = 10 mA	10 kV/ µs min at V_{CM} = 1000 V	1500 Vdc	1-498

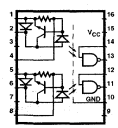
1. Part number HCPL-5301 or DESC SMD 5962-9685201HPX represents Mil-Prf-38534 Class H product. These part numbers are approved for military or high reliability applications. The Class K (space approved) part number is HCPL-530K.

Bold type = new product

High Speed Logic Gate Optocouplers

Single Channel Functional Diagram	Device	Config-uration	Description	Application	Typical Data Rate (NRZ)	Common Mode	Specified Input Current	With-stand Test Voltage	Page No.
	HCPL-5200 1/	8 Pin DIP	Single channel hermetically sealed wide supply voltage optocoupler	High speed logic ground isolation, LSTTL, TTL, CMOS logic interface	5 M bit/s	1000 V/µs at V_{CM} = 50 V	2.0 mA to 8.0 mA	1500 Vdc	1-512
	HCPL-5230 2/	8 Pin DIP	Dual channel hermetically sealed wide supply voltage optocoupler						
	HCPL-6230 3/	20 Terminal LCCC							
	HCPL-6250 4/	16 Pin Flat Pack	Quad channel hermetically sealed wide supply voltage optocoupler						
	HCPL-5400 5/	8 Pin DIP	Single channel hermetically sealed high speed optocoupler	High speed logic isolation, A/D and parallel/serial conversion	40 M bit/s	500 V/µs at V_{CM} = 50 V	6.0 mA to 10.0 mA		1-524
	HCPL-5430 6/	8 Pin DIP	Dual channel hermetically sealed high speed optocoupler	High speed logic isolation, Communications, Networks, Computers					
	HCPL-6430 7/	20 Terminal LCCC							
	6N134 8/	16 Pin DIP	Dual channel hermetically sealed high speed logic gate	Line receiver, Ground isolation for high reliability systems	10 M bit/s	1000 V/µs at V_{CM} = 50 V	10 mA		1-536
	HCPL-5600 9/	8 Pin DIP	Single channel hermetically sealed high speed logic gate						
	HCPL-5630 10/	8 Pin DIP	Dual channel hermetically sealed high speed logic gate						
	HCPL-6630 11/	20 Terminal LCCC							
	HCPL-6650 12/	16 Pin Flat Pack	Quad channel hermetically sealed logic gate						

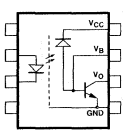
High Speed Logic Gate Optocouplers, continued

Single Channel Functional Diagram	Device	Config-uration	Description	Application	Typical Data Rate (NRZ)	Common Mode	Specified Input Current	With-stand Test Voltage	Page No.
	HCPL-1930 13/	16 Pin DIP	Dual channel hermetically sealed high CMR line receiver optocoupler	Line receiver, High speed logic ground isolation in high ground or induced noise environments	10 M bit/s	1000 V/μs at V_{CM} = 50 V	10 mA	1500 Vdc	1-548

Note: Each part number referenced below is approved for military, space or high reliability applications.

1. Part number HCPL-5201 or DESC SMD 5962-8876801PX represent Mil-Prf-38534 Class H product. The Class K (space approved) part number is HCPL-520K.
2. Part number HCPL-5231 or DESC SMD 5962-8876901PX represent Mil-Prf-38534 Class H product. The Class K (space approved) part number is HCPL-523K.
3. Part number HCPL-6231 or DESC SMD 5962-88769022A represent Mil-Prf-38534 Class H product. The Class K (space approved) part number is HCPL-623K.
4. Part number HCPL-6251 or DESC SMD 5962-8876903FC represent Mil-Prf-38534 Class H product. The Class K (space approved) part number is HCPL-625K.
5. Part number HCPL-5401 or DESC SMD 5962-8957001PX represent Mil-Prf-38534 Class H product. The Class K (space approved) part number is HCPL-540K.
6. Part number HCPL-5431 or DESC SMD 5962-8957101PX represent Mil-Prf-38534 Class H product. The Class K (space approved) part number is HCPL-543K.
7. Part number HCPL-6431 or DESC SMD 5962-89571022A represent Mil-Prf-38534 Class H product. The Class K (space approved) part number is HCPL-643K.
8. Part number 6N134/883B or DESC SMD 8102801EX represent Mil-Prf-38534 Class H product. The Class K (space approved) part number is HCPL-268K.
9. Part number HCPL-5601 or DESC SMD 5962-9085501HPX represent Mil-Prf-38534 Class H product. The Class K (space approved) part number is HCPL-560K.
10. Part number HCPL-5631 or DESC SMD 8102802PX represent Mil-Prf-38534 Class H product. The Class K (space approved) part number is HCPL-563K.
11. Part number HCPL-6631 or DESC SMD 81028032A represent Mil-Prf-38534 Class H product. The Class K (space approved) part number is HCPL-663K.
12. Part number HCPL-6651 or DESC SMD 8102804FC represent Mil-Prf-38534 Class H product. The Class K (space approved) part number is HCPL-665K.
13. Part number HCPL-1931 or DESC SMD 5962-8957201PX represent Mil-Prf-38534 Class H product. The Class K (space approved) part number is HCPL-193K.

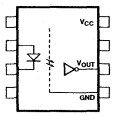
High Speed Transistor Optocouplers

Single Channel Functional Diagram	Device	Config-uration	Description	Application	Typical Data Rate (NRZ)	Current Transfer Ratio	Specified Input Current	With-stand Test Voltage	Page No.
	4N55 1/	16 Pin DIP	Dual channel hermetically sealed analog optical coupler	Line receiver, Analog signal ground isolation, Switching power supply feedback element	700k bit/s	9% Min.	16 mA	1500 Vdc	1-559
	HCPL-5500 2/	8 Pin DIP	Single channel hermetically sealed analog optical coupler						
	HCPL-5530 3/	8 Pin DIP	Dual channel hermetically sealed analog optical coupler						
	HCPL-6530 4/	20 Terminal LCCC							
	HCPL-6550 5/	16 Pin Flat Pack	Quad channel hermetically sealed analog optical coupler						

Note: Each part number referenced below is approved for military, space or high reliability applications.

1. Part number 4N55/883B or DESC SMD 5962-8767901EX represent Mil-Prf-38534 Class H product. The Class K (space approved) part number is HCPL-257K.
2. Part number HCPL-5501 or DESC SMD 5962-9085401HPX represent Mil-Prf-38534 Class H product. The Class K (space approved) part number is HCPL-550K.
3. Part number HCPL-5531 or DESC SMD 5962-8767902PX represent Mil-Prf-38534 Class H product. The Class K (space approved) part number is HCPL-553K.
4. Part number HCPL-6531 or DESC SMD 5962-87679032A represent Mil-Prf-38534 Class H product. The Class K (space approved) part number is HCPL-653K.
5. Part number HCPL-6551 or DESC SMD 5962-8767904FC represent Mil-Prf-38534 Class H product. The Class K (space approved) part number is HCPL-655K.

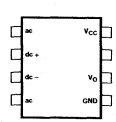
High Gain Optocouplers

Single Channel Functional Diagram	Device	Config-uration	Description	Application	Typical Data Rate (NRZ)	Current Transfer Ratio	Specified Input Current	With-stand Test Voltage	Page No.
	6N140A 1/	16 Pin DIP	Quad channel hermetically sealed low input current high gain optocoupler	Line receiver, Low power ground isolation	100 k bit/s	300% Min.	0.5 mA to 5.0 mA	1500 Vdc	1-571
	HCPL-5700 2/	8 Pin DIP	Single channel hermetically sealed high gain optocoupler	Line receiver, Low power ground isolation, TTL/TTL, LSTTL/TTL, CMOS/TTL					
	HCPL-5730 3/	8 Pin DIP	Dual channel hermeticall sealed high gain optocoupler	Line receiver, Low power ground isolation, Polarity sensing					
	HCPL-6730 4/	20 Terminal LCCC							
	HCPL-6750 5/	16 Pin Flat Pack	Quad channel hermetically sealed high gain optocoupler						

Note: Each part number referenced below is approved for military, space or high reliability applications.

1. Part number 6N140A/883B or DESC SMD 8302401EX represent Mil-Prf-38534 Class H product. The Class K (space approved) part number is HCPL-177K.
2. Part number HCPL-5701 or DESC SMD 5962-8981001PX represent Mil-Prf-38534 Class H product. The Class K (space approved) part number is HCPL-570K.
3. Part number HCPL-5731 or DESC SMD 5962-8978501PX represent Mil-Prf-38534 Class H product. The Class K (space approved) part number is HCPL-573K.
4. Part number HCPL-6731 or DESC SMD 5962-89785022A represent Mil-Prf-38534 Class H product. The Class K (space approved) part number is HCPL-673K.
5. Part number HCPL-6751 or DESC SMD 8302401FC represent Mil-Prf-38534 Class H product. The Class K (space approved) part number is HCPL-675K.

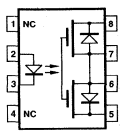
AC/DC to Logic Interface Optocoupler

Functional Diagram	Device	Config-uration	Description	Application	Typical Data Rate	Input Threshold Current	Output Current	With-stand Test Voltage	Page No.
	HCPL-5760 1/	8 Pin DIP	Single channel hermetically sealed threshold sensing optocoupler	Limit switch sensing, Low voltage detector relay contact monitor	10 kHz	2.5 mA TH+ 1.3 mA TH–	2.6 mA	1500 Vdc	1-583

Note:

1. Part number HCPL-5761 or DESC SMD 5962-8947701PX represent Mil-Prf-38534 Class H product. These part numbers are approved for military or high reliability applications. The Class K (space approved) part number is HCPL-576K.

Power MOSFET Optocoupler

Functional Diagram	Device	Config-uration	Description	Application	Output With-Stand Voltage	Output On-Resist-ance	Max. Load Current	Max. Off-State Leakage	Input/ Output Insulation	Page No.
	HSSR-7110 1/	8 Pin DIP	90 V/1.0 Ω hermetically sealed power MOSFET optocoupler	Standard 28 Vdc and 48 Vdc load driver, Standard 24 Vac load driver, ac/dc Electro-mechanical and solid state relay replacement	90	1.0 Ω	0.8 A ac 1.6 A dc	250 mA	1500 Vdc	1-593

Note:

1. Part number HSSR-7111 or DESC SMD 5962-9314001HPX represent Mil-Prf-38534 Class H product. These part numbers are approved for military or high reliability applications.

Hermetic HIgh Performance Optocouplers

Functionally Equivalent Part Types

Package Style	16 Pin DIP		8 Pin DIP		16 Pin Flat Pack	20 Terminal LCCC	Closest Plastic Equivalent
# of Channels	**Quad (4)**	**Dual (2)**	**Dual (2)**	**Single (1)**	**Quad (4)**	**Dual (2)**	
Function							
Darlington Output, Low Input Current, 100 kBd	6N140A **6N140A/883B** *8302401*		HCPL-5730 **HCPL-5731** *5962-8978501*	HCPL-5700 **HCPL-5701** *5962-8981001*	HCPL-6750 **HCPL-6751** *8302401*	HCPL-6730 **HCPL-6731** *5962-8978502*	6N138 or 6N139
Transistor Output, High CMR, 700 kBd		4N55 **4N55/883B** *5962-8767901*	HCPL-5530 **HCPL-5531** *5962-8767902*	HCPL-5500 **HCPL-5501** *5962-9085401*	HCPL-6550 **HCPL-6551** *5962-8767904*	HCPL-6530 **HCPL-6531** *5962-8767903*	6N135/6
High Speed Logic Output, 10 Mbaud	Special P/N	6N134 **6N134/883B** *8102801*	HCPL-5630 **HCPL-5631** *8102802*	HCPL-5600 **HCPL-5601** *5962-9085501*	HCPL-6650 **HCPL-6651** *8102804*	HCPL-6630 **HCPL-6631** *8102803*	HCPL-2601 or 6N137
High Speed Logic, Input Regulation, 10 Mbaud		HCPL-1930 **HCPL-1931** *5962-8957201*					HCPL-2602
Wide V_{CC} from 4.5 to 20 Volts, High CMR, 5 Mbaud			HCPL-5230 **HCPL-5231** *5962-8876901*	HCPL-5200 **HCPL-5201** *5962-8876801*	HCPL-6250 **HCPL-6251** *5962-8876903*	HCPL-6230 **HCPL-6231** *5962-8876902*	HCPL-2200 or HCPL-2230
Very High Speed Logic, 20 Mbaud			HCPL-5430 **HCPL-5431** *5962-8957101*	HCPL-5400 **HCPL-5401** *5962-8957001*		HCPL-6430 **HCPL-6431** *5962-8957102*	HCPL-2400
AC/DC to Logic Interface				HCPL-5760 **HCPL-5761** *5962-8947701*			HCPL-3700
Intelligent Power Module and Gate Drive Interface				HCPL-5300 **HCPL-5301** *5962-9685201*			HCPL-4506
Power MOSFET (relay replacement)				HSSR-7110 **HSSR-7111** *5962-9314001*			

Standard Type refers to commercial product.
Bold type refers to MIL-PRF-38534 Class H Product.
Italic type refers to DESC Drawing parts. Note that these numbers do not include package and lead extention codes. See individual data sheets for package and lead availabilities.

HEWLETT® PACKARD

Intelligent Power Module and Gate Drive Interface Optocouplers

Technical Data

HCPL-5300
HCPL-5301
5962-96852

Features

- **Performance Specified Over Full Military Temperature Range: -55°C to 125°C**
- **Fast Maximum Propagation Delays**
  t_{PHL} = 450 ns,
  t_{PLH} = 650 ns
- **Minimized Pulse Width Distortion (PWD = 450 ns)**
- **High Common Mode Rejection (CMR): 10 kV/μs at V_{CM} = 1000 V**
- **CTR > 30% at I_F = 10 mA**
- **1500 Vdc Withstand Test Voltage**
- **Manufactured and Tested on a MIL-PRF-38534 Certified Line**
- **Hermetically Sealed Packages**
- **Dual Marked with Device Part Number and DESC Drawing Number**
- **QML-38534, Class H and K**
- **HCPL-4506 Function Compatibility**

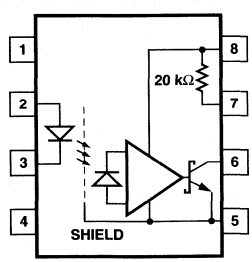
Applications

- **Military and Space**
- **High Reliability Systems**
- **Harsh Industrial Environments**
- **Transportation, Medical, and Life Critical Systems**
- **IPM Isolation**
- **Isolated IGBT/MOSFET Gate Drive**
- **AC and Brushless DC Motor Drives**
- **Industrial Inverters**

Description

The HCPL-5300/5301 devices consist of a GaAsP LED optically coupled to an integrated high gain photo detector in a hermetically sealed package. The products are capable of operation and storage over the full military temperature range and can be purchased as either standard product or with full MIL-PRF-38534 Class Level H or K testing or from the DESC Drawing 5962-96852. All devices are manufactured and tested on a MIL-PRF-38534 certified line and are included in the DESC Qualified Manufacturers List QML-38534 for Hybrid Microcircuits. Minimized propagation delay difference between devices make these optocouplers excellent solutions for improving inverter efficiency through reduced switching dead time. An on chip 20 kΩ output pull-up resistor can be enabled by shorting output pins 6 and 7, thus eliminating the need for an external pull-up resistor in common IPM applications. Specifications and performance plots are given for typical IPM applications.

Schematic Diagram



Truth Table

LED	V_O
ON	L
OFF	H

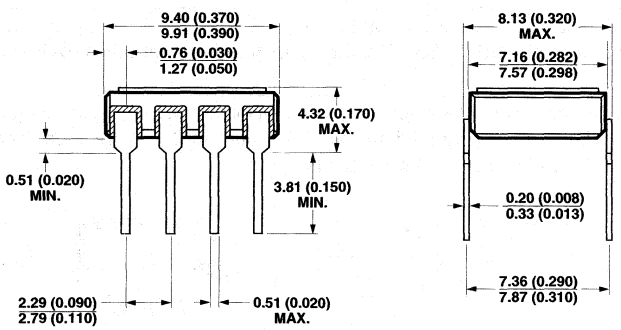
The connection of a 0.1 μF bypass capacitor between pins 5 and 8 is recommended.

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Selection Guide-Package Styles and Lead Configuration Options

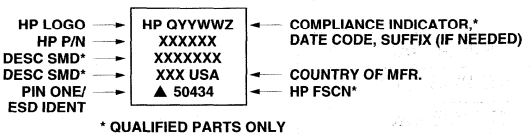
HP Part # and Options	
Commercial	HCPL-5300
MIL-PRF-38534, Class H	HCPL-5301
MIL-PRF-38534, Class K	HCPL-530K
Standard Lead Finish	Gold Plate
Solder Dipped	Option #200
Butt Cut/Gold Plate	Option #100
Gull Wing/Soldered	Option #300
SMD Part #	
Prescript for all below	5962-
Either Gold or Solder	9685201HPX
Gold Plate	9685201HPC
Solder Dipped	9685201HPA
Butt Cut/Gold Plate	9685201HYC
Butt Cut/Soldered	9685201HYA
Gull Wing/Soldered	9685201HXA

Outline Drawing



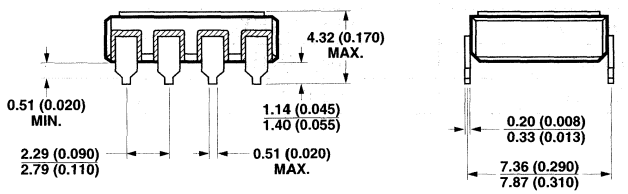
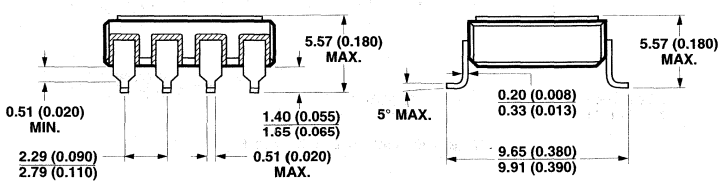
NOTE: DIMENSIONS IN MILLIMETERS (INCHES).

Device Marking



* QUALIFIED PARTS ONLY

Hermetic Optocoupler Options

Option	Description
100	Surface mountable hermetic optocoupler with leads trimmed for butt joint assembly. This option is available on commercial and hi-rel product in 8 pin DIP (see drawings below for details).  NOTE: DIMENSIONS IN MILLIMETERS (INCHES).
200	Lead finish is solder dipped rather than gold plated. This option is available on commercial and hi-rel product in 8 pin DIP. DESC Drawing part numbers contain provisions for lead finish.
300	Surface mountable hermetic optocoupler with leads cut and bent for gull wing assembly. This option is available on commercial and hi-rel product in 8 pin DIP (see drawings below for details). This option has solder dipped leads.  NOTE: DIMENSIONS IN MILLIMETERS (INCHES).

Absolute Maximum Ratings

Storage Temperature (T_S) ..... -65 to 150°C
Operating Temperature (T_A) ..... -55 to 125°C
Junction Temperature (T_J) ..... 175°C
Average Input Current ($I_{F(AVG)}$) ..... 25 mA
Peak Input Current (50% duty cycle, ≤ 1 ms pulse width) ($I_{F(PEAK)}$) ..... 50 mA
Peak Transient Input Current (<1 µs pulse width, 300 pps) ($I_{F(TRAN)}$) ..... 1.0 A
Reverse Input Voltage (Pin 3-2) (V_R) ..... 5 V
Average Output Current (Pin 6) ($I_{O(AVG)}$) ..... 15 mA
Resistor Voltage (Pin 7) (V_7) ..... -0.5 V to V_{CC}
Output Voltage (Pin 6-5) (V_O) ..... -0.5 to 30 V
Supply Voltage (Pin 8-5) (V_{CC}) ..... -0.5 to 30 V
Output Power Dissipation (P_O) ..... 100 mW
Total Power Dissipation (P_T) ..... 145 mW
Lead Solder Temperature (soldering, 10 seconds) ..... 260°C

ESD Classification

(MIL-STD-883, Method 3015)
HCPL-5300/5301 .....(Δ),Class 1

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage	V_{CC}	4.5	30	Volts
Output Voltage	V_O	0	30	Volts
Input Current (ON)	$I_{F(ON)}$	10	20	mA
Input Voltage (OFF)	$V_{F(OFF)}$	-5	0.8	V

Electrical Specifications

Over recommended operating conditions (T_A = -55°C to +125°C, V_{CC} = +4.5 V to 30 V, $I_{F(ON)}$ = 10 mA to 20 mA, $V_{F(OFF)}$ = -5 V to 0.8 V) unless otherwise specified.

Parameter	Symbol	Group A Sub-groups[12]	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR	1, 2, 3	30	90		%	I_F = 10 mA, V_O = 0.6 V		1
Low Level Output Current	I_{OL}	1, 2, 3	3.0	9.0		mA	I_F = 10 mA, V_O = 0.6 V	1, 2	
Low Level Output Voltage	V_{OL}	1, 2, 3		0.3	0.6	V	I_O = 2.4 mA		
Input Threshold Current	I_{TH}	1, 2, 3		1.5	5.0	mA	V_O = 0.8 V, I_O = 0.75 mA	1	7
High Level Output Current	I_{OH}	1, 2, 3		5	75	µA	V_F = 0.8 V	3	
High Level Supply Current	I_{CCH}	1, 2, 3		0.6	1.5	mA	V_F = 0.8 V, V_O = Open		7
Low Level Supply Current	I_{CCL}	1, 2, 3		0.6	1.5	mA	I_F = 10 mA, V_O = Open		7
Input Forward Voltage	V_F	1, 2, 3	1.0	1.5	1.8	V	I_F = 10 mA	4	
Temperature Coefficient of Forward Voltage	$\Delta V_F/\Delta T_A$			-1.6		mV/°C	I_F = 10 mA		
Input Reverse Breakdown Voltage	BV_R	1, 2, 3	5			V	I_R = 100 µA		
Input Capacitance	C_{IN}			90		pF	f = 1 MHz, V_F = 0 V		
Input-Output Insulation Leakage Current	I_{I-O}	1			1.0	µA	RH = 45%, t = 5 sec, V_{I-O} = 1500 Vdc, T_A = 25°C		2
Resistance (Input-Output)	R_{I-O}			10^{12}		Ω	V_{I-O} = 500 Vdc		2
Capacitance (Input-Output)	C_{I-O}			2.4		pF	f = 1 MHz		2
Internal Pull-up Resistor	R_L	1	14	20	28	kΩ	T_A = 25°C		4, 5, 6
Internal Pull-up Resistor Temperature Coefficient	$\Delta R_L/\Delta T_A$			0.014		kΩ/°C			

*All typical values at 25°C, V_{CC} = 15 V.

Switching Specifications (R_L= 20 kΩ External)

Over recommended operating conditions:
(T_A = -55°C to +125°C, V_{CC} = +4.5 V to 30 V, $I_{F(ON)}$ = 10 mA to 20 mA, $V_{F(OFF)}$ = -5 V to 0.8 V) unless otherwise specified.

Parameter	Symbol	Group A Subgrps.[12]	Min.	Typ.*	Max.	Units	Test Conditions		Fig.	Note
Propagation Delay Time to Low Output Level	t_{PHL}	9, 10, 11	30	180	450	ns	C_L = 100 pF	$I_{F(on)}$ = 10 mA, $V_{F(off)}$ = 0.8 V, V_{CC} = 15.0 V, V_{THLH} = 2.0 V, V_{THHL} = 1.5 V	5, 7, 9-12	3, 4, 5, 6, 7
				100		ns	C_L = 10 pF			
Propagation Delay Time to High Output Level	t_{PLH}	9, 10, 11	250	350	650	ns	C_L = 100 pF			
				130			C_L = 10 pF			
Pulse Width Distortion	PWD	9, 10, 11		150	450	ns	C_L = 100 pF			11
Propagation Delay Difference Between Any Two Parts	t_{PLH} - t_{PHL}	9, 10, 11	-170	140	500	ns				8
Output High Level Common Mode Immunity Transient	$\|CM_H\|$	9	10	17		kV/µs	I_F = 0 mA, V_O > 3.0 V	V_{CC} = 15.0 V, C_L = 100 pF, V_{CM} = 1000 V_{P-P} T_A = 25°C	6, 17, 18, 21	9, 13
Output Low Level Common Mode Transient Immunity	$\|CM_L\|$	9	10	17		kV/µs	I_F = 10 mA V_O < 1.0 V			10, 13

*All typical values at 25°C, V_{CC} = 15 V.

Switching Specifications (R_L= Internal Pull-up)

Over recommended operating conditions:
(T_A = -55°C to +125°C, V_{CC} = +4.5 V to 30 V, $I_{F(ON)}$ = 10 mA to 20 mA, $V_{F(OFF)}$ = -5 V to 0.8 V) unless otherwise specified.

Parameter	Symbol	Group A Subgrps.[12]	Min.	Typ.*	Max.	Units	Test Conditions		Fig.	Note
Propagation Delay Time to Low Output Level	t_{PHL}	9, 10, 11	20	185	500	ns	$I_{F(on)}$ = 10 mA, $V_{F(off)}$ = 0.8 V, V_{CC} = 15.0 V, C_L = 100 pF, V_{THLH} = 2.0 V V_{THHL} = 1.5 V		5, 8,	3, 4, 5, 6, 7
Propagation Delay Time to High Output Level	t_{PLH}	9, 10, 11	220	415	750	ns				
Pulse Width Distortion	PWD	9, 10, 11		150	600	ns				11
Propagation Delay Difference Between Any Two Parts	t_{PLH} - t_{PHL}	9, 10, 11	-225	150	650	ns				8
Output High Level Common Mode Transient Immunity	$\|CM_H\|$			10		kV/µs	I_F = 0 mA, V_O > 3.0 V	V_{CC} = 15.0 V, C_L = 100 pF, V_{CM} = 1000 T_A = 25°C	6, 21	9
Output Low Level Common Mode Transient Immunity	$\|CM_L\|$			10		kV/µs	I_F = 16 mA V_O < 1.0 V			10
Power Supply Rejection	PSR			1.0		V_{P-P}	Square Wave, t_{RISE}, t_{FALL} > 5 ns, no bypass capacitors.			7

*All typical values at 25°C, V_{CC} = 15 V.

Notes:

1. CURRENT TRANSFER RATIO in percent is defined as the ratio of output collector current (I_O) to the forward LED input current (I_F) times 100.
2. Device considered a two-terminal device: Pins 1, 2, 3 and 4 shorted together and Pins 5, 6, 7 and 8 shorted together.
3. Pulse: f = 20 kHz, Duty Cycle = 10%
4. The internal 20 kΩ resistor can be used by shorting pins 6 and 7 together.
5. Due to the tolerance of the internal resistor, and since propagation delay is dependent on the load resistor value, performance can be improved by using an external 20 kΩ 1% load resistor. For more information on how propagation delay varies with load resistance, see Figure 8.
6. The R_L = 20 kΩ, C_L = 100 pF represents a typical IPM (Intelligent Power Module) load.
7. Use of a 0.1 µF bypass capacitor connected between pins 5 and 8 can improve performance by filtering power supply line noise.
8. The difference in t_{PLH} and t_{PHL} between any two parts under the same test condition. (See IPM Dead Time and Propagation Delay Specifications section.)
9. Common mode transient immunity in a Logic High level is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (i.e., V_O > 3.0 V).
10. Common mode transient immunity in a Logic Low level is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., V_O < 1.0 V).
11. Pulse Width Distortion (PWD) is defined as the difference between t_{PLH} and t_{PHL} for any given device.
12. Standard parts receive 100% testing at 25°C (Subgroups 1 and 9). Hi-Rel and SMD parts receive 100% testing at 25°C, +125°C, and -55°C (Subgroups 1 and 9, 2 and 10, 3 and 11 respectively).
13. Parameters are tested as part of device initial characterization and after design and process changes. Parameters are guaranteed to limits specified for all lots not specifically tested.

LED Drive Circuit Considerations For Ultra High CMR Performance

Without a detector shield, the dominant cause of optocoupler CMR failure is capacitive coupling from the input side of the optocoupler, through the package, to the detector IC as shown in Figure 14. The HCPL-5300/5301 improves CMR performance by using a detector IC with an optically transparent Faraday shield, which diverts the capacitively coupled current away from the sensitive IC circuitry. However, this shield does not eliminate the capacitive coupling between the LED and the optocoupler output pins and output ground as shown in Figure 15. This capacitive coupling causes perturbations in the LED current during common mode transients and becomes the major source of CMR failures for a shielded optocoupler. The main design objective of a high CMR LED drive circuit becomes keeping the LED in the proper state (on or off) during common mode transients. For example, the recommended application circuit (Figure 13), can achieve 10 kV/μs CMR while minimizing component complexity. Note that a CMOS gate is recommended in Figure 13 to keep the LED off when the gate is in the high state.

Another cause of CMR failure for a shielded optocoupler is direct coupling to the optocoupler output pins through C_{LEDO1} and C_{LEDO2} in Figure 15. Many factors influence the effect and magnitude of the direct coupling including: the use of an internal or external output pull-up resistor, the position of the LED current setting resistor, the connection of the unused input package pins, and the value of the capacitor at the optocoupler output (CL).

Techniques to keep the LED in the proper state and minimize the effect of the direct coupling are discussed in the next two sections.

CMR With The LED On (CMR_L)

A high CMR LED drive circuit must keep the LED on during common mode transients. This is achieved by overdriving the LED current beyond the input threshold so that it is not pulled below the threshold during a transient. The recommended minimum LED current of 10 mA provides adequate margin over the maximum I_{TH} of 5.0 mA (see Figure 1) to achieve 10 kV/μs CMR. Capacitive coupling is higher when the internal load resistor is used (due to C_{LEDO2}) and an I_F = 16mA is required to obtain 10 kV/μs CMR.

The placement of the LED current setting resistor affects the ability of the drive circuit to keep the LED on during transients and interacts with the direct coupling to the optocoupler output. For example, the LED resistor in Figure 16 is connected to the anode. Figure 17 shows the AC equivalent circuit for Figure 16 during common mode transients. During a $+dV_{CM/dt}$ in Figure 17, the current available at the LED anode (I_{TOTAL}) is limited by the series resistor. The LED current (I_F) is reduced from its DC value by an amount equal to the current that flows through C_{LEDP} and C_{LEDO1}. The situation is made worse because the current through C_{LEDO1} has the effect of trying to pull the output high (toward a CMR failure) at the same time the LED current is being reduced. For this reason, the recommended LED drive circuit (Figure 13) places the current setting resistor in series with the LED cathode. Figure 18 is the AC equivalent circuit for Figure 13 during common mode transients. In this case, the LED current is not reduced during a $+dV_{CM/dt}$ transient because the current flowing through the package capacitance is supplied by the power supply. During a $-dV_{CM/dt}$ transient, however, the LED current is reduced by the amount of current flowing through C_{LEDN}. But better CMR performance is achieved since the current flowing in C_{LEDO1} during a negative transient acts to keep the output low.

Coupling to the LED and output pins is also affected by the connection of pins 1 and 4. If CMR is limited by perturbations in the LED on current, as it is for the recommended drive circuit (Figure 13), pins 1 and 4 should be connected to the input circuit common. However, if CMR performance is limited by direct coupling to the output when the LED is off, pins 1 and 4 should be left unconnected.

CMR With The LED Off (CMR_H)

A high CMR LED drive circuit must keep the LED off ($V_F \leq V_{F(OFF)}$) during common mode transients. For example, during a $+dV_{CM/dt}$ transient in Figure 18, the current flowing through C_{LEDN} is supplied by the parallel combination of the LED and series resistor. As long as the voltage developed across the resistor is less than $V_{F(OFF)}$ the LED will remain off and no

common mode failure will occur. Even if the LED momentarily turns on, the 100 pF capacitor from pins 6-5 will keep the output from dipping below the threshold. The recommended LED drive circuit (Figure 13) provides about 10 V of margin between the lowest optocoupler output voltage and a 3 V IPM threshold during a 10 kV/μs transient with V_{CM} = 1000 V. Additional margin can be obtained by adding a diode in parallel with the resistor, as shown by the dashed line connection in Figure 18, to clamp the voltage across the LED below $V_{F(OFF)}$.

Since the open collector drive circuit, shown in Figure 19, cannot keep the LED off during a $+dV_{CM/dt}$ transient, it is not desirable for applications requiring ultra high CMR_H performance. Figure 20 is the AC equivalent circuit for Figure 16 during common mode transients. Essentially all the current flowing through C_{LEDN} during a $+dV_{CM/dt}$ transient must be supplied by the LED. CMR_H failures can occur at dv/dt rates where the current through the LED and C_{LEDN} exceeds the input threshold. Figure 21 is an alternative drive circuit which does achieve ultra high CMR performance by shunting the LED in the off state.

IPM Dead Time and Propagation Delay Specifications

These devices include a Propagation Delay Difference specification intended to help designers minimize "dead time" in their power inverter designs. Dead time is the time period during which both the high and low side power transistors (Q1 and Q2 in Figure 22) are off. Any overlap in Q1 and Q2 conduction will result in large currents flowing through the power devices between the high and low voltage motor rails.

To minimize dead time the designer must consider the propagation delay characteristics of the optocoupler as well as the characteristics of the IPM IGBT gate drive circuit. Considering only the delay characteristics of the optocoupler (the characteristics of the IPM IGBT gate drive circuit can be analyzed in the same way) it is important to know the minimum and maximum turn-on (t_{PHL}) and turn-off (t_{PLH}) propagation delay specifications, preferably over the desired operating temperature range.

The limiting case of zero dead time occurs when the input to Q1 turns off at the same time that the input to Q2 turns on. This case determines the minimum delay between LED1 turn-off and LED2 turn-on, which is related to the worst case optocoupler propagation delay waveforms, as shown in Figure 23. A minimum dead time of zero is achieved in Figure 23 when the signal to turn on LED2 is delayed by ($t_{PLH\ max}$ - $t_{PHL\ min}$) from the LED1 turn off. This delay is the maximum value for the propagation delay difference specification which is specified at 500 ns for the HCPL-5300/5301 over an operating temperature range of -55°C to +125°C.

Delaying the LED signal by the maximum propagation delay difference ensures that the minimum dead time is zero, but it does not tell a designer what the maximum dead time will be. The maximum dead time occurs in the highly unlikely case where one optocoupler with the fastest t_{PLH} and another with the slowest t_{PHL} are in the same inverter leg. The maximum dead time in this case becomes the sum of the spread in the t_{PLH} and t_{PHL} propagation delays as shown in Figure 24. The maximum dead time is also equivalent to the difference between the maximum and minimum propagation delay difference specifications. The maximum dead time (due to the optocouplers) for the HCPL-5300/5301 is 670 ns (= 500 ns - (-170 ns)) over an operating temperature range of -55°C to +125°C.

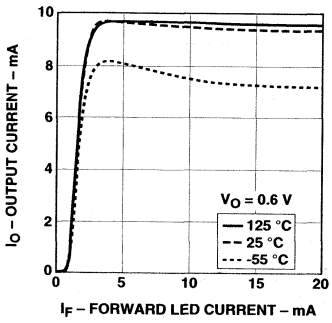


Figure 1. Typical Transfer Characteristics.

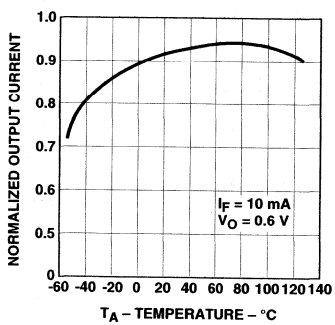


Figure 2. Normalized Output Current vs. Temperature.

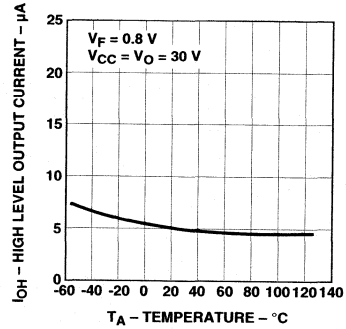


Figure 3. High Level Output Current vs. Temperature.

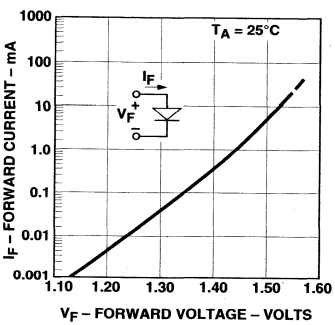
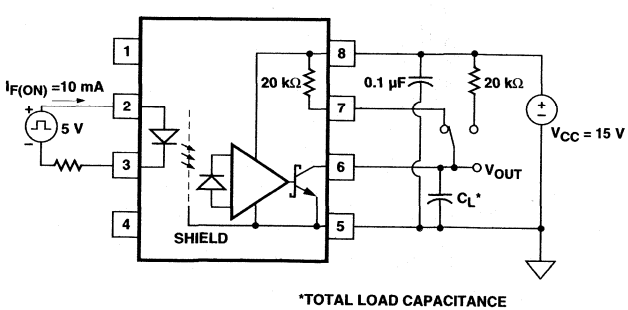


Figure 4. Input Current vs. Forward Voltage.



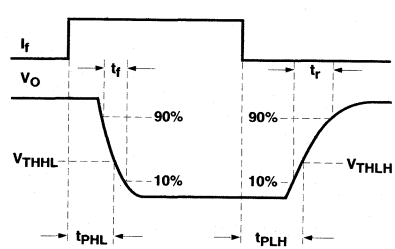


Figure 5. Propagation Delay Test Circuit.

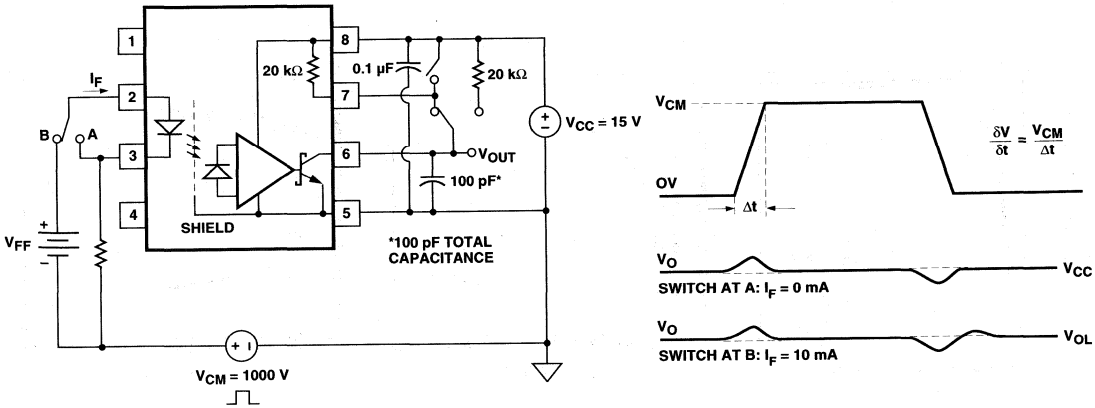


Figure 6. CMR Test Circuit. Typical CMR Waveform.

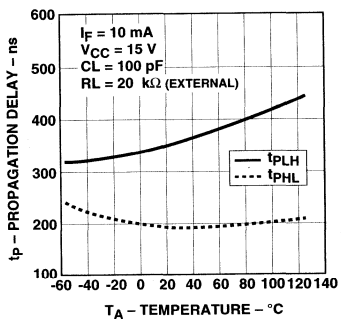


Figure 7. Propagation Delay with External 20 kΩ RL vs. Temperature.

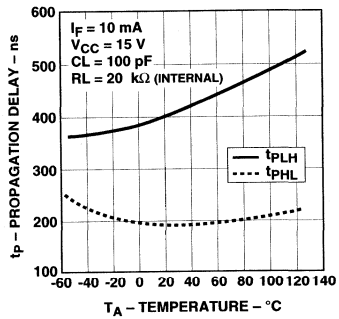


Figure 8. Propagation Delay with Internal 20 kΩ RL vs. Temperature.

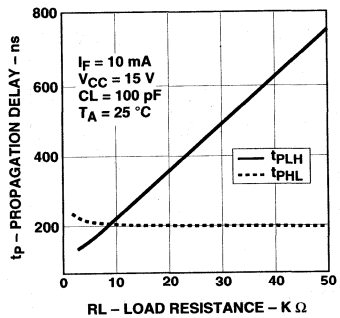


Figure 9. Propagation Delay vs. Load Resistance.

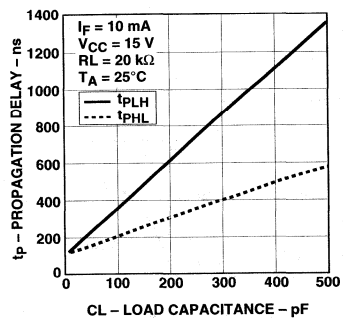


Figure 10. Propagation Delay vs. Load Capacitance.

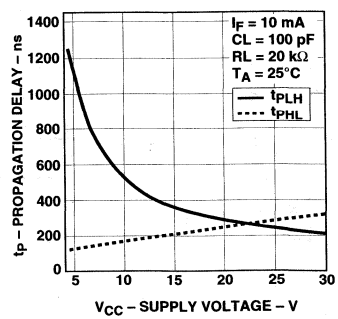


Figure 11. Propagation Delay vs. Supply Voltage.

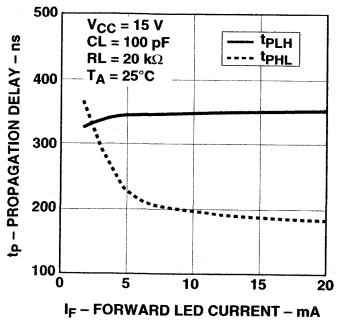


Figure 12. Propagation Delay vs. Input Current.

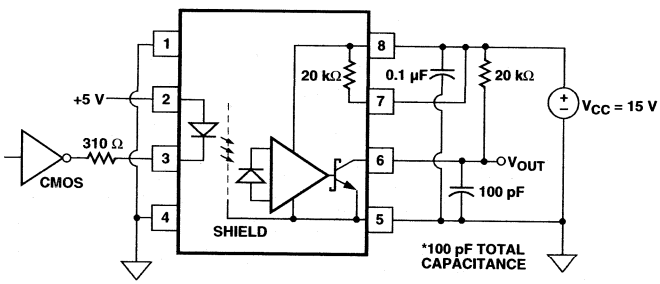


Figure 13. Recommended LED Drive Circuit.

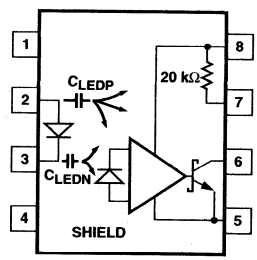


Figure 14. Optocoupler Input to Output Capacitance Model for Unshielded Optocouplers.

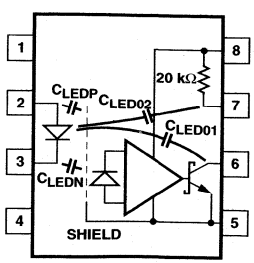


Figure 15. Optocoupler Input to Output Capacitance Model for Shielded Optocouplers.

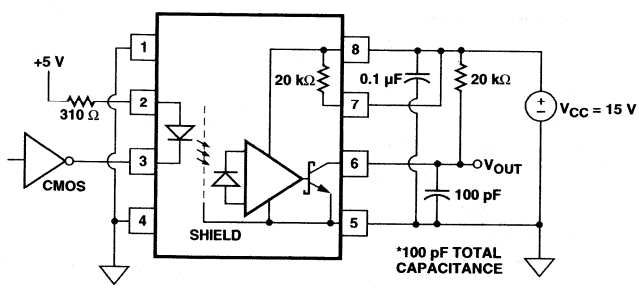


Figure 16. LED Drive Circuit with Resistor Connected to LED Anode (Not Recommended).

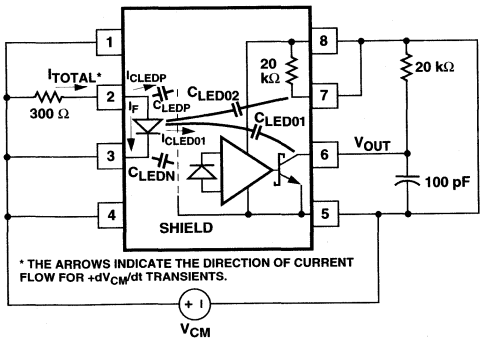


Figure 17. AC Equivalent Circuit for Figure 16 During Common Mode Transients.

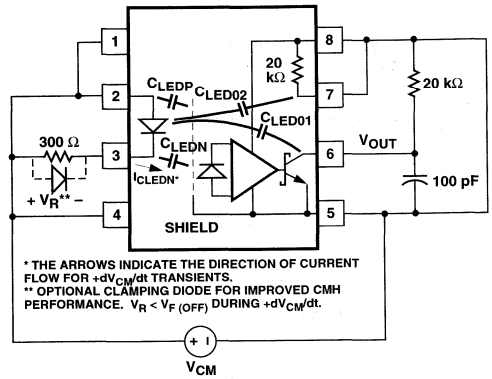


Figure 18. AC Equivalent Circuit for Figure 13 During Common Mode Transients.

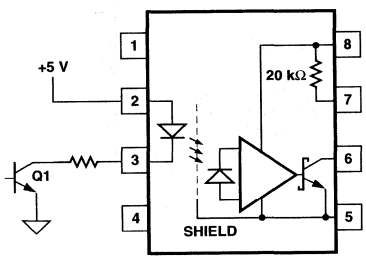


Figure 19. Not Recommended Open Collector LED Drive Circuit.

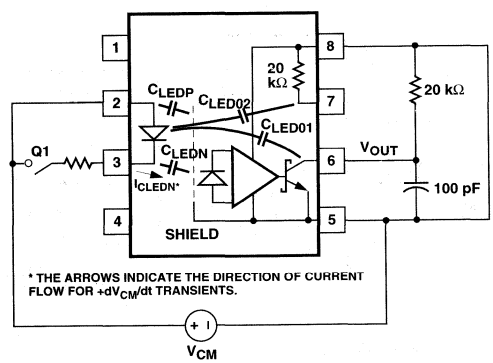


Figure 20. AC Equivalent Circuit for Figure 19 During Common Mode Transients.

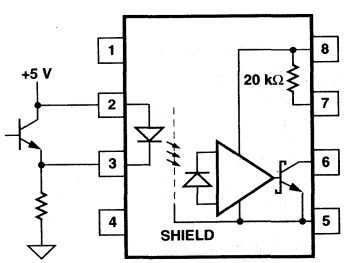


Figure 21. Recommended LED Drive Circuit for Ultra High CMR.

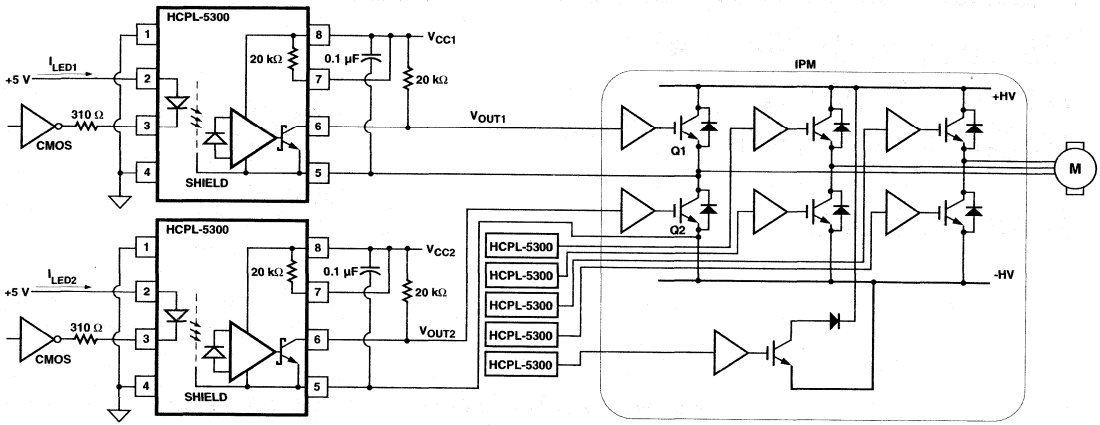


Figure 22. Typical Application Circuit.

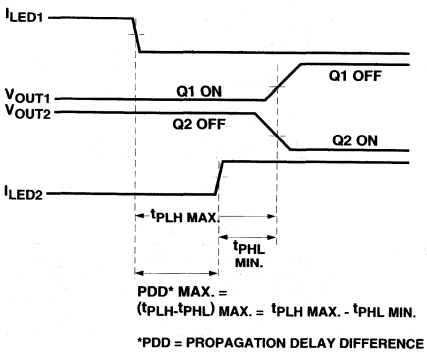


Figure 23. Minimum LED Skew for Zero Dead Time.

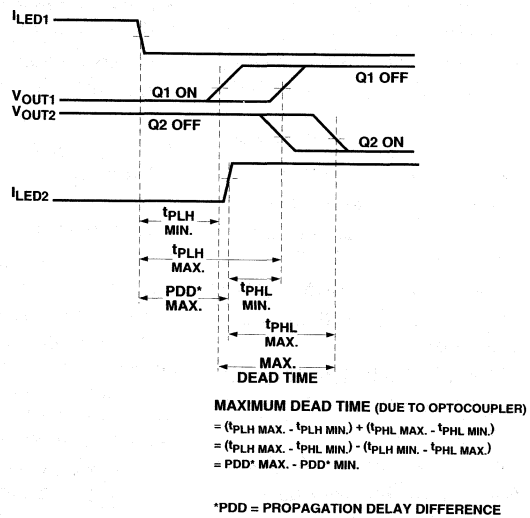


Figure 24. Waveforms for Dead Time Calculations.

MIL-PRF-38534 Class H, Class K, and DESC SMD Test Program

Hewlett-Packard's Hi-Rel Optocouplers are in compliance with MIL-PRF-38534 Classes H and K. Class H devices are also in compliance with DESC drawing 5962-96852.

Testing consists of 100% screening and quality conformance inspection to MIL-PRF-38534.

HEWLETT® PACKARD

Hermetically Sealed, Low I_F, Wide V_{CC}, Logic Gate Optocouplers

Technical Data

HCPL-520X*
5962-88768
HCPL-523X
HCPL-623X
HCPL-625X
5962-88769

*See matrix for available extensions.

Features

- **Dual Marked with Device Part Number and DESC Drawing Number**
- **Manufactured and Tested on a MIL-PRF-38534 Certified Line**
- **QML-38534, Class H and K**
- **Four Hermetically Sealed Package Configurations**
- **Performance Guaranteed over -55°C to +125°C**
- **Wide V_{CC} Range (4.5 to 20 V)**
- **350 ns Maximum Propagation Delay**
- **CMR: > 10,000 V/μs Typical**
- **1500 Vdc Withstand Test Voltage**
- **Three State Output Available**
- **High Radiation Immunity**
- **HCPL-2200/31 Function Compatibility**
- **Reliability Data**
- **Compatible with LSTTL, TTL, and CMOS Logic**

Applications

- **Military and Space**
- **High Reliability Systems**
- **Transportation and Life Critical Systems**
- **High Speed Line Receiver**
- **Isolated Bus Driver (Single Channel)**
- **Pulse Transformer Replacement**
- **Ground Loop Elimination**
- **Harsh Industrial Environments**
- **Computer-Peripheral Interfaces**

Description

These units are single, dual and quad channel, hermetically sealed optocouplers. The products are capable of operation and storage over the full military temperature range and can be purchased as either standard product or with full MIL-PRF-38534 Class Level H or K testing or from the appropriate DESC Drawing. All devices are manufactured and tested on a MIL-PRF-38534 certified line and are included in the DESC Qualified Manufacturers List QML-38534 for Hybrid Microcircuits.

Each channel contains an AlGaAs light emitting diode which is optically coupled to an integrated high gain photon detector. The detector has a threshold with hysteresis which provides differential mode noise immunity and eliminates the potential for output signal chatter. The detector in the single channel units has a tri-state output stage

Truth Tables

(Positive Logic)

Multichannel Devices

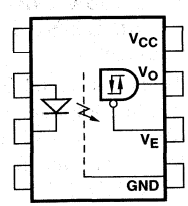
Input	Output
On (H)	H
Off (L)	L

Single Channel DIP

Input	Enable	Output
On (H)	H	Z
Off (L)	H	Z
On (H)	L	H
Off (L)	L	L

Functional Diagram

Multiple Channel Devices Available



CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

5965-3005E

which allows for direct connection to data buses. The output is non-inverting. The detector IC has an internal shield that provides a guaranteed common mode transient immunity of up to 10,000 V/μs. Improved power supply rejection eliminates the need for special power supply bypass precautions.

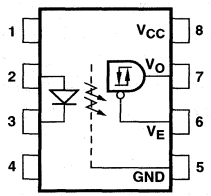
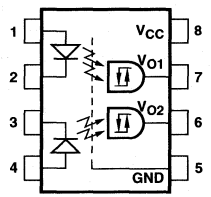
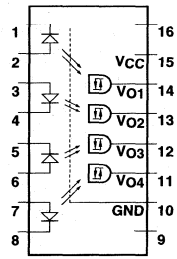
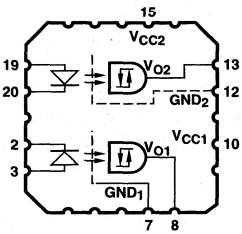
Package styles for these parts are 8 pin DIP through hole (case outline P), 16 pin DIP flat pack (case outline F), and leadless ceramic chip carrier (case outline 2). Devices may be purchased with a variety of lead bend and plating options, see Selection Guide Table for details. Standard Military drawing (SMD) parts are available for each package and lead style.

Because the same electrical die (emitters and detectors) are used for each channel of each device listed in this data sheet, absolute maximum ratings, recommended operating conditions, electrical specifications, and performance characteristics shown in the figures are identical for all parts. Occasional exceptions exist due to package variations and limitations and are as noted. Additionally, the same package assembly processes and materials are used in all devices. These similarities give justification for the use of data obtained from one part to represent other part's performance for die related reliability and certain limited radiation test results.

Selection Guide–Package Styles and Lead Configuration Options

Package	8 Pin DIP	8 Pin DIP	16 Pin Flat Pack	20 Pad LCCC
Lead Style	Through Hole	Through Hole	Unformed Leads	Surface Mount
Channels	1	2	4	2
Common Channel Wiring	None	V_{CC}, GND	V_{CC}, GND	None
HP Part # & Options				
Commercial	HCPL-5200	HCPL-5230	HCPL-6250	HCPL-6230
MIL-PRF-38534, Class H	HCPL-5201	HCPL-5231	HCPL-6251	HCPL-6231
MIL-PRF-38534, Class K	HCPL-520K	HCPL-523K	HCPL-625K	HCPL-623K
Standard Lead Finish	Gold Plate	Gold Plate	Gold Plate	Soldered Pads
Solder Dipped	Option #200	Option #200		
Butt Cut/Gold Plate	Option #100	Option #100		
Gull Wing/Soldered	Option #300	Option #300		
SMD Part #				
Prescript for all below	5962-	5962-	5962-	5962-
Either Gold or Solder	8876801PX	8876901PX	8876903FX	88769022X
Gold Plate	8876801PC	8876901PC	8876903FC	
Solder Dipped	8876801PA	8876901PA		88769022A
Butt Cut/Gold Plate	8876801YC	8876901YC		
Butt Cut/Soldered	8876801YA	8876901YA		
Gull Wing/Soldered	8876801XA	8876901XA		

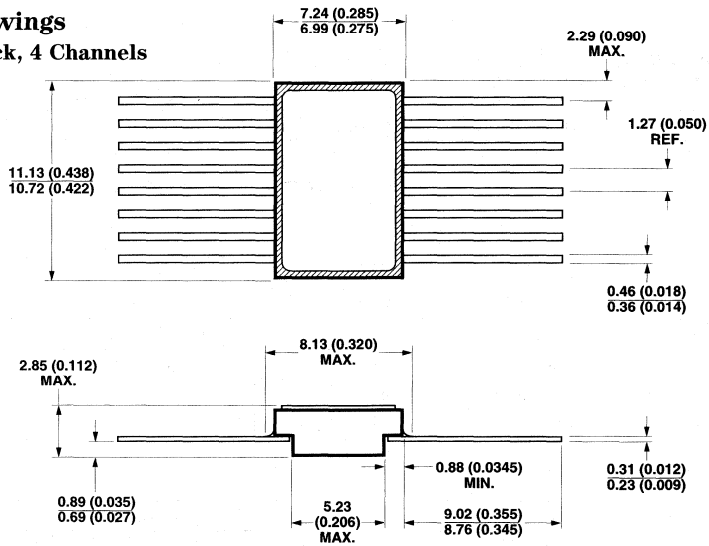
Functional Diagrams

8 Pin DIP	8 Pin DIP	16 Pin Flat Pack	20 Pad LCCC
Through Hole	Through Hole	Unformed Leads	Surface Mount
1 Channel	2 Channels	4 Channels	2 Channels
			

Note: Multichannel DIP and flat pack devices have common V_{CC} and ground. Single channel DIP has an enable pin 6. LCCC (leadless ceramic chip carrier) package has isolated channels with separate V_{CC} and ground connections.

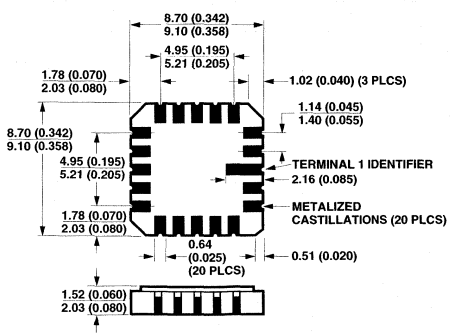
Outline Drawings

16 Pin Flat Pack, 4 Channels



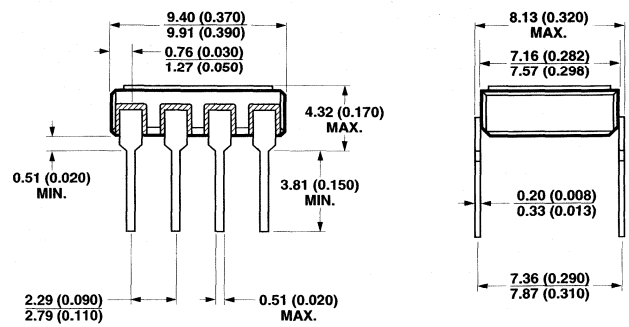
NOTE: DIMENSIONS IN MILLIMETERS (INCHES).

20 Terminal LCCC Surface Mount, 2 Channels



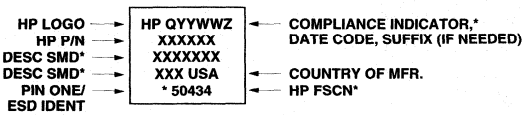
NOTE: DIMENSIONS IN MILLIMETERS (INCHES).
SOLDER THICKNESS 0.127 (0.005) MAX.

8 Pin DIP Through Hole, 1 and 2 Channel



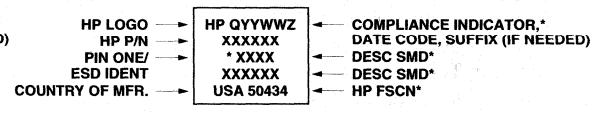
NOTE: DIMENSIONS IN MILLIMETERS (INCHES).

Leaded Device Marking



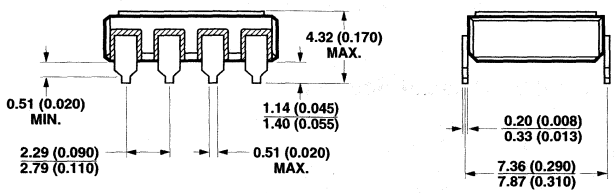
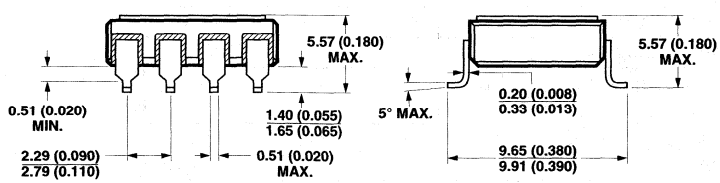
*QUALIFIED PARTS ONLY

Leadless Device Marking



*QUALIFIED PARTS ONLY

Hermetic Optocoupler Options

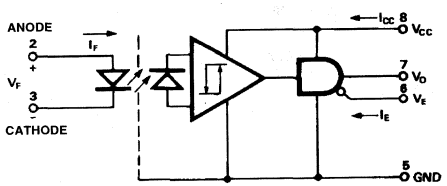
Option	Description
100	Surface mountable hermetic optocoupler with leads trimmed for butt joint assembly. This option is available on commercial and hi-rel product in 8 pin DIP (see drawings below for details).  NOTE: DIMENSIONS IN MILLIMETERS (INCHES).
200	Lead finish is solder dipped rather than gold plated. This option is available on commercial and hi-rel product in 8 pin DIP. DESC Drawing part numbers contain provisions for lead finish. All leadless chip carrier devices are delivered with solder dipped terminals as a standard feature.
300	Surface mountable hermetic optocoupler with leads cut and bent for gull wing assembly. This option is available on commercial and hi-rel product in 8 pin DIP (see drawings below for details). This option has solder dipped leads.  NOTE: DIMENSIONS IN MILLIMETERS (INCHES).

Absolute Maximum Ratings

Storage Temperature Range, T_S ..... -65°C to +150°C
Operating Temperature, T_A ..... -55°C to +125°C
Case Temperature, T_C ..... +170°C
Junction Temperature, T_J ..... +175°C
Lead Solder Temperature ..... 260°C for 10 s
Average Forward Curre, $I_{F\,AVG}$ (each channel) ..... 8 mA
Peak Input Current, $I_{F\,PK}$ (each channel) ..... 20 mA[1]
Reverse Input Voltage, V_R (each channel) ..... 3 V
Supply Voltage ,V_{CC} ..... 0.0 V min., 20 V max.
Average Output Current, I_O (each channel) ..... 15 mA
Output Voltage, V_O (each channel) ..... –0.3 V min., 20 V max.
Package Power Dissipation, P_d (each channel) ..... 200 mW

Single Channel Product Only
Tri-State Enable Voltage, V_E ..... –0.3 V min., 20 V max.

8 Pin Ceramic DIP Single Channel Schematic



Note enable pin 6. An external 0.01 µF to 0.1 µF bypass capacitor is recommended between V_{CC} and ground for each package type.

ESD Classification

(MIL-STD-883, Method 3015)
HCPL-5200/01, HCPL-6230/31 ..... (Δ), Class 1
HCPL-5230/31, HCPL-6250/51 ..... (Dot), Class 3

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage	V_{CC}	4.5	20	V
Input Current, High Level, Each Channel	I_{FH}	2	8	mA
Input Voltage, Low Level, Each Channel	V_{FL}	0	0.8	V
Fan Out (TTL Load) Each Channel	N		4	

Single Channel Product Only

High Level Enable Voltage	V_{EH}	2.0	20	V
Low Level Enable Voltage	V_{EL}	0	0.8	V

Electrical Characteristics

T_A = -55°C to +125°C, 4.5 V ≤ V_{CC} ≤ 20 V, 2 mA ≤ $I_{F(ON)}$ ≤ 8 mA, 0 V ≤ $V_{F(OFF)}$ ≤ 0.8 V, unless otherwise specified.

Parameter		Sym.	Test Conditions		Group A[11] Subgroups	Limit Min.	Limit Typ.*	Limit Max.	Units	Fig.	Notes
Logic Low Output Voltage		V_{OL}	I_{OL} = 6.4 mA (4 TTL Loads)		1, 2, 3			0.5	V	1, 3	2
Logic High Output Voltage		V_{OH}	I_{OH} = -2.6 mA (**V_{OH} = V_{CC} - 2.1 V)		1, 2, 3	2.4	**		V	2, 3	2
			I_{OH} = -0.32 mA		NA		3.1				
Output Leakage Current (V_{OUT} > V_{CC})		I_{OHH}	V_O = 5.5 V	I_F = 8 mA	1, 2, 3			100	µA		2
			V_O = 20 V	V_{CC} = 4.5 V				500			
Logic Low Supply Current	Single Channel	I_{CCL}	V_{CC} = 5.5 V	V_F = 0 V, V_E = Don't Care	1, 2, 3		4.5	6	mA		
			V_{CC} = 20 V				5.3	7.5			
	Dual Channel		V_{CC} = 5.5 V	V_{F1} = V_{F2} = 0 V			9.0	12			
			V_{CC} = 20 V				10.6	15			
	Quad Channel		V_{CC} = 5.5 V	V_{F1} = V_{F2} = V_{F3} = V_{F4} = 0 V			14	24			
			V_{CC} = 20 V				17	30			
Logic High Supply Current	Single Channel	I_{CCH}	V_{CC} = 5.5 V	I_F = 8 mA, V_E = Don't Care	1, 2, 3		2.9	4.5	mA		
			V_{CC} = 20 V				3.3	6			
	Dual Channel		V_{CC} = 5.5 V	I_{F1} = I_{F2} = 8 mA			5.8	9			
			V_{CC} = 20 V				6.6	12			
	Quad Channel		V_{CC} = 5.5 V	I_{F1} = I_{F2} = I_{F3} = I_{F4} = 8 mA			9	18			
			V_{CC} = 20 V				11	24			
Logic Low Short Circuit Output Current		I_{OSL}	V_O = V_{CC} = 5.5 V	V_F = 0 V	1, 2, 3	20			mA		2, 3
			V_O = V_{CC} = 20 V			35					
Logic High Short Circuit Output Current		I_{OSH}	V_{CC} = 5.5 V	I_F = 8 mA, V_O = GND	1, 2, 3			-10	mA		2, 3
			V_{CC} = 20 V					-25			
Input Forward Voltage		V_F	I_F = 8 mA		1, 2, 3	1.0	1.3	1.8	V	4	2
Input Reverse Breakdown Voltage		BV_R	I_R = 10 µA		1, 2, 3	3			V		2
Input-Output Insulation Leakage Current		I_{I-O}	V_{I-O} = 1500 Vdc, t = 5s, RH = 45%, T_A = 25°C		1			1.0	µA		4, 5
Logic High Common Mode Transient Immunity		$\|CM_H\|$	I_F = 2 mA, V_{CM} = 50 V_{P-P}		9, 10, 11	1000	10,000		V/µs	9	2, 6, 12
Logic Low Common Mode Transient Immunity		$\|CM_L\|$	I_F = 0 mA, V_{CM} = 50 V_{P-P}		9, 10, 11	1000	10,000		V/µs	9	2, 6, 12
Propagation Delay Time to Logic Low		t_{PHL}			9, 10, 11		173	350	ns	5, 6	2, 7
Propagation Delay Time to Logic High		t_{PLH}			9, 10, 11		118	350	ns	5, 6	2, 7

Electrical Characteristics Single Channel Product Only

T_A = -55°C to +125°C, 4.5 V ≤ V_{CC} ≤ 20 V, 2 mA ≤ $I_{F(ON)}$ ≤ 8 mA, 0 V ≤ $V_{F(OFF)}$ ≤ 0.8 V, 2.0 V ≤ V_{EH} ≤ 20 V, 0 V ≤ V_{EL} ≤ 0.8 V, unless otherwise specified.

Parameter	Sym.	Test Conditions		Group A[11] Subgroups	Limits Min.	Limits Typ.*	Limits Max.	Units	Fig.	Notes
High Impedance State Output Current	I_{OZL}	V_O = 0.4 V	V_{EN} = 2 V, V_F = 0 V	1, 2, 3			-20	µA		
	I_{OZH}	V_O = 2.4 V	V_{EN} = 2 V, I_F = 8 mA	1, 2, 3			20	µA		
		V_O = 5.5 V					100			
		V_O = 20 V					500			
Logic High Enable Voltage	V_{EH}			1, 2, 3	2.0			V		
Logic Low Enable Voltage	V_{EL}			1, 2, 3			0.8	V		
Logic High Enable Current	I_{EH}	V_{EN} = 2.7 V		1, 2, 3			20	µA		
		V_{EN} = 5.5 V					100			
		V_{EN} = 20 V				0.004	250			
Logic Low Enable Current	I_{EL}	V_{EN} = 0.4 V		1, 2, 3			-0.32	mA		

*All typical values are at V_{CC} = 5 V, T_A = 25°C, $I_{F(ON)}$ = 5 mA unless otherwise specified.

Typical Characteristics

All typical values are at T_A = 25°C, V_{CC} = 5 V, $I_{F(ON)}$ = 5 mA unless otherwise specified.

Parameter	Symbol	Typ.	Units	Test Conditions	Fig.	Notes
Input Current Hysteresis	I_{HYS}	0.07	mA	V_{CC} = 5 V	3	2
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$	-1.25	mV/°C	I_F = 8 mA		2
Resistance (Input-Output)	R_{I-O}	10^{13}	Ω	V_{I-O} = 500 Vdc		2, 8
Capacitance (Input-Output)	C_{I-O}	2.0	pF	f = 1 MHz		2, 8
Input Capacitance	C_{IN}	20	pF	V_F = 0 V, f = 1 MHz		2, 10
Output Rise Time (10-90%)	t_r	45	ns		5, 7	2
Output Fall Time (90-10%)	t_f	10	ns		5, 7	2

Typical Characteristics (cont'd.)

All typical values are at T_A = 25°C, V_{CC} = 5 V, $I_{F(ON)}$ = 5 mA, unless otherwise specified.

Single Channel Product Only

Parameter	Symbol	Typ.	Units	Test Conditions	Fig.	Notes
Output Enable Time to Logic High	t_{PZH}	30	ns		8	
Output Enable Time to Logic Low	t_{PZL}	30	ns		8	
Output Disable Time from Logic High	t_{PHZ}	45	ns		8	
Output Disable Time from Logic Low	t_{PLZ}	55	ns		8	

Dual and Quad Channel Products Only

Input-Input Insulation Leakage Current	I_{I-I}	0.5	nA	RH = 45%, T_A = 25°C, V_{I-I} = 500 V, t = 5 s		9
Resistance (Input-Input)	R_{I-I}	10^{13}	Ω	V_{I-I} = 500 V		9
Capacitance (Input-Input)	$C_{I\,I}$	1.5	pF	f = 1 MH		9

Notes:

1. Peak Forward Input Current pulse width < 50 µs at 1 KHz maximum repetition rate.
2. Each channel of a multichannel device.
3. Duration of output short circuit time not to exceed 10 ms.
4. All devices are considered two-terminal devices: measured between all input leads or terminals shorted together and all output leads or terminals shorted together.
5. This is a momentary withstand test, not an operating condition.
6. CM_L is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic low state (V_O < 0.8 V). CM_H is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic high state (V_O > 2.0 V).
7. t_{PHL} propagation delay is measured from the 50% point on the leading edge of the input pulse to the 1.3 V point on the leading edge of the output pulse. The t_{PLH} propagation delay is measured from the 50% point on the trailing edge of the input pulse to the 1.3 V point on the trailing edge of the output pulse.
8. Measured between each input pair shorted together and all output connections for that channel shorted together.
9. Measured between adjacent input pairs shorted together for each multichannel device.
10. Zero-bias capacitance measured between the LED anode and cathode.
11. Standard parts receive 100% testing at 25°C (Subgroups 1 and 9). SMD and hi-rel parts receive 100% testing at 25, 125, and –55°C (Subgroups 1 and 9, 2 and 10, 3 and 11, respectively).
12. Parameters are tested as part of device initial characterization and after design and process changes. Parameters guaranteed to limits specified for all lots not specifically tested.

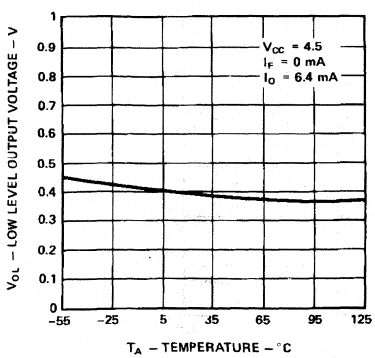


Figure 1. Typical Logic Low Output Voltage vs. Temperature.

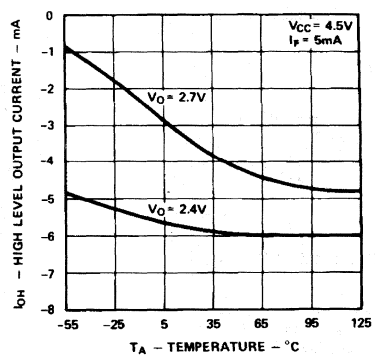


Figure 2. Typical Logic High Output Current vs. Temperature.

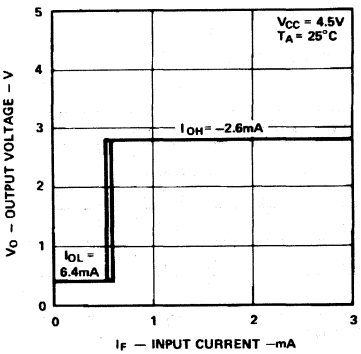


Figure 3. Output Voltage vs. Forward Input Current.

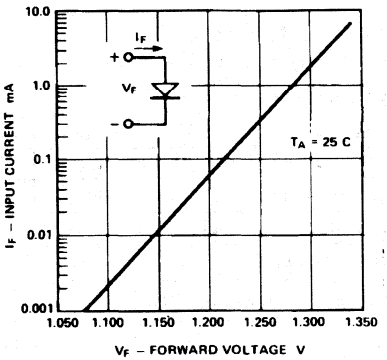
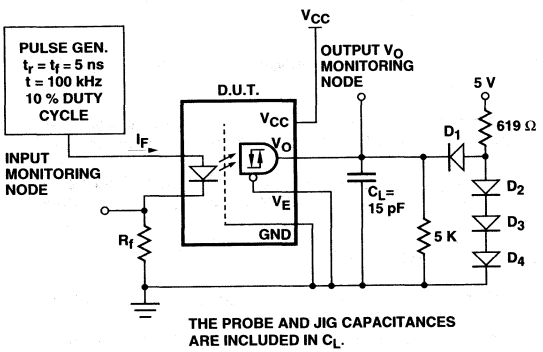


Figure 4. Typical Diode Input Forward Characteristic.



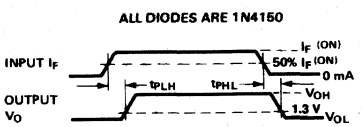


Figure 5. Test Circuit for t_{PLH}, t_{PHL}, t_r, and t_f.

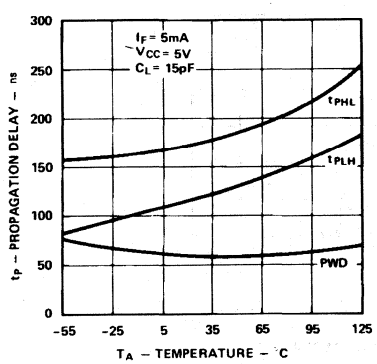


Figure 6. Typical Propagation Delay vs. Temperature.

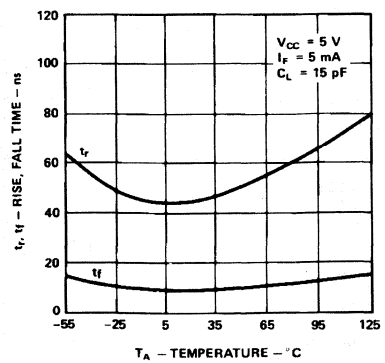


Figure 7. Typical Rise, Fall Time vs. Temperature.

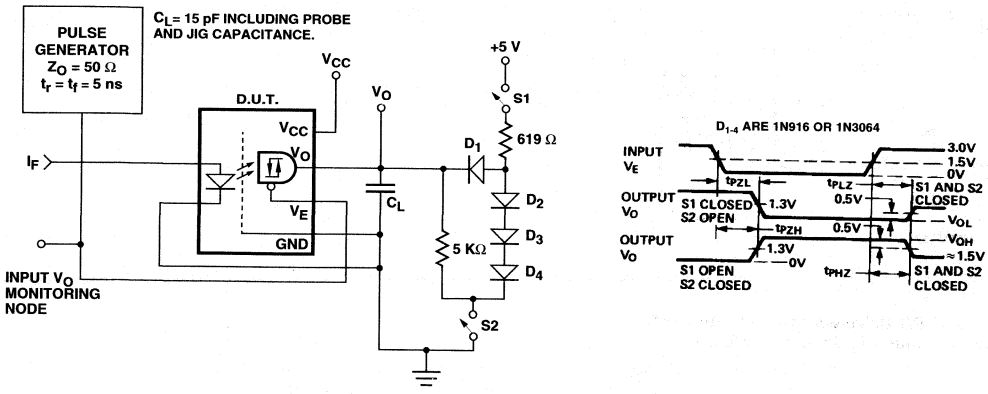


Figure 8. Test Circuit for t_{PHZ}, t_{PZH}, t_{PLZ}, and t_{PZL}.

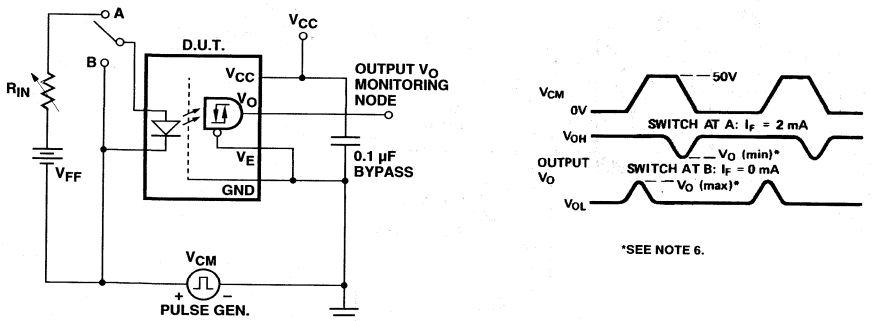


Figure 9. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

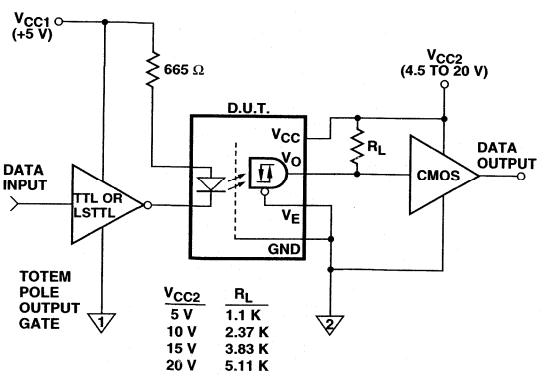


Figure 10. LSTTL to CMOS Interface Circuit.

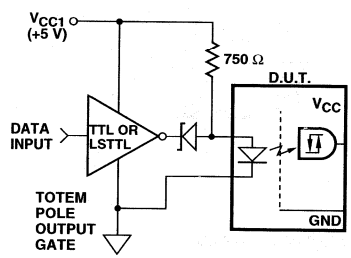


Figure 11. Recommended LED Drive Circuit.

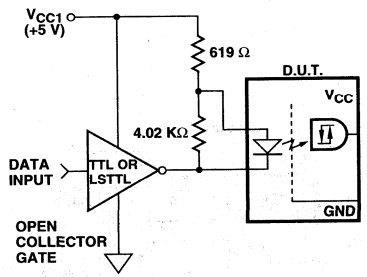


Figure 12. Series LED Drive with Open Collector Gate (4.02 kΩ Resistor Shunts I_{OH} from the LED).

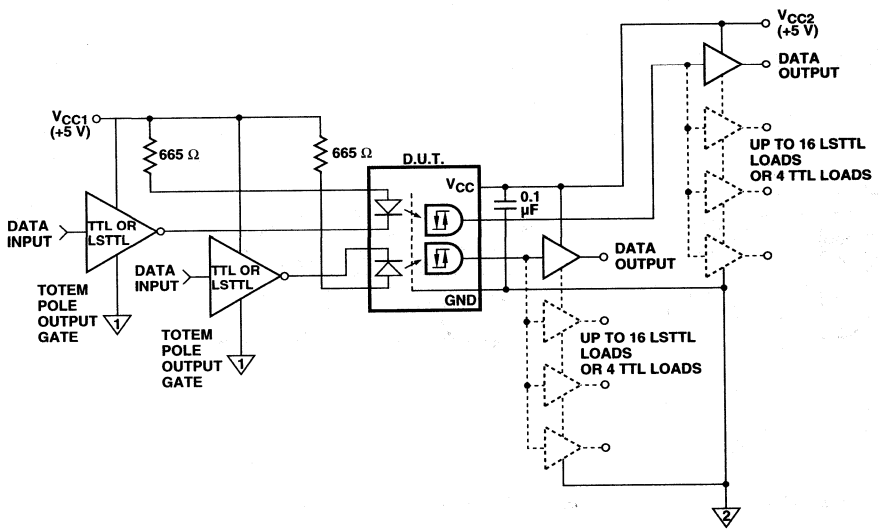


Figure 13. Recommended LSTTL to LSTTL Circuit.

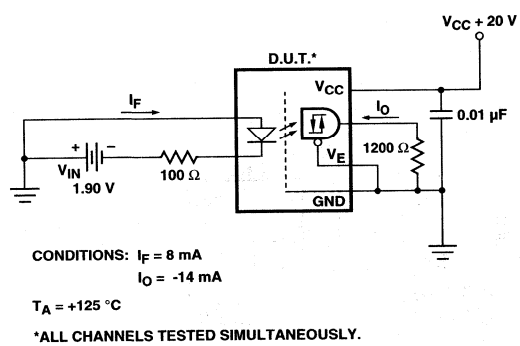


Figure 14. Single Channel Operating Circuit for Burn-in and Steady State Life Tests.

MIL-PRF-38534 Class H, Class K, and DESC SMD Test Program

Hewlett-Packard's Hi-Rel Optocouplers are in compliance with MIL-PRF-38534 Classes H and K. Class H devices are also in compliance with DESC drawings 5962-88768, and 5962-88769.

Testing consists of 100% screening and quality conformance inspection to MIL-PRF-38534.

HEWLETT® PACKARD

Hermetically Sealed, Very High Speed, Logic Gate Optocouplers

Technical Data

HCPL-540X* HCPL-643X
5962-89570 5962-89571
HCPL-543X

*See matrix for available extensions.

Features

- **Dual Marked with Device Part Number and DESC Drawing Number**
- **Manufactured and Tested on a MIL-PRF-38534 Certified Line**
- **QML-38534, Class H and K**
- **Three Hermetically Sealed Package Configurations**
- **Performance Guaranteed over -55°C to +125°C**
- **High Speed: 40 M bit/s**
- **High Common Mode Rejection 500 V/µs Guaranteed**
- **1500 Vdc Withstand Test Voltage**
- **Active (Totem Pole) Outputs**
- **Three Stage Output Available**
- **High Radiation Immunity**
- **HCPL-2400/30 Function Compatibility**
- **Reliability Data**
- **Compatible with TTL, STTL, LSTTL, and HCMOS Logic Families**

Applications

- **Military and Space**
- **High Reliability Systems**
- **Transportation, Medical, and Life Critical Systems**
- **Isolation of High Speed Logic Systems**
- **Computer-Peripheral Interfaces**
- **Switching Power Supplies**
- **Isolated Bus Driver (Networking Applications)- (5400/1 Only)**
- **Pulse Transformer Replacement**
- **Ground Loop Elimination**
- **Harsh Industrial Environments**
- **High Speed Disk Drive I/O**
- **Digital Isolation for A/D, D/A Conversion**

Description

These units are single and dual channel, hermetically sealed optocouplers. The products are capable of operation and storage over the full military temperature range and can be purchased as either standard product or with full MIL-PRF-38534 Class Level H or K testing or from the appropriate DESC Drawing. All devices are manufactured and tested on a MIL-PRF-38534 certified line and are included in the DESC Qualified Manufacturers List QML-38534 for Hybrid Microcircuits.

Each channel contains an AlGaAs light emitting diode which is optically coupled to an integrated high gain photon detector. This combination results in very high

Truth Tables

(Positive Logic)

Multichannel Devices

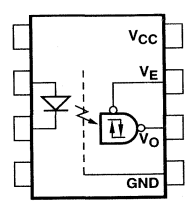
Input	Output
On (H)	H
Off (L)	L

Single Channel DIP

Input	Enable	Output
On (H)	L	L
Off (L)	L	H
On (H)	H	Z
Off (L)	H	Z

Functional Diagram

Multiple Channel Devices Available



CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

5965-3004E

data rate capability. The detector has a threshold with hysteresis, which typically provides 0.25 mA of differential mode noise immunity and minimizes the potential for output signal chatter. The detector in the single channel units has a three state output stage which eliminates the need for a pull-up resistor and allows for direct drive of a data bus.

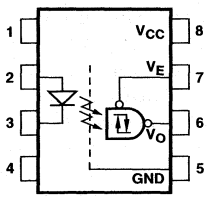
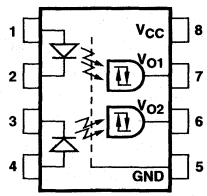
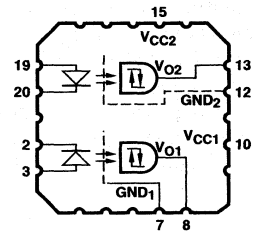
All units are compatible with TTL, STTL, LSTTL, and HCMOS logic families. The 35 ns pulse width distortion specification guarantees a 10 MBd signaling rate at +125°C with 35% pulse width distortion. Figures 13 through 16 show recommended circuits for reducing pulse width distortion and optimizing the signal rate of the product. Package styles for these parts are 8 pin DIP through hole (case outlines P), and leadless ceramic chip carrier (case outline 2). Devices may be purchased with a variety of lead bend and plating options. See Selection Guide Table for details. Standard Military Drawing (SMD) parts are available for each package and lead style.

Because the same electrical die (emitters and detectors) are used for each channel of each device listed in this data sheet, absolute maximum ratings, recommended operating conditions, electrical specifications, and performance characteristics shown in the figures are similar for all parts. Occasional exceptions exist due to package variations and limitations and are as noted. Additionally, the same package assembly processes and materials are used in all devices. These similarities give justification for the use of data obtained from one part to represent other part's performance for die related reliability and certain limited radiation test results.

Selection Guide–Package Styles and Lead Configuration Options

Package	**8 Pin DIP**	**8 Pin DIP**	**20 Pad LCCC**
Lead Style	Through Hole	Through Hole	Surface Mount
Channels	1	2	2
Common Channel Wiring	None	V_{CC}, GND	None
HP Part # & Options			
Commercial	HCPL-5400	HCPL-5430	HCPL-6430
MIL-PRF-38534, Class H	HCPL-5401	HCPL-5431	HCPL-6431
MIL-PRF-38534, Class K	HCPL-540K	HCPL-543K	HCPL-643K
Standard Lead Finish	Gold Plate	Gold Plate	Solder Pads
Solder Dipped	Option #200	Option #200	
Butt Cut/Gold Plate	Option #100	Option #100	
Gull Wing/Soldered	Option #300	Option #300	
SMD Part #			
Prescript for all below	5962-	5962-	5962-
Either Gold or Solder	8957001PX	8957101PX	89571022X
Gold Plate	8957001PC	8957101PC	
Solder Dipped	8957001PA	8957101PA	89571022A
Butt Cut/Gold Plate	8957001YC	8957101YC	
Butt Cut/Soldered	8957001YA	8957101YA	
Gull Wing/Soldered	8957001XA	8957101XA	

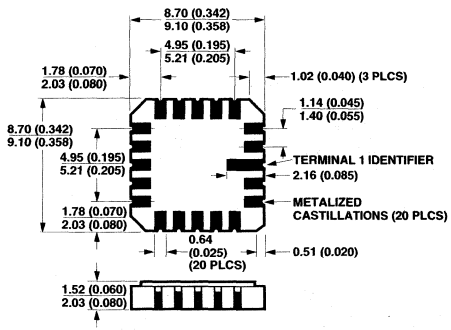
Functional Diagrams

8 Pin DIP	8 Pin DIP	20 Pad LCCC
Through Hole	Through Hole	Surface Mount
1 Channel	2 Channels	2 Channels
		

Note: All DIP devices have common V_{CC} and ground. LCCC (leadless ceramic chip carrier) package has isolated channels with separate V_{CC} and ground connections.

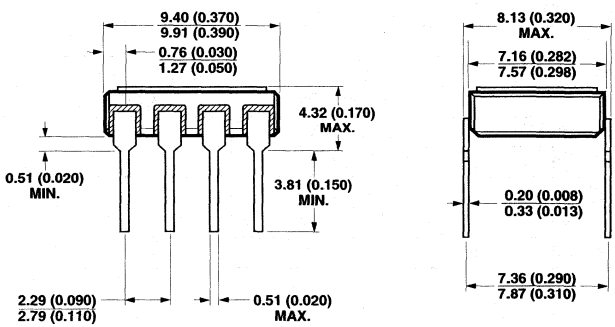
Outline Drawings

20 Terminal LCCC Surface Mount, 2 Channels



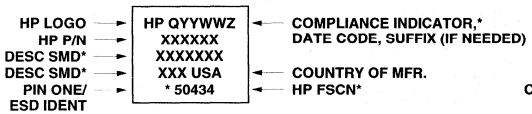
NOTE: DIMENSIONS IN MILLIMETERS (INCHES).
SOLDER THICKNESS 0.127 (0.005) MAX.

8 Pin DIP Through Hole, 1 and 2 Channel



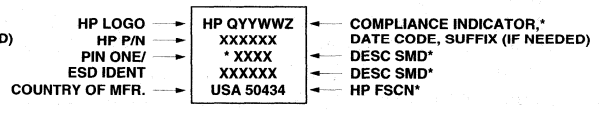
NOTE: DIMENSIONS IN MILLIMETERS (INCHES).

Leaded Device Marking



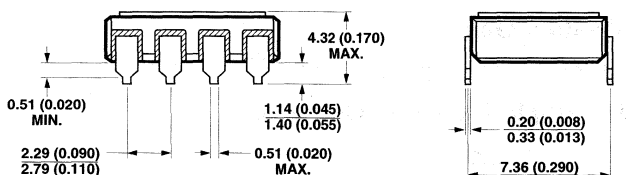
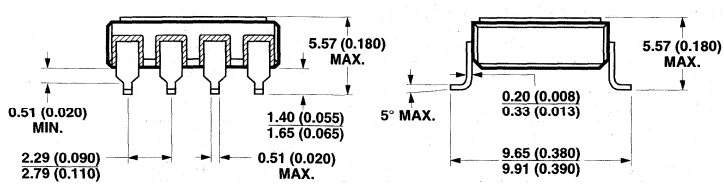
* QUALIFIED PARTS ONLY

Leadless Device Marking



* QUALIFIED PARTS ONLY

Hermetic Optocoupler Options

Option	Description
100	Surface mountable hermetic optocoupler with leads trimmed for butt joint assembly. This option is available on commercial and hi-rel product in 8 pin DIP (see drawings below for details).  NOTE: DIMENSIONS IN MILLIMETERS (INCHES).
200	Lead finish is solder dipped rather than gold plated. This option is available on commercial and hi-rel product in 8 pin DIP. DESC Drawing part numbers contain provisions for lead finish. All leadless chip carrier devices are delivered with solder dipped terminals as a standard feature.
300	Surface mountable hermetic optocoupler with leads cut and bent for gull wing assembly. This option is available on commercial and hi-rel product in 8 pin DIP (see drawings below for details). This option has solder dipped leads.  NOTE: DIMENSIONS IN MILLIMETERS (INCHES).

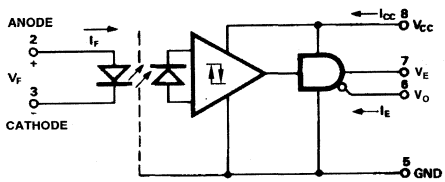
Absolute Maximum Ratings

(No derating required up to +125°C)
Storage Temperature Range, T_S ..... -65°C to +150°C
Operating Temperature, T_A ..... -55°C to +125°C
Case Temperature, T_C ..... +170°C
Junction Temperature, T_J ..... +175°C
Lead Solder Temperature ..... 260°C for 10 s
Average Forward Current, $I_{F\,AVG}$ (each channel) ..... 10 mA
Peak Input Current, $I_{F\,PK}$ (each channel) ..... 20 mA[1]
Reverse Input Voltage, V_R (each channel) ..... 3 V
Supply Voltage, V_{CC} ..... 0.0 V min., 7.0 V max.
Average Output Current, I_O ..... -25 mA min., 25 mA max. (each channel)
Output Voltage, V_O (each channel) ..... -0.5 V min., 10 V max.
Output Power Dissipation, P_O (each channel) ..... 130 mW
Package Power Dissipation, P_D (each channel) ..... 200 mW

Single Channel Product Only

Three State Enable Voltage, V_E ..... -0.5 V min., 10 V max.

8 Pin Ceramic DIP Single Channel Schematic



Note enable pin 7. An external 0.01 µF to 0.1 µF bypass capacitor must be connected between V_{CC} and ground for each package type.

ESD Classification

(MIL-STD-883, Method 3015)
HCPL-5400/01 ..... (ΔΔ), Class 2
HCPL-5430/31 and HCPL-6430/31 ..... (Dot), Class 3

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Input Current (High)	$I_{F(ON)}$	6	10	mA
Supply Voltage, Output	V_{CC}	4.75	5.25	V
Input Voltage (Low)	$V_{F(OFF)}$	–	0.7	V
Fan Out (Each Channel)	N	–	5	TTL Loads
Single Channel Product Only				
High Level Enable Voltage	V_{EH}	2.0	V_{CC}	V
Low Level Enable Voltage	V_{EL}	0	0.8	V

Electrical Characteristics

T_A = -55°C to +125°C, 4.5 V ≤ V_{CC} ≤ 5.25 V, 6 mA ≤ $I_{F(ON)}$ ≤ 10 mA, 0 V ≤ $V_{F(OFF)}$ ≤ 0.7 V, unless otherwise specified.

Parameter		Sym.	Test Conditions	Group A[10] Subgroups	Limits Min.	Typ.*	Max.	Units	Fig.	Notes
Low Level Output Voltage		V_{OL}	I_{OL} = 8.0 mA (5 TTL Loads)	1, 2, 3		0.3	0.5	V	1	9
High Level Output Voltage		V_{OH}	I_{OH} = -4.0 mA	1, 2, 3	2.4			V	2	9
Output Leakage Current		I_{OHH}	V_O = 5.25 V, V_F = 0.7 V	1, 2, 3			100	µA		9
Logic High Supply Current	Single Channel	I_{CCH}	V_{CC} = 5.25 V, V_E = 0 V (Single Channel Only)	1, 2, 3		17	26	mA		
	Dual Channel					34	52			13
Logic Low Supply Current	Single Channel	I_{CCL}		1. 2. 3		19	26	mA		
	Dual Channel					38	52			13
Input Forward Voltage		V_F	I_F = 10 mA	1, 2, 3	1.0	1.35	1.85	V	4	9
Input Reverse Breakdown Voltage		V_R	I_R = 10 µA	1, 2, 3	3.0	4.8		V		9
Input-Output Insulation Leakage Current		I_{I-O}	V_{I-O} = 1500 Vdc, RH = 45%, t = 5 s	1			1.0	µA		2, 3
Propagation Delay Time Logic Low Output		t_{PHL}		9, 10, 11		33	60	ns	5, 6, 7	4, 9
Propagation Delay Time Logic High Output		t_{PLH}		9, 10, 11		30	60	ns	5, 6, 7	4, 9
Pulse Width Distortion		PWD		9, 10, 11		3	35	ns	5, 6, 7	4, 9
Logic High Common Mode Transient Immunity		$\|CM_H\|$	V_{CM} = 50 V_{P-P}, I_F = 0 mA	9, 10, 11	500	3000		V/µs	11	5, 9, 11
Logic Low Common Mode Transient Immunity		$\|CM_L\|$	V_{CM} = 50 V_{P-P}, I_F = 6 mA	9, 10, 11	500	3000		V/µs	11	5, 9, 11

Single Channel Product Only

Parameter	Sym.	Test Conditions	Group A[10] Subgroups	Limits Min.	Typ.*	Max.	Units	Fig.	Notes
Logic High Enable Voltage	V_{EH}		1, 2, 3	2.0			V		
Logic Low Enable Voltage	V_{EL}		1, 2, 3			0.8	V		
Logic High Enable Current	I_{EH}	V_E = 2.4 V	1, 2, 3			20	µA		
		V_E = 5.25 V	1, 2, 3			100			
Logic Low Enable Current	I_{EL}	V_E = 0.4 V	1, 2, 3		-0.28	-0.4	mA		
High Impedance State Supply Current	I_{CCZ}	V_{CC} = 5.25 V, V_E = 5.25 V	1, 2, 3		22	28	mA		
High Impedance State Output Current	I_{OZL}	V_O = 0.4 V, V_E = 2 V	1, 2, 3			-20	µA		
	I_{OZH}	V_O = 2.4 V, V_E = 2 V				20			
		V_O = 5.25 V, V_E = 2 V				100			

*All typical values are at V_{CC} = 5 V, T_A = 25°C, I_F = 8 mA except where noted.

Typical Characteristics

All typical values are at T_A = 25°C, V_{CC} = 5 V, I_F = 8 mA, unless otherwise specified.

Parameter	Symbol	Typ.	Units	Test Conditions	Fig.	Notes
Input Current Hysteresis	I_{HYS}	0.25	mA	V_{CC} = 5 V	3	
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$	-1.11	mV/°C	I_F = 10 mA	4	
Resistance (Input-Output)	R_{I-O}	10^{12}	Ω	V_{I-O} = 500 V		2
Capacitance (Input-Output)	C_{I-O}	0.6	pF	f = 1 MHz, V_{I-O} = 0 V		2
Logic Low Short Circuit Output Current	I_{OSL}	65	mA	V_O = V_{CC} = 5.25 V, I_F = 10 mA		6, 9
Logic High Short Circuit Output Current	I_{OSH}	-50	mA	V_{CC} = 5.25 V, I_F = 0 mA, V_O = GND		6, 9
Output Rise Time (10-90%)	t_r	15	ns		5	
Output Fall Time (90-10%)	t_f	10	ns		5	
Propagation Delay Skew	t_{PSK}	30	ns		10	12
Power Supply Noise Immunity	PSNI	0.5	V_{P-P}	48 Hz ≤ f_{ac} ≤ 50 MHz		7

Single Channel Product Only

Parameter	Symbol	Typ.	Units	Test Conditions	Fig.	Notes
Input Capacitance	C_{IN}	15	pF	f = 1 MHz, V_F = 0 V, Pins 2 and 3		
Output Enable Time to Logic High	t_{PZH}	15	ns		8, 9	
Output Enable Time to Logic Low	t_{PZL}	30	ns		8, 9	
Output Disable Time from Logic High	t_{PHZ}	20	ns		8, 9	
Output Disable Time from Logic Low	t_{PLZ}	15	ns		8, 9	

Dual and Quad Channel Product Only

Input Capacitance	C_{IN}	15	pF	f = 1 MHz, V_O = 0 V		
Input-Input Leakage Current	I_{I-I}	0.5	nA	RH = 45%, V_{I-I} = 500 Vdc		8
Input-Input Resistance	R_{I-I}	10^{12}	Ω	V_{I-I} = 500 V		8
Input-Input Capacitance	C_{I-I}	1.3	pF	f = 1 MHz, V_F = 0 V		8

Notes:

1. Not to exceed 5% duty factor, not to exceed 50 µsec pulse width.
2. All devices are considered two-terminal devices: measured between all input leads or terminals shorted together and all output leads or terminals shorted together.
3. This is a momentary withstand test, not an operating condition.
4. t_{PHL} propagation delay is measured from the 50% point on the rising edge of the input current pulse to the 1.5 V point on the falling edge of the output pulse. The t_{PLH} propagation delay is measured from the 50% point on the falling edge of the input current pulse to the 1.5 V point on the rising edge of the output pulse. Pulse Width Distortion, PWD = $|t_{PHL} - t_{PLH}|$.
5. CM_L is the maximum slew rate of the common mode voltage that can be sustained with the output voltage in the logic low state ($V_{O(MAX)}$ < 0.8 V). CM_H is the maximum slew rate of the common mode voltage that can be sustained with the output voltage in the logic high state ($V_{O(MIN)}$ > 2.0 V).
6. Duration of output short circuit time not to exceed 10 ms.
7. Power Supply Noise Immunity is the peak to peak amplitude of the ac ripple voltage on the V_{CC} line that the device will withstand and still remain in the desired logic state. For desired logic high state, $V_{OH(MIN)}$ > 2.0 V, and for desired logic low state, $V_{OL(MAX)}$ < 0.8 V.
8. Measured between adjacent input pairs shorted together for each multichannel device.
9. Each channel.
10. Standard parts receive 100% testing at 25°C (Subgroups 1 and 9). SMD and hi-rel parts receive 100% testing at 25, 125, and –55°C (Subgroups 1 and 9, 2 and 10, 3 and 11, respectively).
11. Parameters are tested as part of device initial characterization and after design and process changes. Parameters are guaranteed to limits specified for all lots not specifically tested.
12. Propagation delay skew is defined as the difference between the minimum and maximum propagation delays for any given group of optocouplers with the same part number that are all switching at the same time under the same operating conditions.
13. The HCPL-6430 and HCPL-6431 dual channel parts function as two independent single channel units. Use the single channel parameter limits.

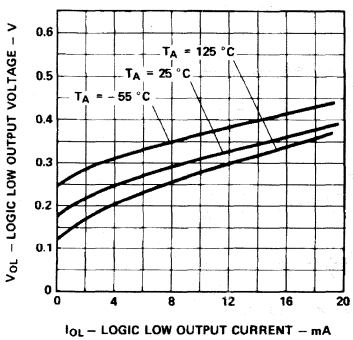


Figure 1. Typical Logic Low Output Voltage vs. Logic Low Output Current.

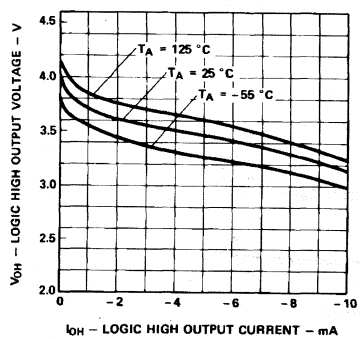


Figure 2. Typical Logic High Output Voltage vs. Logic High Output Current.

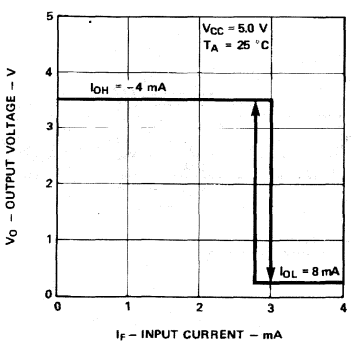


Figure 3. Typical Output Voltage vs. Input Forward Current.

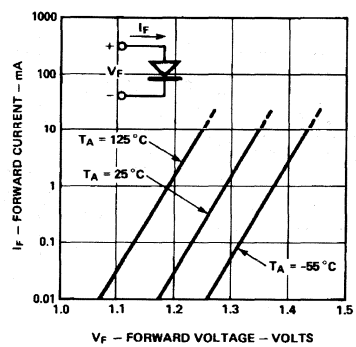
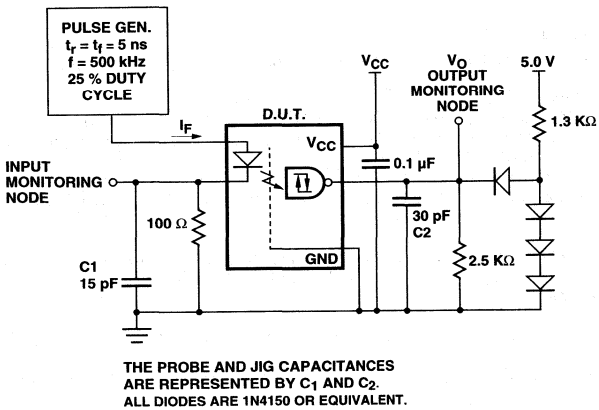


Figure 4. Typical Diode Input Forward Current Characteristic.



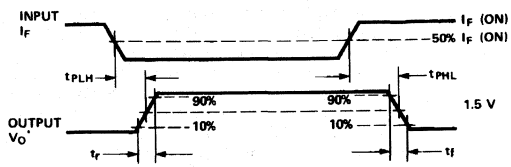


Figure 5. Test Circuit for t_{PLH}, t_{PHL}, t_r, and t_f.

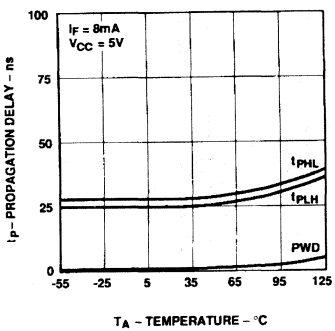


Figure 6. Typical Propagation Delay vs. Ambient Temperature.

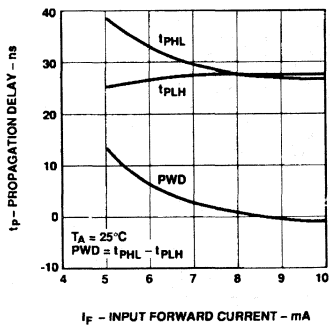
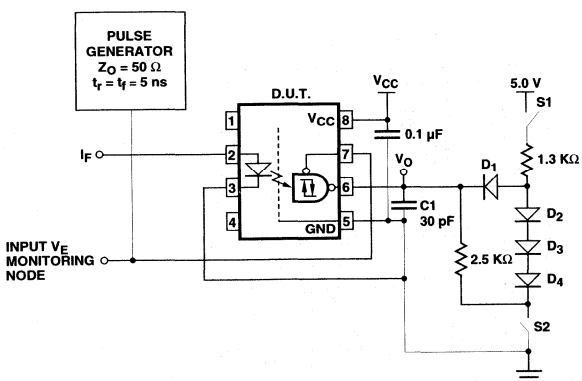
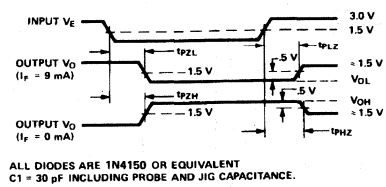


Figure 7. Typical Propagation Delay vs. Input Forward Current.





SWITCH MATRIX

	S_1	S_2
t_{PHZ}	CLOSED	CLOSED
t_{PZH}	OPEN	CLOSED
t_{PLZ}	CLOSED	CLOSED
t_{PZL}	CLOSED	OPEN

Figure 8. Test Circuit for t_{PHZ}, t_{PZH}, t_{PLZ}, and t_{PZL}. (Single Channel Product Only).

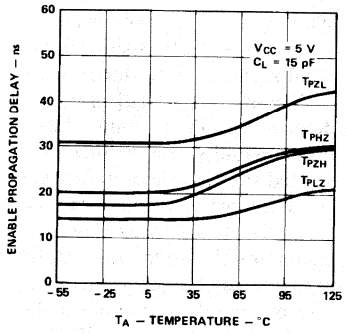


Figure 9. Typical Enable Propagation Delay vs. Ambient Temperature. (Single Channel Product Only).

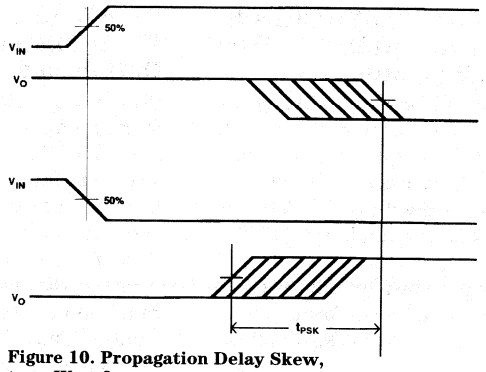


Figure 10. Propagation Delay Skew, t_{PSK}, Waveform.

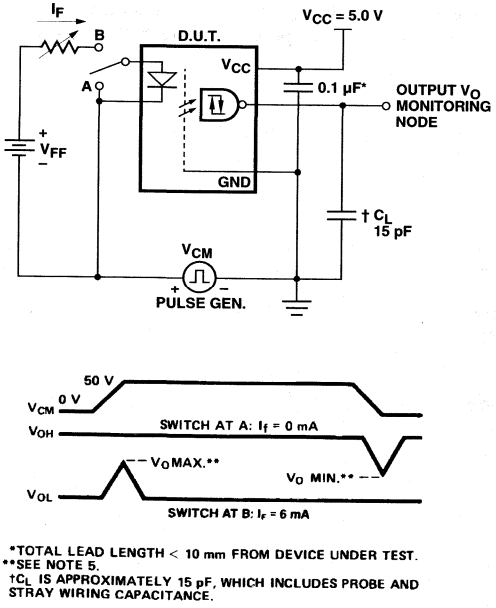


Figure 11. Test Diagram for Common Mode Transient Immunity and Typical Waveforms.

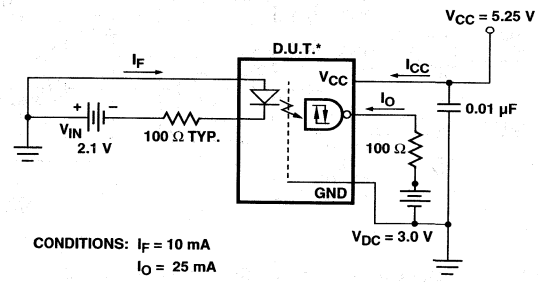


Figure 12. Operating Circuit for Burn-In and Steady State Life Tests.

MIL-PRF-38534 Class H, Class K, and DESC SMD Test Program

Hewlett-Packard's Hi-Rel Optocouplers are in compliance with MIL-PRF-38534 Classes H and K. Class H devices are also in compliance with DESC drawings 5962-89570, and 5962-89571.

Testing consists of 100% screening and quality conformance inspection to MIL-PRF-38534.

Data Rate and Pulse-Width Distortion Definitions

Propagation delay is a figure of merit which describes the finite amount of time required for a system to translate information from input to output when shifting logic levels. Propagation delay from low to high (t_{PLH}) specifies the amount of time required for a system's output to change from a Logic 0 to a Logic 1, when given a stimulus at the input. Propagation delay from high to low (t_{PHL}) specifies the amount of time required for a system's output to change from a Logic 1 to a Logic 0, when given a stimulus at the input (see Figure 5).

When t_{PLH} and t_{PHL} differ in value, pulse width distortion results. Pulse width distortion is defined as $|t_{PHL} - t_{PLH}|$ and determines the maximum data rate capability of a distortion-limited system. Maximum pulse width distortion on the order of 25-35% is typically used when specifying the maximum data rate capabilities of systems. The exact figure depends on the particular application (RS-232, PCM, T-1, etc.).

These high performance optocouplers offer the advantages of specified propagation delay (t_{PLH}, t_{PHL}), and pulse width distortion ($|t_{PLH} - t_{PHL}|$) over temperature and power supply voltage ranges.

Applications

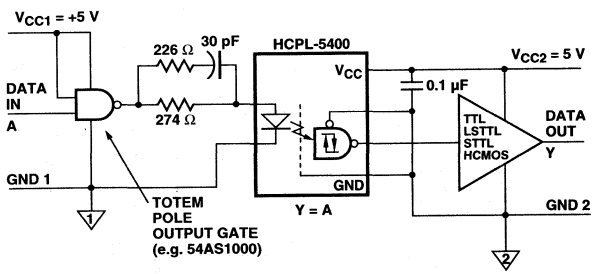


Figure 13. Recommended HCPL-5400 Interface Circuit.

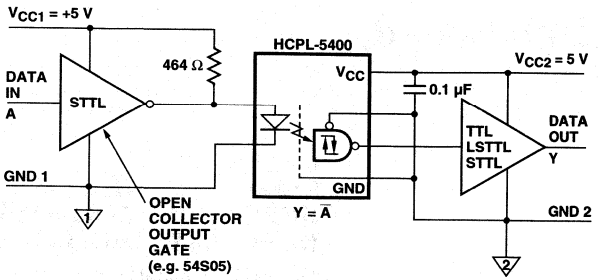


Figure 14. Alternative HCPL-5400 Interface Circuit.

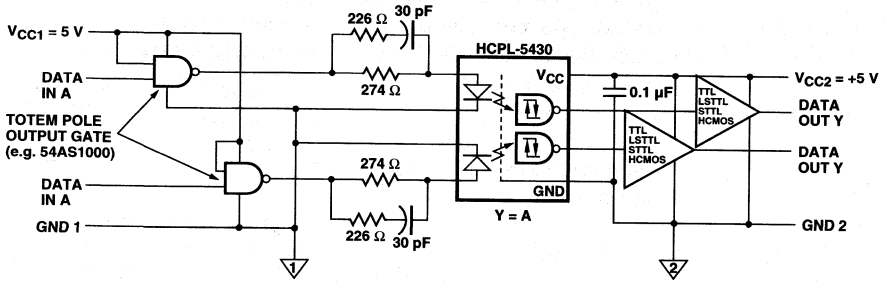


Figure 15. Recommended HCPL-5430 and HCPL-6430 Interface Circuit.

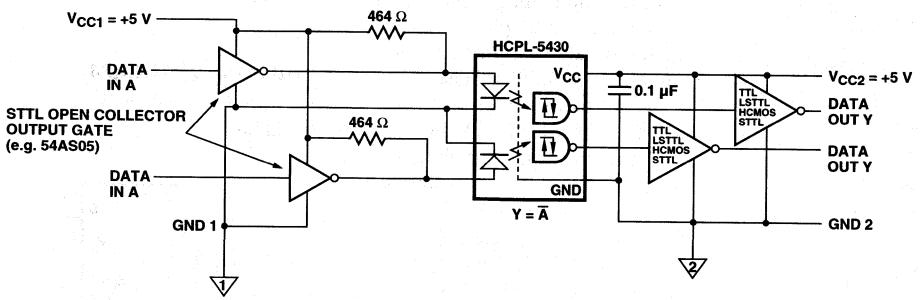


Figure 16. Alternative HCPL-5430 and HCPL-6430 Interface Circuit.

HEWLETT® PACKARD

Hermetically Sealed, High Speed, High CMR, Logic Gate Optocouplers

Technical Data

6N134*
81028 **HCPL-665X**
HCPL-563X **5962-90855**
HCPL-663X **HCPL-560X**

*See matrix for available extensions.

Features

- **Dual Marked with Device Part Number and DESC Drawing Number**
- **Manufactured and Tested on a MIL-PRF-38534 Certified Line**
- **QML-38534, Class H and K**
- **Five Hermetically Sealed Package Configurations**
- **Performance Guaranteed over -55°C to +125°C**
- **High Speed: 10 M Bit/s**
- **CMR: > 10,000 V/µs Typical**
- **1500 Vdc Withstand Test Voltage**
- **High Radiation Immunity**
- **6N137, HCPL-2601, HCPL-2630/-31 Function Compatibility**
- **Reliability Data**
- **TTL Circuit Compatibility**

Applications

- **Military and Space**
- **High Reliability Systems**
- **Transportation, Medical, and Life Critical Systems**
- **Line Receiver**
- **Voltage Level Shifting**
- **Isolated Input Line Receiver**
- **Isolated Output Line Driver**
- **Logic Ground Isolation**
- **Harsh Industrial Environments**
- **Isolation for Computer, Communication, and Test Equipment Systems**

Description

These units are single, dual and quad channel, hermetically sealed optocouplers. The products are capable of operation and storage over the full military temperature range and can be purchased as either standard product or with full MIL-PRF-38534 Class Level H or K testing or from the appropriate DESC Drawing. All devices are manufactured and tested on a MIL-PRF-38534 certified line and are included in the DESC Qualified Manufacturers List QML-38534 for Hybrid Microcircuits. Quad channel devices are available by special order in the 16 pin DIP through hole packages.

Truth Table

(Positive Logic)

Multichannel Devices

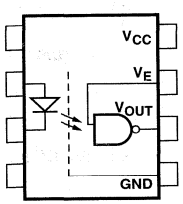
Input	Output
On (H)	L
Off (L)	H

Single Channel DIP

Input	Enable	Output
On (H)	H	L
Off (L)	H	H
On (H)	L	H
Off (L)	L	H

Functional Diagram

Multiple Channel Devices Available



CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Each channel contains a GaAsP light emitting diode which is optically coupled to an integrated high speed photon detector. The output of the detector is an open collector Schottky clamped transistor. Internal shields provide a guaranteed common mode transient immunity specification of 1000 V/μs. Selection for higher levels of CMR values are available by special request. Package styles for these parts are 8 and 16 pin DIP through hole (case outlines P and E respectively), 16 pin DIP flat pack (case outline F), and leadless ceramic chip carrier (case outline 2). Devices may be purchased with a variety of lead bend and plating options. See Selection Guide Table for details. Standard Military Drawing (SMD) parts are available for each package and lead style.

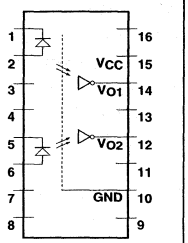
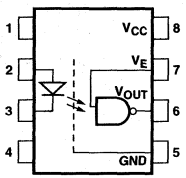
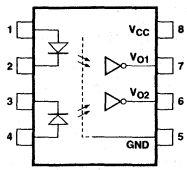
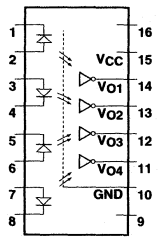
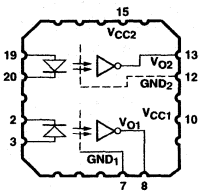
Because the same electrical die (emitters and detectors) are used for each channel of each device listed in this data sheet, absolute maximum ratings, recommended operating conditions, electrical specifications, and performance characteristics shown in the figures are identical for all parts. Occasional exceptions exist due to package variations and limitations, and are as noted. Additionally, the same package assembly processes and materials are used in all devices. These similarities give justification for the use of data obtained from one part to represent other parts' performance for die related reliability and certain limited radiation test results.

Selection Guide–Package Styles and Lead Configuration Options

Package	**16 Pin DIP**	**8 Pin DIP**	**8 Pin DIP**	**16 Pin Flat Pack**	**20 Pad LCCC**
Lead Style	Through Hole	Through Hole	Through Hole	Unformed Leads	Surface Mount
Channels	2	1	2	4	2
Common Channel Wiring	V_{CC}, GND	None	V_{CC}, GND	V_{CC}, GND	None
HP Part # & Options					
Commercial	6N134*	HCPL-5600	HCPL-5630	HCPL-6650	HCPL-6630
MIL-PRF-38534, Class H	6N134/883B	HCPL-5601	HCPL-5631	HCPL-6651	HCPL-6631
MIL-PRF-38534, Class K	HCPL-268K	HCPL-560K	HCPL-563K	HCPL-665K	HCPL-663K
Standard Lead Finish	Gold Plate	Gold Plate	Gold Plate	Gold Plate	Solder Pads
Solder Dipped	Option #200	Option #200	Option #200		
Butt Cut/Gold Plate	Option #100	Option #100	Option #100		
Gull Wing/Soldered	Option #300	Option #300	Option #300		
SMD Part #					
Prescript for all below	None	5962-	None	None	None
Either Gold or Solder	8102801EX	9085501HPX	8102802PX	8102804FX	81028032X
Gold Plate	8102801EC	9085501HPC	8102802PC	8102804FC	
Solder Dipped	8102801EA	9085501HPA	8102802PA		81028032A
Butt Cut/Gold Plate	8102801UC	9085501HYC	8102802YC		
Butt Cut/Soldered	8102801UA	9085501HYA	8102802YA		
Gull Wing/Soldered	8102801TA	9085501HXA	8102802ZA		

*JEDEC registered part.

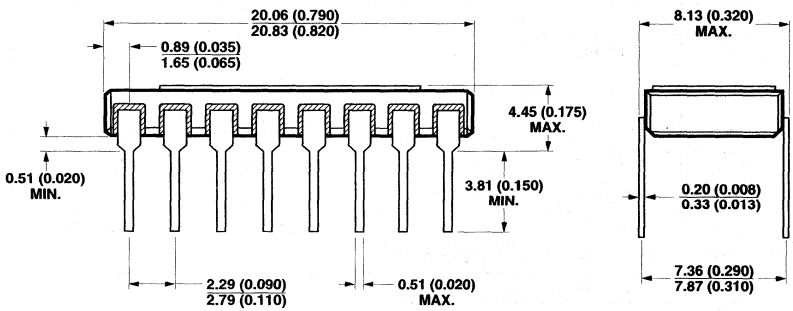
Functional Diagrams

16 Pin DIP	8 Pin DIP	8 Pin DIP	16 Pin Flat Pack	20 Pad LCCC
Through Hole	Through Hole	Through Hole	Unformed Leads	Surface Mount
2 Channels	1 Channel	2 Channels	4 Channels	2 Channels
				

Note: All DIP and flat pack devices have common V_{CC} and ground. Single channel DIP has an enable pin 7. LCCC (leadless ceramic chip carrier) package has isolated channels with separate V_{CC} and ground connections.

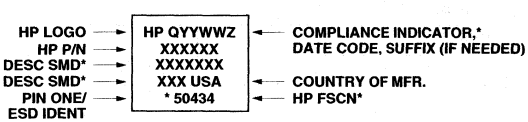
Outline Drawings

16 Pin DIP Through Hole, 2 Channels



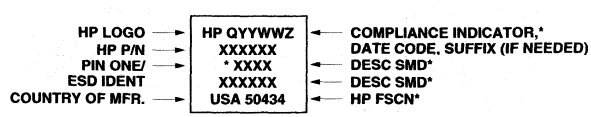
NOTE: DIMENSIONS IN MILLIMETERS (INCHES).

Leaded Device Marking



* QUALIFIED PARTS ONLY

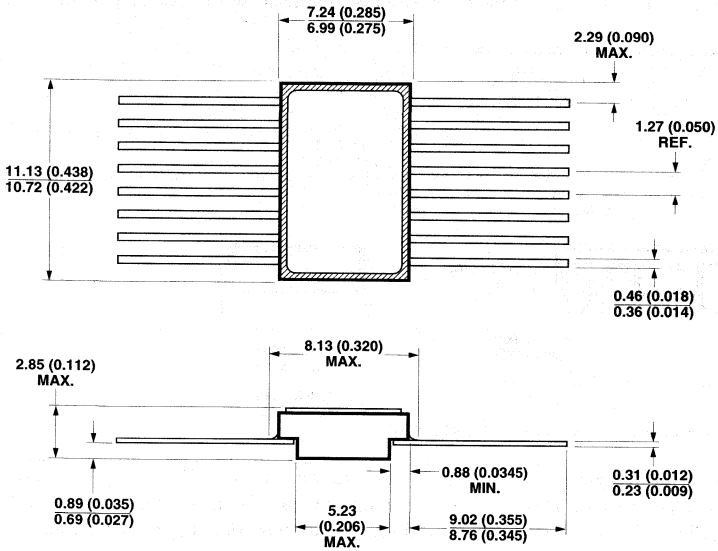
Leadless Device Marking



* QUALIFIED PARTS ONLY

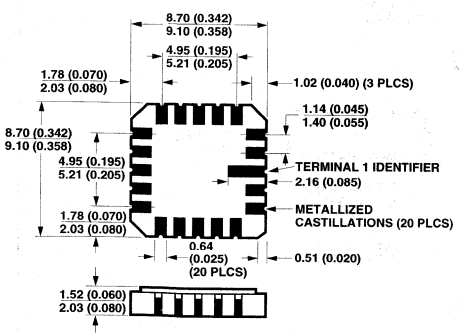
Outline Drawings (continued)

16 Pin Flat Pack, 4 Channels



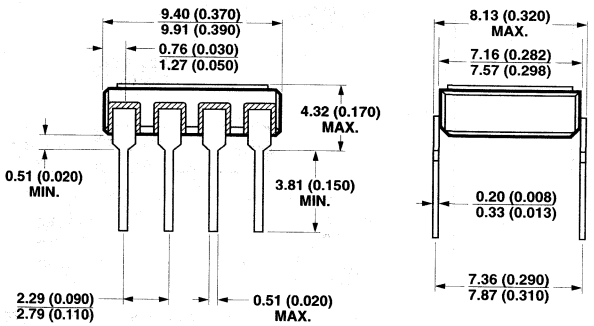
NOTE: DIMENSIONS IN MILLIMETERS (INCHES).

20 Terminal LCCC Surface Mount, 2 Channels



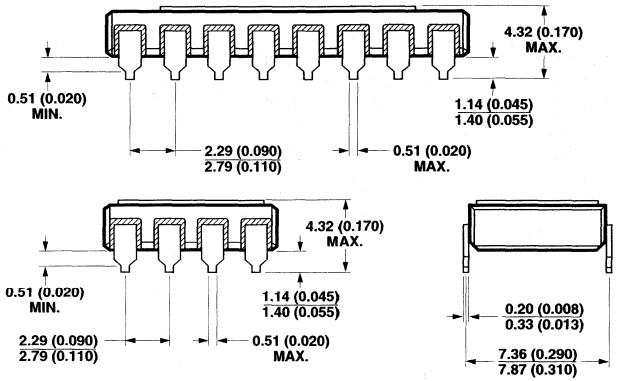
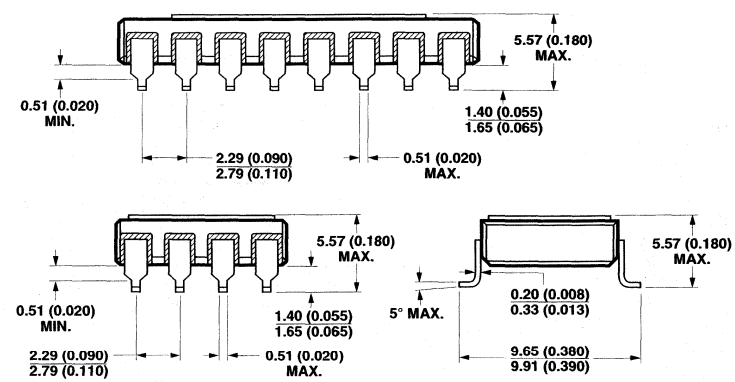
NOTE: DIMENSIONS IN MILLIMETERS (INCHES).
SOLDER THICKNESS 0.127 (0.005) MAX.

8 Pin DIP Through Hole, 1 and 2 Channel



NOTE: DIMENSIONS IN MILLIMETERS (INCHES).

Hermetic Optocoupler Options

Option	Description
100	Surface mountable hermetic optocoupler with leads trimmed for butt joint assembly. This option is available on commercial and hi-rel product in 8 and 16 pin DIP (see drawings below for details).  NOTE: DIMENSIONS IN MILLIMETERS (INCHES).
200	Lead finish is solder dipped rather than gold plated. This option is available on commercial and hi-rel product in 8 and 16 pin DIP. DESC Drawing part numbers contain provisions for lead finish. All leadless chip carrier devices are delivered with solder dipped terminals as a standard feature.
300	Surface mountable hermetic optocoupler with leads cut and bent for gull wing assembly. This option is available on commercial and hi-rel product in 8 and 16 pin DIP (see drawings below for details). This option has solder dipped leads.  NOTE: DIMENSIONS IN MILLIMETERS (INCHES).

Absolute Maximum Ratings

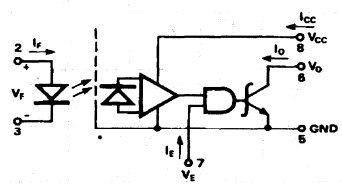
(No derating required up to +125°C)
Storage Temperature Range, T_S ..... -65°C to +150°C
Operating Temperature, T_A ..... -55°C to +125°C
Case Temperature, T_C ..... +170°C
Junction Temperature, T_J ..... +175°C
Lead Solder Temperature ..... 260°C for 10 s
Peak Forward Input Current, $I_{F\,PK}$, (each channel,
≤ 1 ms duration) ..... 40 mA
Average Input Forward Current, $I_{F\,AVG}$ (each channel) ..... 20 mA
Input Power Dissipation (each channel) ..... 35 mW
Reverse Input Voltage, V_R (each channel) ..... 5 V
Supply Voltage, V_{CC} (1 minute maximum) ..... 7 V
Output Current, I_O (each channel) ..... 25 mA
Output Power Dissipation (each channel) ..... 40 mW
Output Voltage, V_O (each channel) ..... 7 V*
Package Power Dissipation, P_D (each channel) ..... 200 mW

*Selection for higher output voltages up to 20 V is available.

Single Channel Product Only

Emitter Input Voltage, V_E ..... 5.5 V

8 Pin Ceramic DIP Single Channel Schematic



Note enable pin 7. An external 0.01 µF to 0.1 µF bypass capacitor must be connected between V_{CC} and ground for each package type.

ESD Classification

(MIL-STD-883, Method 3015)
HCPL-5600/01 ..... (Δ), Class 1
6N134, 6N134/883B, HCPL-5630/31,
HCPL-6630/31 and HCPL-6650/51 ..... (Dot), Class 3

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Input Current, Low Level, Each Channel	I_{FL}	0	250	µA
Input Current, High Level, Each Channel*	I_{FH}	10	20	mA
Supply Voltage, Output	V_{CC}	4.5	5.5	V
Fan Out (TTL Load) Each Channel	N		6	

*Meets or exceeds DESC SMD and JEDEC requirements.

Recommended Operating Conditions (cont'd.)

Single Channel Product Only[10]

Parameter	Symbol	Min.	Max.	Units
High Level Enable Voltage	V_{EH}	2.0	V_{CC}	V
Low Level Enable Voltage	V_{EL}	0	0.8	V

Electrical Characteristics (T_A = -55°C to +125°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Group A[13] Subgroups	Limits Min.	Limits Typ.**	Limits Max.	Units	Fig.	Note
High Level Output Current		I_{OH}*	V_{CC} = 5.5 V, V_O = 5.5 V, I_F = 250 µA	1, 2, 3		20	250	µA	1	1
Low Level Output Voltage		V_{OL}*	V_{CC} = 5.5 V, I_F = 10 mA, I_{OL} (Sinking) = 10 mA	1, 2, 3		0.3	0.6	V	2	1, 9
Current Transfer Ratio		h_F CTR	V_O = 0.6 V, I_F = 10 mA, V_{CC} = 5.5 V	1, 2, 3	100			%		1
Logic High Supply Current	Single Channel	I_{CCH}*	V_{CC} = 5.5 V, I_F = 0 mA	1, 2, 3		9	14	mA		1
	Dual Channel		V_{CC} = 5.5 V, I_{F1} = I_{F2} = 0 mA			18	28	mA		6
	Quad Channel		V_{CC} = 5.5 V, I_{F1} = I_{F2} = I_{F3} = I_{F4} = 0 mA			25	42	mA		
Logic Low Supply Current	Single Channel	I_{CCL}*	V_{CC} = 5.5 V, I_F = 20 mA	1, 2, 3		13	18	mA		1
	Dual Channel		V_{CC} = 5.5 V, I_{F1} = I_{F2} = 20 mA			26	36	mA		6
	Quad Channel		V_{CC} = 5.5 V, I_{F1} = I_{F2} = I_{F3} = I_{F4} = 20 mA			33	50	mA		
Input Forward Voltage		V_F*	I_F = 20 mA	1, 2, 3		1.5	1.9	V	3	1, 15
				1, 2		1.55	1.75	V	3	1, 16
				3			1.85			
Input Reverse Breakdown Voltage		BV_R*	I_R = 10 µA	1, 2, 3	5			V		1
Input-Output Leakage Current		I_{I-O}*	V_{I-O} = 1500 Vdc, RH = 45% T_A = 25°C, t = 5 s	1			1.0	µA		2, 8
Capacitance Between Input/ Output		C_{I-O}	f = 1 MHz, T_C = 25°C	4		1.0	4.0	pF		1, 3, 14

*Identified test parameters for JEDEC registered parts.
**All typical values are at V_{CC} = 5 V, T_A = 25°C.

Electrical Characteristics, (Contd.) T_A = -55°C to +125°C unless otherwise specified

Parameter	Symbol	Test Conditions	Group A[13] Subgroups	Limits Min.	Limits Typ.**	Limits Max.	Units	Fig.	Note
Propagation Delay Time to High Output Level	t_{PLH}*	V_{CC} = 5 V, R_L = 510 Ω, C_L = 50 pF, I_F = 13 mA	9		60	100	ns	4, 5, 6	1, 5
			10, 11			140			
Propagation Delay Time to Low Output Level	t_{PHL}*		9		55	100	ns		
			10, 11			120			
Output Rise Time	t_{LH}	R_L = 510 Ω, C_L = 50 pF, I_F = 13 mA	9, 10, 11		35	90	ns		1
Output Fall Time	t_{HL}				35	40			
Common Mode Transient Immunity at High Output Level	$\|CM_H\|$	V_{CM} = 50 V (PEAK), V_{CC} = 5 V, V_O (min.) = 2 V, R_L = 510 Ω, I_F = 0 mA	9, 10, 11	1000	>10000		V/µs	7	1, 7, 14
Common Mode Transient Immunity at Low Output Level	$\|CM_L\|$	V_{CM} = 50 V (PEAK), V_{CC} = 5 V, V_O (max.) = 0.8 V, R_L = 510 kΩ, I_F = 10 mA	9, 10, 11	1000	>10000		V/µs	7	1, 7, 14

Single Channel Product Only

Low Level Enable Current	I_{EL}	V_{CC} = 5.5 V, V_E = 0.5 V	1, 2, 3		-1.45	-2.0	mA		
High Level Enable Voltage	V_{EH}		1, 2, 3	2.0			V		10
Low Level Enable Voltage	V_{EL}		1, 2, 3			0.8	V		

*Identified test parameters for JEDEC registered part.
**All typical values are at V_{CC} = 5 V, T_A = 25°C.

Typical Characteristics, T_A = 25°C, V_{CC} = 5 V

Parameter	Sym.	Typ.	Units	Test Conditions	Fig.	Note
Input Capacitance	C_{IN}	60	pF	V_F = 0 V, f = 1 MHz		1
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$	-1.5	mV/°C	I_F = 20 mA		1
Resistance (Input-Output)	R_{I-O}	10^{12}	Ω	V_{I-O} = 500 V		2

Single Channel Product Only

Propagation Delay Time of Enable from V_{EH} to V_{EL}	t_{ELH}	35	ns	R_L = 510 Ω, C_L = 50 pF, I_F = 13 mA, V_{EH} = 3 V, V_{EL} = 0 V	8, 9	1, 11
Propagation Delay Time of Enable from V_{EL} to V_{EH}	t_{EHL}	35	ns			1, 12

Dual and Quad Channel Product Only

Input-Input Leakage Current	I_{I-I}	0.5	nA	Relative Humidity = 45% V_{I-I} = 500 V, t = 5 s		4
Resistance (Input-Input)	R_{I-I}	10^{12}	Ω	V_{I-I} = 500 V		4
Capacitance (Input-Input)	C_{I-I}	0.55	pF	f = 1 MHz		4

Notes:

1. Each channel.
2. All devices are considered two-terminal devices; I_{I-O} is measured between all input leads or terminals shorted together and all output leads or terminals shorted together.
3. Measured between each input pair shorted together and all output connections for that channel shorted together.
4. Measured between adjacent input pairs shorted together for each multichannel device.
5. t_{PHL} propagation delay is measured from the 50% point on the leading edge of the input pulse to the 1.5 V point on the leading edge of the output pulse. The t_{PLH} propagation delay is measured from the 50% point on the trailing edge of the input pulse to the 1.5 V point on the trailing edge of the output pulse.
6. The HCPL-6630 and HCPL-6631 dual channel parts function as two independent single channel units. Use the single channel parameter limits for each channel.
7. CM_L is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic low state (V_O < 0.8 V). CM_H is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic high state (V_O > 2.0 V).
8. This is a momentary withstand test, not an operating condition.
9. It is essential that a bypass capacitor (0.01 to 0.1 μF, ceramic) be connected from V_{CC} to ground. Total lead length between both ends of this external capacitor and the isolator connections should not exceed 20 mm.
10. No external pull up is required for a high logic state on the enable input.
11. The t_{ELH} enable propagation delay is measured from the 1.5 V point on the trailing edge of the enable input pulse to the 1.5 V point on the trailing edge of the output pulse.
12. The t_{EHL} enable propagation delay is measured from the 1.5 V point on the leading edge of the enable input pulse to the 1.5 V point on the leading edge of the output pulse.
13. Standard parts receive 100% testing at 25°C (Subgroups 1 and 9). SMD and 883B parts receive 100% testing at 25, 125, and -55°C (Subgroups 1 and 9, 2 and 10, 3 and 11, respectively).
14. Parameters are tested as part of device initial characterization and after design and process changes. Parameters are guaranteed to limits specified for all lots not specifically tested.
15. Not required for 6N134, 6N134/883B and 8102801 types.
16. Required for 6N134, 6N134/883B and 8102801 types only.

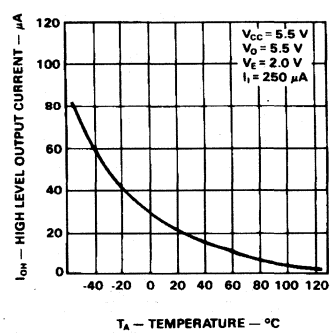


Figure 1. High Level Output Current vs. Temperature.

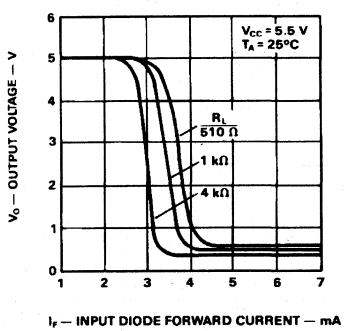


Figure 2. Input-Output Characteristics.

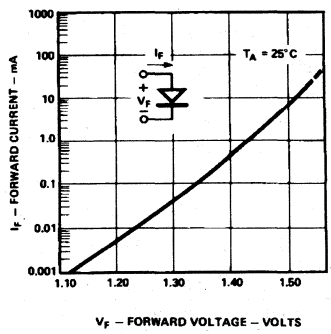
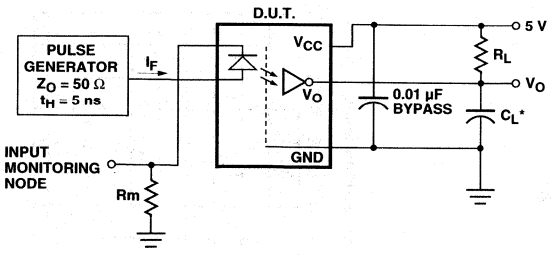


Figure 3. Input Diode Forward Characteristic.



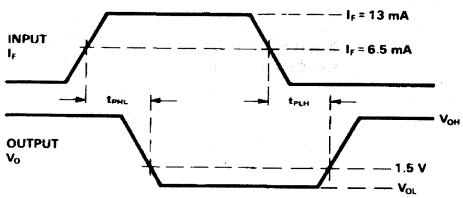


Figure 4. Test Circuit for t_{PHL} and t_{PLH}.*

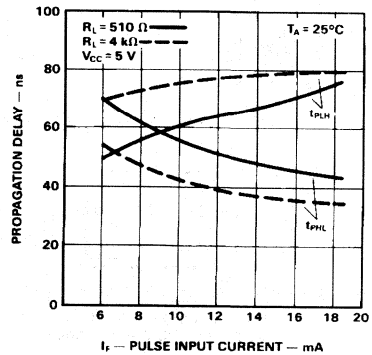


Figure 5. Propagation Delay, t_{PHL} and t_{PLH} vs. Pulse Input Current, I_{FH}.

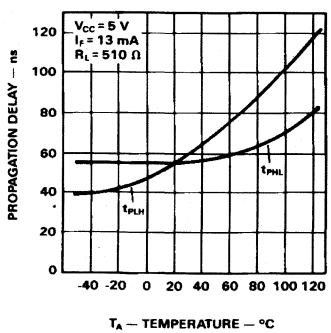


Figure 6. Propagation Delay vs. Temperature.

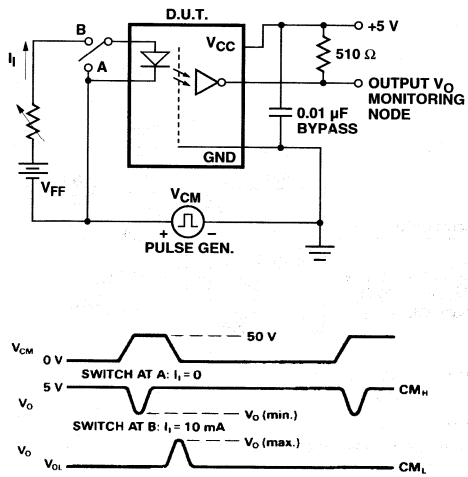


Figure 7. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

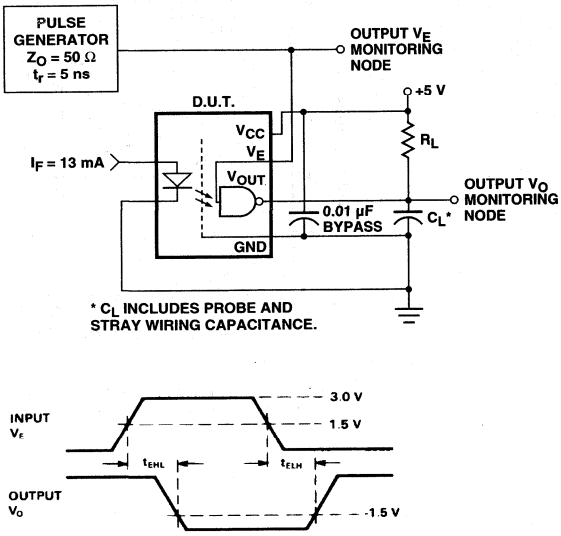


Figure 8. Test Circuit for t_{EHL} and t_{ELH}.

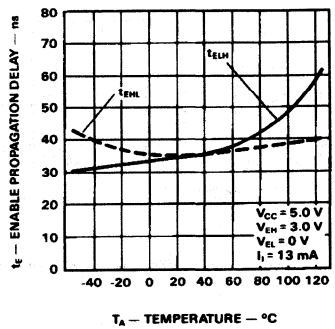


Figure 9. Enable Propagation Delay vs. Temperature.

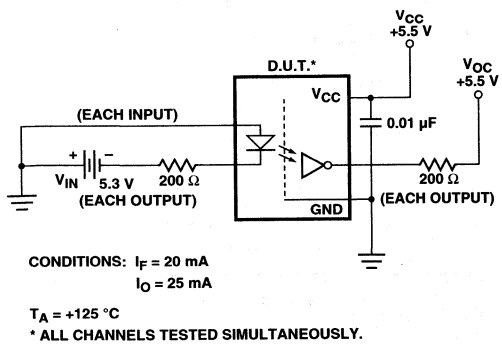


Figure 10. Operating Circuit for Burn-In and Steady State Life Tests.

MIL-PRF-38534 Class H, Class K, and DESC SMD Test Program

Hewlett-Packard's Hi-Rel Optocouplers are in compliance with MIL-PRF-38534 Classes H and K. Class H devices are also in compliance with DESC drawings 81028, and 5962-90855.

Testing consists of 100% screening and quality conformance inspection to MIL-PRF-38534.

HEWLETT® PACKARD

Dual Channel Line Receiver Hermetic Optocoupler

Technical Data

HCPL-193X*
5962-8957201
*See matrix for available extensions

Features

- **Dual Marked with Device Part Number and DESC Standard Military Drawing**
- **Manufactured and Tested on a MIL-PRF-38534 Certified Line**
- **QML-38534, Class H and Class K**
- **Hermetically Sealed 16-pin Dual In-Line Package**
- **Performance Guaranteed Over -55°C to +125°C**
- **High Speed – 10 Mb/s**
- **Accepts a Broad Range of Drive Conditions**
- **Adaptive Line Termination Included**
- **Internal Shield Provides Excellent Common Mode Rejection**
- **External Base Lead Allows "LED Peaking" and LED Current Adjustment**
- **1500 Vdc Withstand Test Voltage**
- **High Radiation Immunity**
- **HCPL-2602 Function Compatibility**
- **Reliability Data Available**

Applications

- **Military and Space**
- **High Reliability Systems**
- **Isolated Line Receiver**
- **Simplex/Multiplex Data Transmission**
- **Computer-Peripheral Interface**
- **Microprocessor System Interface**
- **Harsh Environmental Environments**
- **Digital Isolation for A/D, D/A Conversion**
- **Current Sensing**
- **Instrument Input/Output Isolation**
- **Ground Loop Elimination**
- **Pulse Transformer Replacement**

Truth Table

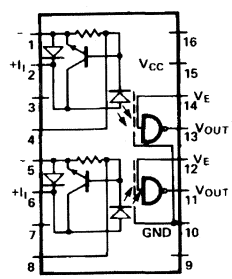
(POSITIVE LOGIC)

INPUT	ENABLE	OUTPUT
ON	H	L
OFF	H	H
ON	L	H
OFF	L	H

Description

The HCPL-1930, HCPL-1931, and 5962-8957201 units are dual channel, hermetically sealed, high CMR, line receiver optocouplers. The products are capable of operation and storage over the full military temperature range and can be purchased as either a standard product or with full MIL-PRF-38534 Class Level H or K testing, or from the DESC Standard Military Drawing (SMD) 5962-89572. This is a sixteen pin DIP which may be purchased with a variety of lead bend and plating options. See selection guide table for details. Standard Military Drawing (SMD) parts are available for each lead style.

Functional Diagram



CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

All devices are manufactured and tested on a MIL-PRF-38534 certified line and are included in the DESC Qualified Manufacturers List QML-38534 for Hybrid Microcircuits.

Each unit contains two independent channels, consisting of a GaAsP light emitting diode, an input current regulator, and an integrated high gain photon detector. The input regulator serves as a line termination for line receiver applications. It clamps the line voltage and regulates the LED current so line reflections do not interfere with circuit performance. The regulator allows a typical LED current of 12.5 mA before it starts to shunt excess current. The output of the detector IC is an open collector Schottky clamped transistor. An enable input gates the detector. The internal detector shield provides a guaranteed common mode transient immunity specification of +1000 V/μsec.

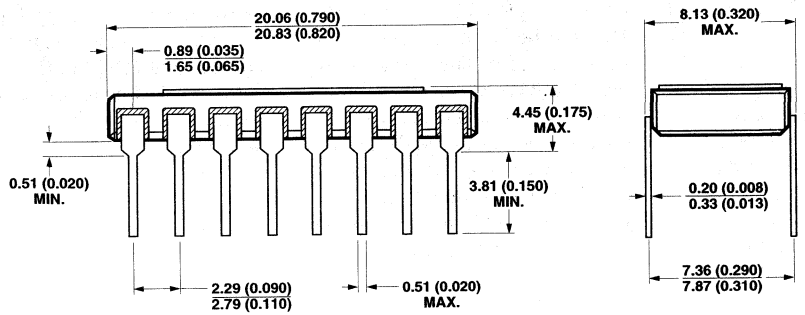
DC specifications are compatible with TTL logic and are guaranteed from -55°C to +125°C allowing trouble-free interfacing with digital logic circuits. An input current of 10 mA will sink a six gate fan-out (TTL) at the output with a typical propagation delay from input to output of only 45 nsec.

Selection Guide–Package Styles and Lead Configuration Options

HP Part # and Options	
Commercial	HCPL-1930
MIL-PRF-38534 Class H	HCPL-1931
MIL-PRF-38534 Class K	HCPL-193K
Standard Lead Finish	Gold
Solder Dipped	Option #200
Butt Joint/Gold Plate	Option #100
Gull Wing/Soldered	Option #300
Crew Cut/Gold Plate	Option #600
SMD Part #	
Prescript for all below	5962-
Either Gold or Soldered	8957201EX
Gold Plate	8957201EC
Solder Dipped	8957201EA
Butt Joint/Gold Plate	8957201YC
Butt Joint/Soldered	8957201YA
Gull Wing/Soldered	8957201XA
Crew Cut/Gold Plate	Available
Crew Cut/Soldered	Available

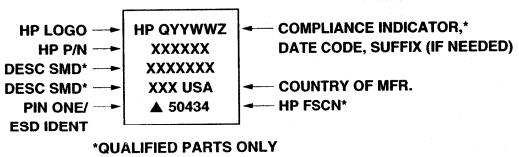
Outline Drawings

16 Pin DIP Through Hole, 2 Channels



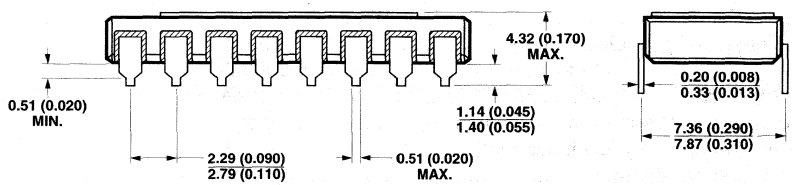
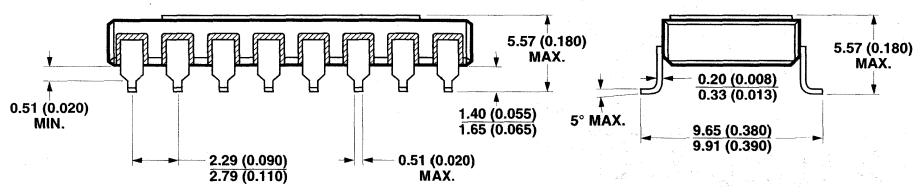
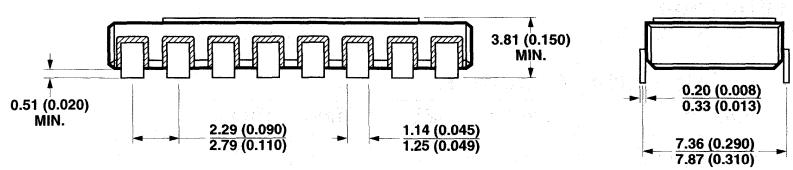
NOTE: DIMENSIONS IN MILLIMETERS (INCHES).

Device Marking



*QUALIFIED PARTS ONLY

Hermetic Optocoupler Options

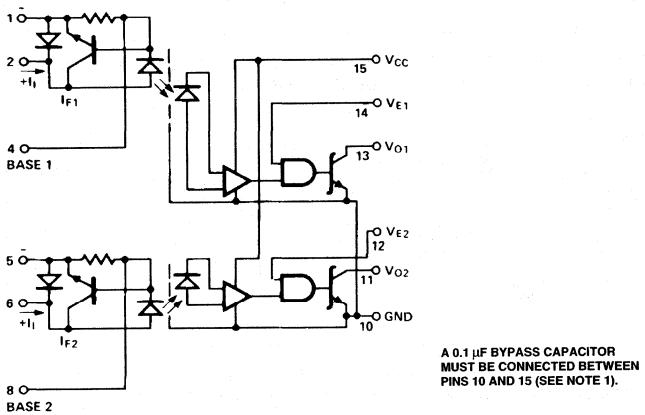
Option	Description
100	Surface mountable hermetic optocoupler with leads trimmed for butt joint assembly. This option is available on commercial and hi-rel product. 
200	Lead finish is solder dipped rather than gold plated. This option is available on commercial and hi-rel product. DESC Drawing part numbers contain provisions for lead finish.
300	Surface mountable hermetic optocoupler with leads cut and bent for gull wing assembly. This option is available on commercial and hi-rel product. This option has solder dipped leads. 
600	Surface mountable hermetic optocoupler with leads trimmed for butt joint assembly. This option is available on commercial and hi-rel product. Contact factory for the availability of this option on DESC part types. 

Note: Dimensions in millimeters (inches).

Absolute Maximum Ratings

Storage Temperature ..... -65°C to +150°C
Operating Temperature ..... -55°C to +125°C
Lead Solder Temperature ..... 260°C for 10 s
1.6 mm below seating plane
Forward Input Current – I_I (each channel) ..... 60 mA[2]
Reverse Input Current ..... 60 mA
Supply Voltage – V_{CC} ..... 7 V (1 Minute Maximum)
Enable Input Voltage – V_E (each channel) ..... 5.5 V
Not to exceed V_{CC} by more than 500 mV
Output Collector Current – I_O (each channel) ..... 25 mA
Output Collector Power Dissipation (each channel) ..... 40 mW
Output Collector Voltage – V_O (each channel) ..... 7 V
Total Package Power Dissipation ..... 564 mW
Input Power Dissipation (each channel) ..... 168 mW

Schematic



ESD Classification

(MIL-STD-883, Method 3015) ..... (Δ), Class 1

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Input Current, Low Level	I_{IL}	0	250	µA
Input Current, High Level*	I_{IH}	12.5	60	mA
Supply Voltage, Output	V_{CC}	4.5	5.5	V
High Level Enable Voltage	V_{EH}	2.0	V_{CC}	V
Low Level Enable Voltage	V_{EL}	0	0.8	V
Fan Out (@ R_L = 4 kΩ)	N		5	TTL Loads
Operating Temperature	T_A	-55	125	°C

*12.5 mA condition permits at least 20% guardband for optical coupling variation. Initial switching threshold is 10 mA or less.

Electrical Specifications T_A = -55°C to 125°C unless otherwise stated. See note 15.

Parameter	Symbol	Test Conditions	Group A Sub-groups	Limits			Units	Fig.	Note
				Min.	Typ.*	Max.			
High Level Output Current	I_{OH}	V_{CC} = 5.5 V, V_O = 5.5 V I_I = 250 µA, V_E = 2.0 V	1, 2, 3		20	250	µA	3	3
Low Level Output Voltage	V_{OL}	V_{CC} = 5.5 V; I_I = 10 mA V_E = 2.0 V, I_{OL} (Sinking) = 10 mA	1, 2, 3		0.3	0.6	V	1	3
Input Voltage	V_I	I_I = 10 mA	1, 2, 3		2.2	2.6	V	2	3
		I_I = 60 mA			2.35	2.75			
Input Reverse Voltage	V_R	I_R = 10 mA	1, 2, 3		0.8	1.10	V		3
Low Level Enable Current	I_{EL}	V_{CC} = 5.5 V, V_E = 0.5 V	1, 2, 3		-1.45	-2.0	mA		3
High Level Enable Voltage	V_{EH}		1, 2, 3	2.0			V		3, 12
Low Level Enable Voltage	V_{EL}		1, 2, 3			0.8	V		3
High Level Supply Current	I_{CCH}	V_{CC} = 5.5 V; I_I = 0, V_E = 0.5 V both channels	1, 2, 3		21	28	mA		
Low Level Supply Current	I_{CCL}	V_{CC} = 5.5 V; I_I = 60 mA, V_E = 0.5 V both channels	1, 2, 3		27	36	mA		
Input-Output Insulation Leakage Current	I_{I-O}	Relative Humidity = 45% t = 5 s, V_{I-O} = 1500 Vdc	1			1	µA		4
Propagation Delay Time to High Output Level	t_{PLH}	R_L = 510 Ω; C_L = 50 pF, I_I = 13 mA,V_{CC} = 5.0 V	9		55	100	ns	4, 5	3, 5
			10, 11			140			
Propagation Delay Time to Low Output Level	t_{PHL}	R_L = 510 Ω; C_L = 50 pF, I_I = 13 mA, V_{CC} = 5.0 V	9		60	100	ns	4, 5	3, 6
			10, 11			120			
Common Mode Transient Immunity at High Output Level	$\|CM_H\|$	V_{CM} = 50 V (peak), V_O (min.) = 2 V, R_L = 510 Ω; I_I = 0 mA, V_{CC} = 5.0 V	9, 10, 11	1000	10,000		V/µs	8, 9	3, 9, 14
Common Mode Transient Immunity at Low Output Level	$\|CM_L\|$	V_{CM} = 50 V (peak), V_O (max.) = 0.8 V, R_L = 510 Ω; I_I = 10 mA, V_{CC} = 5.0 V	9, 10, 11	1000	10,000		V/µs	8, 9	3, 10, 14

*All typical values are at V_{CC} = 5 V, T_A = 25°C.

Typical Specifications

T_A = 25°C, V_{CC} = 5 V

Parameter	Symbol	Typ.	Units	Test Conditions	Fig.	Note
Resistance (Input-Output)	R_{I-O}	10^{12}	Ω	V_{I-O} = 500 V dc		3, 13
Capacitance (Input-Output)	C_{I-O}	1.7	pF	f = 1 MHz		3, 13
Input-Input Insulation Leakage Current	I_{I-I}	0.5	nA	45% Relative Humidity, V_{I-I} = 500 Vdc, t = 5 s		11
Resistance (Input-Input)	R_{I-I}	10^{12}	Ω	V_{I-I} = 500 Vdc		11
Capacitance (Input-Input)	C_{I-I}	0.55	pF	f = 1 MHz		11
Propagation Delay Time of Enable from V_{EH} to V_{EL}	t_{ELH}	35	ns	R_L = 510 Ω, C_L = 15 pF, I_I = 13 mA, V_{EH} = 3 V, V_{EL} = 0 V	6, 7	3, 7
Propagation Delay Time of Enable from V_{EL} to V_{EH}	t_{EHL}	35	ns		6, 7	3, 8
Output Rise Time (10-90%)	t_r	30	ns	R_L = 510 Ω, C_L = 15 pF, I_I = 13 mA		3
Output Fall Time (90-10%)	t_f	24	ns			3
Input Capacitance	C_I	60	pF	f = 1 MHz, V_I = 0, PINS 1 to 2 or 5 to 6		3

Notes:

1. Bypassing of the power supply line is required, with a 0.1 µF ceramic disc capacitor adjacent to each isolator. The power supply bus for the isolators should be separate from the bus for any active loads, otherwise additional bypass capacitance may be needed to suppress regenerative feedback via the power supply.
2. Derate linearly at 1.2 mA/°C above T_A = 100°C.
3. Each channel.
4. Device considered a two terminal device: pins 1 through 8 are shorted together, and pins 9 through 16 are shorted together.
5. The t_{PLH} propagation delay is measured form the 6.5 mA point on the trailing edge of the input pulse to the 1.5 V point on the trailing edge of the output pulse.
6. The t_{PHL} propagation delay is measured from the 6.5 mA point on the leading edge of the input pulse to the 1.5 V point on the leading edge of the output pulse.
7. The t_{ELH} enable propagation delay is measured from the 1.5 V point on the trailing edge of the enable input pulse to the 1.5 V point on the trailing edge of the output pulse.
8. The t_{EHL} enable propagation delay is measured from the 1.5 V point on the leading edge of the enable input pulse to the 1.5 V point on the leading edge of the output pulse.
9. CM_H is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state, i.e. V_{OUT} > 2.0 V.
10. CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state, i.e. V_{OUT} < 0.8 V.
11. Measured between adjacent input leads shorted together, i.e. between 1, 2 and 4 shorted together and pins 5, 6 and 8 shorted together.
12. No external pull up is required for a high logic state on the enable input.
13. Measured between pins 1 and 2 or 5 and 6 shorted together, and pins 10 through 15 shorted together.
14. Parameters shall be tested as part of device initial characterization and after process changes. Parameters shall be guaranteed to the limits specified for all lots not specifically tested.
15. Standard parts receive 100% testing at 25°C (Subgroups 1 and 9). SMD and Class H parts receive 100% testing at 25, 125, and -55°C (Subgroups 1 and 9, 2 and 10, 3 and 11, respectively).

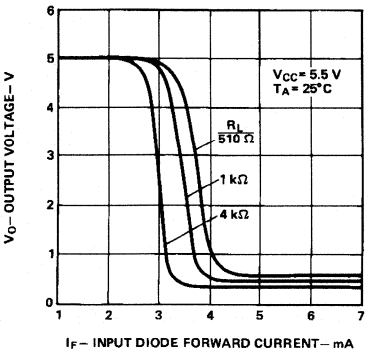


Figure 1. Input-Output Characteristics.

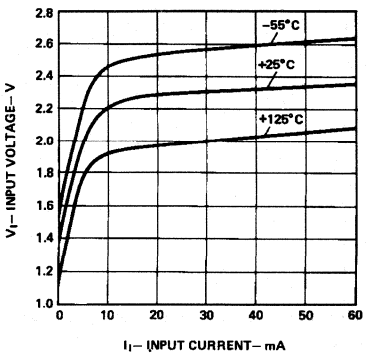


Figure 2. Input Characteristics.

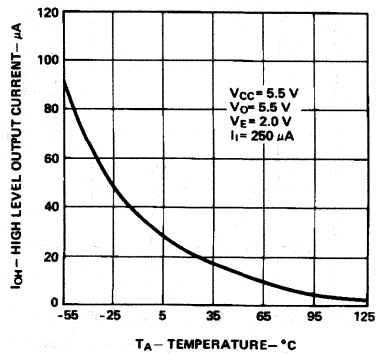


Figure 3. High Level Output Current vs. Temperature.

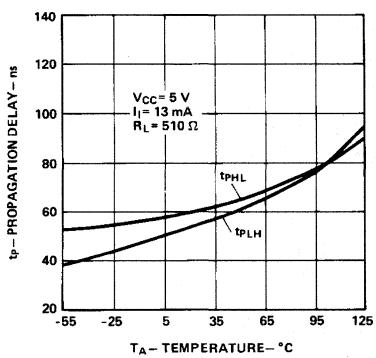


Figure 4. Propagation Delay vs. Temperature.

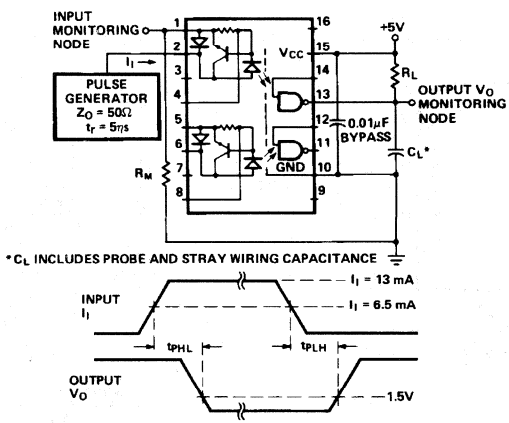


Figure 5. Test Circuit for t_{PHL} and t_{PLH}.

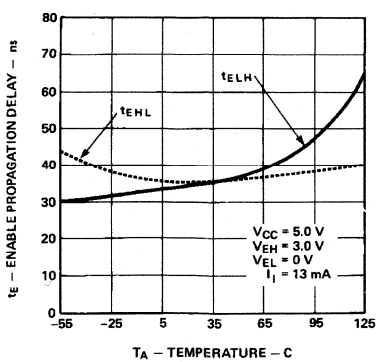


Figure 6. Enable Propagation Delay vs. Temperature.

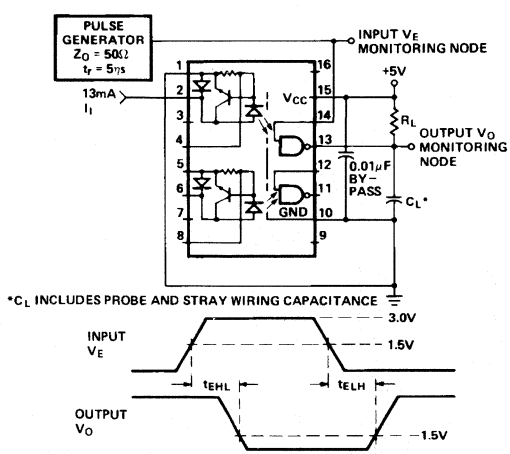


Figure 7. Test Circuit for t_{EHL} and t_{ELH}.

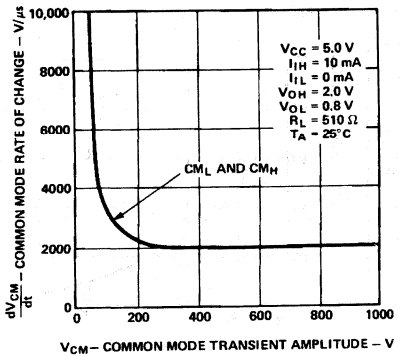


Figure 8. Typical Common Mode Transient Immunity.

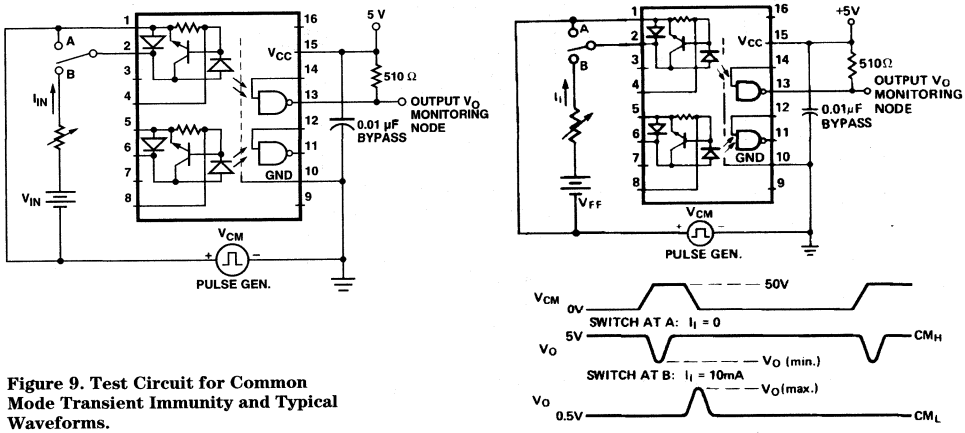


Figure 9. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

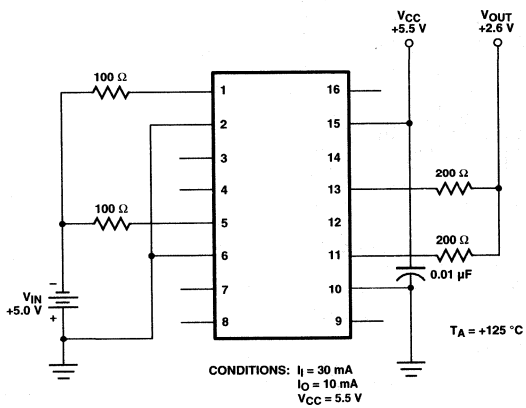
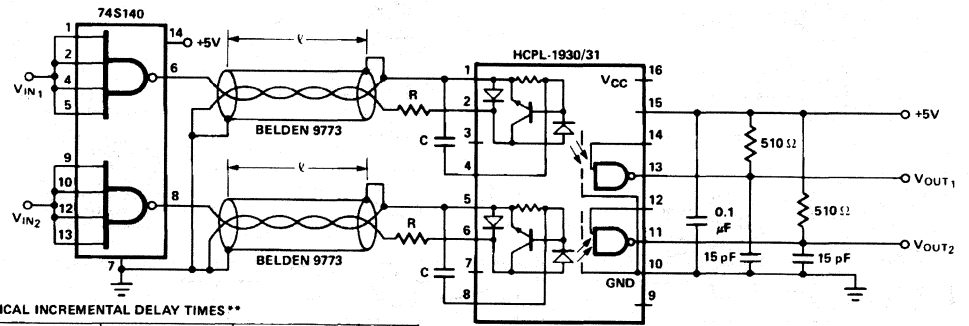


Figure 10. Burn In Circuit.

Application Circuits*

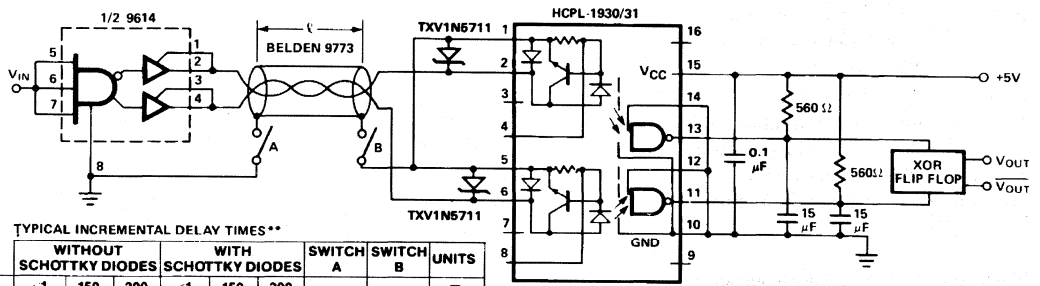


TYPICAL INCREMENTAL DELAY TIMES**

	R = 0, C = OPEN			R =33Ω, C = OPEN			R=33Ω, C = 390pF			UNITS
ℓ	<1	150	300	<1	150	300	<1	150	300	m
t_{PHL}	42	27	121	43	47	171	28	37	146	nsec
t_{PLH}	31	121	296	31	31	71	26	11	46	nsec

PROPAGATION DELAY TIMES SHOWN EXCLUDE DRIVER AND LINE DELAYS.

Figure A_1. Polarity Non-Reversing.



TYPICAL INCREMENTAL DELAY TIMES**

	WITHOUT SCHOTTKY DIODES			WITH SCHOTTKY DIODES			SWITCH A	SWITCH B	UNITS
ℓ	<1	150	300	<1	150	300	—	—	m
tp	112	455	820	78	365	700	OPEN	OPEN	nsec
	52	410	730	54	305	580	OPEN	CLOSED	nsec
	52	410	490	54	395	490	CLOSED	CLOSED	nsec

PROPAGATION DELAY TIMES SHOWN EXCLUDE DRIVER AND LINE DELAYS
USING 1/3 74LS04 INVERTERS AND 74LS00 QUAD NAND

Figure A_2. Polarity Reversing, Split Phase.

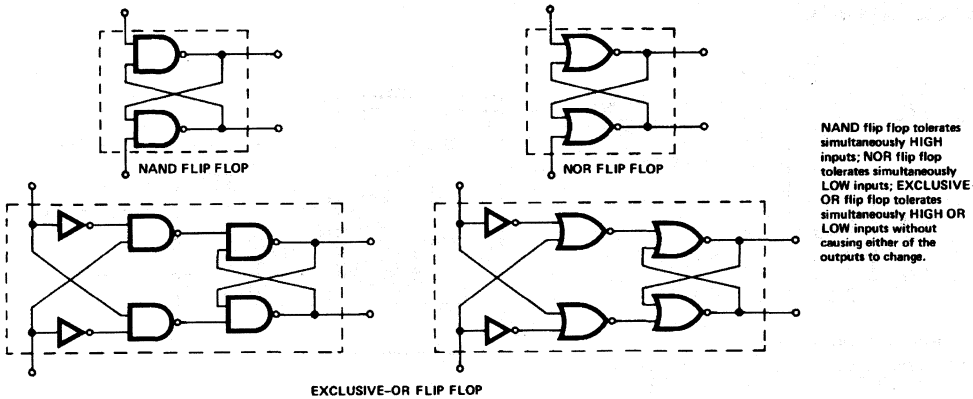


Figure A_3. Flop-Flop Configurations.

MIL-PRF-38534 Class H, Class K, and DESC SMD Test Program

Hewlett-Packard's Hi-Rel Optocouplers are in compliance with MIL-PRF-38534 Class H and K. Class H devices are also in compliance with DESC drawing 5962-89572.

Testing consists of 100% screening and quality conformance inspection to MIL-PRF-38534.

Hermetically Sealed, Transistor Output Optocouplers for Analog and Digital Applications

Technical Data

4N55*
5962-87679 HCPL-655X
HCPL-553X 5962-90854
HCPL-653X HCPL-550X

*See matrix for available extensions.

Features

- **Dual Marked with Device Part Number and DESC Drawing Number**
- **Manufactured and Tested on a MIL-PRF-38534 Certified Line**
- **QML-38534, Class H and K**
- **Five Hermetically Sealed Package Configurations**
- **Performance Guaranteed, Over -55°C to +125°C**
- **High Speed: Typically 400 kBit/s**
- **9 MHz Bandwidth**
- **Open Collector Output**
- **2-18 Volt V_{CC} Range**
- **1500 Vdc Withstand Test Voltage**
- **High Radiation Immunity**
- **6N135, 6N136, HCPL-2530/ -2531, Function Compatibility**
- **Reliability Data**

Applications

- **Military and Space**
- **High Reliability Systems**
- **Vehicle Command, Control, Life Critical Systems**
- **Line Receivers**
- **Switching Power Supply**
- **Voltage Level Shifting**
- **Analog Signal Ground Isolation (see Figures 7, 8, and 13)**
- **Isolated Input Line Receiver**
- **Isolated Output Line Driver**
- **Logic Ground Isolation**
- **Harsh Industrial Environments**
- **Isolation for Test Equipment Systems**

Description

These units are single, dual and quad channel, hermetically sealed optocouplers. The products are capable of operation and storage over the full military temperature range and can be purchased as either standard product or with full MIL-PRF-38534 Class Level H or K testing or from the appropriate DESC Drawing. All devices are manufactured and tested on a MIL-PRF-38534 certified line and are included in the DESC Qualified Manufacturers List QML-38534 for Hybrid Microcircuits.

Each channel contains a GaAsP light emitting diode which is optically coupled to an integrated photon detector. Separate connections for the photodiodes and output transistor collectors improve the speed up to a hundred times that of a conventional phototransistor optocoupler by reducing the base-collector capacitance.

These devices are suitable for wide bandwidth analog applications, as well as for interfacing TTL to LSTTL or CMOS. Current Transfer Ratio (CTR) is 9% minimum at I_F = 16 mA. The 18 V V_{CC}

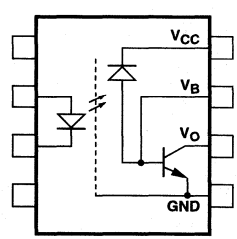
Truth Table

(Positive Logic)

Input	Output
On (H)	L
Off (L)	H

Functional Diagram

Multiple Channel Devices Available



CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

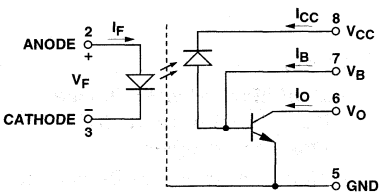
capability will enable the designer to interface any TTL family to CMOS. The availability of the base lead allows optimized gain/bandwidth adjustment in analog applications. The shallow depth of the IC photodiode provides better radiation immunity than conventional phototransistor couplers.

These products are also available with the transistor base node connected to improve common mode noise immunity and ESD susceptibility. In addition, higher CTR minimums are available by special request.

Package styles for these parts are 8 and 16 pin DIP through hole (case outlines P and E respectively), 16 pin DIP flat pack (case outline F), and leadless ceramic chip carrier (case outline 2). Devices may be purchased with a variety of lead bend and plating options, see Selection Guide Table for details. Standard Military Drawing (SMD) parts are available for each package and lead style.

Because the same functional die (emitters and detectors) are used for each channel of each device listed in this data sheet, absolute maximum ratings, recommended operating conditions, electrical specifications, and performance characteristics shown in the figures are identical for all parts. Occasional exceptions exist due to package variations and limitations and are as noted. Additionally, the same package assembly processes and materials are used in all devices. These similarities give justification for the use of data obtained from one part to represent other part's performance for die related reliability and certain limited radiation test results.

8 Pin Ceramic DIP Single Channel Schematic



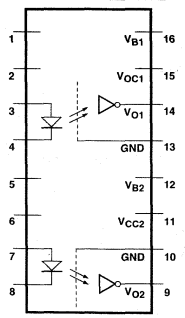
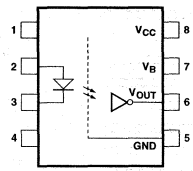
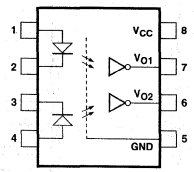
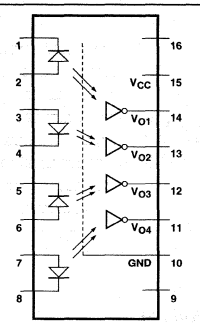
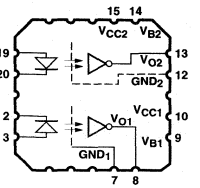
Note base pin 7.

Selection Guide–Package Styles and Lead Configuration Options

Package	16 Pin DIP	8 Pin DIP	8 Pin DIP	16 Pin Flat Pack	20 Pad LCCC
Lead Style	Through Hole	Through Hole	Through Hole	Unformed Leads	Surface Mount
Channels	2	1	2	4	2
Common Channel Wiring	None	None	V_{CC} GND	V_{CC} GND	None
HP Part # & Options					
Commercial	4N55*	HCPL-5500	HCPL-5530	HCPL-6550	HCPL-6530
MIL-PRF-38534, Class H	4N55/883B	HCPL-5501	HCPL-5531	HCPL-6551	HCPL-6531
MIL-PRF-38534, Class K	HCPL-257K	HCPL-550K	HCPL-553K	HCPL-655K	HCPL-653K
Standard Lead Finish	Gold Plate	Gold Plate	Gold Plate	Gold Plate	Solder Pads
Solder Dipped	Option #200	Option #200	Option #200		
Butt Cut/Gold Plate	Option #100	Option #100	Option #100		
Gull Wing/Soldered	Option #300	Option #300	Option #300		
SMD Part #					
Prescript for all below	5962-	5962-	5962-	5962-	5962-
Either Gold or Solder	8767901EX	9085401HPX	8767902PX	8767904FX	87679032X
Gold Plate	8767901EC	9085401HPC	8767902PC	8767904FC	
Solder Dipped	8767901EA	9085401HPA	8767902PA		87679032A
Butt Cut/Gold Plate	8767901UC	9085401HYC	8767902YC		
Butt Cut/Soldered	8767901UA	9085401HYA	8767902YA		
Gull Wing/Soldered	8767901TA	9085401HXA	8767902XA		

*JEDEC registered part.

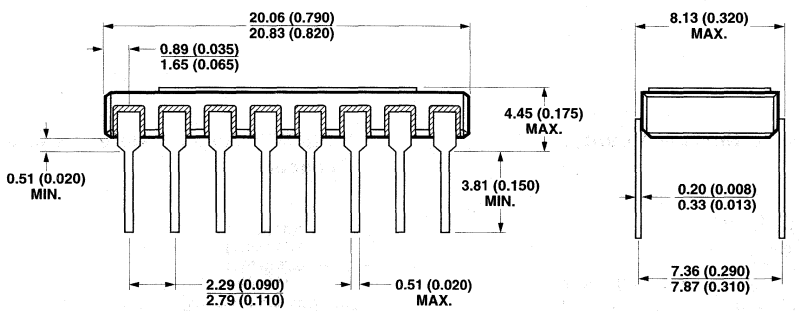
Functional Diagrams

16 Pin DIP	8 Pin DIP	8 Pin DIP	16 Pin Flat Pack	20 Pad LCCC
Through Hole	Through Hole	Through Hole	Unformed Leads	Surface Mount
2 Channels	1 Channel	2 Channels	4 Channels	2 Channels
				

Note: 8 pin DIP and flat pack devices have common V_{CC} and ground. 16 pin DIP and LCCC (leadless ceramic chip carrier) packages have isolated channels with separate V_{CC} and ground connections.

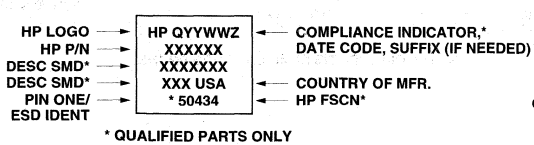
Outline Drawings

16 Pin DIP Through Hole, 2 Channels



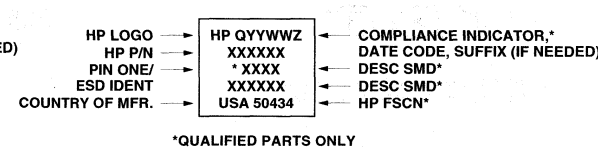
NOTE: DIMENSIONS IN MILLIMETERS (INCHES).

Leaded Device Marking



* QUALIFIED PARTS ONLY

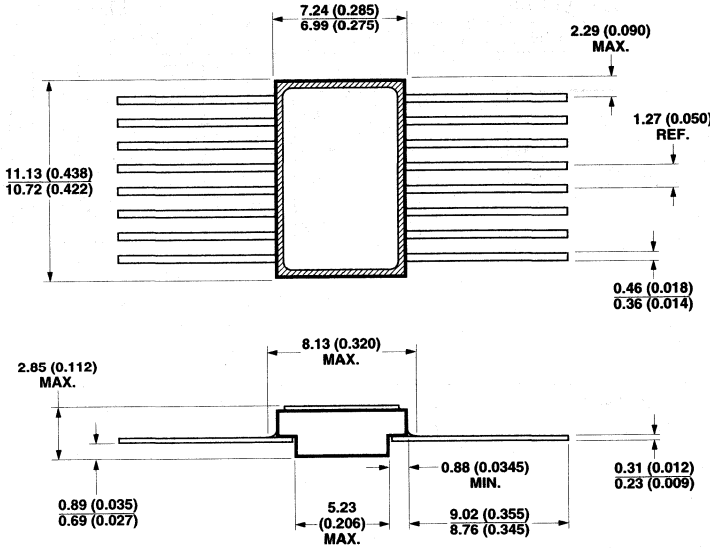
Leadless Device Marking



*QUALIFIED PARTS ONLY

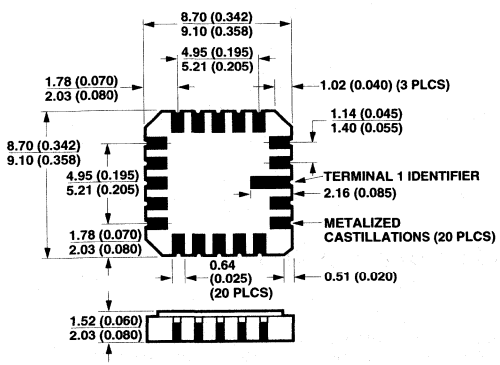
Outline Drawings (contd.)

16 Pin Flat Pack, 4 Channels



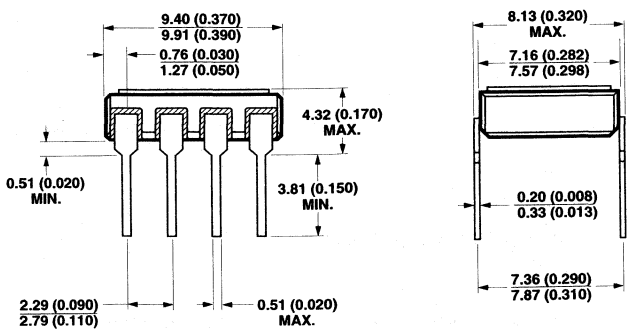
NOTE: DIMENSIONS IN MILLIMETERS (INCHES).

20 Terminal LCCC Surface Mount, 2 Channels



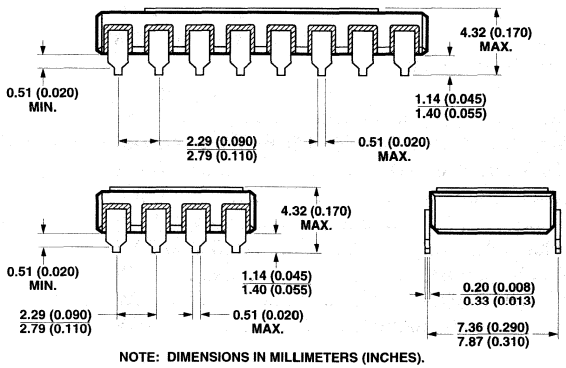
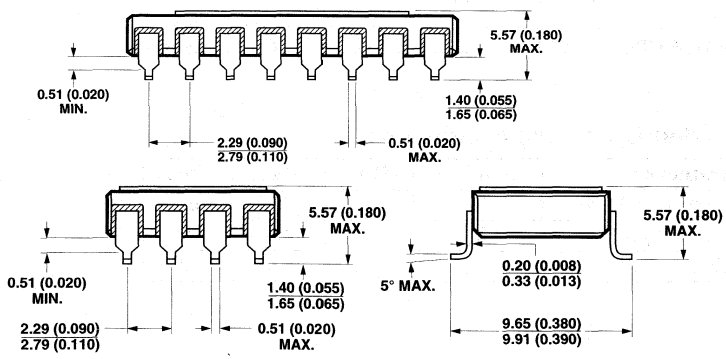
NOTE: DIMENSIONS IN MILLIMETERS (INCHES).
SOLDER THICKNESS 0.127 (0.005) MAX.

8 Pin DIP Through Hole, 1 and 2 Channel



NOTE: DIMENSIONS IN MILLIMETERS (INCHES).

Hermetic Optocoupler Options

Option	Description
100	Surface mountable hermetic optocoupler with leads trimmed for butt joint assembly. This option is available on commercial and hi-rel product in 8 and 16 pin DIP (see drawings below for details).  NOTE: DIMENSIONS IN MILLIMETERS (INCHES).
200	Lead finish is solder dipped rather than gold plated. This option is available on commercial and hi-rel product in 8 and 16 pin DIP. DESC drawing part numbers contain provisions for lead finish. All leadless chip carrier devices are delivered with solder dipped terminals as a standard feature.
300	Surface mountable hermetic optocoupler with leads cut and bent for gull wing assembly. This option is available on commercial and hi-rel product in 8 and 16 pin DIP (see drawings below for details). This option has solder dipped leads.  NOTE: DIMENSIONS IN MILLIMETERS (INCHES).

Absolute Maximum Ratings

(No derating required up to +125°C)
Storage Temperature Range, T_S ..... -65°C to +150°C
Operating Temperature, T_A ..... -55°C to +125°C
Case Temperature, T_C ..... +170°C
Junction Temperature, T_J ..... +175°C
Lead Solder Temperature ..... 260°C for 10 s
Peak Forward Input Current, (each channel,
≤ 1 ms duration), $I_{F\,PK}$ ..... 40 mA
Average Input Forward Current, $I_{F\,AVG}$ (each channel) ..... 20 mA
Reverse Input Voltage, BV_R ..... See Electrical Characteristics
Average Output Current, I_O (each channel) ..... 8 mA
Peak Output Current, I_O (each channel) ..... 16 mA
Supply Voltage, V_{CC} ..... -0.5 V to 20 V
Output Voltage, V_O (each channel) ..... -0.5 V to 20 V
Input Power Dissipation (each channel) ..... 36 mW
Output Power Dissipation (each channel) ..... 50 mW
Package Power Dissipation, P_D (each channel) ..... 200 mW

Single Channel 8 Pin, Dual Channel 16 Pin, and LCCC Only

Emitter Base Reverse Voltage, V_{EBO} ..... 3.0 V
Base Current, I_B (each channel) ..... 5 mA

ESD Classification

(MIL-STD-883, Method 3015)
4N55, 4N55/883B, HCPL-5500/01, and
HCPL-6530/31 ..... (Δ), Class 1
HCPL-5530/31, HCPL-6550/51 ..... (Dot), Class 3

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Input Current, Low Level	I_{FL}		250	μA
Input Current, High Level	I_{FH}	12	20	mA
Supply Voltage, Output	V_{CC}	2	18	V

Electrical Characteristics (T_A = -55°C to +125°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Group A[12] Sub-groups	Limits Min.	Limits Typ.**	Limits Max.	Units	Fig.	Note
Current Transfer Ration	CTR*	V_O = 0.4 V, I_F = 16 mA, V_{CC} = 4.5 V	1, 2, 3	9	20		%	2, 3	1, 2, 10
Logic High Output Current	I_{OH}	I_F = 0, $I_{F\ (other\ channels)}$ = 20 mA, V_O = V_{CC} = 18 V	1, 2, 3		5	100	µA	4	1
Output Leakage Current	I_{OLeak}*	I_F = 250 µA, $I_{F\ (other\ channels)}$ = 20 mA, V_O = V_{CC} = 18 V	1, 2, 3		30	250	µA	4	1
Input-Output Insulation Leakage Current	I_{I-O}*	V_{I-O} = 1500 Vdc, RH = 45% T_A = 25°C, t = 5 s	1			1.0	µA		3, 9
Input Forward Voltage	V_F*	I_F = 20 mA	1, 2, 3		1.55	1.8	V	1	1, 14
						1.9			1, 13
Reverse Breakdown Voltage	BV_R*	I_R = 10 µA	1, 2, 3	5			V		1, 14
				3					1, 13
Logic High Supply Current — Single Channel	I_{CCH}*	V_{CC} = 18 V, I_F = 0 mA	1, 2, 3		0.1	10	µA		1
Logic High Supply Current — Dual Channel		V_{CC} = 18 V, I_F = 0 mA (all channels)			0.2	20			1, 4
Logic High Supply Current — Quad Channel		V_{CC} = 18 V, I_F = 0 mA (all channels)			0.4	40			1
Logic Low Supply Current — Single Channel	I_{CCL}*	V_{CC} = 18 V, I_F = 20 mA	1, 2, 3		35	200	µA	5	1
Logic Low Supply Current — Dual Channel		V_{CC} = 18 V, I_{F1} = I_{F2} = 20 mA			70	400			1, 4
Logic Low Supply Current — Quad Channel		V_{CC} = 18 V, I_{F1} = I_{F2} = I_{F3} = I_{F4} = 20 mA			140	800			1
Propagation Delay Time to Logic High at Output	t_{PLH}*	R_L = 8.2 kΩ, C_L = 50 pF, I_F = 16 mA, V_{CC} = 5 V	9, 10, 11		1.0	6.0	µs	6, 9	1, 6
Propagation Delay Time to Logic Low at Output	t_{PHL}*				0.4	2.0			

*For JEDEC registered parts.
**All typical values are at V_{CC} = 5 V, T_A = 25°C.

Typical Characteristics, T_A = 25°C, V_{CC} = 5 V

Parameter	Symbol	Typ.	Units	Test Conditions	Fig.	Note
Input Capacitance	C_{IN}	60	pF	V_F = 0 V, f = 1 MHz		1
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$	-1.5	mV/°C	I_F = 20 mA		1
Resistance (Input-Output)	R_{I-O}	10^{12}	Ω	V_{I-O} 500 V		3
Capacitance (Input-Output)	C_{I-O}	1.0	pF	f = 1 MHz		1, 11
Transistor DC Current Gain	h_{FE}	250	-	V_O = 5 V, I_O = 3 mA		1
Small Signal Current Transfer Ratio	$\frac{\Delta I_O}{\Delta I_F}$	21	%	V_{CC} = 5 V, V_O = 2 V	7	1
Common Mode Transient Immunity at Logic High Level Output	$\|CM_H\|$	1000	V/µs	I_F = 0 mA, R_L = 8.2 kΩ, V_O (min) = 2.0 V V_{CM} = 10 V_{P-P}	10	1, 7
Common Mode Transient Immunity at Logic Low Level Output	$\|CM_L\|$	-1000	V/µs	I_F = 16 mA, R_L = 8.2 kΩ, V_O (max) = 0.8 V V_{CM} = 10 V_{P-P}	10	1, 7
Bandwidth	BW	9	MHz		8	8

Multi-Channel Product Only

Input-Input Insulation Leakage Current	I_{I-I}	1	pA	Relative Humidity = 45% V_{I-I} = 500 V, t = 5 s		5, 9
Resistance (Input-Input)	R_{I-I}	10^{12}	Ω	V_{I-I} = 500 V		5
Capacitance (Input-Input)	C_{I-I}	0.8	pF	f = 1 MHz		5

Notes:

1. Each channel of a multi-channel device.
2. Current Transfer Ratio is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%. CTR is known to degrade slightly over the unit's lifetime as a function of input current, temperature, signal duty cycle, and system on time. Refer to Application Note 1002 for more detail. In short, it is recommended that designers allow at least 20-25% guardband for CTR degradation.
3. All devices are considered two-terminal devices; measured between all input leads or terminals shorted together and all output leads or terminals shorted together.
4. The 4N55, 4N55/883B, HCPL-6530 and HCPL-6531 dual channel parts function as two independent single channel units. Use the single channel parameter limits. I_F = 0 mA for channel under test and I_F = 20 mA for other channels.
5. Measured between adjacent input pairs shorted together for each multichannel device.
6. t_{PHL} propagation delay is measured from the 50% point on the leading edge of the input pulse to the 1.5 V point on the leading edge of the output pulse. The t_{PLH} propagation delay is measured from the 50% point on the trailing edge of the input pulse to the 1.5 V point on the trailing edge of the output pulse.
7. CM_L is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic low state (V_O < 0.8 V). CM_H is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic high state (V_O > 2.0 V).
8. Bandwidth is the frequency at which the ac output voltage is 3 dB below the low frequency asymptote. For the HCPL-5530 the typical bandwidth is 2 MHz.
9. This is a momentary withstand test, not an operating condition.
10. Higher CTR minimums are available to support special applications.
11. Measured between each input pair shorted together and all output connections for that channel shorted together.
12. Standard parts receive 100% testing at 25°C (Subgroups 1 and 9). SMD and 883B parts receive 100% testing at 25, 125, and -55°C (Subgroups 1 and 9, 2 and 10, 3 and 11, respectively).
13. Not required for 4N55, 4N55/883B and 5962-8767901 types.
14. Required for 4N55, 4N55/883B and 5962-8767901 types only.

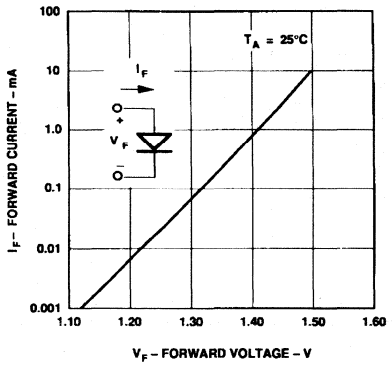


Figure 1. Input Diode Forward Current vs. Forward Voltage.

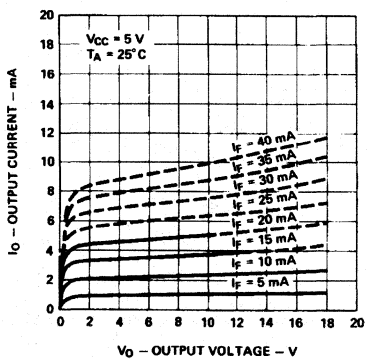


Figure 2. DC and Pulsed Transfer Characteristic.

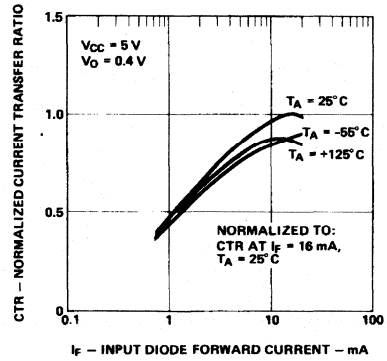


Figure 3. Normalized Current Transfer Ratio vs. Input Diode Forward Current.

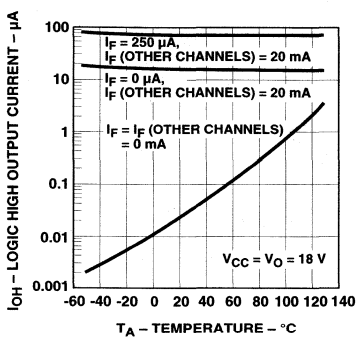


Figure 4. Logic High Output Current vs. Temperature.

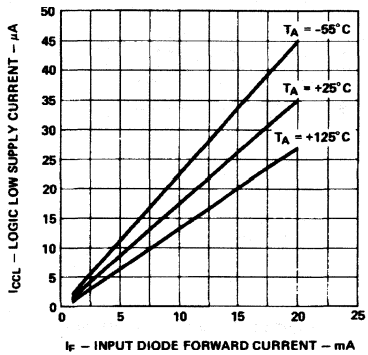


Figure 5. Logic Low Supply Current vs. Input Diode Forward Current.

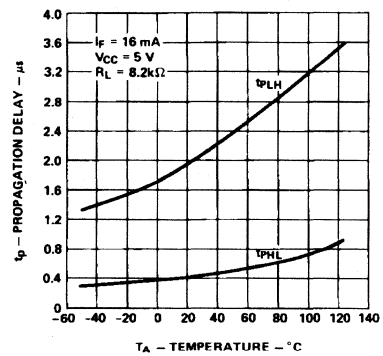


Figure 6. Propagation Delay vs. Temperature.

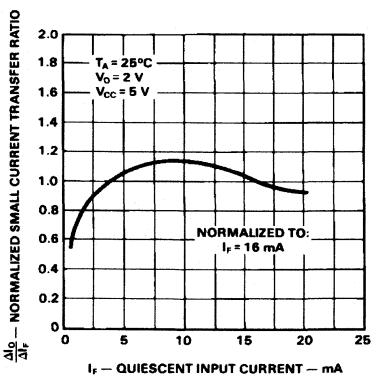
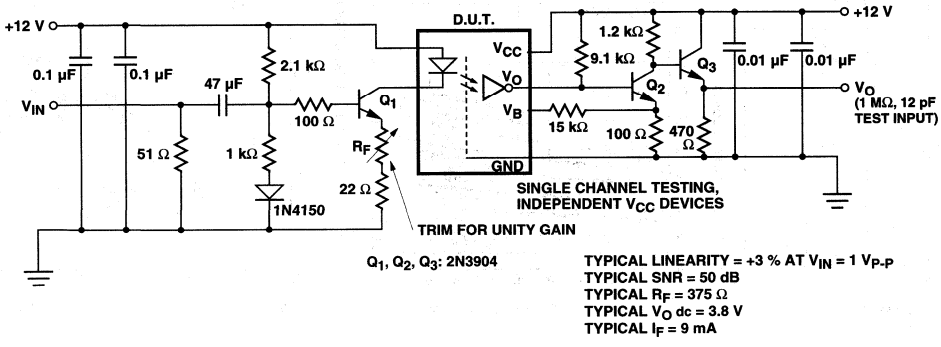
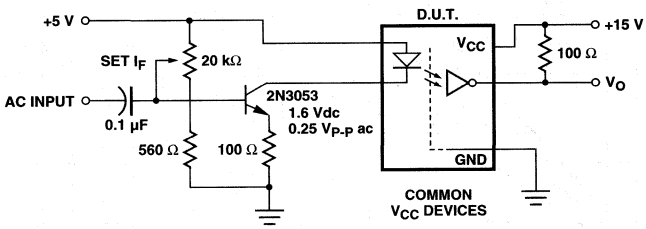


Figure 7. Normalized Small Signal Current Transfer Ratio vs. Quiescent Input Current.





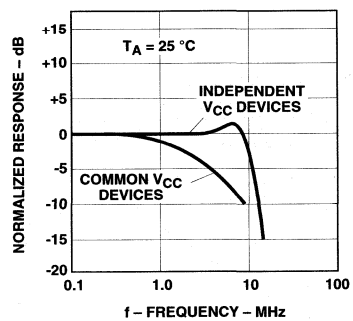
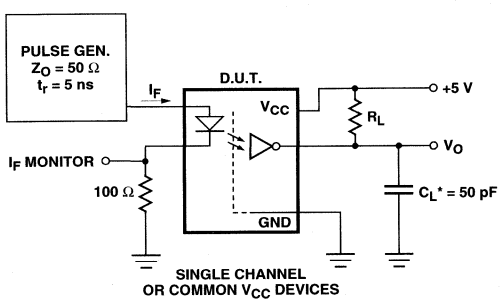
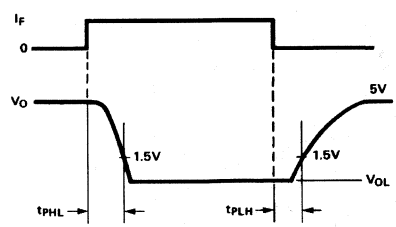


Figure 8. Frequency Response.





10 % DUTY CYCLE
1/f < 100 µs

NOTES:
* C_L INCLUDES PROBE AND STRAY WIRING CAPACITANCE.
BASE LEAD NOT CONNECTED.

Figure 9. Switching Test Circuit.*

*JEDEC Registered Data.

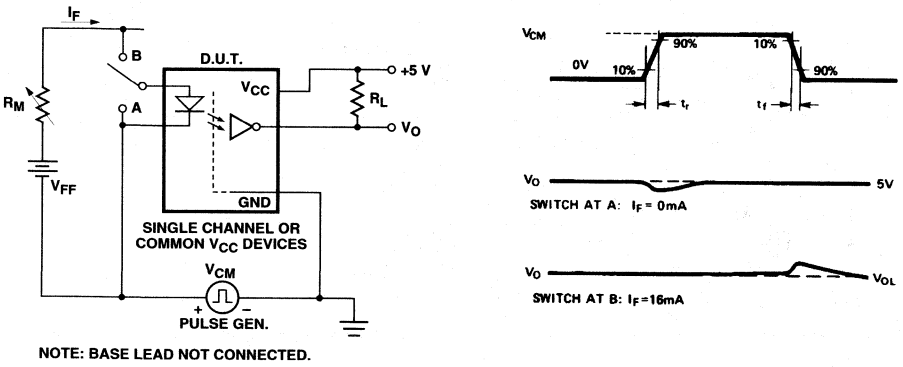
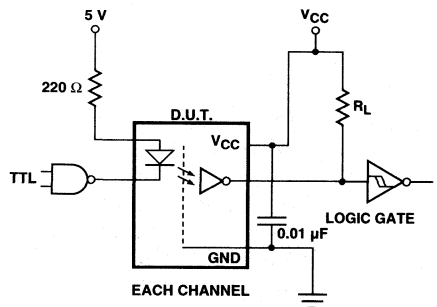


Figure 10. Test Circuit for Transient Immunity and Typical Waveforms.



Logic Family	LSTTL	CMOS	
Device No.	54LS14	CD40106BM	
V_{CC}	5 V	5 V	15 V
R_L 5% Tolerance	18 kΩ*	8.2 kΩ	22 kΩ

*The equivalent output load resistance is affected by the LSTTL input current and is approximately 8.2 kΩ.

This is a worst case design which takes into account 25% degradation of CTR. See App. Note 1002 to assess actual degradation and lifetime.

Figure 11. Recommended Logic Interface.

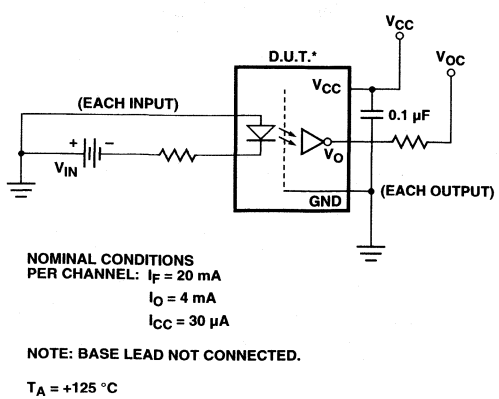


Figure 12. Operating Circuit for Burn-In and Steady State Life Tests. All Channels Tested Simultaneously.

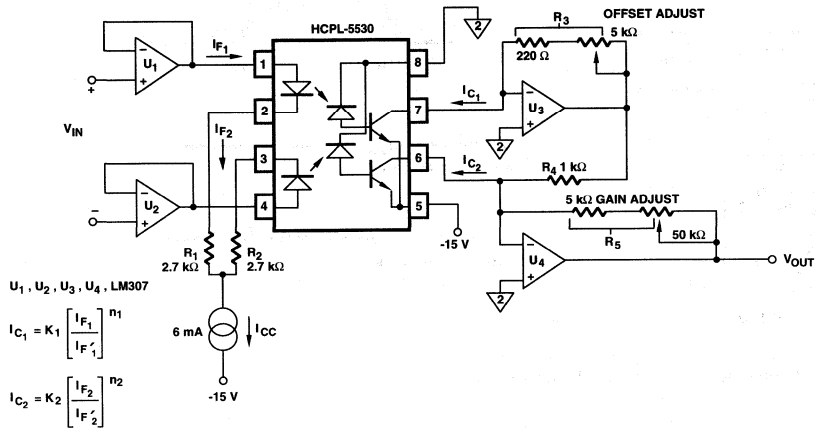


Figure 13. Isolation Amplifier Application Circuit.

Description

The schematic uses a dual-channel, high-speed optocoupler (HCPL-5530) to function as a servo type dc isolation amplifier. This circuit operates on the principle that two optocouplers will track each other if their gain changes by the same amount over a specific operating region.

Performance of Circuit

- 1% linearity for 10 V peak-to-peak dynamic range
- Gain drift: -0.03%/°C
- Offset Drift: ± 1 mV/°C
- 25 kHz bandwidth (limited by Op-Amps U1, U2)

MIL-PRF-38534 Class H, Class K, and DESC SMD Test Program

Hewlett-Packard's Hi-Rel Optocouplers are in compliance with MIL-PRF-38534 Classes H and K. Class H devices are also in compliance with DESC drawings 5962-87679, and 5962-90854.

Testing consists of 100% screening and quality conformance inspection to MIL-PRF-38534.

Hermetically Sealed, Low I_F, Wide V_{CC}, High Gain Optocouplers

Technical Data

6N140A* **5962-89810**
HCPL-675X **HCPL-573X**
83024 **HCPL-673X**
HCPL-570X **5962-89785**

*See matrix for available extensions.

Features

- **Dual Marked with Device Part Number and DESC Drawing Number**
- **Manufactured and Tested on a MIL-PRF-38534 Certified Line**
- **QML-38534, Class H and K**
- **Five Hermetically Sealed Package Configurations**
- **Performance Guaranteed, Over -55°C to +125°C**
- **Low Input Current Requirement: 0.5 mA**
- **High Current Transfer Ratio: 1500% Typical @ I_F = 0.5 mA**
- **Low Output Saturation Voltage: 0.11 V Typical**
- **1500 Vdc Withstand Test Voltage**
- **High Radiation Immunity**
- **6N138/9, HCPL-2730/31 Function Compatibility**
- **Reliability Data**

Applications

- **Military and Space**
- **High Reliability Systems**
- **Telephone Ring Detection**
- **Microprocessor System Interface**
- **Transportation, Medical, and Life Critical Systems**
- **Isolated Input Line Receiver**
- **EIA RS-232-C Line Receiver**
- **Voltage Level Shifting**
- **Isolated Input Line Receiver**
- **Isolated Output Line Driver**
- **Logic Ground Isolation**
- **Harsh Industrial Environments**
- **Current Loop Receiver**
- **System Test Equipment Isolation**
- **Process Control Input/Output Isolation**

Description

These units are single, dual, and quad channel, hermetically sealed optocouplers. The products are capable of operation and storage over the full military temperature range and can be purchased as either standard product or with full MIL-PRF-38534 Class Level H or K testing or from the appropriate DESC Drawing. All devices are manufactured and tested on a MIL-PRF-38534 certified line and are included in the DESC Qualified Manufacturers List QML-38534 for Hybrid Microcircuits.

Each channel contains a GaAsP light emitting diode which is optically coupled to an integrated high gain photon detector. The high gain output stage features an open collector output providing both lower saturation voltage and higher signaling speed than possible with conventional photo-Darlington optocouplers. The shallow depth and small junctions offered by the IC process provides better radiation immunity than conventional photo transistor optocouplers.

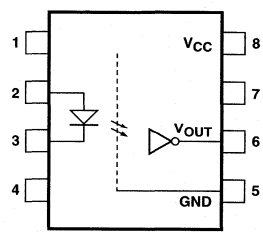
Truth Table

(Positive Logic)

Input	Output
On (H)	L
Off (L)	H

Functional Diagram

Multiple Channel Devices Available



CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

The supply voltage can be operated as low as 2.0 V without adversely affecting the parametric performance.

These devices have a 300% minimum CTR at an input current of only 0.5 mA making them ideal for use in low input current applications such as MOS, CMOS, low power logic interfaces or line receivers. Compatibility with high voltage CMOS logic systems is assured by specifying I_{CCH} and I_{OH} at 18 Volts.

Upon special request, the following device selections can be made: CTR minimum of up to 600% at 0.5 mA, lower drive currents to 0.1 mA, and lower output leakage current levels to 100 μA.

Package styles for these parts are 8 and 16 pin DIP through hole (case outlines P and E respectively), 16 pin DIP flat pack (case outline F), and leadless ceramic chip carrier (case outline 2). Devices may be purchased with a variety of lead bend and plating options. See Selection Guide table for details. Standard Military Drawing (SMD) parts are available for each package and lead style.

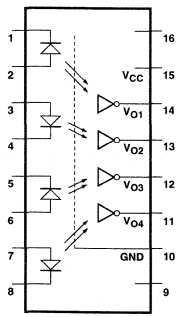
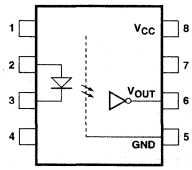
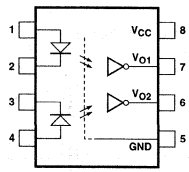
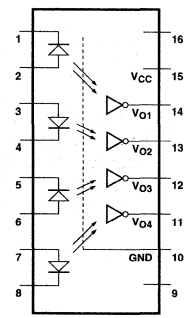
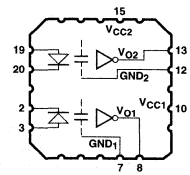
Because the same electrical die (emitters and detectors) are used for each channel of each device listed in this data sheet, absolute maximum ratings, recommended operating conditions, electrical specifications, and performance characteristics shown in the figures are similar for all parts except as noted. Additionally, the same package assembly processes and materials are used in all devices. These similarities justify the use of a common data base for die related reliability and certain limited radiation test results.

Selection Guide-Package Styles and Lead Configuration Options

Package	**16 pin DIP**	**8 pin DIP**	**8 pin DIP**	**16 pin Flat Pack**	**20 Pad LCCC**
Lead Style	Through Hole	Through Hole	Through Hole	Unformed Leads	Surface Mount
Channels	4	1	2	4	2
Common Channel Wiring	V_{CC}, GND	None	V_{CC}, GND	V_{CC}, GND	None
HP Part # & Options					
Commercial	6N140A*	HCPL-5700	HCPL-5730	HCPL-6750	HCPL-6730
MIL-PRF-38534 Class H	6N140A/883B	HCPL-5701	HCPL-5731	HCPL-6751	HCPL-6731
MIL-PRF-38534 Class K	HCPL-177K	HCPL-570K	HCPL-573K	HCPL-675K	HCPL-673K
Standard Lead Finish	Gold Plate	Gold Plate	Gold Plate	Gold Plate	Solder Pads
Solder Dipped	Option #200	Option #200	Option #200		
Butt Cut/Gold Plate	Option #100	Option #100	Option #100		
Gull Wing/Soldered	Option #300	Option #300	Option #300		
Crew Cut/Gold Plate	Option #600	Option #600	Option #600		
SMD Part #					
Prescript for all below	None	5962-	5962-	None	5962-
Either Gold or Solder	8302401EX	8981001PX	8978501PX	8302401FX	89785022X
Gold Plate	8302401EC	8981001PC	8978501PC	8302401FC	
Solder Dipped	8302401EA	8981001PA	8978501PA		89785022A
Butt Cut/Gold Plate	8302401YC	8981001YC	8978501YC		
Butt Cut/Soldered	8302401YA	8981001YA	8978501YA		
Gull Wing/Soldered	8302401XA	8981001XA	8978501ZA		
Crew Cut/Gold Plate	8302401ZC	Available	Available		
Crew Cut/Soldered	8302401ZA	Available	Available		

*JEDEC registered part.

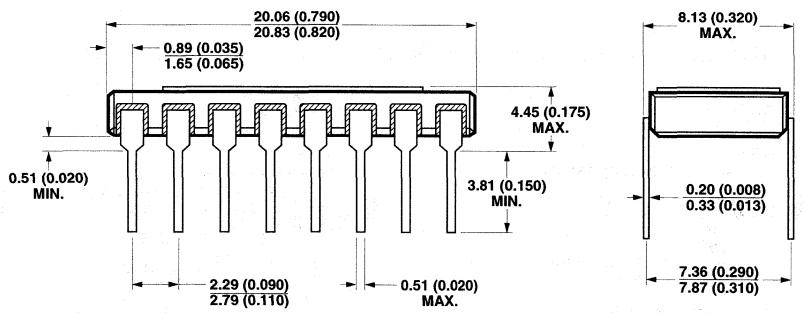
Functional Diagrams

16 pin DIP	8 pin DIP	8 pin DIP	16 pin Flat Pack	20 Pad LCCC
Through Hole	Through Hole	Through Hole	Unformed Leads	Surface Mount
4 Channels	1 Channel	2 Channels	4 Channels	2 Channels
				

Note: All DIP and flat pack devices have common V_{CC} and ground. LCCC (leadless ceramic chip carrier) package has isolated channels with separate V_{CC} and ground connections.

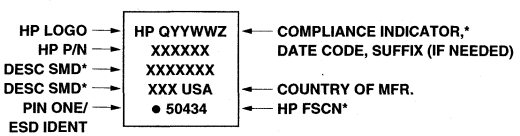
Outline Drawings

16 Pin DIP Through Hole, 4 Channels



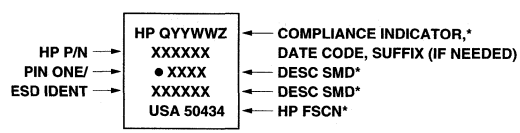
NOTE: DIMENSIONS IN MILLIMETERS (INCHES).

Leaded Device Marking



*QUALIFIED PARTS ONLY

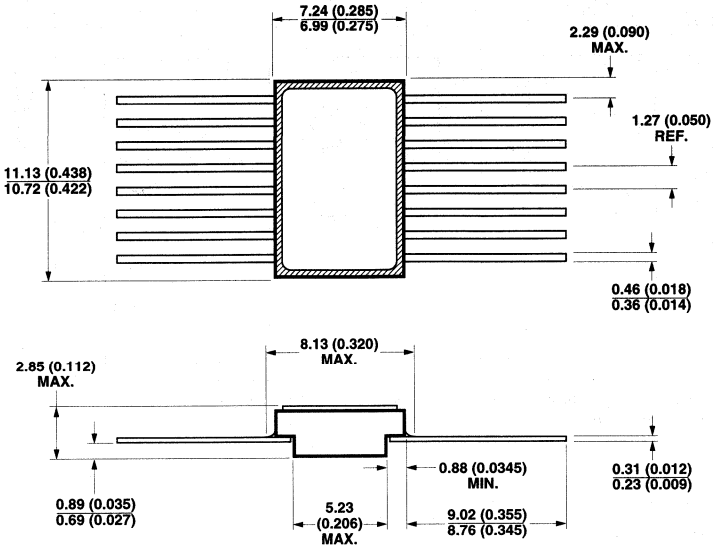
Leadless Device Marking



*QUALIFIED PARTS ONLY

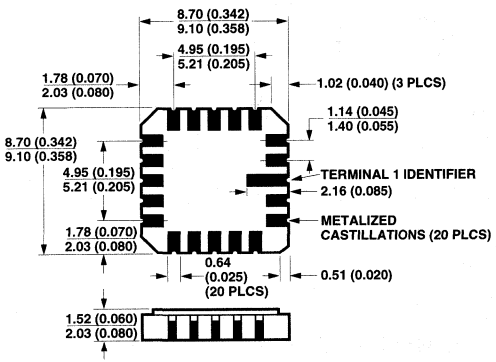
Outline Drawings (continued)

16 Pin Flat Pack, 4 Channels



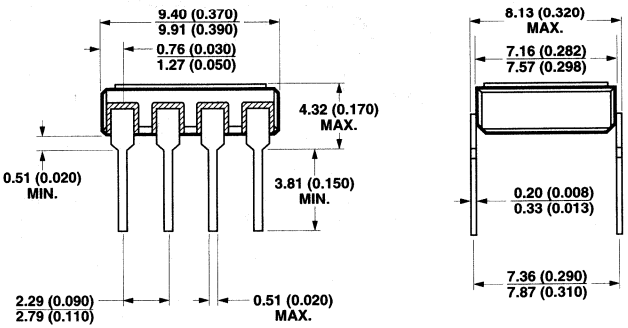
NOTE: DIMENSIONS IN MILLIMETERS (INCHES).

20 Terminal LCCC Surface Mount, 2 Channels



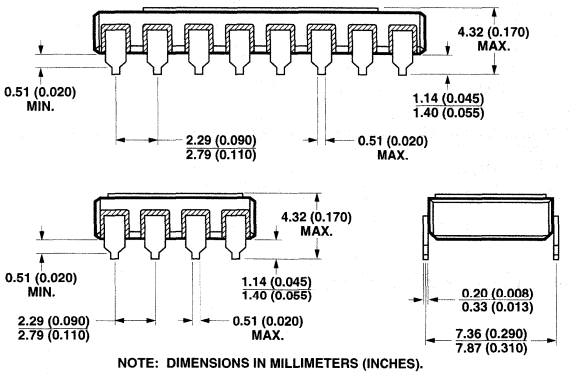
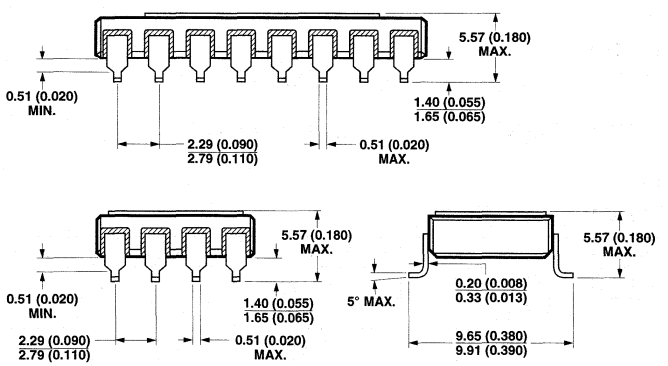
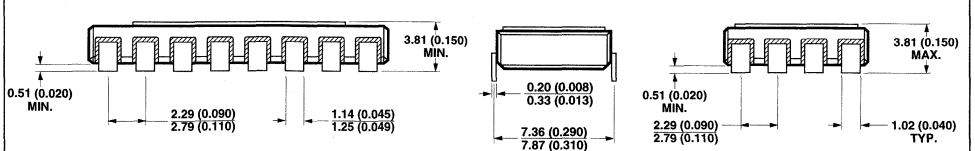
NOTE: DIMENSIONS IN MILLIMETERS (INCHES).
SOLDER THICKNESS 0.127 (0.005) MAX.

8 Pin DIP Through Hole, 1 and 2 Channel



NOTE: DIMENSIONS IN MILLIMETERS (INCHES).

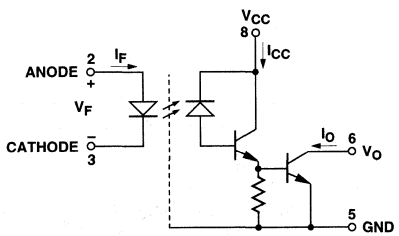
Hermetic Optocoupler Options

Option	Description
100	Surface mountable hermetic optocoupler with leads trimmed for butt joint assembly. This option is available on commercial and hi-rel product in 8 and 16 pin DIP (see drawings below for details).  NOTE: DIMENSIONS IN MILLIMETERS (INCHES).
200	Lead finish is solder dipped rather than gold plated. This option is available on commercial and hi-rel product in 8 and 16 pin DIP. DESC Drawing part numbers contain provisions for lead finish. All leadless chip carrier devices are delivered with solder dipped terminals as a standard feature.
300	Surface mountable hermetic optocoupler with leads cut and bent for gull wing assembly. This option is available on commercial and hi-rel product in 8 and 16 pin DIP (see drawings below for details). This option has solder dipped leads.  NOTE: DIMENSIONS IN MILLIMETERS (INCHES).
600	Surface mountable hermetic optocoupler with leads trimmed for butt joint assembly. This option is available on commercial and hi-rel product in 8 and 16 pin DIP (see drawings below for details). Contact factory for the availability of this option on DESC part types.  NOTE: DIMENSIONS IN MILLIMETERS (INCHES).

Absolute Maximum Ratings

Storage Temperature Range, T_S ..... -65°C to +150°C
Operating Temperature, T_A ..... -55°C to +125°C
Case Temperature, T_C ..... +170°C
Junction Temperature, T_J ..... +175°C
Lead Solder Temperature ..... 260°C for 10s
Output Current, I_O (Each Channel) ..... 40 mA
Output Voltage, V_O (Each Channel) ..... -0.5 to 20 V[1]
Supply Voltage, V_{CC} ..... -0.5 to 20 V[1]
Output Power Dissipation (Each Channel) ..... 50 mW[2]
Peak Input Current (Each Channel, <1 ms Duration) ..... 20 mA
Average Input Current, I_F (Each Channel) ..... 10 mA[3]
Reverse Input Voltage, V_R (Each Channel) 5V
Package Power Dissipation, P_D (each channel) ..... 200 mW

8 Pin Ceramic DIP Single Channel Schematic



ESD Classification

(MIL-STD-883, Method 3015)
HCPL-5700/01 and 6730/31 ..... (ΔΔ), Class 2
6N140A, 6N140A/883B,
HCPL-6750/51 and HCPL-5730/31 ..... (Dot), Class 3

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Input Voltage, Low Level (Each Channel)	$V_{F(OFF)}$		0.8	V
Input Current, High Level (Each Channel)	$I_{F(ON)}$	0.5	5	mA
Supply Voltage	V_{CC}	2.0	18	V
Output Voltage	V_O	2.0	18	V

Electrical Characteristics, T_A = -55°C to +125°C, unless otherwise specified

Parameter		Symbol	Test Conditions	Group A[13] Sub-Group	Limits Min.	Limits Typ.**	Limits Max.	Units	Fig.	Note
Current Transfer Ratio		CTR*	I_F = 0.5 mA, V_O = 0.4 V, V_{CC} = 4.5 V	1,2,3	300	1500		%	3	4,5
			I_F = 1.6 mA, V_O = 0.4 V, V_{CC} = 4.5 V		300	1000				
			I_F = 5 mA, V_O = 0.4 V, V_{CC} = 4.5 V		200	500				
Logic Low Output Voltage		V_{OL}	I_F = 0.5 mA, I_{OL} = 1.5 mA, V_{CC} = 4.5 V	1,2,3		0.11	0.4	V	2	4
			I_F = 1.6 mA, I_{OL} = 4.8 mA, V_{CC} = 4.5 V			0.13	0.4			4,16
			I_F = 5 mA, I_{OL} = 10 mA, V_{CC} = 4.5 V			0.16	0.4			4
Logic High Output Current		I_{OH}*	I_F = 2 µA, V_O = 18 V, V_{CC} = 18 V	1,2,3		0.001	250	µA		4
		I_{OHX}					250	µA		4,6
Logic Low Supply Current	Single Channel and LCCC	I_{CCL}*	I_F = 1.6 mA, V_{CC} = 18 V	1,2,3		1.0	2	mA		15
	Dual Channel		I_{F1} = I_{F2} = 1.6 mA, V_{CC} = 18 V			1.0	4		4	
	Quad Channel		I_{F1} = I_{F2} = I_{F3} = I_{F4} = 1.6 mA V_{CC} = 18 V			1.7	4			
Logic High Supply Current	Single Channel and LCCC	I_{CCH}*	I_F = 0 mA, V_{CC} = 18 V	1,2,3		0.001	20	µA		15
	Dual Channel		I_{F1} = I_{F2} = 0 mA, V_{CC} = 18 V				40			
	Quad Channel		I_{F1} = I_{F2} = I_{F3} = I_{F4} = 0 mA V_{CC} = 18 V				40			
Input Forward Voltage	Single and Dual Channel	V_F*	I_F = 1.6 mA	1	1.0	1.4	1.7	V	1	4
				2			1.7			
				3			1.8			
	LCCC			1,2,3	1.0	1.4	1.8			
	Quad Channel			1,2		1.4	1.7			
				3			1.8			
Input Reverse Breakdown Voltage		BV_R*	I_R = 10 µA	1,2,3	5			V		4
Input-Output Insulation Leakage Current		I_{I-O}*	45% Relative Humidity T_A = 25°C, t = 5 s, V_{I-O} = 1500 VDC	1			1.0	µA		7,12
Capacitance Between Input-Output		C_{I-O}	f = 1 MHz, T_A = 25°C	4			4	pF		4,8 14,17

*For JEDEC registered parts.
**All typical values are at V_{CC} = 5 V, T_A = 25°C.

Electrical Characteristics (cont) T_A = -55°C to +125°C, unless otherwise specified

Parameter	Sym-bol	Test Conditions		Group A[13] Sub-Group	Limits Min.	Limits Typ.**	Limits Max.	Units	Fig.	Note
Propagation Delay Time to Logic Low at Output	t_{PHL}*	I_F = 0.5 mA, R_L = 4.7 kΩ, V_{CC} = 5 V		9, 10, 11		30	100	µs	5, 6, 7, 8	4
	t_{PHL}	I_F = 1.6 mA, R_L = 1.5 kΩ, V_{CC} = 5 V		9, 10, 11		5	30			4, 16
	t_{PHL}*	I_F = 5 mA, R_L = 680 Ω, V_{CC} = 5 V		9		2	5			4, 17
				10, 11			10			
				9, 10, 11			10			4, 16
Propagation Delay Time to Logic High at Output	t_{PLH}*	I_F = 0.5 mA, R_L = 4.7 kΩ, V_{CC} = 5 V		9, 10, 11		17	60	µs	5, 6, 7, 8	4
	t_{PLH}	I_F = 1.6 mA, R_L = 1.5 kΩ, V_{CC} = 5 V		9, 10, 11		14	50			4, 16
	t_{PLH}*	I_F = 5 mA, R_L = 680 Ω, V_{CC} = 5 V		9		8	20			4, 17
				10, 11			30			
				9, 10, 11			30			4, 16
Common Mode Transient Immunity at Low Output Level	$\|CM_L\|$	V_{CC} = 5 V, I_F = 1.6 mA R_L = 1.5 kΩ	$\|V_{CM}\|$ = 25 V_{P-P}[17]	9, 10, 11	500	1000		V/µs	9	4, 10 11, 14
			$\|V_{CM}\|$ = 50 V_{P-P}[16]							
Common Mode Transient Immunity at High Output Level	$\|CM_H\|$	V_{CC} = 5 V, I_F = 0 mA R_L = 1.5 kΩ	$\|V_{CM}\|$ = 25 V_{P-P}[17]	9, 10, 11	500	1000		V/µs	9	4, 10 11, 14
			$\|V_{CM}\|$ = 50 V_{P-P}[16]							

*For JEDEC registered parts.
**All typical values are at V_{CC} = 5 V, T_A = 25°C.

Typical Characteristics, T_A = 25°C, V_{CC} = 5V

Parameter	Sym.	Typ.	Units	Test Conditions	Note
Input Capacitance	C_{IN}	60	pF	V_F = 0V, f = 1 MHz	4
Input Diode Temperature Coefficient	$\Delta V_F/\Delta T_A$	-1.8	mV/°C	I_F = 1.6 mA	4
Resistance (Input-Output)	R_{I-O}	10^{12}	Ω	V_{I-O} = 500 V	4, 8
Capacitance (Input-Output)	C_{I-O}	2.0	pF	f = 1MHz	4, 8

Dual and Quad Channel Product Only

Input-Input Leakage Current	I_{I-I}	0.5	nA	Relative Humidity = 45%, V_{I-I} = 500 V, t = 5 s	9
Resistance (Input-Input)	R_{I-I}	10^{12}	Ω	V_{I-I} = 500 V	9
Capacitance (Input-Input)	C_{I-I}	1.0	pF	f = 1 MHz	9

Notes:

1. GND Pin should be the most negative voltage at the detector side. Keeping V_{CC} as low as possible, but greater than 2.0 V, will provide lowest total I_{OH} over temperature.
2. Output power is collector output power plus total supply power for the single channel device. For the dual channel device, output power is collector output power plus one half the total supply power. For the quad channel device, output power is collector output power plus one fourth of total supply power. Derate at 1.66 mW/°C above 110°C.
3. Derate I_F at 0.33 mA/°C above 110°C.
4. Each channel.
5. CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
6. I_{OHX} is the leakage current resulting from channel to channel optical crosstalk. I_F = 2 μA for channel under test. For all other channels, I_F = 10 mA.
7. All devices are considered two-terminal devices; measured between all input leads or terminals shorted together and all output leads or terminals shorted together.
8. Measured between each input pair shorted together and all output connections for that channel shorted together.
9. Measured between adjacent input pairs shorted together for each multi-channel device.
10. CM_L is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic low state (V_O < 0.8 V). CM_H is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic high state (V_O > 2.0 V).
11. In applications where dV/dt may exceed 50,000 V/μs (such as a static discharge) a series resistor, R_{CC}, should be included to protect the detector ICs from destructively high surge currents. The recommended value is:

$$R_{CC} = \frac{1\ (V)}{0.15\ I_F\ (mA)}\ k\Omega$$

for single channel;

$$R_{CC} = \frac{1\ (V)}{0.3\ I_F\ (mA)}\ k\Omega$$

for dual channel;

$$R_{CC} = \frac{1\ (V)}{0.6\ I_F\ (mA)}\ k\Omega$$

for quad channel.

12. This is a momentary withstand test, not an operating condition.
13. Standard parts receive 100% testing at 25°C (Subgroups 1 and 9). SMD and 883B parts receive 100% testing at 25,125, and -55°C (Subgroups 1 and 9, 2 and 10, 3 and 11, respectively).
14. Parameters tested as part of device initial characterization and after design and process changes. Parameters guaranteed to limits specified for all lots not specifically tested.
15. The HCPL-6730 and HCPL-6731 dual channel parts function as two independent single channel units. Use the single channel parameter limits.
16. Not required for 6N140A, 6N140A/883B, HCPL-6750, HCPL-6751 and 8302401 types.
17. Required for 6N140A, 6N140A/883B, HCPL-6750, HCPL-6751 and 8302401 types only.

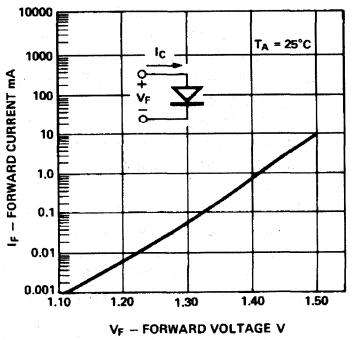


Figure 1. Input Diode Forward Current vs. Forward Voltage.

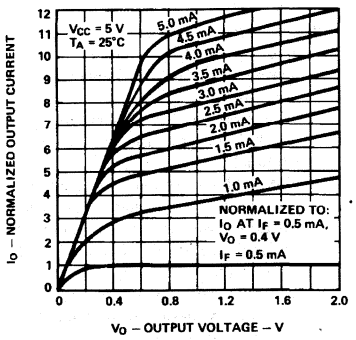


Figure 2. Normalized DC Transfer Characteristics.

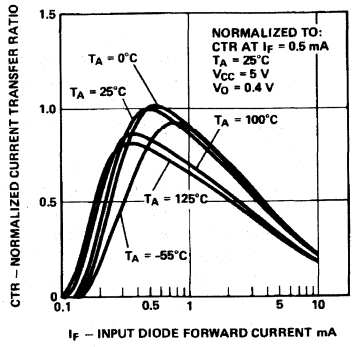


Figure 3. Normalized Current Transfer Ratio vs. Input Diode Forward Current.

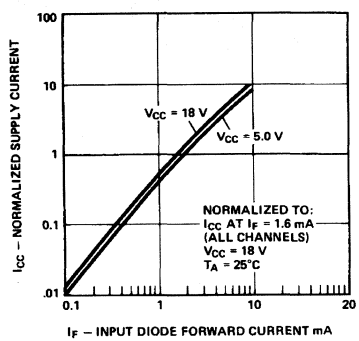


Figure 4. Normalized Supply Current vs. Input Diode Forward Current.

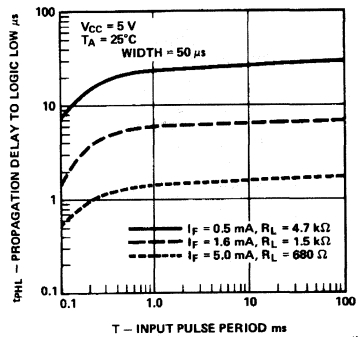


Figure 5. Propagation Delay to Logic Low vs. Input Pulse Period.

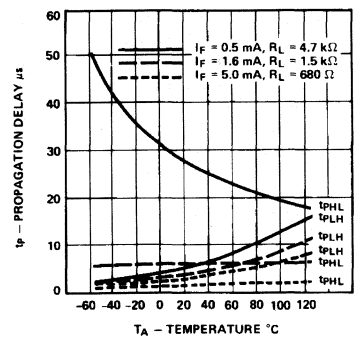


Figure 6. Propagation Delay vs. Temperature.

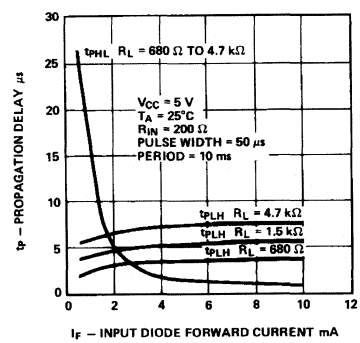
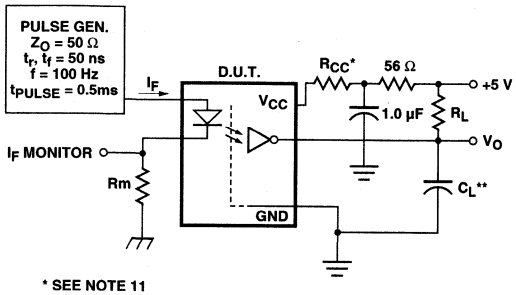


Figure 7. Propagation Delay vs. Input Diode Forward Current.



* SEE NOTE 11

** C_L INCLUDES PROBE AND STRAY WIRING CAPACITANCE.

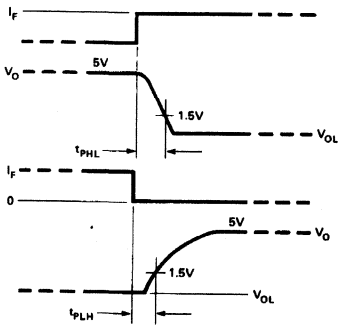
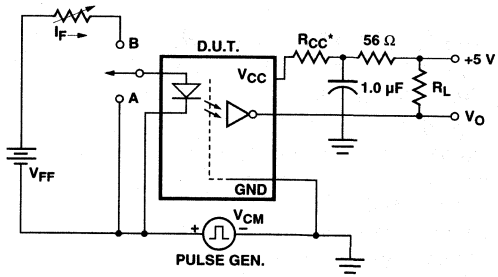


Figure 8. Switching Test Circuit (f, t_P not JEDEC registered).



* SEE NOTE 11

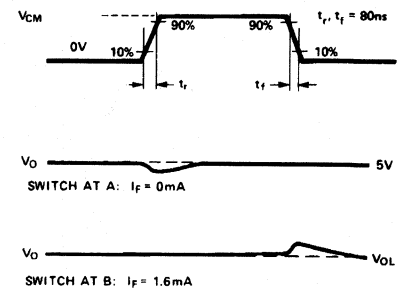


Figure 9. Test Circuit for Transient Immunity and Typical Waveforms.

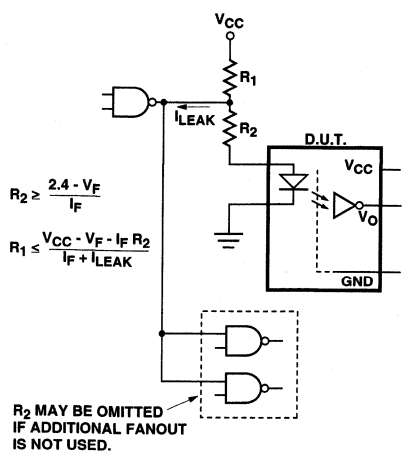


Figure 10. Recommended Drive Circuitry Using TTL Open-Collector Logic.

MIL-PRF-38534 Class H, Class K, and DESC SMD Test Program

Hewlett-Packard's Hi-Rel Optocouplers are in compliance with MIL-PRF-38534 Class H and K. Class H devices are also in compliance with DESC drawings 83024, 5962-89785 and 5962-89810.

Testing consists of 100% screening and quality conformance inspection to MIL-PRF-38534.

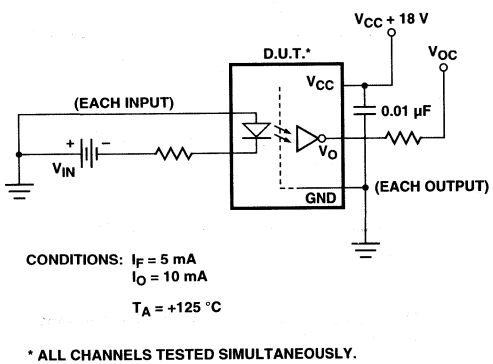


Figure 11. Operating Circuit for Burn-In and Steady State Life Tests.

AC/DC to Logic Interface Hermetically Sealed Optocouplers

Technical Data

HCPL-576X*
5962 8947701
*See matrix for available extensions

Features

- **Dual Marked with Device Part Number and DESC Standard Military Drawing**
- **Manufactured and Tested on a MIL-STD-1772 Certified Line**
- **QML-38534, Class H and K**
- **Hermetically Sealed 8-pin Dual In-Line Packages**
- **Performance Guaranteed over -55°C to +125°C**
- **ac or dc Input**
- **Programmable Sense Voltage**
- **Hysteresis**
- **HCPL-3700 Operating Compatibility**
- **Logic Compatible Output**
- **1500 Vdc Withstand Test Voltage**
- **Thresholds Guaranteed over Temperature**
- **Thresholds Independent of LED Characteristics**

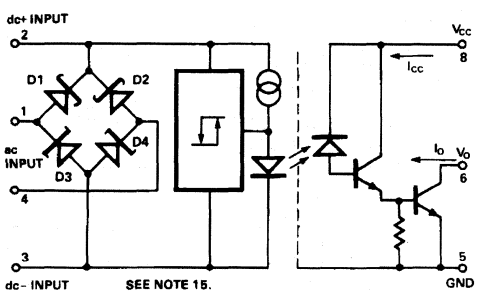
Applications

- **Military and Space**
- **High Reliability Systems**
- **Transportation, Medical, and Life Critical Systems**
- **Limit Switch Sensing**
- **Low Voltage Detector**
- **ac/dc Voltage Sensing**
- **Relay Contact Monitor**
- **Relay Coil Voltage Monitor**
- **Current Sensing**
- **Microprocessor Interface**
- **Telephone Ring Detection**
- **Harsh Industrial Environments**

Description

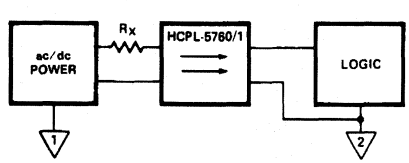
The HCPL-5760, HCPL-5761, and 5962-8947701 are single channel, hermetically sealed, voltage/current threshold detection optocouplers. The products are capable of operation and storage over the full military temperature range and can be purchased as either standard product, or with full MIL-PRF-38534 Class Level H or K testing, or from the DESC Standard Military Drawing (SMD) 5962-89477. All devices

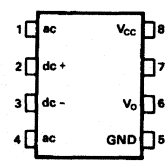
Schematic



TRUTH TABLE

INPUT	OUTPUT
$H(V_{TH+} < V_{dc})$(on)	L
$L(V_{dc} < V_{TH-})$(off)	H





CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

are manufactured and tested on a MIL-PRF-38534 certified line and are included in the DESC Qualified Manufacturers List, QML-38534 for Hybrid Microcircuits.

Each unit contains a light emitting diode (LED), a threshold sensing input buffer IC, and a high gain photon detector to provide an optocoupler which permits adjustable external threshold levels. The input buffer circuit has a nominal turn on threshold of 2.5 mA (I_{TH+}) and 3.6 volts (V_{TH+}). The addition of one or more external attenuation resistors permits the use of this device over a wide range of input voltages and currents. Threshold sensing prior to the LED and detector elements minimizes effects of any variation in optical coupling. Hysteresis is also provided in the buffer for extra noise immunity and switching stability.

The buffer circuit is designed with internal clamping diodes to protect the circuitry and LED from a wide range of over-voltage and over-current transients while the diode bridge enables easy use with ac voltage input.

These units combine several unique functions in a single package, providing the user with an ideal component for computer input boards and other applications where a predetermined input threshold optocoupler level is desirable.

The high gain output stage features an open collector output providing both TTL compatible saturation voltages and CMOS compatible breakdown voltages.

This is an eight pin DIP which may be purchased with a variety of lead bend and plating options. See Selection Guide Table for details. Standard Military Drawing (SMD) parts are available for each lead style.

Selection Guide–Package Styles and Lead Configuration Options

HP Part # and Options	
Commercial	HCPL-5760
MIL-PRF-38534 Class H	HCPL-5761
MIL-PRF-38534 Class K	HCPL-576K
Standard Lead Finish	Gold
Solder Dipped	Option #200
Butt Joint/Gold Plate	Option #100
Gull Wing/Soldered	Option #300
Crew Cut/Gold Plate	Option #600
SMD Part #	
Prescript for all below	5962-
Either Gold or Soldered	8947701PX
Gold Plate	8947701PC
Solder Dipped	8947701PA
Butt Joint/Gold Plate	8947701YC
Butt Joint/Soldered	8947701YA
Gull Wing/Soldered	8947701XA
Crew Cut/Gold Plate	Available
Crew Cut/Soldered	Available

Absolute Maximum Ratings

Storage Temperature Range ..... -65°C to +150°C
Operating Temperature ..... -55°C to 125°C
Lead Solder Temperature ..... 260°C for 10 s[2]
Average Input Current, I_{IN} ..... 15 mA[3]
Surge Input Current, $I_{IN,SG}$ ..... 140 mA[3,4]
Peak Transient Input Current, $I_{IN,PK}$ ..... 500 mA[3,4]
Input Power Dissipation, P_{IN} ..... 195 mW[5]
Total Package Power Dissipation, P_d ..... 260 mW
Output Power Dissipation, P_O ..... 65 mW
Average Output Current, I_O ..... 40 mA
Supply Voltage, V_{CC} (Pins 8-5) ..... -0.5 min., 20 V max.
Output Voltage, V_O (Pins 6-5) ..... -0.5 min., 20 V max.

ESD Classification

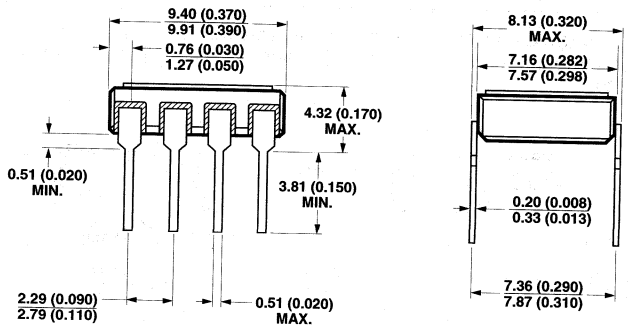
(MIL-STD-883, Method 3015) ..... (ΔΔ), Class 2

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply	V_{CC}	3.0	18	V
Operating Frequency[1]	f	0	10	KHz

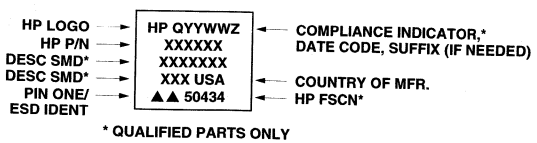
Outline Drawing

8 Pin DIP Through Hole



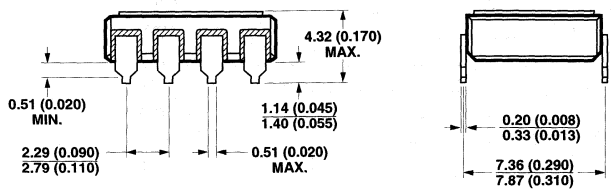
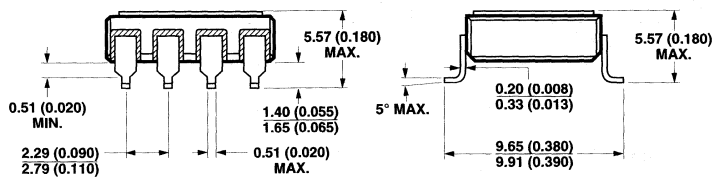
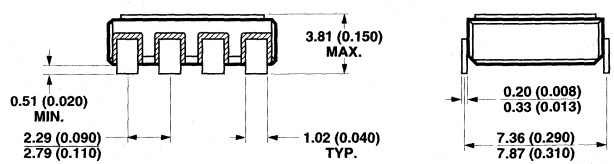
NOTE: DIMENSIONS IN MILLIMETERS (INCHES).

Device Marking



* QUALIFIED PARTS ONLY

Hermetic Optocoupler Options

Option	Description
100	Surface mountable hermetic optocoupler with leads trimmed for butt joint assembly. This option is available on commercial and hi-rel product. 
200	Lead finish is solder dipped rather than gold plated. This option is available on commercial and hi-rel product. DESC Drawing part numbers contain provisions for lead finish.
300	Surface mountable hermetic optocoupler with leads cut and bent for gull wing assembly. This option is available on commercial and hi-rel product. This option has solder dipped leads. 
600	Surface mountable hermetic optocoupler with leads trimmed for butt joint assembly. This option is available on commercial and hi-rel product. Contact factory for the availability of this option on DESC part types. 

Note: Dimensions in millimeters (inches).

Electrical Characteristics T_A = -55°C to 125°C, unless otherwise specified. See note 16.

Parameter		Symbol	Conditions	Group A Subgroup	Min.	Typ.*	Max.	Units	Fig.	Note
Input Threshold Current		I_{TH+}	$V_{IN} = V_{TH+}$; V_{CC} = 4.5 V; V_O = 0.4 V; $I_O \geq$ 2.6 mA	1, 2, 3	1.75	2.5	3.20	mA		
		I_{TH-}	$V_{IN} = V_{TH-}$; V_{CC} = 4.5 V; V_O = 2.4 V; $I_{OH} \leq$ 250 µA	1, 2, 3	0.93	1.3	1.62	mA		
Input Threshold Voltage	dc (Pins 2, 3)	V_{TH+}	$V_{IN} = V_2 - V_3$; Pins 1 & 4 Open V_{CC} = 4.5 V; V_O = 0.4 V; $I_O \geq$ 2.6 mA	1, 2, 3	3.18	3.6	4.10	V		7
		V_{TH-}	$V_{IN} = V_2 - V_3$; Pins 1 & 4 Open V_{CC} = 4.5 V; V_O = 2.4 V; $I_O \leq$ 250 µA	1, 2, 3	1.90	2.5	3.00	V	1, 2	
	ac (Pins 1, 4)	V_{TH+}	$V_{IN} = \lvert V_1 - V_4 \rvert$; Pins 2 & 3 Open V_{CC} = 4.5 V; V_O = 0.4 V; $I_O \geq$ 2.6 mA	1, 2, 3	3.79	5.0	5.62	V		7, 8
		V_{TH-}	$V_{IN} = \lvert V_1 - V_4 \rvert$; Pins 2 & 3 Open V_{CC} = 4.5 V; V_O = 2.4 V; $I_O \leq$ 250 µA	1, 2, 3	2.57	3.7	4.52	V		
Input Clamp Voltage		V_{IHC1}	$V_{IHC1} = V_2 - V_3$; V_3 = GND; I_{IN} = 10 mA; Pin 1 & 4 Connected to Pin 3	1, 2, 3	5.3	5.9	6.7	V	3	15
		V_{IHC2}	$V_{IHC2} = \lvert V_1 - V_4 \rvert$; $\lvert I_{IN} \rvert$ = 10 mA; Pins 2 & 3 Open	1, 2, 3	6.0	6.6	7.4	V		
		V_{IHC3}	$V_{IHC3} = V_2 - V_3$; V_3 = GND; I_{IN} = 15 mA; Pins 1 & 4 Open	1, 2, 3		12.0	13.0	V		
Input Current		I_{IN}	$V_{IN} = V_2 - V_3$ = 5.0 V; Pins 1 & 4 Open	1, 2, 3	3.0	3.9	4.5	mA	4	
Logic Low Output Voltage		V_{OL}	V_{CC} = 4.5 V; I_{OL} = 2.6 mA	1, 2, 3		0.05	0.4	V	4	7
Logic High Output Current		I_{OH}	$V_{OH} = V_{CC}$ = 18 V	1, 2, 3			250	µA		
Logic Low Supply Current		I_{CCL}	$V_2 - V_3$ = 5.0 V; V_O = Open; V_{CC} = 18 V	1, 2, 3		0.8	3.0	mA		
Logic High Supply Current		I_{CCH}	V_{CC} = 18 V; V_O = Open	1, 2, 3		0.001	20	µA	5	
Input-Output Insulation		I_{I-O}	45% RH, t = 5 s; V_{I-O} = 1500 Vdc; T_A = 25°C	1			1	µA		9, 10

Electrical Characteristics T_A = -55°C to 125°C, V_{CC} = 5.0 V, unless otherwise specified (continued).

Parameter	Symbol	Conditions		Group A Subgroup	Min.	Typ.*	Max.	Units	Fig.	Note
Propagation Delay Time to Logic Low Output Level	t_{PHL}	R_L =1.8 kΩ, C_L = 15 pF		9, 10, 11		4	20	µs	6, 7	6, 11
Propagation Delay Time to Logic High Output Level	t_{PLH}	R_L =1.8 kΩ, C_L = 15 pF		9, 10, 11		8	40	µs		6, 12
Logic High Common Mode Transient Immunity	$\|CM_H\|$	V_{CM} = 50 V	T_A = 25°C, I_{IN} = 0 mA	9	1000	≥ 10,000		V/µs	8	13, 14, 17
		V_{CM} = 450 V				≥ 10,000				
Logic Low Common Mode Transient Immunity	$\|CM_L\|$	V_{CM} = 50 V	T_A = 25°C, I_{IN} = 4 mA	9	1000	≥ 5,000		V/µs		
		V_{CM} = 250 V				≥ 5,000				

*All typical values are at T_A = 25°C, V_{CC} = 5 V unless otherwise noted.

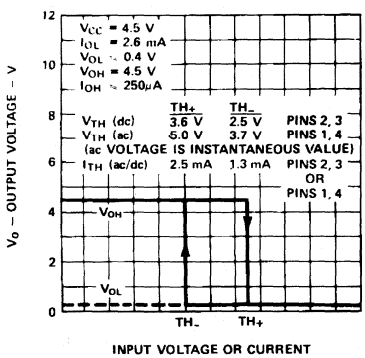


Figure 1. Typical Transfer Characteristics.

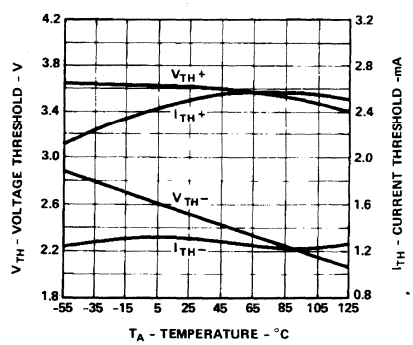


Figure 2. Typical dc Threshold Levels vs. Temperature.

Typical Characteristics All typical values are at T_A = 25°C, V_{CC} = 5 V, unless otherwise specified.

Parameter	Symbol	Typ.	Units	Conditions	Fig.	Note
Hysteresis	I_{HYS}	1.2	mA	$I_{HYS} = I_{TH+} - I_{TH-}$	1	
	V_{HYS}	1.1	V	$V_{HYS} = V_{TH+} - V_{TH-}$		
Input Clamp Voltage	V_{ILC}	-0.76	V	$V_{ILC} = V_2 - V_3$; V_3 = GND; I_{IN} = -10 mA		
Bridge Diode Forward Voltage	$V_{D1,2}$	0.62		I_{IN} = 3 mA (see schematic)		
	$V_{D3,4}$	0.73				
Input-Output Resistance	R_{I-O}	10^{12}	Ω	V_{I-O} = 500 Vdc		9
Input-Output Capacitance	C_{I-O}	2.0	pF	f = 1 MHz, V_{I-O} = 0 Vdc		
Input Capacitance	C_{IN}	50	pF	f = 1 MHz; V_{IN} = 0 V, Pins 2 & 3, Pins 1 & 4 Open		
Output Rise Time (10-90%)	t_r	10	µs		7	
Output Fall Time (90-10%)	t_f	0.5	µs		7	

Notes:

1. Maximum operating frequency is defined when output waveform (Pin 6) attains only 90% of V_{CC} with R_L = 1.8 kΩ, C_L = 15 pF using a 5 V square wave input signal.
2. Measured at a point 1.6 mm below seating plane.
3. Current into/out of any single lead.
4. Surge input current duration is 3 ms at 120 Hz pulse repetition rate. Transient input current duration is 10 µs at 120 Hz pulse repetition rate. Note that maximum input power, P_{IN}, must be observed.
5. Derate linearly above 100°C free-air temperature at a rate of 4.26 mW/°C. Maximum input power dissipation of 195 mW allows an input IC junction temperature of 150°C at an ambient temperature of T_A = 125°C with a typical thermal resistance from junction to ambient of θ_{JAi} = 235°C/W. The typical thermal resistance from junction to case is equal to 170°C/W. Excessive P_{IN} and T_J may result in device degradation.
6. The 1.8 kΩ load represents 1 TTL unit load of 1.6 mA and the 4.7 kΩ pull-up resistor.
7. Logic low output level at Pin 6 occurs under the conditions of $V_{IN} \geq V_{TH+}$ as well as the range of $V_{IN} > V_{TH}$ – once V_{IN} has exceeded V_{TH+}. Logic high output level at Pin 6 occurs under the conditions of $V_{IN} \leq V_{TH-}$ as well as the range of $V_{IN} < V_{TH+}$ once V_{IN} has decreased below V_{TH-}.
8. The ac voltage is instantaneous voltage.
9. Device considered a two terminal device: Pins 1, 2, 3, 4 connected together, Pins 5, 6, 7 8 connected together.
10. This is a momentary withstand test, not an operating condition.
11. The t_{PHL} propagation delay is measured from the 2.5 V level of the leading edge of a 5.0 V input pulse (1 µs rise time) to the 1.5 V level on the leading edge of the output pulse (see Figure 7).
12. The t_{PLH} propagation delay is measured from the 2.5 V level of the trailing edge of a 5.0 V input pulse (1 µs fall time) to the 1.5 V level on the trailing edge of the output pulse (see Figure 7).
13. Common mode transient immunity in Logic High level is the maximum tolerable $dV_{CM/dt}$ of the common mode voltage, V_{CM}, to ensure that the output will remain in a Logic High state (i.e., V_O > 2.0 V). Common mode transient immunity in Logic Low level is the maximum tolerable $dV_{CM/dt}$ of the common mode voltage, V_{CM}, to ensure that the output will remain in a Logic Low state (i.e., V_O < 0.8 V). See Figure 8.
14. In applications where $dV_{CM/dt}$ may exceed 50,000 V/µs (such as static discharge), a series resistor, R_{CC}, should be included to protect the detector IC from destructively high surge currents. The recommended value for R_{CC} is 240 Ω per volt of allowable drop in V_{CC} (between Pin 8 and V_{CC}) with a minimum value of 240 Ω.
15. D_1 and D_2 are Schottky diodes; D_3 and D_4 are zener diodes.
16. Standard parts receive 100% testing at 25°C (Subgroups 1 and 9). SMD and Class H parts receive 100% testing at 25, 125, and -55°C (Subgroups 1 and 9, 2 and 10 ,3 and 11, respectively.)
17. Parameters shall be tested as part of device initial characterization and after process changes. Parameters shall be guaranteed to the limits specified for all lots not specifically tested.

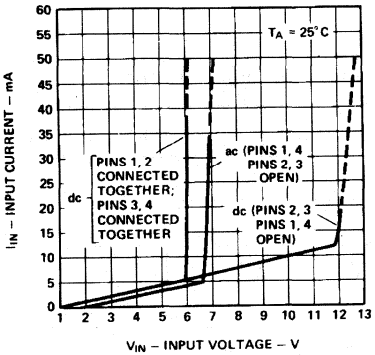


Figure 3. Typical Input Characteristics, I_{IN} vs. V_{IN}. (AC Voltage is Instantaneous Value.)

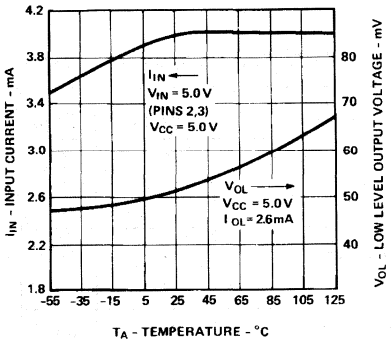


Figure 4. Typical Input Current, I_{IN}, and Low Level Output Voltage, V_{OL}, vs. Temperature.

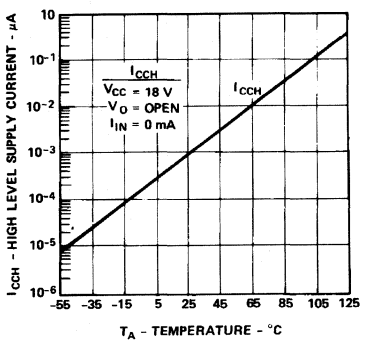


Figure 5. Typical High Level Supply Current, I_{CCH} vs. Temperature.

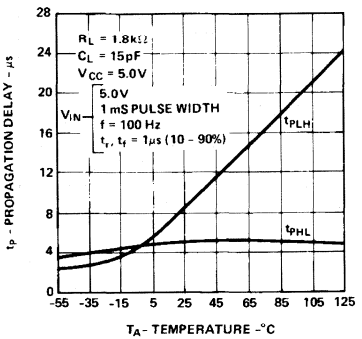


Figure 6. Typical Propagation Delay vs. Temperature.

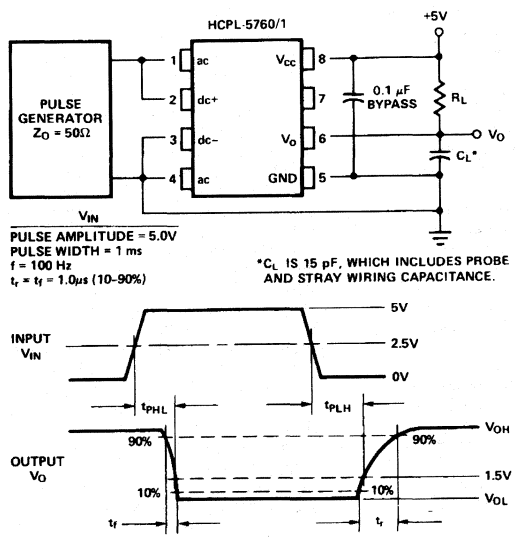


Figure 7. Switching Test Circuit.

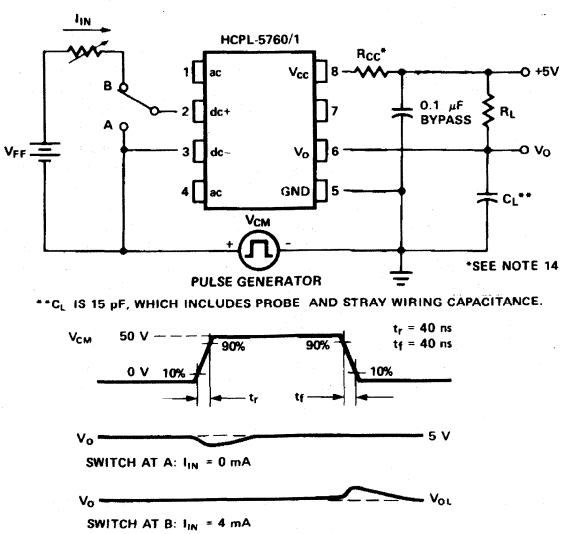


Figure 8. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

Electrical Considerations

The HCPL-5760, HCPL-5761, or 5962-89477 optocoupler has internal temperature compensated, predictable voltage and current threshold points which allow selection of an external resistor, R_x, to determine larger external threshold voltage levels. For a desired external threshold voltage, $V_{\pm}$, a corresponding typical value of R_x can be obtained from Figure 10. Specific calculation of R_x can be obtained from Equation (1) of Figure 11. Specification of both V_+ and V_- voltage threshold levels simultaneously can be obtained by the use of R_x and R_p as shown in Figure 11 and determined by Equations (2) and (3).

R_x can provide over-current transient protection by limiting input current during a transient condition. For monitoring contacts with a relay or switch, the HCPL-5760/1, or 5962-89477 combination with R_x and R_p can be used to allow a specific current to be conducted through the contacts for cleaning purposes (wetting current).

The choice of which input voltage clamp level to choose depends upon the application of this device (see Figure 3). It is recommended that the low clamp condition be used when possible to lower the input power dissipation as well as the LED current, which minimizes LED degradation over time.

In applications where $dV_{CM/dt}$ may be extremely large (such as static discharge), a series resistor, R_{CC}, should be connected in series with V_{CC} and Pin 8 to protect the detector IC from destructively high surge currents. See note 14 for determination of R_{CC}. In addition, it is recommended that a ceramic disc bypass capacitor of 0.01 µF to 0.1 µF be placed between Pins 8 and 5 to reduce the effect of power supply noise.

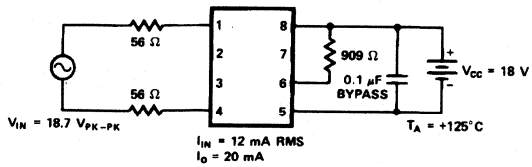


Figure 9. Operating Circuit for Burn-In and Steady State Life Tests.

For interfacing ac signals to TTL systems, output low pass filtering can be performed with a pullup resistor of 1.5 kΩ and 20 µF capacitor. This application requires a Schmitt trigger gate to avoid slow rise time chatter problems. For ac input applications, a filter capacitor can be placed across the dc input terminals for either signal or transient filtering.

Either ac (Pins 1, 4) or dc (Pins 2, 3) input can be used to determine external threshold levels.

For one specifically selected external threshold voltage level V_+ or V_-, R_x can be determined without use of R_p via

$$R_x = \frac{V_+ - V_{TH+}}{I_{TH+}} \quad \begin{matrix}(-)\\(-)\end{matrix} \quad (1)$$

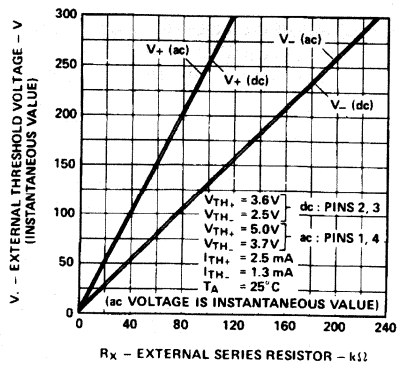


Figure 10. Typical External Threshold Characteristic, $V_{\pm}$ vs. R_x.

For two specifically selected external threshold voltage levels, V_+ and V_-, the use of R_x and R_p will permit this selection via equations (2), (3) provided the following conditions are met:

$$\frac{V_+}{V_-} \geq \frac{V_{TH+}}{V_{TH-}} \text{ and } \frac{V_+ - V_{TH+}}{V_- - V_{TH-}} < \frac{I_{TH+}}{I_{TH-}}$$

$$R_x = \frac{V_{TH-}(V_+) - V_{TH+}(V_-)}{I_{TH+}(V_{TH-}) - I_{TH-}(V_{TH+})} \quad (2)$$

$$R_p = \frac{V_{TH-}(V_+) - V_{TH+}(V_-)}{I_{TH+}(V_- - V_{TH-}) + I_{TH-}(V_{TH+} - V_+)} \quad (3)$$

See Application Note 1004 for more information.

MIL-PRF-38534 Class H, Class K, and DESC SMD Test Program

Hewlett-Packard's Hi-Rel Optocouplers are in compliance with MIL-PRF-38534 Class H and K. Class H devices are also in compliance with DESC drawing 5962-89477.

Testing consists of 100% screening and quality conformance inspection to MIL-PRF-38534.

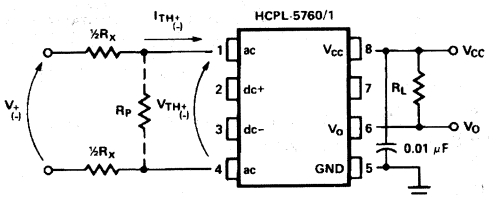


Figure 11. External Threshold Voltage Level Selection.

90 V/1.0 Ω, Hermetically Sealed, Power MOSFET Optocoupler

Technical Data

HSSR-711X*
5962-9314001
*See matrix for available extensions

Features

- **Dual Marked with Device Part Number and DESC Standard Military Drawing**
- **ac/dc Signal & Power Switching**
- **Compact Solid-State Bidirectional Switch**
- **Manufactured and Tested on a MIL-PRF-38534 Certified Line**
- **QML-38534**
- **MIL-PRF-38534 Class H**
- **Space Level Processing Available**
- **Hermetically Sealed 8-Pin Dual In-Line Package**
- **Small Size and Weight**
- **Performance Guaranteed over -55°C to +125°C**
- **Connection A 0.8 A, 1.0 Ω**
- **Connection B 1.6 A, 0.25 Ω**
- **1500 Vdc Withstand Test Voltage**
- **High Transient Immunity**
- **5 Amp Output Surge Current**

Applications

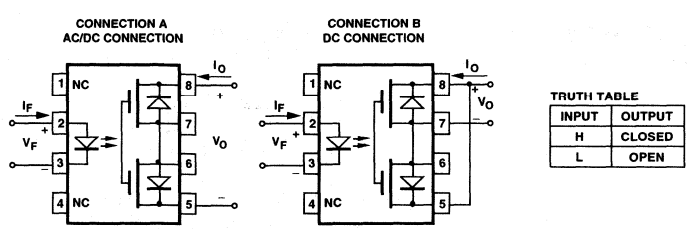
- **Military and Space**
- **High Reliability Systems**
- **Standard 28 Vdc and 48 Vdc Load Driver**
- **Standard 24 Vac Load Driver**
- **Aircraft Controls**
- **ac/dc Electromechanical and Solid State Relay Replacement**
- **I/O Modules**
- **Harsh Industrial Environments**

Description

The HSSR-7110, HSSR-7111 and SMD 5962-9314001 are single channel power MOSFET optocouplers, constructed in eight-pin, hermetic, dual-in-line, ceramic packages. The devices operate exactly like a solid-state relay. The products are capable of operation and storage over the full military temperature range and can be purchased as a standard product (HSSR-7110), with full MIL-PRF-38534 Class H testing (HSSR-7111), or from the DESC Standard Military Drawing (SMD) 5962-93140.

These devices may be purchased with a variety of lead bend and plating options. See Selection Guide Table for details. Standard Military Drawing (SMD) parts are available for each lead style.

Functional Diagrams



TRUTH TABLE

INPUT	OUTPUT
H	CLOSED
L	OPEN

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

All devices are manufactured and tested on a MIL-PRF-38534 certified line and are included in the DESC Qualified Manufacturers List, QML-38534 for Hybrid Microcircuits. Each device contains an AlGaAs light emitting diode optically coupled to a photovoltaic diode stack which drives two discrete power MOSFETs. The device operates as a solid-state replacement for single-pole, normally open, (1 Form A) relays used for general purpose switching of signals and loads in high reliability applications.

The devices feature logic level input control and very low output on-resistance, making them suitable for both ac and dc loads. Connection A, as shown in the Functional Diagram, allows the device to switch either ac or dc loads. Connection B, with the polarity and pin configuration as shown, allows the device to switch dc loads only. The advantage of Connection B is that the on-resistance is significantly reduced, and the output current capability increases by a factor of two.

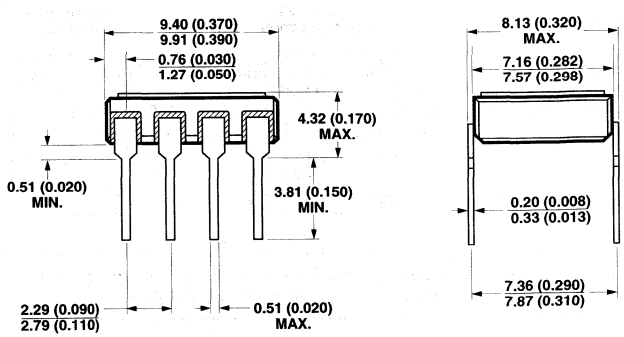
The devices are convenient replacements for mechanical and solid state relays where high component reliability with standard footprint lead configuration is desirable. Devices may be purchased with a variety of lead bend and plating options. See Selection Guide table for details. Standard Military Drawing (SMD) parts are available for each package and lead style.

The HSSR-7110, HSSR-7111, and SMD 5962-93140 are designed to switch loads on 28 Vdc power systems. They meet 80 V surge and ± 600 V spike requirements.

Selection Guide–Package Styles and Lead Configuration Options

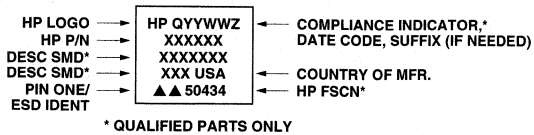
HP Part # and Options	
Commercial	HSSR-7110
MIL-PRF-38534 Class H	HSSR-7111
Standard Lead Finish	Gold
Solder Dipped	Option #200
Butt Joint/Gold Plate	Option #100
Gull Wing/Soldered	Option #300
Crew Cut/Gold Plate	Option #600
SMD Part #	
Prescript for all below	5962-
Either Gold or Soldered	9314001HPX
Gold Plate	9314001HPC
Solder Dipped	9314001HPA
Butt Joint/Gold Plate	9314001HYC
Butt Joint/Soldered	9314001HYA
Gull Wing/Soldered	9314001HXA
Crew Cut/Gold Plate	9314001HZC
Crew Cut/Soldered	9314001HZA

Outline Drawing
8-pin DIP Through Hole



NOTE: DIMENSIONS IN MILLIMETERS (INCHES).

Device Marking



Absolute Maximum Ratings

Storage Temperature Range ..... -65°C to +150°C
Operating Ambient Temperature – T_A ..... -55°C to +125°C
Junction Temperature – T_J ..... +150°C
Operating Case Temperature – T_C ..... +145°C[1]
Lead Solder Temperature ..... 260°C for 10 s
(1.6 mm below seating plane)
Average Input Current – I_F ..... 20 mA
Peak Repetitive Input Current – I_{FPK} ..... 40 mA
(Pulse Width < 100 ms; duty cycle < 50%)
Peak Surge Input Current – I_{FPK} surge ..... 100 mA
(Pulse Width < 0.2 ms; duty cycle < 0.1%)
Reverse Input Voltage – V_R ..... 5 V
Average Output Current – Figure 2
Connection A – I_O ..... 0.8 A
Connection B – I_O ..... 1.6 A
Single Shot Output Current – Figure 3
Connection A – I_{OPK} surge (Pulse width < 10 ms) ..... 5.0 A
Connection B – I_{OPK} surge (Pulse width < 10 ms) ..... 10.0 A
Output Voltage
Connection A – V_O ..... -90 V to +90 V
Connection B – V_O ..... 0 V to +90 V
Average Output Power Dissipation – Figure 4 ..... 800 mW[2]

Thermal Resistance

Maximum Output MOSFET Junction to Case – θ_{JC} = 15°C/W

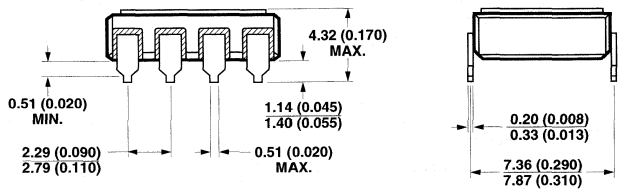
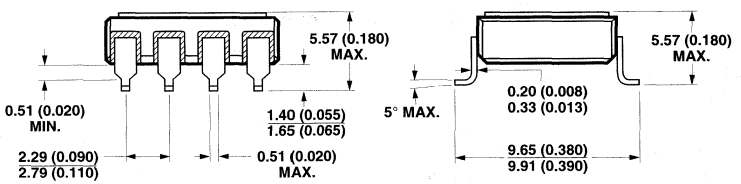
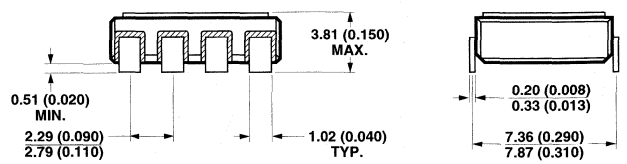
ESD Classification

(MIL-STD-883, Method 3015) ..... (ΔΔ), Class 2

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Input Current (on)	$I_{F(ON)}$	5	20	mA
Input Voltage (off)	$V_{F(OFF)}$	0	0.6	V
Operating Temperature	T_A	-55	+125	°C

Hermetic Optocoupler Options

Option	Description
100	Surface mountable hermetic optocoupler with leads trimmed for butt joint assembly. This option is available on commercial and hi-rel product. 
200	Lead finish is solder dipped rather than gold plated. This option is available on commercial and hi-rel product. DESC Drawing part numbers contain provisions for lead finish.
300	Surface mountable hermetic optocoupler with leads cut and bent for gull wing assembly. This option is available on commercial and hi-rel product. This option has solder dipped leads. 
600	Surface mountable hermetic optocoupler with leads trimmed for butt joint assembly. This option is available on commercial and hi-rel product. 

Note: Dimensions in millimeters (inches).

Electrical Specifications

T_A =-55°C to +125°C, unless otherwise specified. See note 9.

Parameter		Sym.	Group A, Sub-group	Test Conditions	Min.	Typ.*	Max.	Units	Fig.	Notes
Output Withstand Voltage		$\|V_{O(OFF)}\|$	1, 2, 3	V_F = 0.6 V, I_O = 10 µA	90	110		V	5	
Output On-Resistance	Connection A	$R_{(ON)}$	1, 2, 3	I_F = 10 mA, I_O = 800 mA, (pulse duration ≤ 30 ms)		0.40	1.0	Ω	6,7	3
	Connection B			I_F = 10 mA, I_O = 1.6 A, (pulse duration ≤ 30 ms)		0.12	0.25			
Output Leakage Current		$I_{O(OFF)}$	1, 2, 3	V_F = 0.6 V, V_O = 90 V,		10^{-4}	10	µA	8	
Input Forward Voltage		V_F	1, 2, 3	I_F = 10 mA	1.0	1.24	1.7	V	9	
Input Reverse Breakdown Voltage		V_R	1, 2, 3	I_R = 100 µA	5.0			V		
Input-Output Insulation		I_{I-O}	1	RH ≤ 45%, t = 5 s, V_{I-O} = 1500 Vdc, T_A = 25°C			1.0	µA		4, 5
Turn On Time		t_{ON}	9, 10, 11	I_F = 10 mA, V_{DD} = 28 V, I_O = 800 mA		1.25	6.0	ms	1,10, 11,12, 13	
Turn Off Time		t_{OFF}	9,10,11	I_F = 10 mA, V_{DD} = 28 V, I_O = 800 mA		0.02	0.25	ms	1,10, 14,15	
Output Transient Rejection		$\left\|\frac{dVo}{dt}\right\|$	9	V_{PEAK} = 50 V, C_M = 1000 pF, C_L = 15 pF, R_M ≥ 1 MΩ	1000			V/µs	17	
Input-Output Transient Rejection		$\left\|\frac{dVio}{dt}\right\|$	9	V_{DD} = 5 V, $V_{I-O(PEAK)}$ = 50 V, R_L = 20 kΩ, C_L = 15 pF	500			V/µs	18	

*All typical values are at T_A = 25°C, $I_{F(ON)}$ = 10 mA, $V_{F(OFF)}$ = 0.6 V unless otherwise specified.

Typical Characteristics

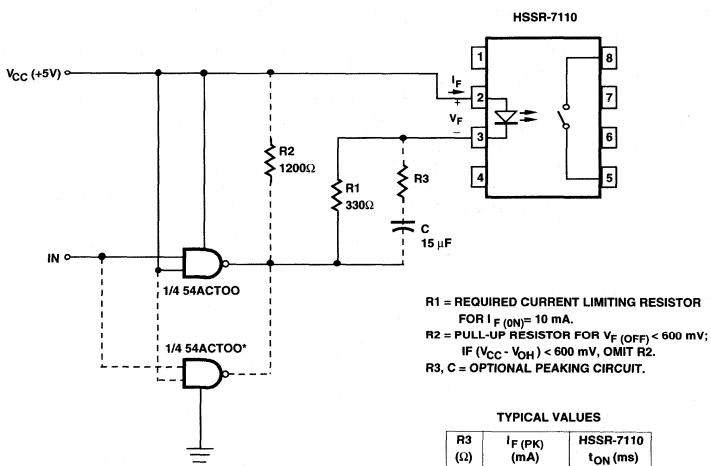
All typical values are at T_A = 25°C, $I_{F(ON)}$ = 10 mA, $V_{F(OFF)}$ = 0.6 V unless otherwise specified.

Parameter	Symbol	Test Conditions	Typ.	Units	Fig.	Notes
Output Off-Capacitance	$C_{O(OFF)}$	V_O = 28 V, f = 1 MHz	145	pF	16	
Output Offset Voltage	$\|V_{OS}\|$	I_F = 10 mA, I_O = 0 mA	2	µV	19	7
Input Diode Temperature Coefficient	$\Delta V_F/\Delta T_A$	I_F = 10 mA	-1.4	mV/C		
Input Capacitance	C_{IN}	V_F = 0 V, f = 1 MHz	20	pF		8
Input-Output Capacitance	C_{I-O}	V_{I-O} = 0 V, f = 1 MHz	1.5	pF		4
Input-Output Resistance	R_{I-O}	V_{I-O} = 500 V, t = 60 s	10^{13}	Ω		4
Turn On Time With Peaking	t_{ON}	I_{FPK} = 100 mA, I_{FSS} = 10 mA V_{DD} = 28 V, I_O = 800 mA	0.22	ms	1	6

Notes:

1. Maximum junction to case thermal resistance for the device is 15°C/W, where case temperature, T_C, is measured at the center of the package bottom.
2. For rating, see Figure 4. The output power P_O rating curve is obtained when the part is handling the maximum average output current I_O as shown in Figure 2.
3. During the pulsed R_{ON} measurement (I_O duration <30 ms), ambient (T_A) and case temperature (T_C) are equal.
4. Device considered a two terminal device: pins 1 through 4 shorted together and pins 5 through 8 shorted together.
5. This is a momentary withstand test, not an operating condition.
6. For a faster turn-on time, the optional peaking circuit shown in Figure 1 may be implemented.
7. V_{OS} is a function of I_F, and is defined between pins 5 and 8, with pin 5 as the reference. V_{OS} must be measured in a stable ambient (free of temperature gradients).
8. Zero-bias capacitance measured between the LED anode and cathode.
9. Standard parts receive 100% testing at 25°C (Subgroups 1 and 9). SMD and class H parts receive 100% testing at 25°C, 125°C and -55°C (Subgroups 1 and 9, 2 and 10, 3 and 11 respectively).

CAUTION: Maximum Switching Frequency – Care should be taken during repetitive switching of loads so as not to exceed the maximum output current, maximum output power dissipation, maximum case temperature, and maximum junction temperature.



R3 (Ω)	IF (PK) (mA)	HSSR-7110 tON (ms)
–	10 (NO PK)	2.0
330	20	1.0
100	40	0.48
33	100	0.22

Figure 1. Recommended Input Circuit.

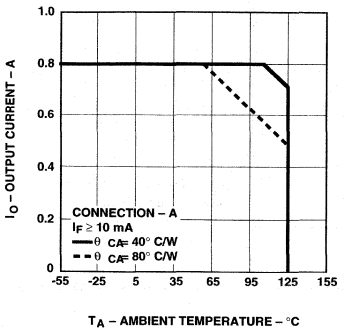


Figure 2. Maximum Average Output Current Rating vs. Ambient Temperature.

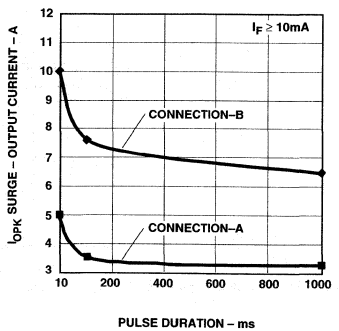


Figure 3. Single Shot (non-repetitive) Output Current vs. Pulse Duration.

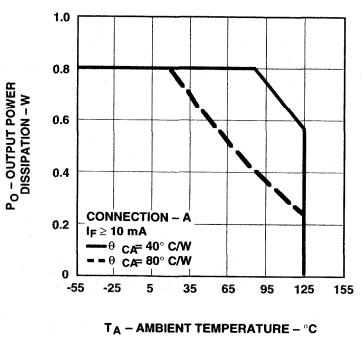


Figure 4. Output Power Rating vs. Ambient Temperature.

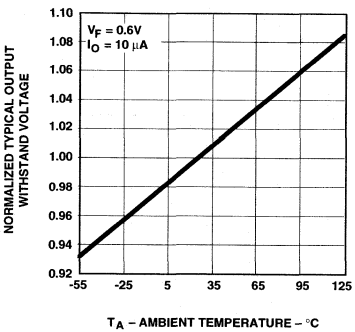


Figure 5. Normalized Typical Output Withstand Voltage vs. Temperature.

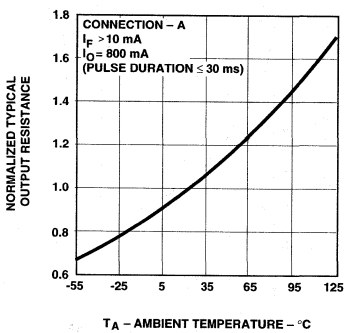


Figure 6. Normalized Typical Output Resistance vs. Temperature.

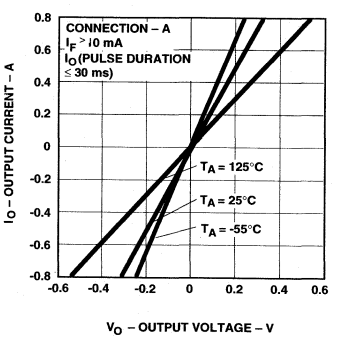


Figure 7. Typical On State Output I-V Characteristics.

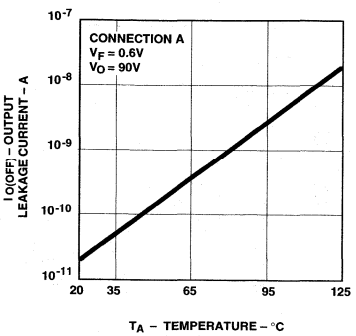


Figure 8. Typical Output Leakage Current vs. Temperature.

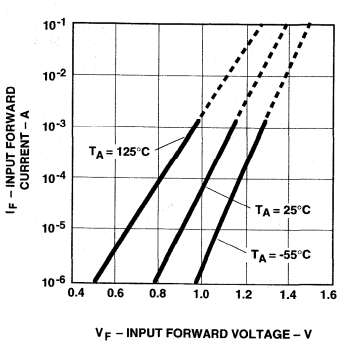


Figure 9. Typical Input Forward Current vs. Input Forward Voltage.

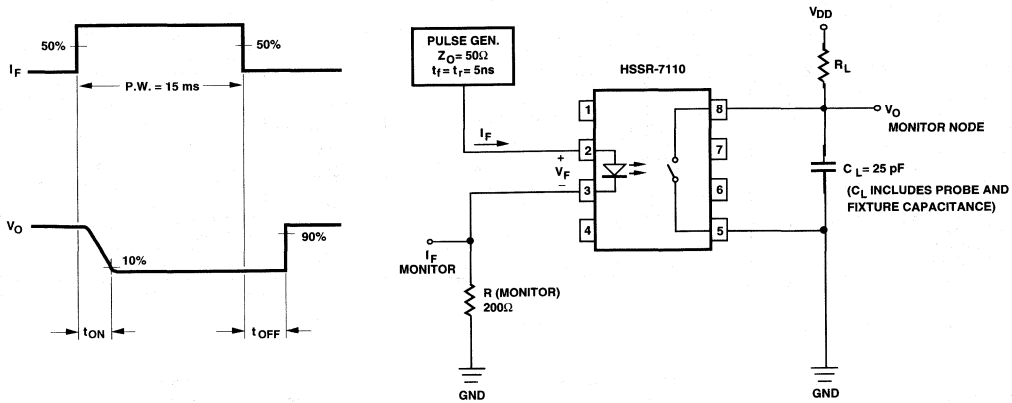


Figure 10. Switching Test Circuit for t_{ON}, t_{OFF}.

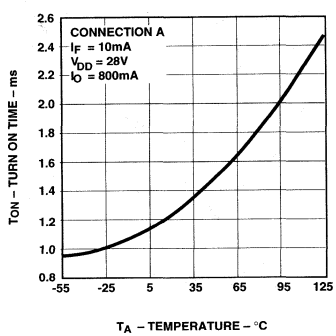


Figure 11. Typical Turn On Time vs. Temperature.

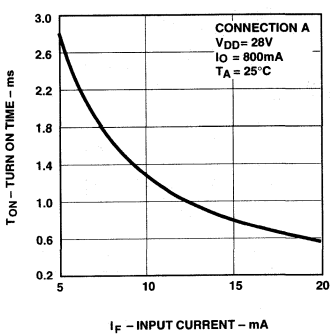


Figure 12. Typical Turn On Time vs. Input Current.

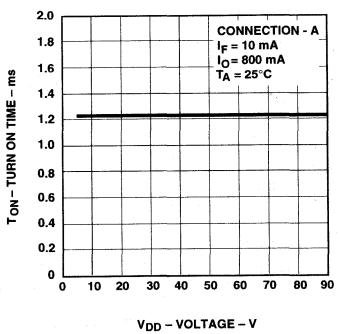


Figure 13. Typical Turn On Time vs. Voltage.

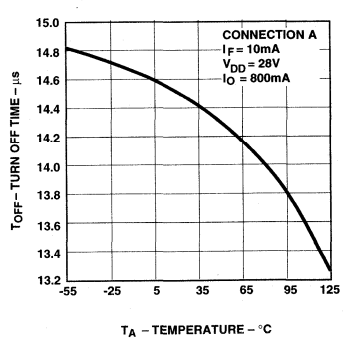


Figure 14. Typical Turn Off Time vs. Temperature.

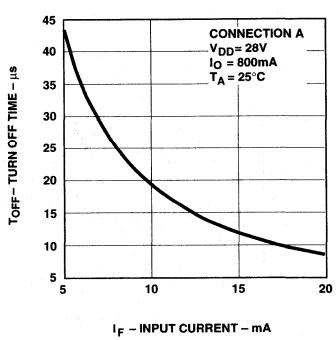


Figure 15. Typical Turn Off Time vs. Input Current.

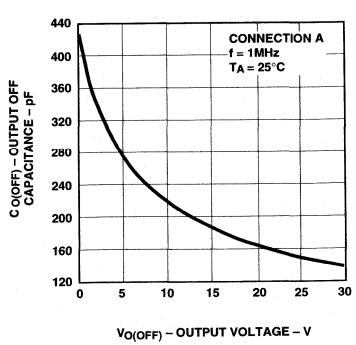
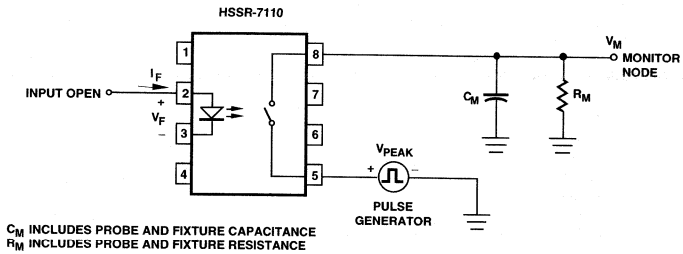


Figure 16. Typical Output Off Capacitance vs. Output Voltage.



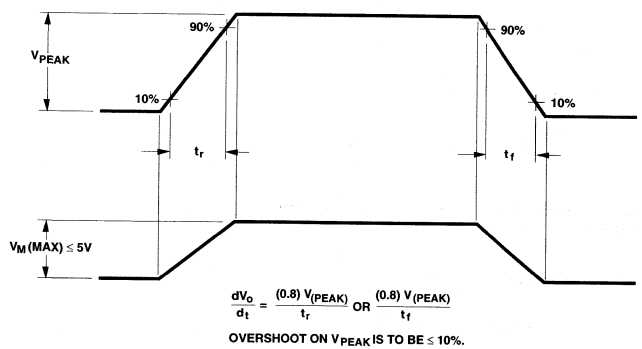


Figure 17. Output Transient Rejection Test Circuit.

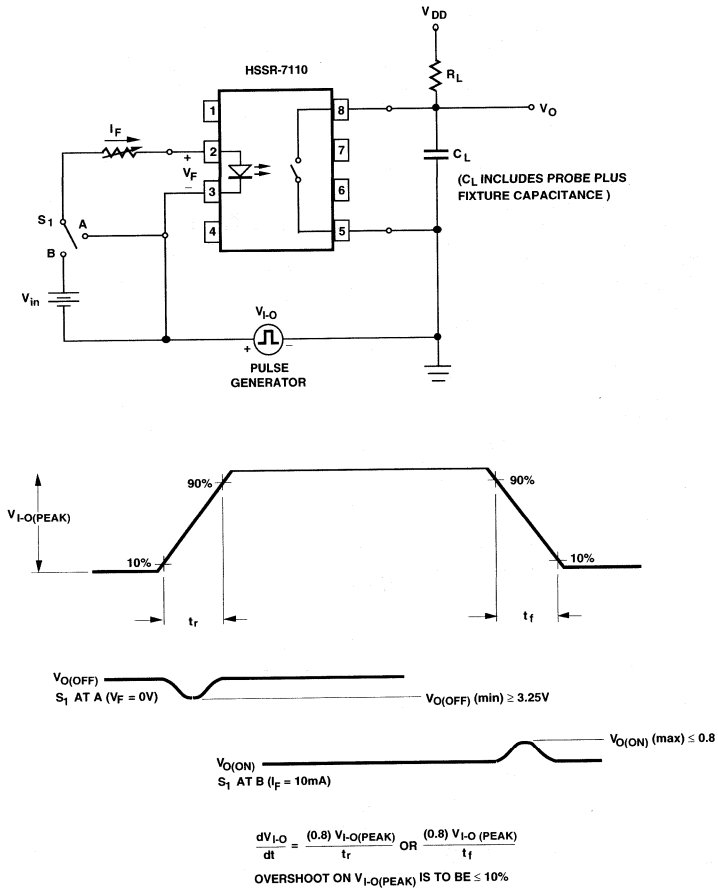


Figure 18. Input-Output Transient Rejection Test Circuit.

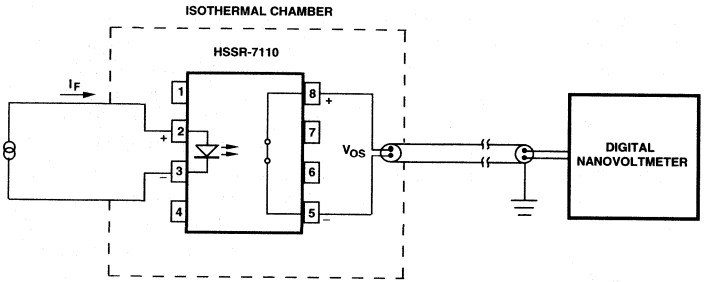


Figure 19. Voltage Offset Test Setup.

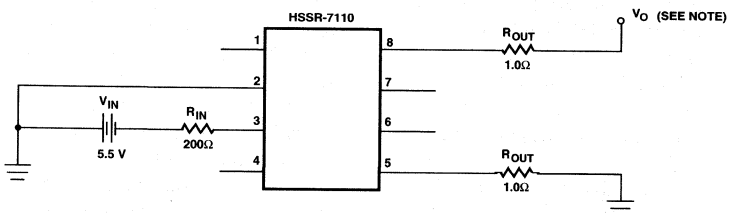
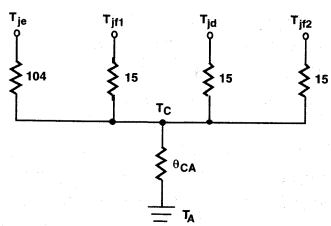


Figure 20. Burn-In Circuit.

NOTE:
IN ORDER TO DETERMINE V_{OUT} CORRECTLY, THE CASE TO AMBIENT THERMAL IMPEDANCE MUST BE MEASURED FOR THE BURN-IN BOARDS TO BE USED. THEN, KNOWING θ_{CA}, DETERMINE THE CORRECT OUTPUT CURRENT PER FIGURES 2 AND 4 TO INSURE THAT THE DEVICE MEETS THE DERATING REQUIREMENTS AS SHOWN.



T_{je} = LED JUNCTION TEMPERATURE
T_{jf1} = FET 1 JUNCTION TEMPERATURE
T_{jf2} = FET 2 JUNCTION TEMPERATURE
T_{jd} = FET DRIVER JUNCTION TEMPERATURE
T_C = CASE TEMPERATURE (MEASURED AT CENTER OF PACKAGE BOTTOM)
T_A = AMBIENT TEMPERATURE (MEASURED 6" AWAY FROM THE PACKAGE)
θ_{CA} = CASE-TO-AMBIENT THERMAL RESISTANCE

ALL THERMAL RESISTANCE VALUES ARE IN °C/W

Figure 21. Thermal Model.

Applications Information

Thermal Model

The steady state thermal model for the HSSR-7110 is shown in Figure 21. The thermal resistance values given in this model can be used to calculate the temperatures at each node for a given operating condition. The thermal resistances between the LED and other internal nodes are very large in comparison with the other terms and are omitted for simplicity. The components do, however, interact indirectly through θ_{CA}, the case-to-ambient thermal resistance. All heat generated flows through θ_{CA}, which raises the case temperature T_C accordingly. The value of θ_{CA} depends on the conditions of the board design and is, therefore, determined by the designer.

The maximum value for each output MOSFET junction-to-case thermal resistance is specified as 15°C/W. The thermal resistance from FET driver junction-to-case is also 15°C/W. The power dissipation in the FET driver, however, is negligible in comparison to the MOSFETs.

On-Resistance and Rating Curves

The output on-resistance, R_{ON}, specified in this data sheet, is the resistance measured across the output contact when a pulsed current signal (I_O = 800 mA) is applied to the output pins. The use of a pulsed signal (≤ 30 ms) implies that each junction temperature is equal to the ambient and case temperatures. The steady-state resistance, R_{SS}, on the other hand, is the value of the resistance measured across the output contact when a DC current signal is applied to the output pins for a duration sufficient to reach thermal equilibrium. R_{SS} includes the effects of the temperature rise of each element in the thermal model.

Rating curves are shown in Figures 2 and 4. Figure 2 specifies the maximum average output current allowable for a given ambient temperature. Figure 4 specifies the output power dissipation allowable for a given ambient temperature. Above 55°C (for θ_{CA} = 80°C/W) and 107°C (for θ_{CA} = 40°C/W), the maximum allowable output current and power dissipation are related by the expression $R_{SS} = P_O(max)/(I_O(max))^2$ from which R_{SS} can be calculated. Staying within the safe area assures that the steady-state junction temperatures remain less than 150°C. As an example, for T_A = 95°C and θ_{CA} = 80°C/W, Figure 2 shows that the output current should be limited to less than 610 mA. A check with Figure 4 shows that the output power dissipation at T_A = 95°C and I_O = 610 mA, will be limited to less than 0.35 W. This yields an R_{SS} of 0.94 Ω.

Design Considerations for Replacement of Electro-Mechanical Relays

The HSSR-7110 family can replace electro-mechanical relays with comparable output voltage and current ratings. The following design issues need to be considered in the replacement circuit.

Input Circuit: The drive circuit of the electro-mechanical relay coil needs to be modified so that the average forward current driving the LED of the HSSR-7110 does not exceed 20 mA. A nominal forward drive current of 10 mA is recommended. A recommended drive circuit with 5 volt V_{CC} and CMOS logic gates is shown in Figure 1. If higher V_{CC} voltages are used, adjust the current limiting resistor to a nominal LED forward current of 10 mA. One important consideration to note is that when the LED is turned off, no more than 0.6 volt forward bias should be applied across the LED. Even a few microamps of current may be sufficient to turn on the HSSR-7110, although it may take a considerable time. The drive circuit should maintain at least 5 mA of LED current during the ON condition. If the LED forward current is less than the 5 mA level, it will cause the HSSR-7110 to turn on with a longer delay. In addition, the power dissipation in the output power MOSFETs increases, which, in turn, may violate the power dissipation guidelines and affect the reliability of the device.

Output Circuit: Unlike electro-mechanical relays, the designer should pay careful attention to the output on-resistance of solid state relays. The previous section, "On-Resistance and Rating Curves" describes the issues that need to be considered. In addition, for strictly dc applications the designer has an advantage using Connection B which has twice the

output current rating as Connection A. Furthermore, for dc-only applications, with Connection B the on-resistance is considerably less when compared to Connection A.

Output over-voltage protection is yet another important design consideration when replacing electro-mechanical relays with the HSSR-7110. The output power MOSFETs can be protected using Metal oxide varistors (MOVs) or TransZorbs against voltage surges that exceed the 90 volt output withstand voltage rating. Examples of sources of voltage surges are inductive load kick-backs, lightning strikes, and electro-static voltages that exceed the specifications on this data sheet. For more information on output load and protection refer to Application Note 1047.

References:

1. Application Note 1047, "Low On-Resistance Solid State Relays for High Reliability Applications."
2. Reliability Data for HSSR-7110.

MOV is a registered trademark of GE/RCA Solid State.
TransZorb is a registered trademark of General Semiconductor.

MIL-PRF-38534 Class H and DESC SMD Test Program

Hewlett-Packard's Hi-Rel Optocouplers are in compliance with MIL-PRF-38534 Class H. Class H devices are also in compliance with DESC drawing 5962-93140.

Testing consists of 100% screening and quality conformance inspection to MIL-PRF-38534.

HEWLETT® PACKARD

Applications

The following application information is either published in this catalog or available from your local Hewlett-Packard sales office, authorized distributor, or representative.

Application Notes

AN 1036 – Small Signal Solid State Relays 1-607
AN 1043 – Common-Mode Noise: Sources and Solutions 1-616
AN 1046 – Low On-Resistance Solid State Relays 1-622
AN 1074 – Optocoupler Input-Output Endurance Voltage 1-636
AN 1078 – Designing with Hewlett-Packard Isolation Amplifiers 1-642
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Abstracts*

AN 951-1 Applications for Low-Input-Current, High-Gain Optocouplers 1-662
AN 951-2 Linear Applications of Optocouplers 1-662
AN 1004 Threshold Sensing for Industrial Control Systems with the HCPL-3700 Interface Optocoupler 1-662
AN 1018 Designing with the HCPL-4100 and HCPL-4200 Current-Loop Optocoupler 1-662
AN 1023 Radiation Immunity of Hewlett-Packard Optocouplers 1-663
AN 1024 Ring Detection with the HCPL-3700 Optocoupler 1-663
AN 1047 Low On-Resistance Solid-State Relays for High-Reliability Applications 1-663
AN 1058 Power Transistor Gate/Base Drive Optocouplers 1-663
AN 1059 High-CMR Isolation Amplifier for Current-Sensing Applications 1-663
AN 1094 Regulatory Guide to Isolation Circuits 1-664

*Complete Application Note is available from your HP sales office.

Small Signal Solid State Relays

Application Note 1036

Introduction

Traditionally, isolated control of signal paths has been provided by the Electro-Magnetic Relay (EMR). The purpose of this application note is to present an alternative, the Solid State Relay (SSR), and to describe some of the ways in which the SSR can be used.

An SSR, as the name implies, is entirely composed of solid state devices—no mechanical movement takes place in its operation. An LED on the control side converts the electrical input into optical power. On the contact side, the optical power is converted back into an electrical signal that supplies power for a switch driver to energize a solid state switch. In some classes of SSR a small fraction of the power from the circuit being switched is used to operate the solid state switch (e.g. thyristor), but in others the power for switch operation comes exclusively from the optical signal (e.g. HSSR-8200) making the contacts completely passive.

Some of the relative merits of SSRs and EMRs are immediately seen in the schematic comparison of Figure 1. On the CONTROL side, the EMR presents an inductive load that may suffer from or radiate magnetic disturbances; the collapse of the magnetic field, when it is de-energized, may produce transient voltages requiring suppression. The SSR control is simply an LED that neither suffers from nor causes magnetic disturbances; and the low voltage change at turn-on or turn-off seldom requires transient suppression. While the EMR can usually be energized by either polarity of voltage and current, the SSR requires current in the direction shown. Either-polarity operation of the SSR is easily accomplished with a bridge rectifier.

On the CONTACT side, SSRs are of three general classes: ac only, dc only, and bi-directional (ac or dc). Bi-directional types, like the EMR, can pass current in either direction when closed, and can withstand voltage of either polarity when open. In some types of EMR, a single control circuit can operate more than one set of contacts, and these contacts could be form A (normally open), form B (normally closed), form C (double throw), or any combination of these options. Most SSRs offer form A contacts but form B and form C can also be made. Also, in most SSRs a single control operates a single set of contacts, but multi-function operation of SSRs can be achieved easily with simple circuits, as shown later.

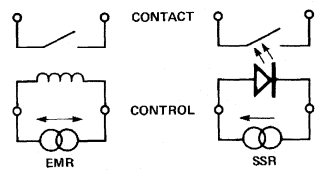

Figure 1. Schematic Comparison of EMR and SSR.

The IMPORTANT differences between SSRs and EMRs do not appear schematically, but functionally. In SSRs there are no mechanical movements and consequently they enjoy four distinct advantages over EMRs:

1. No contact bounce—closure is always clean
2. No problems with shock, vibration, or mounting position
3. No wearout mechanism limiting the number of operations
4. No minimum contact "wetting" current

In EMRs, the contact bounce problem can be addressed with mercury-wetted contacts, but

this may impose a restriction on mounting orientation relative to gravity; SSRs can be mounted and operated in any position. In environments of heavy shock and vibration, SSRs provide clean operation—unless the mechanical abuse causes physical damage. A particularly important advantage of SSRs is the unlimited number of operations. EMRs typically function reliably for only about one billion operations; at 1,000 operations per second such EMRs are good for only two weeks and should then be replaced.

Summary of Characteristics

Some features of the SSR from Hewlett-Packard, the HSSR-8200, can be described relative to the circuit diagram in Figure 2 and the approximate equivalent circuit of Figure 3.

First, notice the construction is in 8-pin DIP size, but of course only four pins are needed. Hewlett-Packard uses the four corner pins 1, 4, 5, and 8, to make handling easier, especially by machinery for automatic insertion.

Next, consider the control side. Polarity is defined in Figure 2.

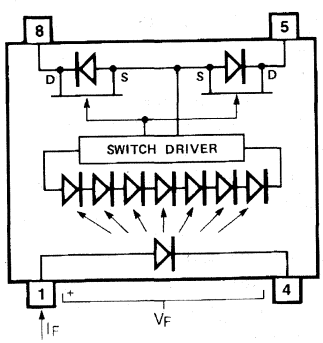

Figure 2. Circuit Diagram of HSSR-8200.

The HSSR-8200 is energized (contacts closed) with I_F as low as 1.0 mA at V_F only slightly more than 1.0 V (some SSRs may have higher I_F and V_F requirements). In some applications it may be desirable to operate with higher current, but since the current varies exponentially as the voltage this would require only a slightly higher voltage. Operation at higher current causes faster closure of the contacts. and reduces $R_{(ON)}$ slightly; it also increases the offset voltage, $V_{O\ (OS)}$. To de-energize the SSR (contacts open) requires a lower current, but a more reliable assurance of the de-energized condition is to make the forward voltage less than 0.8 V. A complete switching of the contacts from open to closed requires a voltage change usually less than 0.4 V, and seldom more than 0.9 V.

In the energized condition, optical radiation from the LED is converted by a photodiode array into sufficient voltage and current to operate the SWITCH DRIVER (Fig. 2) and also to drive the gate-source electrodes of the two FETs. It is important to notice here that all the power to operate the switch comes from the photodiode array—no power is required from the circuit being operated by the switch.

The contact side appears complicated, but in most applications it is possible to ignore some or all of the extraneous circuit elements. It is therefore worthwhile to give some thought to the equivalent circuit of Figure 3, and check the data sheet values to see if they can indeed be ignored. In many situations the values of $R_{(ON)}$ are so low and $R_{(OFF)}$ so high that they can be ignored, and the same may

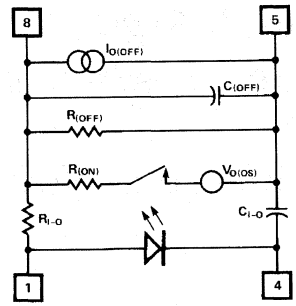

Figure 3. Approximate Equivalent Circuit of HSSR-8200.

be true of the other parameters as well. For the HSSR-8200, $R_{(ON)}$ is less than 0.00025 megohms and $R_{(OFF)}$ is more than 50,000 megohms; consequently, in circuits having few-megohms impedances they may be regarded as short and open, respectively, with error of only a few parts per million. For circuits having variable impedances, the ratio of $R_{(OFF)}$ to $R_{(ON)}$ is significant as it relates to the ratio of impedances, relative to which the error may be ignored.

The HSSR-8200 is distinguished relative to other SSRs and mechanical relays by its high speed of operation, low offset voltage $V_{O\ (OS)}$, low offset current $I_{O(OFF)}$, and small value of off-capacitance.

Where very low signals are to be switched, $V_{O\ (OS)}$ and $I_{O\ (OFF)}$ should be considered. With voltage applied to the open contacts, part of the resulting current $I_{O\ (OFF)}$ is flowing in $R_{O\ (OFF)}$, and part is the reverse current in whichever of the two diodes in the contact circuit (see Figure 2) is reverse biased. When the LED is turned on and the switch closes, the magnitude of $V_{O\ (OS)}$ initially rises, then falls as heat from the LED spreads through the contact

circuit and largely balances out thermocouple voltages. The data sheet values for $V_{O\ (OS)}$ are taken at peak, occurring a few seconds after the control LED is energized, and the polarity is consistent.

Although $C_{(OFF)}$ is extremely small, at 1,000 Hz the reactance of $C_{(OFF)}$ is below 100 megohms; consequently, to switch signals having frequencies even as low as the audio range it may be necessary to employ special techniques to deal with $C_{(OFF)}$. Such techniques might be as simple as lowering the circuit impedances, but could also require series-shunt combinations of form A and form B switching, or applying neutralization.

Another consideration is the range of circuit currents with which the SSR contacts can be used. At the low end, there is the leakage current, $I_{O\ (OFF)}$. At the high end, the current may be limited only by the maximum rating of $I_{O\ (ON)}$, (40 mA for HSSR-8200), or it may be limited by the linearity of $R_{(ON)}$. Notice in Figure 2 that the contact consists of two FETs in anti-series to provide bidirectional symmetry. Across each FET there is a source-to-drain diode. Since each FET has a channel resistance approximately equal to half $R_{(ON)}$, this diode begins to turn on when the contact current rises to a level at which the voltage drop across the contact is approximately two diode drops. Above this level, the dynamic resistance has approximately half the value it has at contact currents below this level.

In the de-energized condition the open contacts of the HSSR-8200 can withstand voltages up to 200 V of either polarity. In some applications these contacts may be exposed to harmfully high transient voltages. The FET drain electrodes may require that external means be provided to protect them from such transients. Similarly, in the energized condition there is a limit on how much current can be permitted to flow through the closed switch without damaging it.

Between the control side and the contact side are the unavoidable parasitics $R_{I\text{-}O}$ and $C_{I\text{-}O}$ seen in Figure 3. Having a value of more than a million megohms, $R_{I\text{-}O}$ can usually be ignored. $C_{I\text{-}O}$ can usually be disregarded with respect to large transient voltages relative to the contact circuit. Transients with sufficient amplitude could couple enough charge through $C_{I\text{-}O}$ to cause a temporary improper condition of the contacts. However, as seen in the data sheet, the values given for Control-Contact Transient Rejection are so high that it is extremely unlikely that common-mode transients of such magnitude could occur. Even if large transients are not present, there could be a situation in which the control and contact circuits have line voltages be tween their common points. At 115 V rms, 60 Hz, a capacitance of 1.0 pF couples a current of approximately 50 nA rms, and in a 1-megohm load this would produce a 50-mV rms "hum" voltage.

Applications Suggestions

In the arrangements suggested here, only the contacts and their intended closure sequences are shown. Later on, the details of how to obtain such sequences are described.

The signals $E_1 \ldots E_n$ in Figure 4 might come from sources in which the levels are too low to permit processing directly; that is, they may require amplification or impedance conversion. A/D converters and amplifiers are costly, so one motivation for multiplexing is to have the amplifier cost shared among a number of sources. Another, and perhaps more important, consideration is the desirability of having precisely the same gain applied to each of several signals so that ratios of the amplified levels $V_1 \ldots V_n$ will relate to ratios of their unamplified counterparts, $E_1 \ldots E_n$.

Figure 5a shows a configuration that takes advantage of the low offset and negligible nonlinearity of the closed contacts. Without

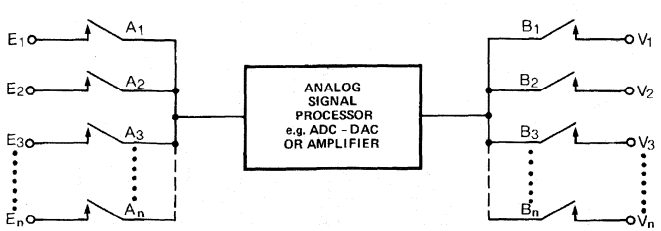

Figure 4. Multiplexing and Demultiplexing.

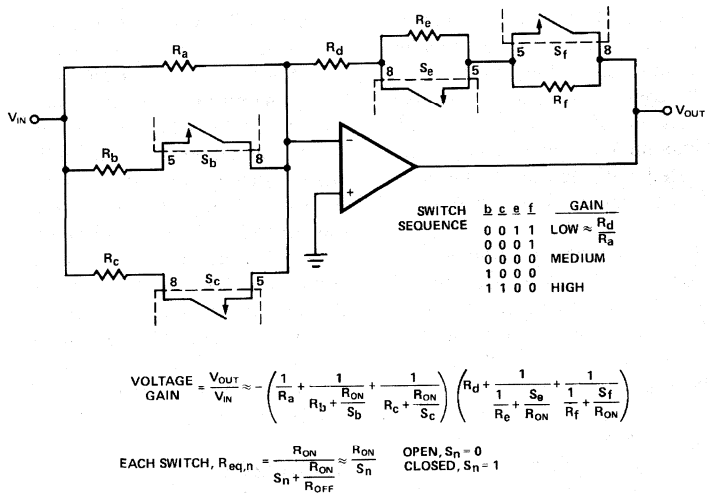

Figure 5a. Inverting Amplifier Gain Switching.

encountering serious error at either a high or a low signal level this arrangement can perform inverting gain selection over a four-decade range. Another possibility is shown in Figure 5b; here On-Resistance of the closed contacts is even less significant than in the arrangement of Figure 5a.

Where speed of operation is unimportant, the SSR can be operated at a much lower control current than is required for usual applications. This would be useful in an application such as the battery-powered alarm system shown in Figure 6. Here the alarm circuit, which would be a relatively heavy drain on the battery, is disconnected until the sensor circuit energizes the control circuit of the SSR. At that point, as the contacts begin to close, the control circuit current is augmented, and latches the alarm.

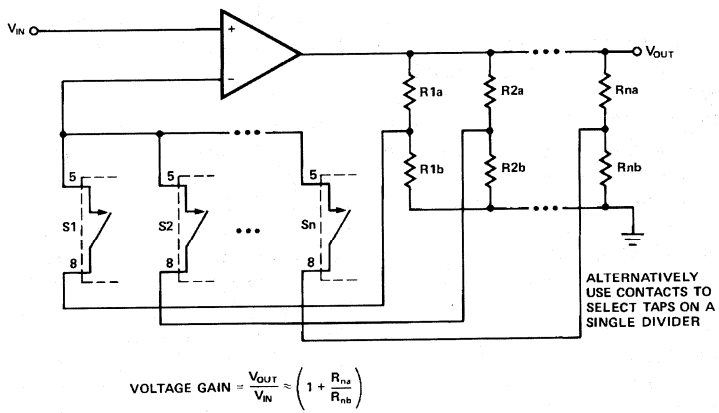

Figure 5b. Non-Inverting Amplifier Gain Switching.

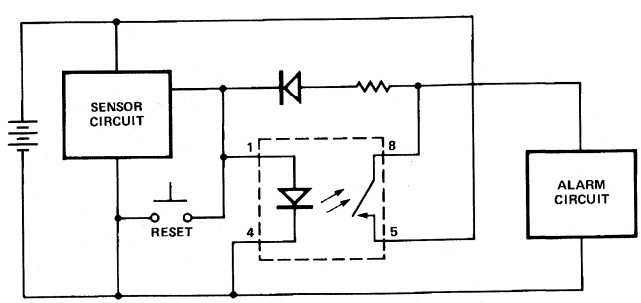

Figure 6. Low-Control-Current Battery Saver.

Control Drive Circuit Suggestions

Operation of the HSSR-8200 control requires a forward current for the energized (ON) condition to close the contacts; for the de-energized (OFF) condition the forward voltage must be less than 0.8 volts. $R_{(ON)}$ is specified for forward current of 1.0 mA, and operation at higher forward current does not reduce $R_{(ON)}$ very much. On the other hand, increasing the control current increases the offset voltage – almost linearly. The only benefit from operation at control current greater than 1.0 mA is

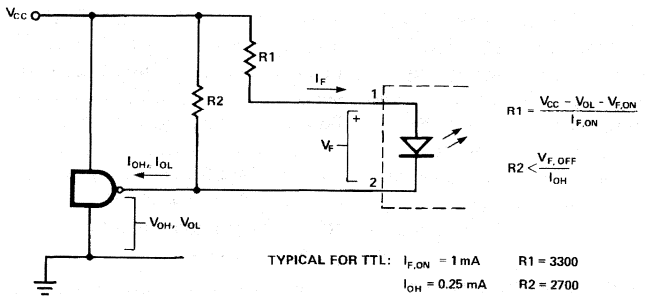

Figure 7. Logic-Driven Control Circuit.

the better-than-linear reduction in turn-ON time; there is also a slight reduction in turn-OFF time. A simple circuit for obtaining the desired ON current and OFF voltage is shown in Figure 7. The logic series used can be almost anything; any of the TTL logic family, open-collector or totem pole, will work in the arrangement shown. The same is true for CMOS, provided only that the current-sinking capability is adequate. R1 sets the level of forward current, independent of R2. The purpose of R2 is to bypass logic-high leakage current with sufficiently small voltage drop to ensure an OFF-voltage less than 0.8 V. In some cases R2 is not required; some logic outputs have internal pullup circuits that are able to satisfy the OFF-voltage requirement without the external pull-up provided by R2. With open-collector TTL outputs, R2 is always required because the HSSR-8200 can actually be operated (though at higher ON resistance) with just a few microamperes of forward current.

In computing the resistor values for this and other drive circuits a useful approximation for the relationship between the forward voltage and the forward current is given by: The circuit in Figure 7 is basically a series-drive type because the active current is

$$V = Va + (dV/dT)*(25 - T) + Vb*\log(I)$$

V in volts, T in degrees Celsius, I in milliamperes

where $1.1 < Va < 1.5$ volts

$0.07 < Vb < 0.12$ volts

$0.0015 < (dV/dT) < 0.002$ volts/degree Celsius

switched by a device in series with the LED. As will be seen later, this type of drive circuit has a great deal of flexibility in achieving other design objectives. It can be used with TTL having either active pull-up (totem-pole) output or open-collector output. If open collector TTL is available for driving the control, a simpler alternative is the shunt switching of Figure 8. It requires only a single resistor, and the logic-low voltage does not influence the ON current. The OFF voltage requirement is inherently satisfied by the logic-low voltage.

As mentioned earlier, turn-ON time is influenced by the level of forward current. As forward current is increased, the turn-ON time becomes shorter. However, it may not be desirable to operate with a high steady-state forward current because that would increase the offset voltage due to heat transferred from the LED control to the

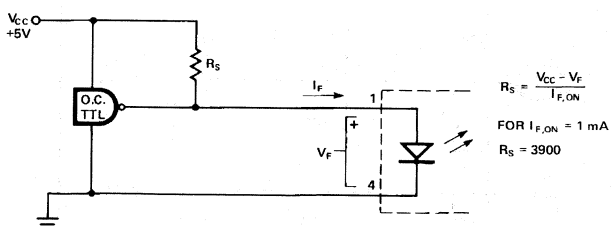

Figure 8. Shunt-Driven Control.

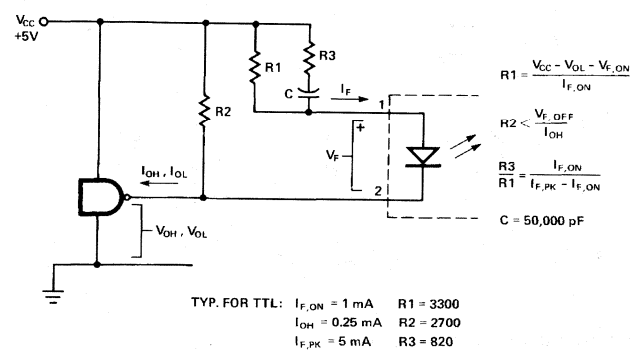

Figure 9. Peaking to Shorten Turn-On Time.

contact side. In situations requiring fast turn- ON but low offset, a peaking circuit can be used, like that in Figure 9. When the logic output is high, R2 assures that the current through the LED is so small that the capacitor is completely discharged. Then when the logic output goes low, there will be a surge of current through both R1 and R3 until the capacitor is charged to the voltage across R1, and thereafter the steady-state current is set by R1 only. Thus peaking permits fast turn-ON as well as low steady-state current (low offset in the contact circuit).

Closing the contacts requires charging the capacitances in the SWITCH DRIVER circuit (Figure 2). This charge is the time-integrated photocurrent from the photodiode array, and translates into a certain amount of charge that must pass through the LED (of the order of 200 nanocoulombs). That amount of charge is set by the value of the peaking capacitor and the voltage across R1. For this reason it is not necessary to change the value of the capacitor when other (higher) values of peak current are desired; it is necessary only to reduce the value of R3 and make sure that the logic output is capable of sinking the higher current.

Figure 10 shows a combination of series-shunt drive. The column drivers do the series switching and the row drivers operate in shunt mode. With the ENABLE input high, selection is made of desired row and column (high true) but the selected LED remains OFF until the ENABLE goes low. This provision is necessary to ensure "break-before make" operation of the contacts. With turn-OFF time longer than turn-ON time, there must be a "dead" time of 0.2 milliseconds or more to prevent overlapping contact closure. The values of R1 and R2 are selected as described for the circuits of Figures 7 and 9, and, if desired, the R3,C peaking may be added in parallel with each R1.

The matrix arrangement in Figure 10 is worth considering only if a very large number of switches are to be selectively operated. To make a selection from a smaller number of switches, a much simpler circuit is shown in Figure 11, where a decoder/demultiplexer IC is used. The values of the resistors R1 and R2 are NOT computed in the same way as for the circuits of Figures 7 and 9. Here the principle is to select a ratio R1/R2 such that the forward voltage across the LED is less than 0.8 volts when the 74154 output is high, then establish this ratio with resistor values small enough to allow adequate forward current when the 74154 output is low. Actual selection of resistor values is most easily done by first selecting R1 with a large margin in the inequality to provide a wide range for selection of R2 to fit within the two sided inequality. If peaking is desired on any or on all three of the anode bus lines, the R3,C peaking circuit may be added with no effect on the choice of R1 and R2 values. The peaking circuit may be connected either to V_{CC} or to ground. An important concern is operation of the ENABLE inputs of the 74154 decoder. Both of these must be low to make the output (selected by the address) go low. It is recommended that at least one of the ENABLE inputs be

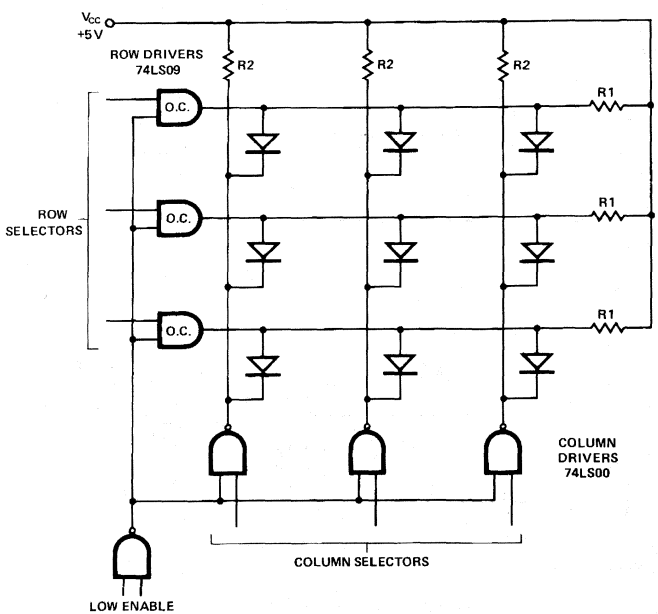

Figure 10. Matrix-Driven Control Circuit.

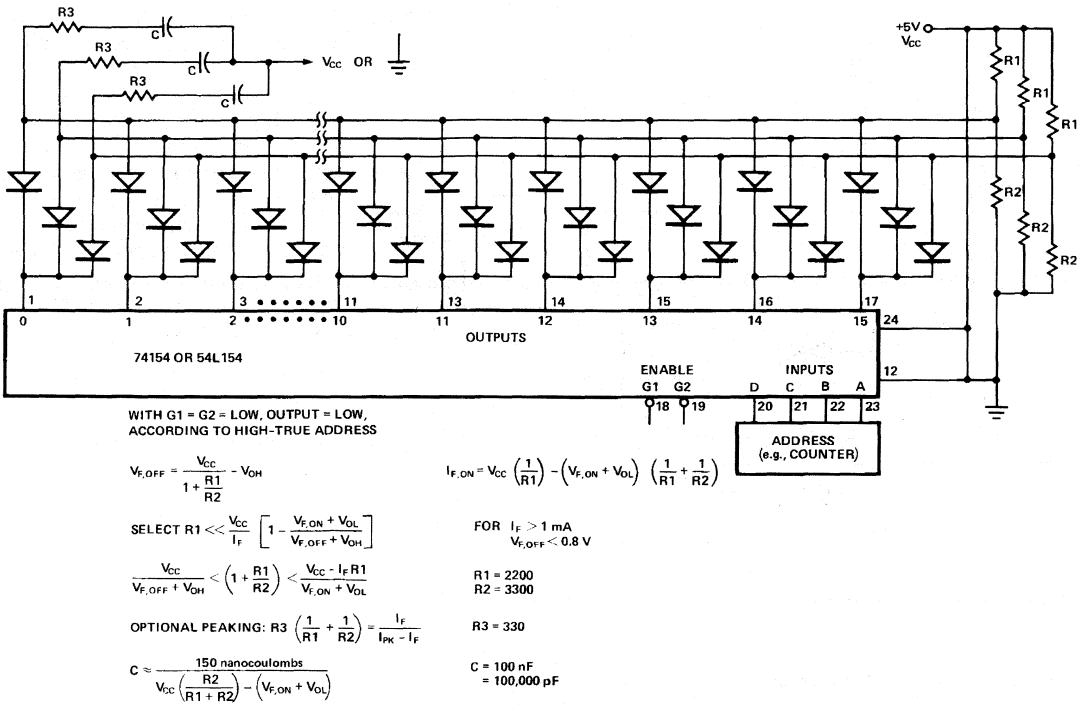

Figure 11. Control Circuit for 16-Channel Multiplexer.

made high for an interval of 0.2 milli- seconds or more, following address selection, to prevent overlapping contact closure.

In Figure 11 (also in Figure 10) the length of time that any individual contact is held closed may depend on how fast the contact circuit can respond to the contact closure. It depends also on the offset voltage property of the HSSR-8200 as a function of time following application of control current, shown in Figure 13. At the initial closure, heat from the LED produces a thermal gradient in the contact drive IC, causing the offset voltage to begin increasing (negative polarity); after a few seconds, the offset voltage reaches a peak and then decreases as the thermal gradient disperses. The polarity of the offset voltage is consistent, however, so two sets of contacts in a differential arrangement will cause the offset voltage (either in steady state or during the transient) to be partially cancelled. For this reason the contacts should be arranged as in Figure 12, and the control LEDs should be driven in triplets, as in Figure 11. Two of the contacts perform differential signal selection while the third connects the "guard" driver to the appropriate shield.

Overvoltage Protection

In some applications there is a possibility that the contacts may be exposed to destructively high voltages. One such situation is partially illustrated in Figure 12, where the HSSR-8200 is being used to select one set of inputs from among several and present this set to the Signal Processor. The differential inputs (H and L) are shielded by a guard (G) driven by the Processor. When open, the

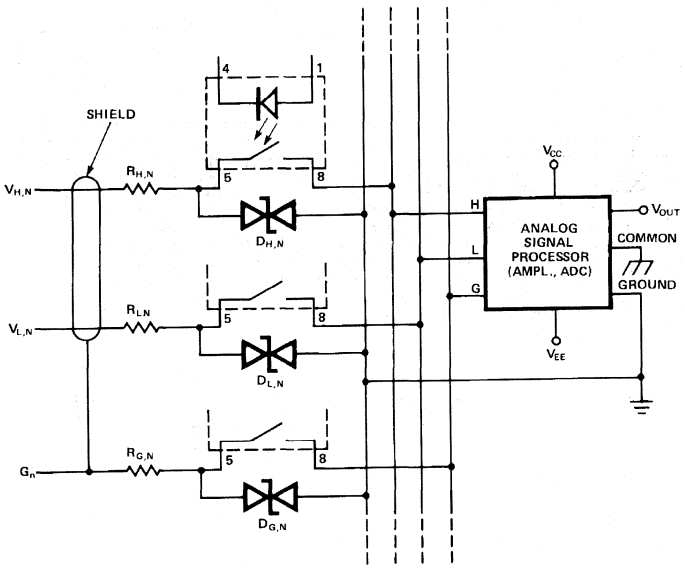

Figure 12. Contact Circuit for One Triplet of Several in Multiplexing.

contacts of the HSSR-8200 can withstand 200 volts, positive or negative. Protection against damage due to exceeding 200 volts is provided by the breakdown devices shown. These devices may be either General Semiconductor TransZorbs™ or GE/RCA MOVs™ (Metal Oxide Varistors). They break down and conduct heavily when the voltage across them rises above a design level. As indicated by the symbol, the breakdown voltage is of either polarity, but single-polarity devices are also available. TransZorbs can tolerate more blows but MOVs have lower shunt capacitance. Both types fail "short" so protection does not fail even if operation does. The series resistors must be large enough to limit surge current to values specified for the protection devices.

Selection of the breakdown voltage of the protection devices may depend on the particular situation. To see this more clearly consider Figure 13, illustrating just one of the three signal buses and the contacts connecting it to one of several signal sources. If one of the contacts is closed, the voltage appearing across the open contacts is the DIFFERENCE between the voltage at the closed contact and the voltage at the open contact. Consequently, if voltages of either polarity are allowed at the inputs, the breakdown device must be selected to protect at less than HALF the withstand voltage rating of the open contacts, and dual-polarity breakdown is required. On the other hand, if the voltages at the inputs are all of the same polarity, a unipolar breakdown device can be used up to the FULL withstand voltage of the open contacts.

For either polarity of protection, a series resistor should be used to limit the current to the level for which the protection device is rated. The relationships between input voltages and the characteristics of the breakdown device and its series resistance are summarized in Figure 13.

TM MOV is a registered trademark of GE/RCA Solid State

TransZorb is a registered trademark of General Semiconductor

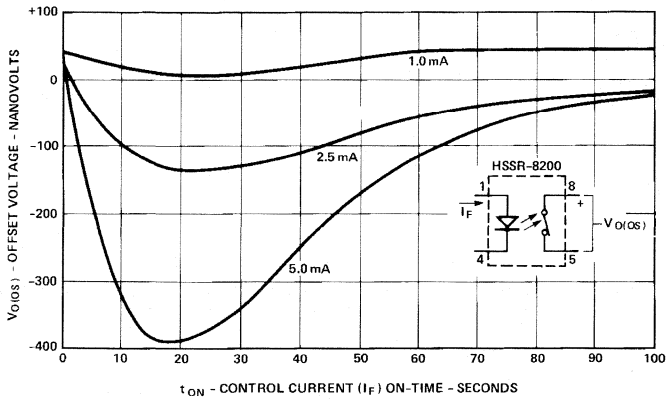

Figure 13. Typical Contact Offset Voltage.

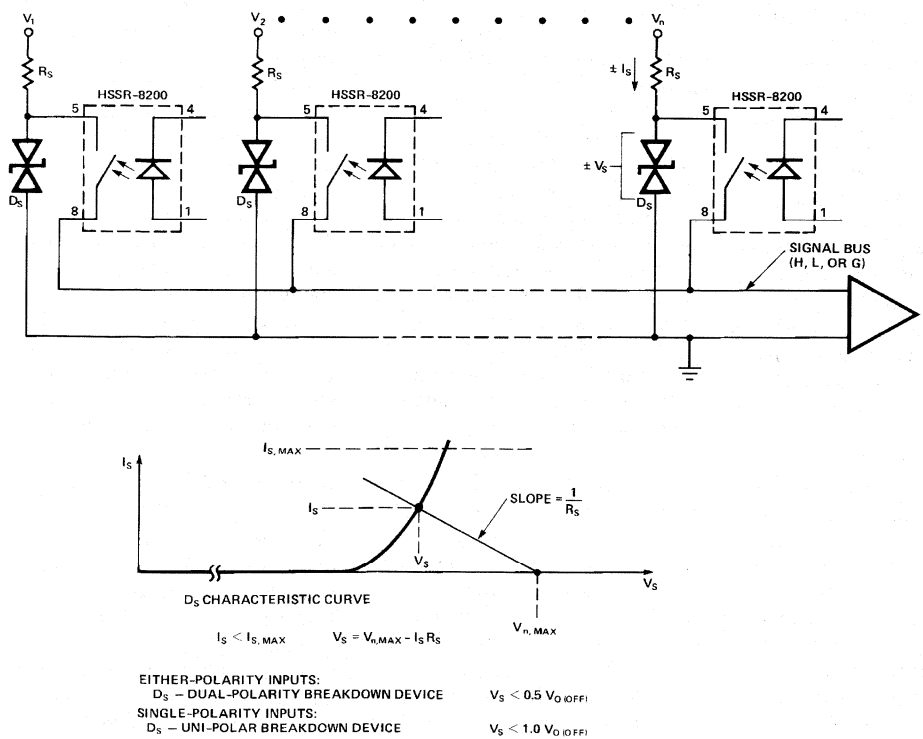

Figure 14. Over-Voltage Protection in Multiplexer Application.

HEWLETT® PACKARD

Common-Mode Noise: Sources and Solutions

Application Note 1043

Introduction

Circuit designers often encounter the adverse effects of common-mode noise on a design. Once a common-mode problem is identified, there are several ways that it can be resolved. However, common-mode interference manifests itself in many ways; therefore, it may be hard to determine whether or not this is the cause of your circuit's misbehavior. If a system is connected and running but only produces erroneous data, common-mode noise may be the reason. This application note describes sources of common-mode problems, presents possible solutions, and concludes with a description of Hewlett-Packard's approach to addressing common-mode noise.

Common-mode noise problems exist in many electrical circuits. Any device or system with either its input or its output floating may be susceptible to common-mode noise. A common-mode signal is a signal that appears common to either set of floating points. It can be either ac or dc. The overall effect is that excessive common-mode noise causes spurious results at the output, disrupting safe, precise measurements.

Common-mode interference is sometimes inherent in a system design, but most often it is inductively or capacitively coupled from an external source. A good example of common-mode noise is the 60-Hz signal induced on a pair of wires by nearby power lines. In this case, the noise signal is "common" to each of the two wires. An inherent common-mode signal is one in which the circuit itself causes the interference. An example of this is the half bridge power inverter. In such an application, the driver circuits of the power transistors rise and fall hundreds of volts with respect to signal ground in only tens of nanoseconds.

Definition of CMR

Common-mode rejection (CMR) is a measure of the ability of a device to tolerate common-mode noise. It can be specified in several ways. The common-mode specification is sometimes given as CMV, or common-mode voltage. This value specifies the maximum common-mode voltage amplitude that can be applied to the device without causing a problem. The CMR of analog devices is commonly specified in dB as the ratio of the differential-mode gain to the common-mode gain. This specification is often called the common-mode rejection ratio, or CMRR. Another way to specify CMR is as a common-mode transient rejection (CMTR). CMTR describes the maximum tolerable rate-of-rise (or fall) of a common-mode voltage. It is usually given in volts per microsecond. In order to be complete, the CMTR should also include the amplitude of the common-mode voltage that can be tolerated. Common-mode interference that exceeds the maximum specification might result in abnormal voltage transitions or excessive noise on the output signal.

Sources of CMR Problems

Common-mode signals can originate from several different sources. A full-bridge power inverter, shown in Figure 1, is a good example of an application that can exhibit large amounts of common-mode noise. Full bridge inverters are commonly found in motor-speed control and

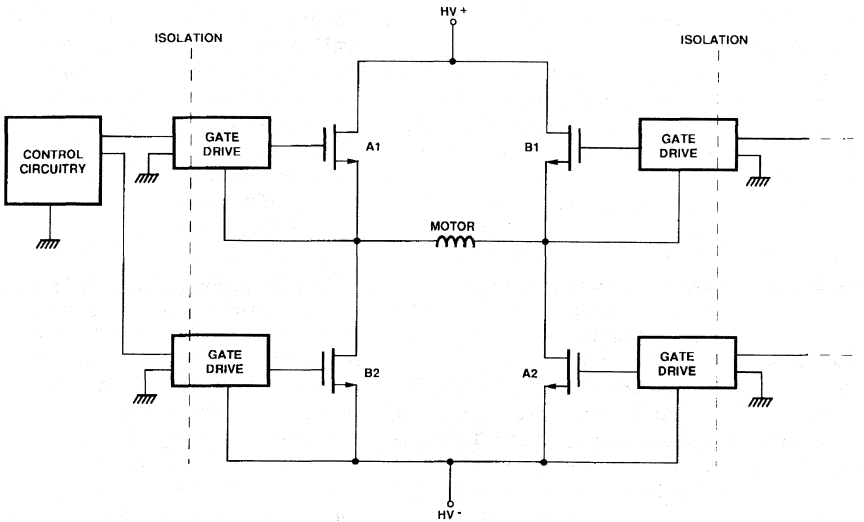

Figure 1. Full-Bridge Power Switch Configuration.

switching power supply applications. The power inverter is generally used to produce an ac output from a dc input. In a full-bridge inverter application like that shown in Figure 1, the source of one set of transistors (A1, B1) is attached to the drain of a second set of transistors (A2, B2). When transistor set A turns on, set B turns off. Current flows from the positive supply, through transistor A1, through the load, and through transistor A2. When set B turns on, set A turns off, and the polarity of the current through the inductive load is reversed.

How does this operation create a common-mode problem? The input of each gate drive circuitry is referenced to the ground of the digital control circuitry; the output common, on the other hand, is floating and referenced to the source of its associated power transistor. The floating common of the gate drive circuitry rapidly switches between the positive and negative power supplies. This rapid switching creates a large voltage swing across the input to output of the gate drive circuitry. As an example, a half bridge circuit that switches between +250 V and -250 V in 100 ns creates a common-mode transient signal of 5000 V/µs with an amplitude of 500 V (see Figure 2). The device that carries the control information to each MOSFET must be able to withstand this level of common-mode interference. Although this example may seem

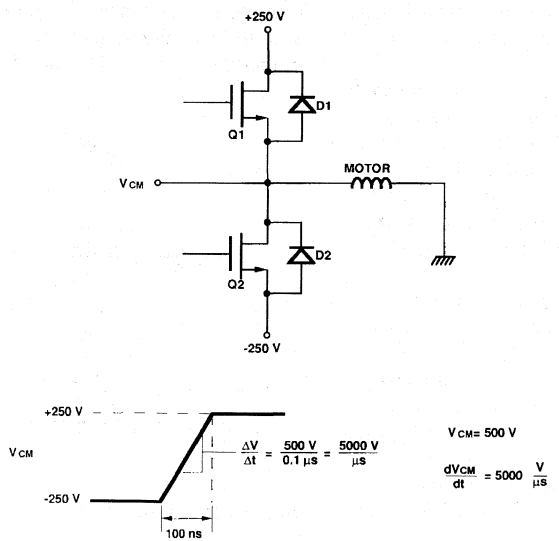

Figure 2. Half-Bridge Example.

extreme, it is a fact that engineers continue to use faster switching transistors to increase efficiency. Power MOSFETs, for example, are commonly used in power inverter applications because they are capable of high frequency, high power switching. The fast switching speeds of the transistors, however, can generate common-mode signals with very high rates of change (dVcm/dt).

The common-mode signal rate-of-rise can also be affected by the reverse recovery characteristics of diodes D1 and D2 in the power inverter shown in Figure 2; these diodes are often referred to as "free-wheeling" diodes. If the inverter is driving an inductive load, such as a motor winding, these diodes may become forward biased during the normal operation of the inverter. For example, assume that Q1 of Figure 2 is turned on, Q2 is off, and current is flowing through Q1 and into the inductive load. When Q1 turns off, voltage Vcm swings in the negative direction until diode D2 becomes forward biased and conducts the load current.

It is when Q1 turns back on that very high rates of rise can be generated. In extreme cases, when Q1 turns on again, the rate of rise of voltage Vcm is determined by how quickly diode D2 recovers from forward conduction. The voltage and current waveforms shown in Figure 3 illustrate what happens when Q1 turns back on. As Q1 starts to turn on, the current through D2 begins to decrease. The current through D2 continues to decrease and actually goes negative for a short time due to the storage of minority carrier charge in its junction. It is when this charge has been depleted that D2 begins to turn off and Vcm begins to increase. If D2 turns off very quickly, Vcm can also rise very quickly, generating a large common-mode transient signal.

High electrical noise levels can also contribute to common-mode problems. A significant amount of electrical noise is found in industrial environments as a result of the starting and operating of electric motors. When a large motor first turns on, it normally requires a large inrush current to reach operating speed. This large current spike can generate a significant amount of electrical noise in its own and nearby systems. Even the electric motors in a typical household environment vary in size from fractional to low integral horsepower units and are often noisy ac-operated or brushed dc-motors. Other sources of electrical noise include microwave ovens, welding equipment, and automobile ignitions.

Common-mode noise can enter a system through conductive, inductive, or capacitive coupling.

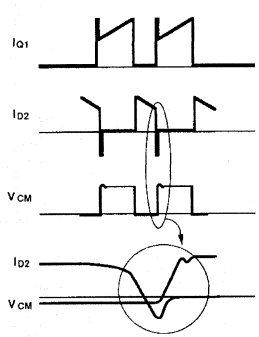

Figure 3. Half-Bridge Inverter Waveforms.

An example of a "conducted" noise voltage is the difference in ground potential that may exist between two connected systems in a plant. The two systems may experience a small voltage difference between their ground references. This voltage difference might cause a ground-loop current to flow. If the impedance of the path through which the ground-loop current flows is large enough, a significant amount of interference will result. Capacitive or inductive coupling may occur when signal wires run close to ac power cables. Electromagnetically induced interference (EMI) can also be coupled from adjacent signal lines or nearby equipment, especially in factory environments. Other sources of common-mode noise that can be coupled into a system include lightning strikes and electro-static discharge (ESD).

Solutions

There are a number of ways to limit the amount of common-mode noise entering a system. Employing good design techniques is one way to obtain better common-mode rejection. For example, a designer should carefully lay out his board to ensure that signal lines do not run adjacent to power lines. This minimizes the amount of 60-Hz noise coupled onto the signal lines. Generous use of bypass capacitors and filters helps to reduce the effect of common-mode voltages coupled onto the power supply lines. An engineer might also design a completely differential circuit, taking advantage of the inherent common-mode rejection of differential circuitry. Ideally, both inputs to the differential circuit should be referenced to the same

point. Otherwise, a small potential between the two reference points will add directly to the differential signal and may cause problems. Especially in high-frequency circuits, the positive and negative lines should run parallel and have the same length. This ensures that the two lines have the same impedance and balanced common-mode coupling.

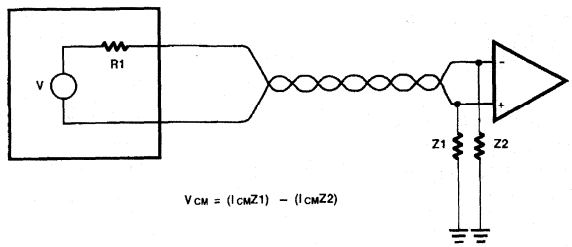

Figure 4. Twisted Pair Line.

Capacitive isolation is an effective and inexpensive way to eliminate dc common-mode signals. The most common application for capacitive isolation is in interstage coupling. For example, multi-stage amplifiers are often ac coupled. Coupling capacitors are useful for removing dc common mode voltages but do not block ac common-mode interference. Because capacitors block dc voltages, this technique cannot be used in applications for which dc signals must be transferred.

Twisted-pair wire, when used with a differential line receiver, can help to reduce the effects of common-mode noise by balancing the common-mode coupling of both electric and magnetic effects. However, if an interfering common-mode signal is not coupled equally to both lines, the net unbalance will appear as a differential-mode signal. Another problem may result if the impedances measured to ground of the two lines differ; a fraction of the common-mode signal at the end of the twisted-pair line will appear differential and interfere with the desired signal, as illustrated in Figure 4. A typical application involves the use of twisted-pair wire with an RS-422 differential line receiver. An advantage of the differential line receiver is its fast response. Also, a differential line receiver can pass both ac and dc signals. Disadvantages of line receivers are that they do not provide isolation between input and output and can tolerate only a limited range of common-mode voltages. For example, a typical RS-422 receiver can tolerate common-mode voltages of +15 V. Shielding a twisted-pair wire will provide better common mode rejection because the shield provides additional protection from electric and magnetic interference.

Transformers also provide common-mode rejection. They are often used in power applications and frequently in data communication applications such as Ethernet. An advantage of the transformer is that it provides isolation. This means that the input and the output of a system are electrically separated, and common ground connections are broken. In general, the input and the output of a transformer are symmetrical, which means that data can be transmitted in either direction across the transformer. Also, a transformer does not require an isolated power supply to operate.

A disadvantage of the transformer is that although it can pass high-frequency signals with relative ease, it cannot pass dc. Therefore, the transformer is not useful for data formats like Non-Return-to-Zero (NRZ) where the duty factor can range from zero up to 100 percent. With a transformer, NRZ data would require the use of more complex encoding and decoding circuitry, such as Manchester, which is used in Ethernet applications. In some applications, it may be difficult to obtain a usable waveform with the transformer. The transformer experiences a "sag" in the waveform which may cause problems with the design. Another difficulty with the transformer is that obtaining good common-mode rejection requires a balanced primary with symmetrical capacitances. Otherwise, a common-mode voltage injected into the center tap causes unbalanced voltages in the primary winding which, in turn, becomes a differential mode signal. A transformer with an electrostatic shield between its primary and secondary offers higher common-mode rejection than a transformer without a shield. The shield makes the transformer more expensive, but minimizes noise transferred across the windings. Other disadvantages of transformers are that they radiate and are susceptible to magnetic fields; they can be complex to design with; and they

may occupy a significant amount of space on the printed circuit board.

Optical isolation is another useful technique for reducing common-mode interference. Optocouplers, like transformers, provide isolation between the input and output of a system. Optocouplers use light for data transmission; therefore, they do not radiate nor are they affected by stray magnetic fields. Optocouplers typically provide better common-mode rejection than transformers because optocouplers do not have the high primary-to-secondary capacitance that transformers do. The CMR specification of an optocoupler ranges from 10 -1500 V amplitude and 50-30,000 V/µs rate of change, depending on the product. Another advantage of the optocoupler is that it can pass both ac and dc signals, eliminating the need for data conversion when transmitting NRZ data. Also, optocouplers are usually available in standard DIP or small-outline packages, so they require minimal board space. Disadvantages of the optocoupler are that it may require the use of an isolated power supply, and it can pass data only in a single direction.

HP's High CMR Technology

An optocoupler consists of an input LED and an output photodetector in a single package. The photodetector can be either a phototransistor, a photodiode with a transistor, or a photodiode with an integrated logic circuit. Ideally, an optocoupler would have complete isolation between its input and its output. However, the physical proximity of the input

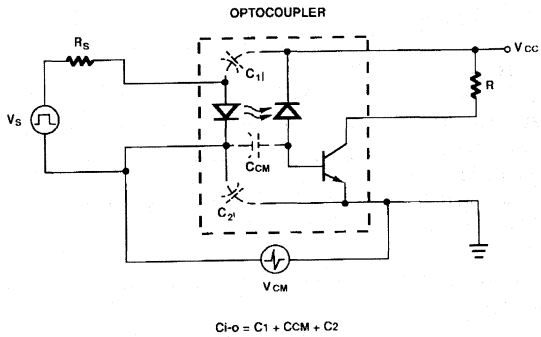

Figure 5. Input-to-Output Capacitance.

lead frame to the output lead frame creates a small capacitance between the two. This capacitance, known as Ci-o, is measured between shorted input pins and shorted output pins.

The most important factor in the common-mode interference capability of an optocoupler is the common-mode coupling capacitance, Ccm. Ccm, as shown in Figure 5, is only a fraction of the total input-to output capacitance Ci-o, but it is the main parameter that affects the common-mode capability of an optocoupler. Therefore, the smaller the value of Ccm, the better the common-mode rejection. As an example of how a common-mode signal can affect an output, Figure 6 shows a positive common-mode transient coupled through Ccm. This noise signal is amplified by the output gain stages, and tends to turn the output ON when it should be OFF. To enhance the common-mode rejection capability of its optocouplers, Hewlett-Packard inserts an internal shield between the input LED and the photodiode of each device. The internal shield is a transparent conductive shield which allows optical coupling to the photo diode but diverts electrically coupled current to the ground pin. The shield, as shown in Figure 7, reduces Ccm by at least an order of magnitude, improving the common-mode rejection of the optocoupler. A typical unshielded optocoupler might have a specified common mode rejection of 10 or 50 V peak and 1000 V/µsec rate of change. Using the electric shield technology, HP is able to produce high CMR optocouplers with CMR ratings up to 1500 V peak and 30,000 V/µsec rate of change (HCPL-4503).

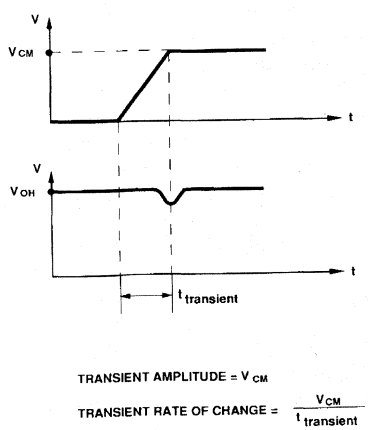

Figure 6. Common-Mode Interference Effect.

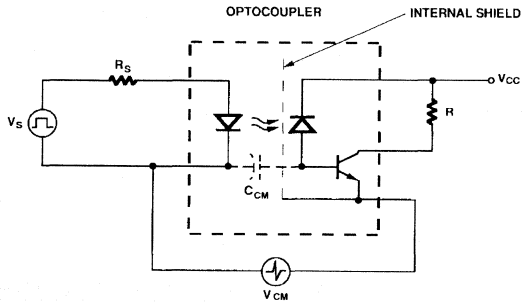

Figure 7. Enhanced Common-Mode Transient Immunity.

As shown in Figure 8, the interference by a common-mode signal can be explained in terms of a current and a voltage. A common-mode signal with a large dVcm/dt produces an interfering signal, which is a current, Ib. This current, Ib, adds or subtracts from the photodiode current, Ip. A common-mode signal with a large amplitude (Vcm) produces an interfering signal which is a voltage, Vbe. This voltage can turn on or turn off the base emitter junction of the transistor. The overall impact of a common-mode signal results from the combined effects of dVcm/dt and Vcm. For this reason, it is important for an optocoupler to specify both the slope (dVcm/dt) and the amplitude (Vcm) of a tolerable common-mode signal. A common-mode signal of 10 kV/µs at 1 kV, for example, is much worse than a common-mode signal of 10 kV/µs at 10 V.

Hewlett-Packard specifies the CMR of its optocouplers as $|CM_H|$, Common Mode Transient Immunity at High Output Level, and as $|CM_L|$, Common Mode Transient Immunity at Low Output Level. CM_H is the maximum tolerable rate-of-rise of the common-mode voltage to ensure that the output will remain in a high logic state. Likewise, CML is the maximum tolerable rate-of-fall of the common-mode voltage to ensure that the output will remain in a low logic state. Each CM_H and CM_L specification includes the common-mode voltage amplitude (Vcm) as well as its rate of rise (dVcm/dt).

Hewlett-Packard offers a variety of high CMR optocouplers for both analog and digital applications. Specifications for these optocouplers can be found in the current Optoelectronics Designer's Catalog.

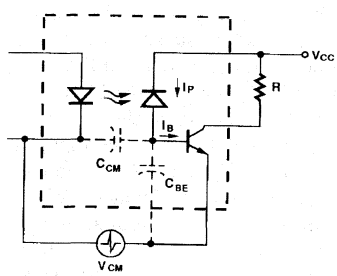

Figure 8. Common-Mode Interference Model.

Conclusion

In summary, common-mode noise problems can occur in almost any electrical circuit. The noise can be coupled from an external source, as in data communications, or be an inherent part of the design, as in switch-mode power supplies. Several techniques for reducing the effects of common-mode noise have been discussed. Hewlett-Packard offers a wide variety of high CMR opto-couplers to help solve these types of noise problems. Additionally, Applications Engineers and Field Sales Engineers are available for technical assistance and product support.

HEWLETT® PACKARD

Low On-Resistance Solid State Relays

Application Note 1046

Introduction

The on-resistance is an important specification for a solid state relay that uses MOSFETs at its output. In general, a lower on-resistance rating will allow a higher contact current rating. The HSSR-8060 and HSSR-8400 are single-pole, normally open, solid state relays (SSR) with very low on-resistances. Each SSR consists of a high-voltage circuit, optically coupled with a light-emitting diode (LED). When a control current flows through the input terminals of the SSR, the LED emits light onto a photodiode array. The photodiode array, illustrated in Figure 1, generates sufficient voltage and current to operate the FET driver circuit and also to drive the gate-to-source voltages above the thresholds of the two output FETs. This application note describes the main characteristics of the HSSR-8060 and HSSR-8400, suggests a control drive circuit, and presents various applications for the SSRs. Additional information regarding SSRs in general can be found in Hewlett-Packard's Application Note 1036.

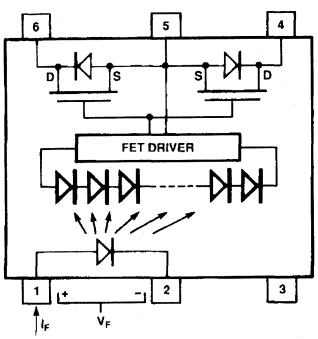

Figure 1. Circuit Diagram of HSSR-8060/8400.

Summary of Characteristics

The HSSR-8060/8400 is packaged in a 6-pin DIP, but only five pins are used. Pins one and two are the anode and the cathode of the input LED, respectively. Pins four, five, and six, at the output side of the SSR, can be configured as either Connection A or Connection B as shown in Figure 2. With Connection A, the signal at the output of the SSR can have either positive or negative polarity. This means that the SSR can pass either ac or dc signals. With Connection B, the signal at the output of the SSR must have its polarity as indicated in Figure 2b. In this configuration, pins 4 and 6 are tied together, and the SSR can control dc signals only. The advantage of using Connection B is that it places the two output FETs in parallel with each other, rather than in series.

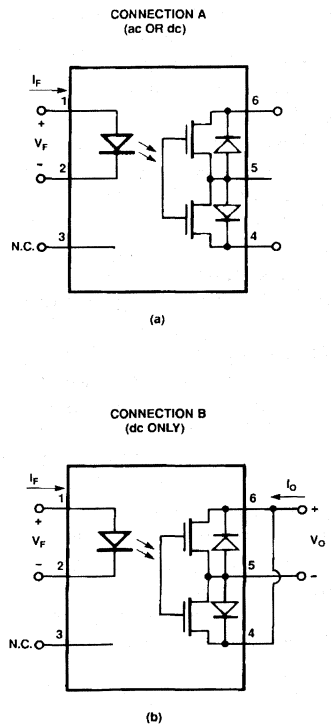

Figure 2. HSSR-8060/8400 Schematic.

This configuration reduces the output on-resistance of the SSR significantly and increases its output current capability by a factor of two. Figure 2 also defines the polarity for the input side of the SSR. The HSSR-8060/8400 turns on (its contact closes) with a minimum input current, I_F, of 5 mA at a typical forward voltage, V_F, of 1.6 V. Operation at higher currents causes faster closure of the contacts. The SSR turns off (its contact opens) when V_F is equal to 0.8 V or less.

Both the HSSR-8060 and the HSSR-8400 have guaranteed input-to-output insulation voltage ratings of 2500 Vac, 1 minute. Additionally, the HSSR-8060 has an output transient rejection of 1000 V/μs at 60 V, and the HSSR-8400 has an output transient rejection of 1000 V/μs at 100 V. The input-to-output transient rejection specification of both SSRs is 2500 V/μs at 1000 V.

The HSSR-8060 has an output withstand voltage rating of 60 V at room temperature. If the SSR is used as shown in Connection A to pass ac signals, then 60 V is the maximum amount of peak positive or negative voltage that should be applied across the output contact. The HSSR-8060 is distinguished by its low on-resistance, $R_{(on)}$, and large output current capability, I_O. At room temperature, with Connection A, the maximum on-resistance of the HSSR-8060 is 0.7 ohm, and the average output current rating is 0.75 A. With Connection B, the on-resistance is reduced to 0.2 ohm and the average output current rating is increased to 1.5 A. As mentioned in the data sheet, the on-resistance specification for both the HSSR-8060 and HSSR-8400 refers to the resistance measured across the output contact when a pulsed current signal is applied to the output pins. The use of a pulsed signal (≤ 30 ms) implies that each junction temperature is equal to the ambient and case temperatures.

The HSSR-8400 has an output withstand voltage of 400 V at room temperature. If the SSR is used as shown in Connection A to pass ac signals, then 400 V is the maximum amount of peak positive or negative voltage that should be applied across the output contact. Similar to the HSSR-8060, the HSSR-8400 has a low on-resistance and large output current rating. At room temperature, the maximum on-resistance value is 10 ohms, and the average output current capability is 0.15 A. With Connection B, the maximum on-resistance is 2.5 ohms and the average output current rating increases to 0.3 A.

The output current rating of an electromechanical relay (EMR) is usually limited by its ability to interrupt that current when opening. The output current rating of the HSSR-8060/8400, on the other hand, is limited by the highest junction temperature (125°C) its MOSFETs can withstand. This junction temperature is a function of the on-resistance, the load current, the thermal resistances, and the ambient temperature. As the junction temperature rises, the on-resistance also rises. To limit power dissipation at higher case and ambient temperatures, the output current rating must then be derated. It is important for SSR specifications to include this derating effect. The data sheets for both the HSSR-8060 and HSSR-8400 include graphs that show the effect of temperature on the output current rating, I_O. If these SSRs are operated within the "safe area of operation" indicated on these current derating graphs, the corresponding "power versus temperature" graph illustrates the maximum amount of power dissipated by the SSR. Operation within this area ensures that the steady-state junction temperatures remain below 125°C.

The output current derating graphs for the HSSR-8060 are shown in Figure 3. The output power dissipation versus case temperature graph is shown in

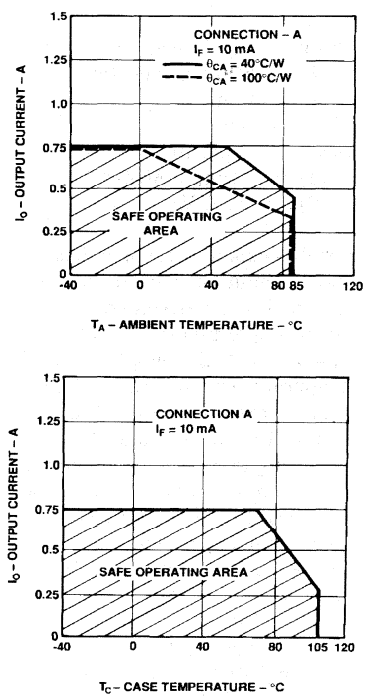

Figure 3. HSSR-8060 Output Current Derating Graphs.

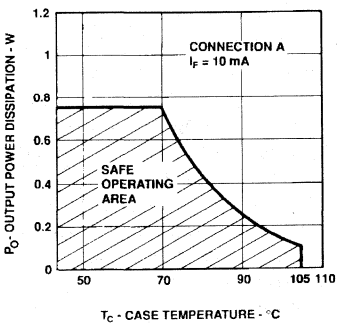

Figure 4. Output Power Dissipation vs. Case Temperature.

Figure 4. The following example uses these graphs to calculate the MOSFET junction temperatures and the maximum recommended value of the case-to-ambient thermal resistance, $\theta_{C\text{-}A}$.

Designer's specifications:
HSSR-8060, Connection A
I_O = 500mA
T_A = 25°C
Data sheet specification:
Typical Output MOSFET
$\theta_{J\text{-}C}$ = 55°C/W

For this example, assume that the above conditions have been specified by the designer. According to Figure 3b, for I_O = 500 mA, the maximum case temperature allowed is 86°C. At T_C = 86°C, the maximum output power dissipation is 0.3 W, according to Figure 4. Therefore, the maximum power dissipated by each MOSFET is 0.15 W. Hence, the maximum junction temperature of each MOSFET is as follows:

$$T_J = \theta_{J\text{-}C}(P_O) + T_C$$
$$= 55°C/W\ (0.15\ W) + 86°C$$
$$= 94.25°C$$

Now, to calculate the maximum recommended $\theta_{C\text{-}A}$, the following formula must be used: $\theta_{C\text{-}A} = [(T_C - T_A)/P_{total}]$. The maximum power dissipated by the input LED is equal to $[(I_F)(V_F)] = [(10\ mA)(1.85\ V)] = 0.019$ W. Therefore, the total power dissipated by the SSR must be less than 0.319 W. Hence, the value of $\theta_{C\text{-}A}$ must be no greater than [(86 - 25)/0.319], or 191.22°C/W. This will ensure that T_C remains below 86°C. One suggestion for minimizing $\theta_{C\text{-}A}$ is to enlarge the pc-board copper traces surrounding the output pins of the SSR. Another suggestion is to force cool airflow across the board.

Maximum Signal Frequency

When using the HSSR-8060/ 8400 to control ac signals, the maximum frequency of the signal may be limited by the off-capacitance, $C_{(off)}$, of the relay. The off-capacitance is voltage dependent and is specified as 135 pF typical for the HSSR 8060 and 60 pF typical for the HSSR-8400 at V_O = 25 V. The data sheets for both SSRs include graphs for the typical output capacitance versus output voltage. Besides the off-capacitance, the maximum signal frequency depends on the load impedance, the circuit configuration, and the amount of attenuation required by the designer. The attenuation refers to the amount of signal passed through the contact in its OFF state versus its ON state. For example, -40 dB of attenuation implies that the current that passes through the contact in its OFF state will be one hundred times smaller than the current that passes through the contact in its ON state.

For comparison, typical SSRs were configured as simple series switches and tested at room temperature for maximum signal frequency. Each SSR was tested with a load resistor, R_L = 100 ohm and an output sine wave, V_O = 1 Vp-p. The maximum signal frequency of each SSR to obtain a signal attenuation of -40 dB was as follows:

HSSR-8060: 40 kHz
HSSR-8400: 65 kHz
HSSR-8200: 2800 kHz

The HSSR-8200 is another SSR made by Hewlett-Packard. It has a very low $C_{(off)}$ specification of 4.5 pF maximum.

Figures 5a and 5b show a circuit model and its off-state equivalent circuit for a simple series switch using an SSR. The frequency response of this circuit is shown in Figure 6. The break frequency, f_B, is the frequency above which there is no attenuation in the signal.

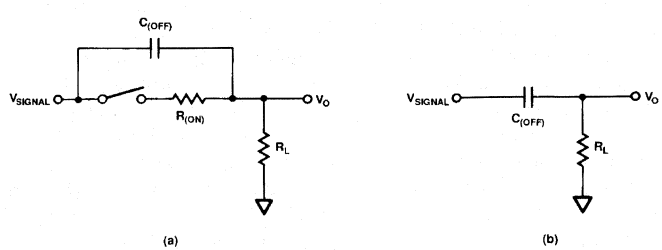

Figure 5. Simple Series Configuration.

This means that the same amount of signal will pass through the contact whether it is opened or closed. As shown in Figure 6, the signal amplitude decreases by 20 dB for each decade decrease in the signal frequency. A designer who requires -40 dB of attenuation when the SSR is off must have a maximum signal frequency that is at least two decades below the break frequency. As an example, the break frequency is about 800 kHz for a load resistance, R_L, of 1 kΩ and a $C_{(off)}$ of 200 pF. If a designer requires at least -40 dB of attenuation when the relay is off, the maximum signal frequency is two decades below 800 kHz, or 8 kHz.

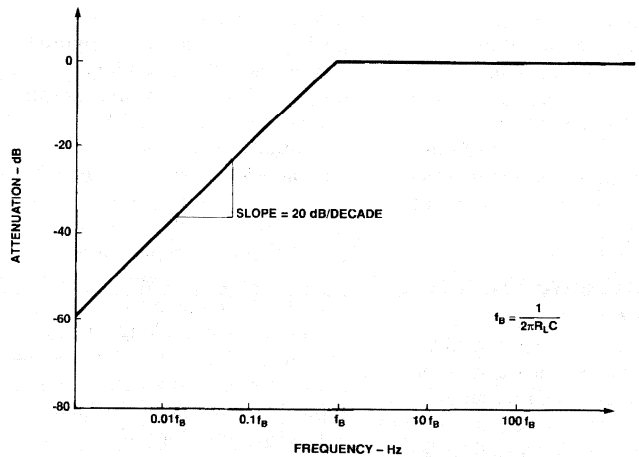

Figure 6. Simple Series Frequency Response.

To control higher-frequency signals, two SSRs can be used in the series-shunt configuration shown in Figure 7a. In the ON state, the series SSR is closed, and the shunt SSR is opened. In the OFF state, the series SSR is opened and the shunt SSR is closed. Figure 7b shows the equivalent circuit for this OFF condition, and Figure 8 illustrates its frequency response. This series-shunt configuration produces a higher break frequency than the simple series configuration. The reason for this improvement is that the break frequency equation now uses the low on-resistance value of the SSR rather than the load resistance value. The series shunt configuration allows higher signal frequencies to be used or gives increased attenuation at lower signal frequencies. As an example, using two relays with $C_{(off)}$ = 200 pF, $R_{(on)}$ = 6 Ω, and R_L = 1 kΩ, the break frequency for the series-shunt configuration is about 66 MHz.

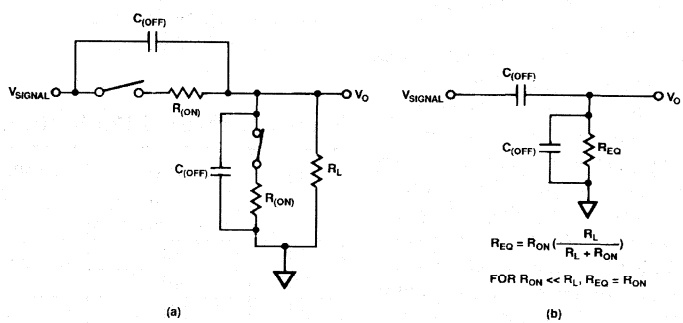

Figure 7. Series-Shunt Configuration.

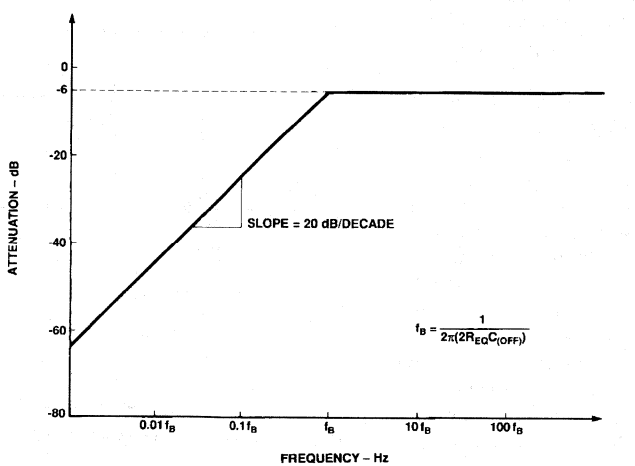

Figure 8. Series-Shunt Frequency Response.

The maximum signal frequency to ensure at least -40 dB of attenuation is approximately two decades below 66 MHz, or 660 kHz. Notice that because $R_{(on)} << R_L$, the value of the load resistance has virtually no effect on the calculation of the break frequency.

Control Drive Circuit Suggestions

Operation of the HSSR-8060/8400 requires at least 5 mA of input current. A larger amount of input current results in faster turn-on of the SSR and a slightly faster turn-off. A simple circuit for obtaining the desired ON current and OFF voltage is shown in Figure 9. The logic series used can be either TTL or CMOS, as long as the current sinking capability is adequate. Resistor R1 sets the level of steady-state input current, I_F. The purpose of R2 is to bypass logic-high leakage current with sufficiently small voltage drop to ensure an OFF-voltage less than 0.8 V. R2 is not required if the logic output has an internal pullup circuit that is able to satisfy the OFF-voltage requirement of the SSR. With open collector TTL outputs, R2 is always required to ensure that $V_{F(OFF)} < 0.8$ V.

As mentioned earlier, turn-ON time is influenced by the level of input current. As input current is increased, the turn-ON time becomes shorter. However, it may not be desirable to operate with a high steady-state input current because that would increase the output offset voltage, V_{OS}, due to heat transferred from the LED control to the contact side. Also, a lower steady-state current minimizes input power consumption. In situations requiring fast turn-ON but low offset, the peaking circuit shown in Figure 9 can be used. When the logic output is high, R2 assures that the current through the LED is so small that the capacitor is completely discharged. Then when the logic output goes low, a surge of current flows through both R1 and R3 until the capacitor is charged to the voltage across R1. The steady-state current is set by R1 alone. Thus peaking permits fast turn-ON as well as low steady-state current. Table 1 shows the typical turn-on times obtained with different values of resistor R3.

Turn-on of the output MOSFETs requires charging the gate capacitances in the FET DRIVER circuit. This charge is the time-integrated photocurrent from the photodiode array, and translates into a certain amount of current that must pass through the LED. The corresponding amount of LED charge is set by the value of the peaking capacitor and the voltage across R1. For this reason, it is not necessary to change the value of the capacitor when other values of peak current are desired; it is necessary only to change the value of R3 and make sure that the logic output is capable of sinking the higher current.

Telecommunication Applications

SSRs are commonly used by the telecommunications industry. Some examples of applications

Table 1. Typical Peaked Turn-on Times.

R_3 (Ω)	$I_{F(PEAK)}$ (mA)	HSSR-8060 t_{ON} (ms)	HSSR-8400 t_{ON} (ms)
–	10 (No Peak)	0.93	0.50
330	20	0.53	0.29
100	40	0.32	0.17
33	100	0.17	0.09

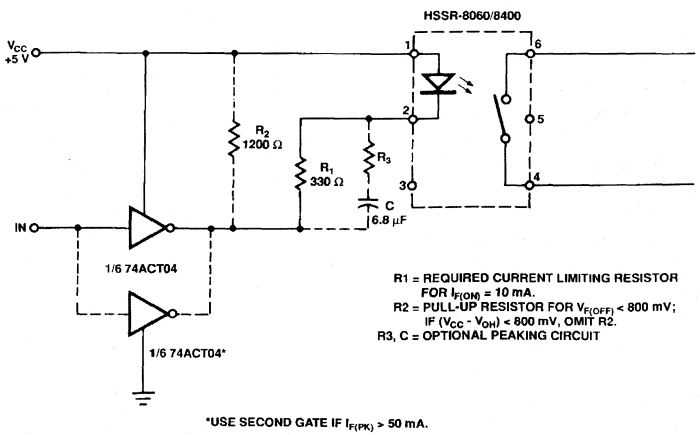

Figure 9. Recommended Input Circuit.

include on/off-hook switching, test and maintenance equipment, PBX and central-office switching, and pulse dialing. Compared to EMRs, SSRs are useful in these areas because they are small and require little board space. They have no mechanical parts so they last longer, thereby increasing the number of operations that can be performed. In addition, SSRs have no contact bounce, arcing, or acoustic noise.

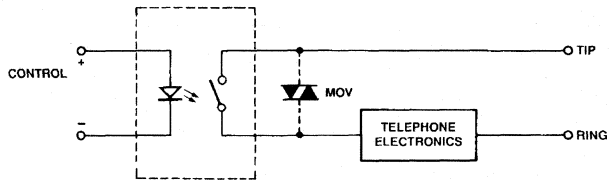

Figure 10. Telephone Switchhook.

In telephone loop applications, it is often necessary to isolate the telephone equipment from the incoming telephone lines. Isolation is important to protect the electronics from harmful voltages and currents induced from lightning or noise coupled onto the lines. Modern line interface circuits, such as those used for modems and fax machines, consist of a ring detector, an on-off hook control, isolation, and surge protection. An advantage of using an SSR as the on-off hook switch is that it provides both high-voltage isolation and surge protection. Figure 10 shows the SSR in a telephone switchhook application. In the ON-state, the SSR's contact on-resistance contributes to the total impedance of the telephone loop, which is between 500 and 2100 ohms. Therefore, the on-resistance should be as small as possible. At room temperature, the HSSR-8060 has a maximum on-resistance of 0.7 ohm, and the HSSR-8400 has a maximum on-resistance of 10 ohms.

The purpose of the on-off hook switch is to connect or disconnect the telephone equipment from the PBX (private branch exchange) or the PSTN (public switched telephone network). When a person wishes to place an outgoing call or answer an incoming call, the relay is turned on to allow current to flow between the tip and ring conductors. In this relay application, an overvoltage protection device is often required to protect the contact from possible lightning damage. For example, a metal oxide varistor (MOV™) is a bidirectional device that breaks down and conducts heavily when the voltage across it rises above a threshold level. As shown in Figure 10, an MOV is placed across the output contact of the SSR. The device protects the SSR by limiting the tip-to-ring voltage to a value below the maximum load voltage of the SSR. The MOV acts as a Zener diode but dissipates more energy. When a large current surge occurs, the "Zener" voltage of the MOV can cause significant overshoot. For this reason, the SSR's load voltage must be higher than the highest voltage of the protection device at any given current surge. Most of the SSRs used in telephone-line interface applications are rated for at least 350 to 400 volts. The HSSR-8400 has a high contact withstand voltage rating of 400 V.

Telecommunication companies may also use SSRs for test and maintenance equipment. When a subscriber reports a problem with his or her telephone service, the telephone company can use relays to switch test equipment onto the line to verify the problem. Telephone companies might also use relays to switch test equipment onto a line to examine the quality of the line. This is done to locate potential problems. Another application for SSRs in the telecom industry is in PBXs and Central Office Switching Stations. SSRs may be used to multiplex incoming signals, such as concentrating several subscriber loops onto a single interface circuit. Or, SSRs may be used in the cross-point matrixes of these switching stations.

In a telephone line interface, SSRs can also be used for the pulse dialing function. With pulse dialing, a relay is used to interrupt the line current. The number of line interrupts corresponds to the specific digit that was dialed. A "1", for example, is identified by one break while a "9" is identified by nine breaks in the line.

Multiplexing

Sometimes, signals that need to be measured require amplification or conversion. As shown in Figure 11, multiplexing allows a single device to process a number of signals. This technique reduces cost by using one device for a number of channels rather than one device per channel. Also, multiplexing ensures that the same amount of gain is applied to each signal so that the ratios of the amplified levels V1...Vn will relate to ratios of their unamplified counterparts, E1...En. Compared to EMRs, SSRs are especially useful in multiplexing applications because of their increased life and reliability. Also, their fast switching speeds allow more efficient multiplexing of signals. The HSSR-8060/ 8400 have turn-on times under 1.8 ms and turn-off times under 0.1 ms. Both relays will turn on faster using the peak circuit mentioned earlier.

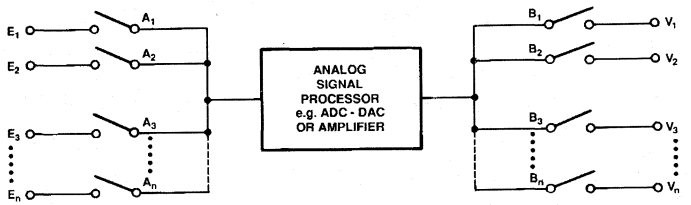

Figure 11. Multiplexing and Demultiplexing.

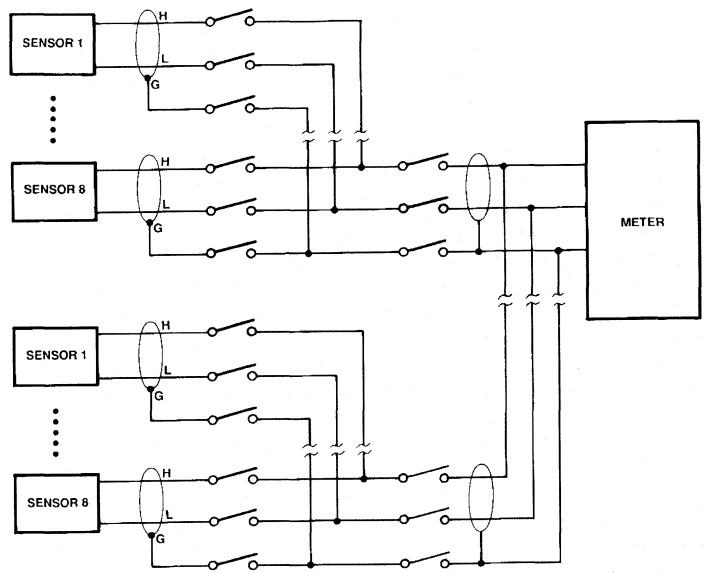

Figure 12. Multiplex System.

In any application, it is important for the amount of current passed through the contact in its OFF state to be negligible with respect to the actual amount of current being controlled. With power switching applications, the leakage current of the SSR is small relative to the amount of current being switched. In signal switching applications, however, the amount of current controlled by the SSR is relatively low. Therefore, the SSR should have negligible leakage current. When multiplexing or switching low-level signals such as thermocouple outputs, an SSR with a low leakage specification is preferred. The HSSR-8060 has a typical output leakage current of 0.1 nA, and the HSSR-8400 has a typical output leakage current of 0.6 nA. Figure 12 shows an example of a multiplexing system. In this diagram, SSRs are used to multiplex or scan low-level differential signals. The configuration uses three switches per channel to connect the signal HI, signal LO, and guard to the measurement system. In Figure 13, SSRs are used in a flying capacitor circuit. When relays 1 and 2 are closed, the voltage is acquired from the sensor and stored across the capacitor. After relays 1 and 2 open, relays 3 and 4 close, and the signal is read by the multiplexer. A number of sensors can be connected to the multiplexer in this fashion.

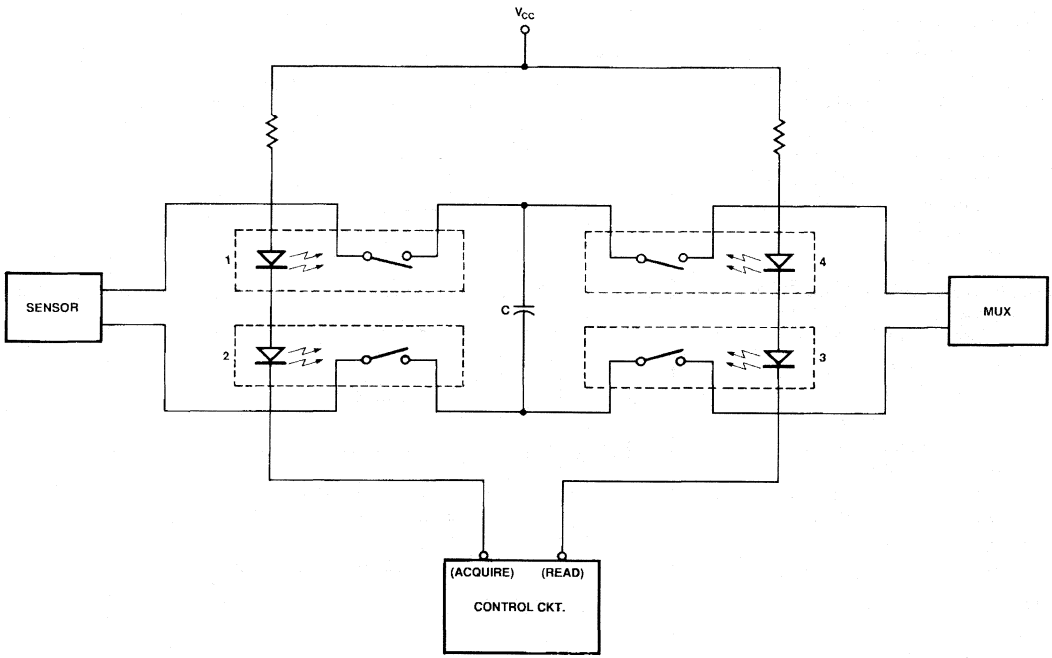

Figure 13. Flying Capacitor Multiplexer.

Industrial Control

In programmable controllers, input and output modules allow microprocessors to sense and control various loads. An ac input module generates a logic level voltage corresponding to the presence or absence of an ac load voltage. Likewise, a dc input module generates a logic level voltage corresponding to the presence or absence of a dc load voltage. Input modules receive signals from a variety of instruments on the factory floor, including robotics assembly equipment, chemical process units, injection molding systems, and so forth. An ac output module allows logic-level voltages to control a switch that turns ac loads on and off. For example, the output module of a process controller might be used to control the motor starters of adjustable frequency drives, position valves, or dampers. A dc output module allows logic level voltages to control a switch that turns dc loads on and off.

Figure 14 shows an example of a six-channel ac output module. The HSSR-8060/8400 may be used to sense and control signals in any one of these input and output modules.

Another application for SSRs in industrial control equipment is on scanner cards or matrix cards. These cards may be used in larger instruments such as programmable thermometers, temperature scanners, and multimeters. Scanners are very similar to

multiplexers, however scanners measure sequentially while multiplexers allow any order. Figure 15 shows an example of relays used on a matrix card. In this configuration, a number of sources can be connected, through the device under test (DUT), to a number of measurement devices.

In an automated test system, such as a data acquisition unit, efficient switching is important. In addition to their fast switching speeds, SSRs provide high voltage isolation, which is often required in industrial environments. Another benefit of SSRs in industrial control applications is that they do not have mechanical contacts, which could eventually deteriorate from arcing or dust particles.

Various Loads

Depending on the type of load, an SSR may be required to withstand a substantial amount of surge current. A purely resistive load is the easiest type for an SSR to switch since it has no surge current requirement. Other typical loads of the HSSR-8060/8400 and their related inrush versus steady state currents are shown in Table 2.

The surge requirement of the load should be within the peak surge current rating of the relay. Therefore, an SSR that switches one of these types of loads should have current specifications that

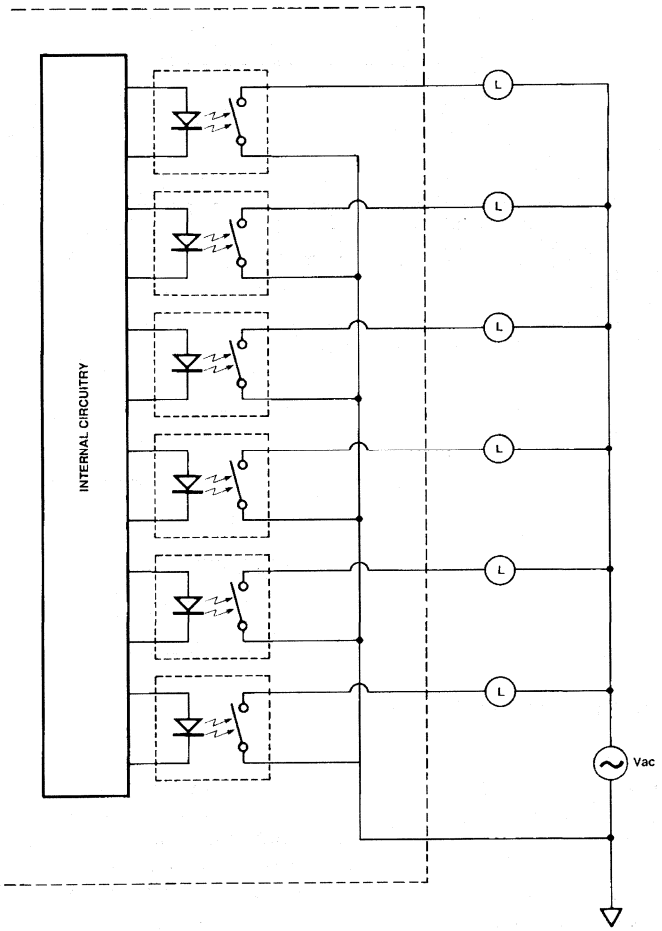

Figure 14. Six-Channel AC Output Module.

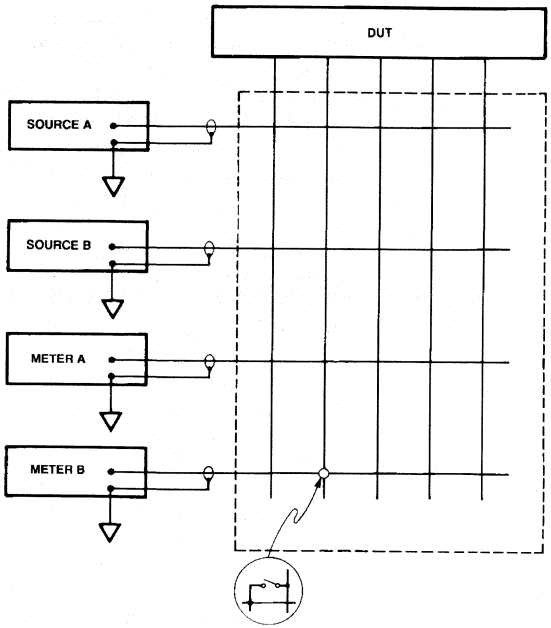

Figure 15. Matrix Card Example.

Table 2. HSSR-8060/8400 Load Types.

Load Type	Typical Inrush vs. Steady State Current	Inrush Duration
Small Solenoid	10-20X	70-100 ms
Fractional Horsepower Motor	5-10X	200-500 ms
Miniature Incandescent Lamp	20-15X	30-100 ms
Capacitive Load	20-40X	10-40 ms

meet both the steady-state and surge requirements. Compared to EMRs, SSRs are more tolerant of surge currents because they do not have contact bounce, which results in arcing with EMR contacts. The high-temperature arc could cause melting and eventual degradation of the EMR contact. With Connection A, the HSSR-8060 has a single shot, peak output current rating of 3.75 A for a 100 ms pulse width. The HSSR-8400 has a rating of 1.0 A for a 100 ms pulse width. For longer pulse widths, the single-shot, peak output current rating would decrease. Figures 16 and 17 show the results of an experiment performed on seventy units of the HSSR-8060 and HSSR-8400. Each graph shows the peak surge current values that we were able to apply to the output of seventy typical SSRs without any one of them failing.

Another experiment was conducted to determine the maximum repetitive surge current that twenty typical SSRs could withstand. Ten units each of the HSSR-8060 and HSSR-8400 were tested for fifteen minutes each with surge current pulses applied for 100 ms at 100 ms intervals (fifty percent duty cycle). Under these conditions, the maximum repetitive surge current to failure was 1.2 A for the HSSR-8060 and 0.25 A for the HSSR-8400.

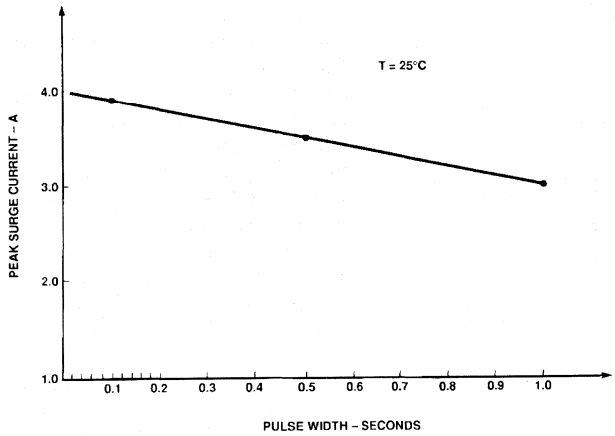

Figure 16. HSSR-8060 Peak Surge Current Experiment Results.

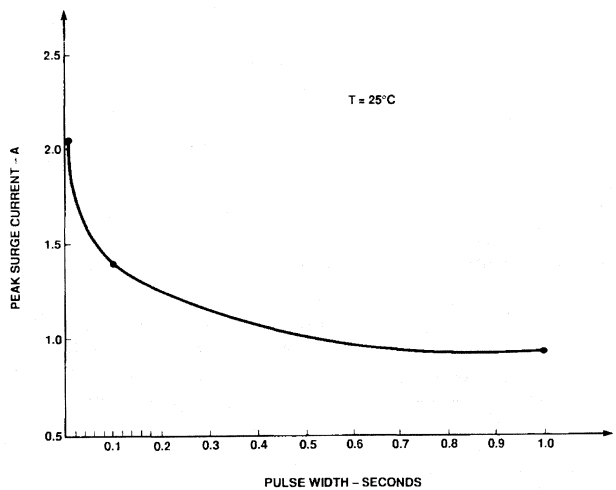

Figure 17. HSSR-8400 Peak Surge Current Experiment Results.

Figure 18 illustrates the use of SSRs in a lamp sequence control. Some areas that use SSRs to control lamp loads include process equipment, navigational devices, illuminated signs, and games. In aircraft applications, SSRs may control lamps for cabin lighting, instrumentation lighting, and status indicators. Compared to EMRs, SSRs are especially useful in aircraft environments because they are immune to shock and vibration and are unaffected by electro-magnetic interference. Upon turn-on, the current through a lamp is very high initially because of the Tungsten filament's low resistance at room temperature. The current decreases as the filament heats up. Hence, the inrush current can be reduced by using a "keep alive" voltage across the filament to keep it warm but below the level of incandescence.

Similar to a lamp load, a capacitive load will cause a surge current to flow through the output MOSFETs of the SSR, upon initial turn-on. This surge current will depend on the load capacitor value and the rate of rise of the load voltage. In addition, the frequency at which the SSR is switched will affect the output power dissipation. Ten units of the HSSR-8060 were tested at room temperature under the following conditions:

Input current, I_F = 10 mA (1 Hz)
Load, C = 100 μF capacitor
Load voltage, V = 60 V

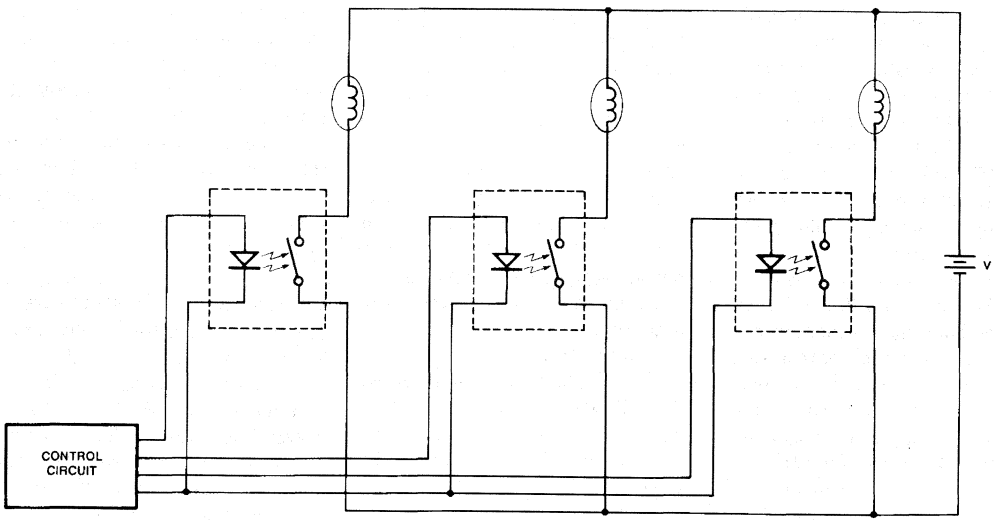

Figure 18. Lamp Control.

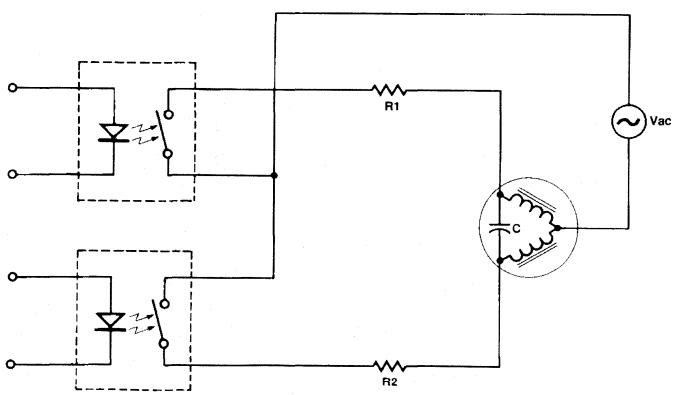

Figure 19. Motor Reversing Control.

The load capacitor was charged by the load voltage through an 80-ohm series resistor. The output of the SSR-under-test was placed in parallel with the capacitor to discharge it. After the testing, each SSR was tested for 1.2 million cycles and passed. There were no catastrophic failures or parameter drifts.

The HSSR-8060/8400 can be used to drive fractional horsepower motors. A reversing control for a synchronous ac motor is shown in Figure 19. For motors that cycle on and off frequently, an SSR is often preferred over an EMR because it can handle surges better and does not produce EMI. An SSR might also be used to control small dc motor loads such as those used in computer disk drives, audio and video equipment, household electronics, or automotive electronics.

An SSR may be used to control the input coil of an EMR, which is a highly inductive load. Other inductive loads include small transformers, contactors, solenoid valves, magnetic couplings, etc. When SSRs drive inductive loads, very high peak voltages can occur across the output when switching off the loads. The MOSFETs in the output of the SSR are able to withstand a reasonable amount of inductive overload. For example, ten units of the HSSR-8060 were tested at room temperature under the following conditions:

Input current, I_F = 10 mA (1 Hz)
Load, L = 1-H inductor
Load voltage, V = 60 V
Load current = 670 mA

Each unit was tested for one million cycles and passed. There were no catastrophic failures or parameter drifts. No overvoltage protection for the SSR was used in this experiment. However, overvoltage protection is recommended whenever the chance exists for an event where both the withstand voltage rating and output power dissipation or surge rating are exceeded, or where the energy content of the transient is very large as in lightning-induced events.

Overvoltage Protection

Metal oxide varistors (MOVs) or TransZorbs™ can be used for overvoltage protection of the contacts of an SSR. They both break down and conduct heavily when the voltage across them rises above a specified level. For ac voltages, either an MOV or a bidirectional TransZorb can be used. Both devices fail "short" so that protection is always in place, even though operation may cease. As shown in Figure 20, the protection device is placed across the output contact

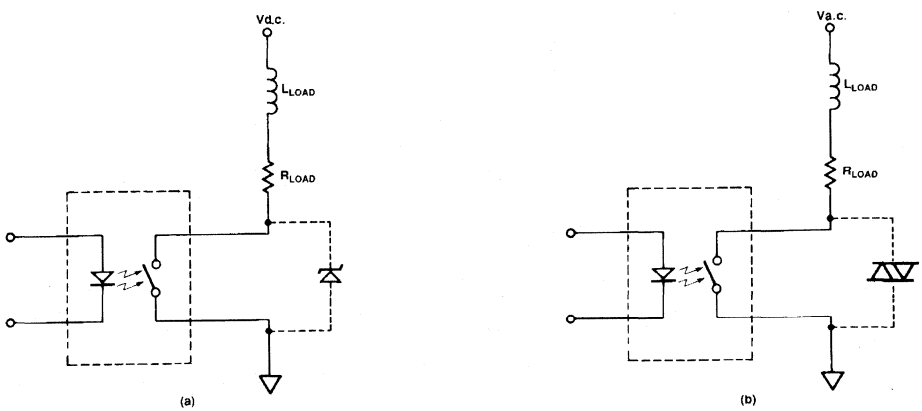

Figure 20. Overvoltage Protection.

pins of the relay and is used when the contact is susceptible to voltages greater than the rated output withstand voltage, V_O. For adequate protection of the contact, the protection device should be in a fully conductive state at a voltage just below the maximum output voltage. However, it must be in a high-impedance state for any voltage below the maximum line voltage.

When the SSR is used to control small dc voltages, a single Zener diode, illustrated in Figure 20a, provides adequate protection. Again, the clamp voltage of the Zener should be greater than the controlled voltage but less than the maximum rating of the SSR contact.

TM MOV is a registered trademark of GE/RCA Solid State.

TransZorb is a registered trademark of General Semiconductors.

HEWLETT® PACKARD

Optocoupler Input-Output Endurance Voltage

Application Note 1074

Introduction

A major concern of circuit designers is the reliability of an optocoupler when subjected to repeated and long-term, high-voltage stress between its input and output. Most of the technical data on optocouplers adequately address the capability of an optocoupler to withstand one-time high-voltage transients, but they do not adequately address the issues of:

a) how long one can apply a steady state ac or dc voltage between the input and output of the optocoupler before degrading the semiconductors or the insulation inside the optocoupler, and

b) how often one can apply high-voltage transients before degrading the optocoupler.

In attempting to answer these questions, a series of operating life tests were conducted on Hewlett-Packard (HP) optocouplers. Several optocoupler lots were subjected to different input-output high-voltage stress tests to examine the failure rate and the time taken to fail. Upon completion of these tests, the test data was analyzed to create safe operating areas for long-term, input-output high-voltage stress. The boundary of the safe operating areas for the steady-state input-output high-voltage stress is referred to as Endurance Voltage.

Figure 1 describes the concept of Endurance Voltage for one family of HP optocouplers. As shown in this figure, the bottom region is the safe operating area for steady-state ac and dc input-output voltage stress meant for continuous application of a high-voltage stress. The middle region is the safe operating region for transient voltage stress. Operating outside both of these safe operating regions causes the optocoupler to wear-out either in functionality or in isolation capability, and is not recommended for use.

This application note discusses an HP input-output voltage stress study that was conducted on HP optocouplers. The results from these tests indicate that HP optocouplers are robust for long-term survival in applications where a continuous high-voltage stress is applied across the input-output. HP optocouplers can safely withstand a continuous voltage up to either 800 Vac, or 1000 Vdc. Before discussing the high-voltage stress test details, it is worthwhile to define some of the common high-voltage terminology and put that in context with Endurance Voltage.

High-Voltage Terminology

The basic purpose of an optocoupler is to send signals between two circuits or systems that need electrical insulation from one another. During signal transmission between the two circuits or systems the optocoupler must also have the capability to reject common mode voltages and transients and this capability is referred to as signal isolation. There are several terms used in the industry to define and quantify the signal isolation and electrical insulation capability of an optocoupler. Some of the common terms used in Hewlett-Packard technical literature are described.

5965-5977E

Signal Isolation
The isolation function of an optocoupler is defined by its ability to pass desired signals and reject unwanted signals or transients. Optocoupler isolation capability is largely determined by its input-output capacitance and the electrical design of the detector circuit. Most optocouplers use the common-mode rejection parameter to define and quantify the signal isolation capability.

Electrical Insulation
When an optocoupler acts as a coupling device between two circuits or systems that have a potential difference, then the insulation capability of the optocoupler is defined by its ability to prevent physical damage to the surrounding circuitry as well as to itself. Electrical insulation is often a safety issue which is regulated by many countries' safety agencies* at both the component level and at the equipment level. Safety standards are often set up to establish the requirements for the insulation barrier between safe and hazardous voltages within equipment. They also define test, material and dimensional requirements based on conditions which are expected to be encountered. Definitions of safe and hazardous voltage levels vary among countries and equipment. Components like optocouplers, which are often part of the insulation barrier, are sometimes addressed separately in order to simplify equipment level qualification. There are five major ways of defining and quantifying the insulation properties of an optocoupler.

Input-Output Resistance:
To measure the input-output resistance of an optocoupler, usually 500 Vdc is applied between the optocoupler input and output for a duration of one minute, and the leakage current is measured. With the leakage current value, one can calculate the input-output resistance. The input-output resistance is merely one type of short duration insulation test and it gives the circuit designer an indication of the amount of dc leakage current for a particular input-output voltage.

Input-Output Insulation Voltage or Dielectric Withstand Voltage:
This is usually defined by a one minute rating for the maximum voltage that can be applied between the input and output of an optocoupler. Either long duration or repeated application of high-voltage stress may cause permanent damage and functional failure of the optocoupler. The one-minute Dielectric Withstand Voltage does not indicate the capability of the optocoupler to withstand long-term application of high-voltage stress nor does it tell you how often and how many times one can apply these high-voltage pulses.

Internal Clearance: The shortest direct through-insulation distance between the input and output circuitry within the optocoupler.

External Clearance: The shortest air-gap distance between the input and output leads of the optocoupler.

External Creepage: The shortest external surface distance between the input and output leads of the optocoupler.

The Internal Clearance, External Clearance, and External Creepage specifications of optocouplers are useful for obtaining component and equipment regulatory insulation safety approvals in various countries, as well as for determining the Working Voltage of an optocoupler, which is defined below.

Working Voltage
The highest steady-state voltage that can be applied across the input-output insulation of an optocoupler as defined by equipment standards and Regulatory Agency guidelines is called the Working Voltage. Some of the considerations for determining the Working Voltage of an optocoupler are the type of equipment the optocoupler is designed into, the relevant safety issues in the use of the equipment, the mains voltage of the equipment, and the environment in which the equipment is used.

In situations where a Regulatory Agency is not involved, then the Working Voltage is defined by the equipment application. In such a case, the Working Voltage is the maximum input-output steady state voltage that the optocoupler encounters in the circuit application.

Endurance Voltage
The Endurance Voltage, a term defined by Hewlett-Packard, is the maximum voltage that can be applied between the input and output terminals of an optocoupler for extended periods of time without damaging the optocoupler. Damage to an optocoupler can include loss of

* Examples of Safety Agencies are UL in USA, VDE in Germany, and CSA in Canada.

operation or loss of insulation. Endurance Voltage is based on the inherent properties of the optocoupler and is not based on a Regulatory Agency guideline or the equipment application.

Some factors affecting insulation and operating life include input and output biases, applied input-output voltage, temperature, humidity, moisture, mechanical stress and exposure to a variety of chemical agents. For determining the use of an optocoupler in a particular equipment, a designer should consult the regulatory guidelines and the appropriate Working Voltage for that application. For proper use, the Endurance Voltage of an optocoupler must be equal to or greater than the Working Voltage.

Description of the HP-Internal Input-Output Voltage Stress Study

The objectives for the optocoupler input-output voltage stress tests conducted at HP included determining which temperature is the worst case temperature for partial discharge related wear-out, establishing data bases for demonstration data to extract ac and dc Endurance Voltages, and voltage and temperature acceleration factors. The following table shows the stress cells that were set up with combinations of temperatures and voltages to satisfy these objectives.

The cells at room temperature and 85°C were intended for the demonstration data base and the cells at 100°C and above were intended for determining the acceleration factors. The cells at 2000 Vac, -40°C were used to test whether room temperature or -40°C cell was the worst case and then to profile data at this temperature.

Table 1. Stress Cell Matrix.

	-40°C	Room Temp. (25°C)	85°C	100°C	125°C	150°C
1000 Vac		✓	✓•		✓	✓
1500 Vac	✓					
1800 Vac		✓				
2000 Vac	✓			✓	✓	✓
2500 Vac	✓	✓				
3000 Vac	✓				✓	✓
3800 Vac						✓
4000 Vac	✓	✓				
5000 Vac		✓				
2000 Vdc			✓•		✓•	✓•
2500 Vdc						✓•
3000 Vdc			✓•			
4000 Vdc					✓•	
5000 Vdc		✓				✓•

✓ Indicates that a high-voltage stress test was conducted for a group of optocouplers.
• Indicates cells with input and output operating biases.

Only 8-pin P-DIP (7.62 mm wide), and SO-8 plastic optocouplers were used in the input-output high-voltage stress tests. The test units consisted of optocoupler and solid state relay samples from several product families. Refer to Figures 1, 2, and 3 for a full list of products that were subjected to these tests. In general, test units were conditioned prior to stress with a solder dip, 500 temperature cycles and 96 hours of pressure pot sequence. The SO-8 surface mount optocouplers were assembled on ceramic carriers and sent through an infra-red solder reflow process. The intent of the conditioning was to accelerate the aging of the optocoupler that would otherwise occur through its normal operating life.

Summary of Results of Input-Output High-Voltage Stress Tests

Input-Output Voltage-ac The insulation failure rate of optocouplers caused by partial discharge related wear-out was worse at -40°C than at room and higher temperatures. The -40°C wear out is accelerated by at least a factor of three over room temperature tests at the high-voltages.

There was no evidence of systematic parametric drift due to ac input-output voltage found

in the cells without operating bias. The failure rate with an operating bias is only slightly higher than for the test without the operating bias. The ac Endurance Voltage was set by the results of tests at -40°C as this condition defined the worst case. No failures occurred in all of the 1000 Vac stress cells for the full length of each test group. Some 1000 Vac stress tests were over 15,000 hours.

Input-Output Voltage-dc

The failure rate for dc input-output voltage stress is greater at high temperatures than at low temperatures. All the dc stress tests were conducted with an operating bias. No failures occurred in the 85°C, 2000 Vdc and 3000 Vdc cells for the entire test periods. Some of these cells were stressed over 5000 hours.

Recommended Operating Areas

Based on the high-voltage stress study conducted at HP, Endurance Voltage boundaries, and safe operating areas have been drawn up for different HP optocouplers. Figures 1, 2, and 3 show the recommended operating areas for input-output voltages that can be applied for three categories of HP optocouplers. Referring to Figures 1, 2, and 3, the safe operating region below 800 Vac is applicable for long-term continuous high-voltage stress. The safe operating region above 800 Vac is applicable only for transient voltages. The X-axis on these figures shows the maximum cumulative time that can be applied for the high-voltage stress. Exceeding this maximum cumulative time may cause either the optocoupler's insulation or its electrical functionality to fail. The safe operating region

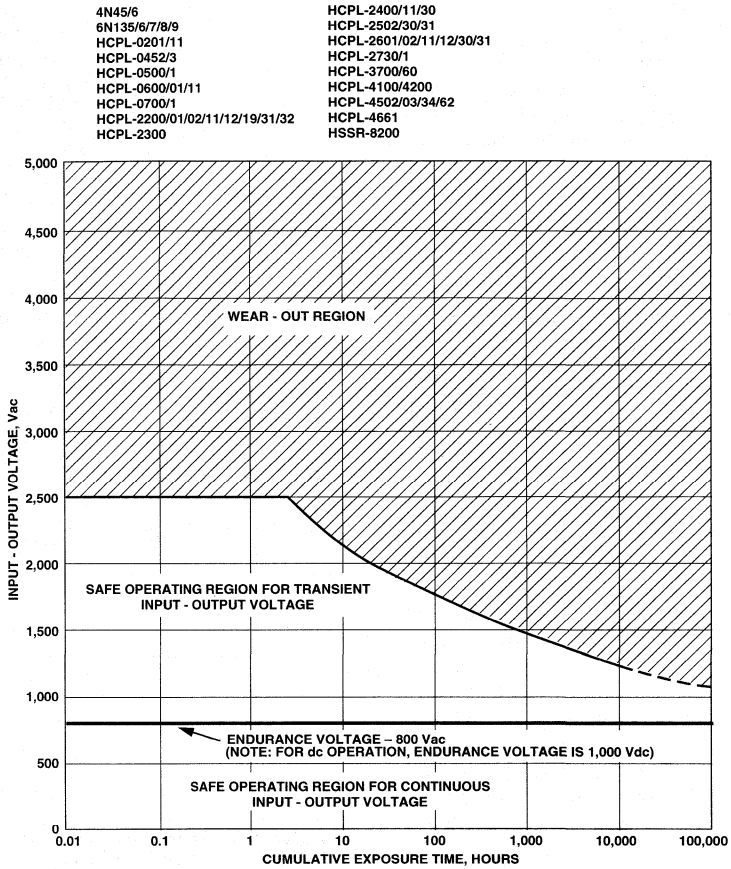

Figure 1. Recommended Safe Operating Area for Input-Output Voltage-Endurance Voltage for Category 1 Optocouplers.

guidelines are applicable when the optocoupler is used under normal conditions in a pollution free environment and within the maximum operating conditions. This includes operating the optocoupler within its specified ambient temperature range.

Although the HP time-to-failure tests were conducted at various temperature and voltage stress combinations after conditioning the test units to simulate end use with temperature cycling, solder processing and exposure to humidity, the test environment was relatively clean, where no condensation, precipitation or accumulation of corrosive or conductive material was expected. Consequently, the Endurance Voltage is primarily an indicator of internal characteristics. For the use of an optocoupler in specific equipment and environment, refer to the appropriate Safety Agencies such as UL and VDE for standards that determine the maximum allowable input-output voltages as defined by the Working Voltage. These standards generally consider attributes such as

arc track resistance, corrosion resistance, and physical dimensions (creepage and clearance) for determining the Working Voltage and the maximum transient input-output voltages.

The Endurance Voltage defines a stable region for operation. Operation within this region for input-output voltage and within the other recommended operating parameters, allows the optocoupler to maintain the performance specified within its data sheet. Operation above the optocoupler Endurance Voltage region may result in damage leading to failure of the optocoupler either in insulation or in electrical functioning.

Temperature is another key factor for operating life. The insulating materials within Hewlett-Packard plastic optocouplers are organic polymers and one would expect that an Arrhenius relationship exists between insulation life and temperature. However, the temperature characteristics are such that the life time of the optocoupler does not appear to be limited by the temperature induced insulation failures if the optocoupler is operated within the Endurance Voltage. This appears to be the case within the recommended operating region. But due to the construction of the optocoupler, a worst case condition exists at the coldest operating temperature that, in turn, defines the maximum acceptable ac Endurance Voltage.

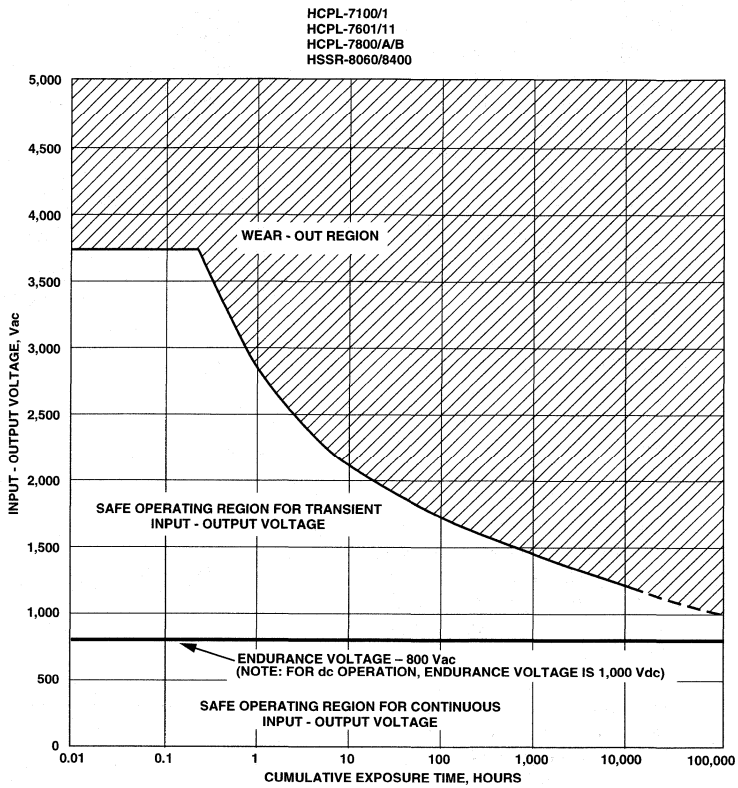

Figure 2. Recommended Safe Operating Area for Input-Output Voltage-Endurance Voltage for Category 2 Optocouplers.

Conclusion

Technical data specified on an HP optocoupler is valid at the time of shipment from HP's factory, or at the beginning of product life. Just like any semiconductor product, an optocoupler can potentially have some parameters degrade over the life of the product even though the optocoupler continues to be functional. The circuit designer who uses an optocoupler must consider any parameter that is likely to degrade over the product life, and must design sufficient margin so that the optocoupler still functions. This application note specifically addresses the insulation capability of an optocoupler as measured by a term called Endurance Voltage. The Endurance Voltage of an optocoupler is defined as the maximum voltage that can be applied between the input and output of an optocoupler for extended periods of time without causing functional failure of the optocoupler. By following the Endurance Voltage guidelines shown in Figures 1, 2, and 3, the optocoupler can be operated

normally for its useful life without unduly increasing the risk of insulation or electrical failure.

Always take the Endurance Voltage guideline as having a lower precedence to the Safety Agency and equipment use standards such as Working Voltage. The Endurance Voltage guideline is applicable in a pollution free laboratory environment and is useful for determining the likelihood of failure of an optocoupler's insulation or electrical operation. The HP optocouplers tested in this study have been proved to withstand a continuous voltage of either 800 Vac, or 1000 Vdc, and this allows HP optocouplers to be safely used in a wide array of industrial applications.

WARNING: ***In all cases where regulatory compliance is required, Working Voltage sets the maximum allowable steady state input-output voltage. Working Voltage cannot be exceeded in a design that has to meet regulatory requirements.***

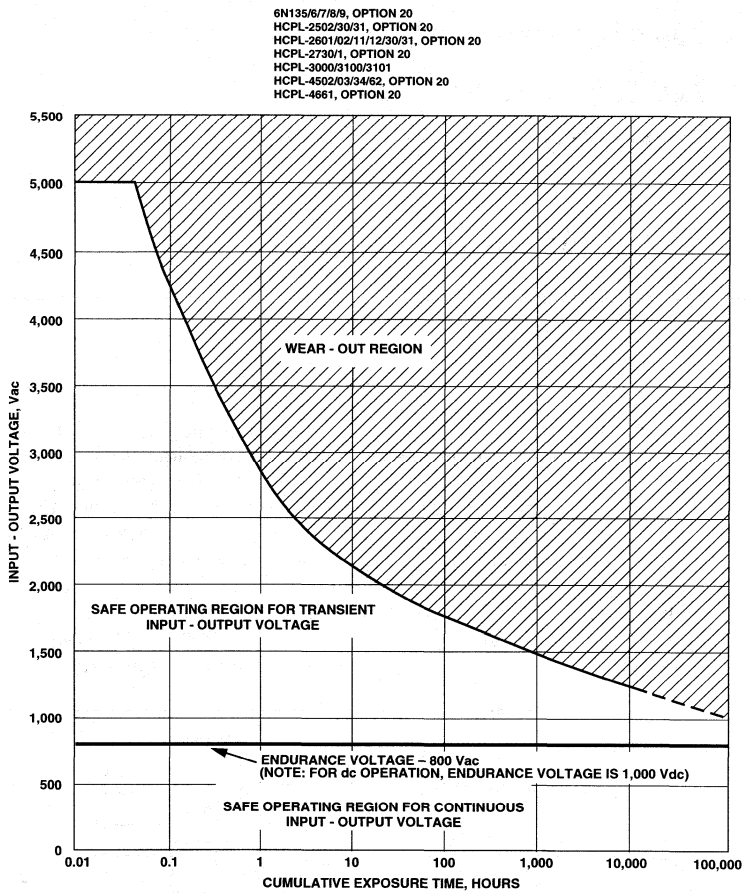

Figure 3. Recommended Safe Operating Area for Input-Output Voltage-Endurance Voltage for Category 3 Optocouplers.

HEWLETT® PACKARD

Designing with Hewlett-Packard Isolation Amplifiers

Application Note 1078

Introduction

One of the more difficult problems that designers may face is trying to isolate precision analog signals in an extremely noisy environment. A good example is monitoring the motor phase current in a high-performance motor drive. A typical three-phase induction motor drive, shown in Figure 1, first rectifies and filters the three-phase AC line voltage to obtain a high-voltage DC power supply; the output transistors then invert the DC supply voltage back into an AC signal to drive the three-phase induction motor. The motor drive commonly uses pulse-width modulation (PWM) to generate a variable voltage, variable frequency drive signal for the motor. High performance motor drives usually incorporate some form of current sensing in their design. The difficulty in isolating precision analog signals arises from the large voltage transients that are generated by the

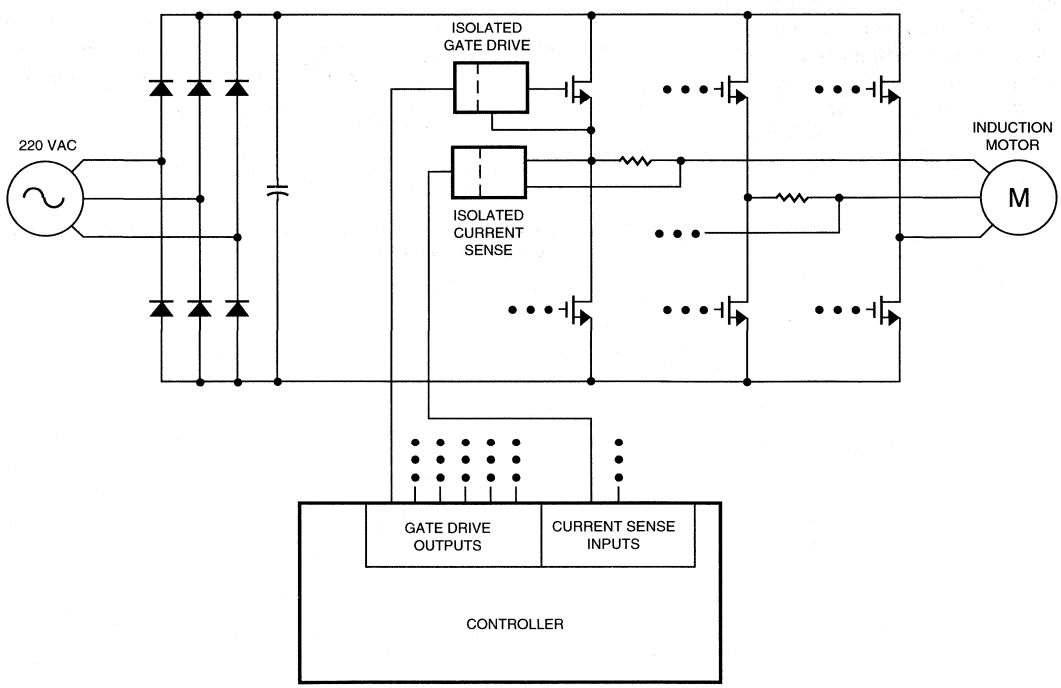

Figure 1. Typical Three-Phase AC Induction Motor Drive.

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switching of the inverter transistors. These very large transients (at least equal in amplitude to the DC supply voltage) can exhibit extremely fast rates of rise (greater than 10 kV/μs), making it extremely difficult to sense the current flowing through each of the motor phases.

Hewlett-Packard's line of isolation amplifiers was specifically developed as a compact low-cost solution for just this type of design problem; these isolation amplifiers allow designers to sense current in extremely noisy environments while maintaining excellent gain and offset accuracy. They exhibit outstanding stability over both time and temperature, as well as unequaled common-mode transient noise rejection (CMR). The small input voltage range helps minimize power dissipation in the current-sensing resistor (current shunt), and both positive and negative input voltages can be sensed with only a single +5V input power supply.

Compared to Hall-effect sensors, another commonly used current-sensing device, Hewlett-Packard's isolation amplifiers have excellent gain and offset characteristics, including very low drift over temperature. In addition, they exhibit superior common-mode transient noise immunity, are not affected by external magnetic fields, and do not exhibit residual magnetization effects that can affect offset. They are also easily mounted on a printed circuit board and are very flexible for designers to use. This flexibility allows the same circuit and layout to be used to sense different current ranges simply by substituting different current-sensing resistors. These features make the Hewlett-Packard line of isolation amplifiers an excellent choice for sensing current in many different applications.

Functional Description

Figure 2 shows the primary functional blocks of the HCPL-7820, a representative Hewlett-Packard isolation amplifier. In operation, the sigma-delta modulator converts the analog input signal into a high-speed serial bit stream; the time average of the bit stream is directly proportional to the input signal, as shown in Figure 3. This high-speed stream of digital data is encoded and optically transmitted to the detector circuit. The detected signal is decoded and converted back into an analog signal, which is filtered to obtain the final output signal.

In the sigma-delta modulator, the input signal is sampled at a very high rate (5-10 million samples per second) using a switched-capacitor circuit similar to that shown in Figure 4. Because the input sampling capacitors need to fully charge within only one half of a clock cycle, the peak input current of the isolation amplifier can be much larger than the average input current. These peak input currents are the primary reason for the recommended bypass capacitors at the inputs of the isolation amplifier.

The input bypass capacitors also form part of a simple anti-aliasing filter, which is recommended to prevent high-frequency noise from aliasing down to lower frequencies and interfering with the input signal.

Hewlett-Packard isolation amplifiers incorporate additional features specifically designed to improve their performance in current-sensing applications, particularly in motor drives.

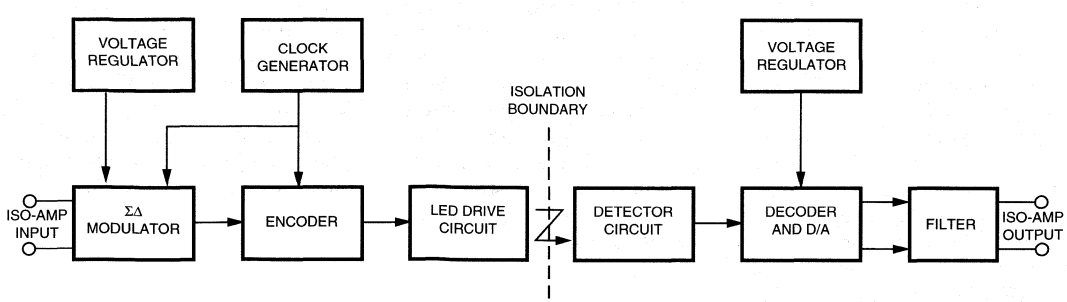


Figure 2. HCPL-7820 Block Diagram.

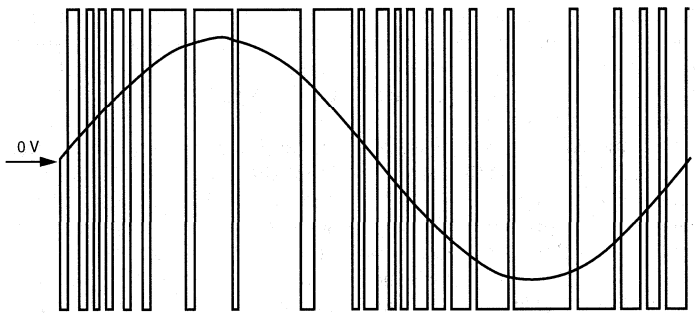


Figure 3. Example Sigma-Delta Modulation.

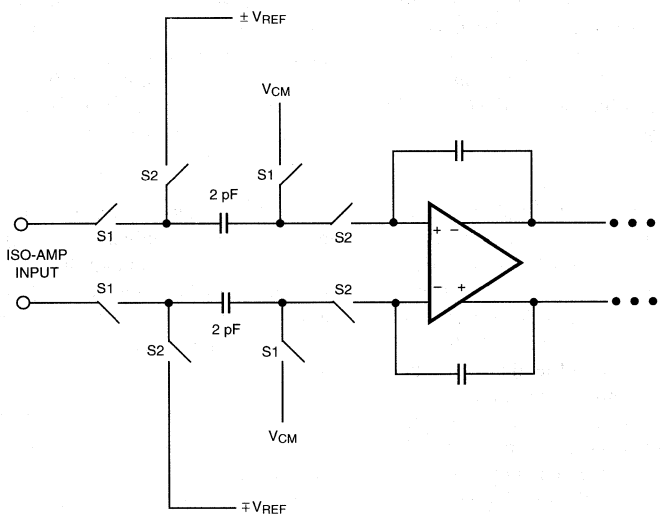


Figure 4. Input Sampling Network.

Chopper stabilization of all critical internal amplifiers and a fully differential circuit topology allow operation with small full-scale input voltages while maintaining excellent input offset and offset drift performance. Small input voltages help to minimize power dissipation in the external current sensing resistor. In addition, a unique input circuit allows accurate sensing of input signals below ground, eliminating the need for split supplies for the input circuit and allowing the use of a single +5 V supply.

Application Circuit

The recommended application circuit is shown in Figure 5. A floating power supply (which in many applications could be the same supply that is used to drive the high-side power transistor) is regulated to 5 V using a simple three-terminal voltage regulator (U1). The voltage from the current sensing resistor or shunt (Rsense) is applied to the input of the HCPL-7820 (U2) through an RC anti-aliasing filter (R5 and C3). And finally, the differential output of the isolation amplifier is converted to a ground-referenced single-ended output voltage with a simple differential amplifier circuit (U3 and associated components). Although the application circuit is relatively simple, a few recommendations should be followed to ensure optimal performance.

Supplies and Bypassing

The power supply for the isolation amplifier is most often obtained from the same supply used to power the power transistor gate drive circuit. If a dedicated supply is required, in many cases it is possible to add an additional winding on an existing transformer. Otherwise, some sort of simple isolated supply can be used, such as a line powered transformer or a high-frequency DC-DC converter.

As mentioned above, an inexpensive 78L05 three-terminal regulator (U1) can be used to reduce the gate-drive power supply voltage to 5 V. To help attenuate high-frequency power supply noise or ripple, a resistor or inductor can be used in series with the input of the regulator to form a low-pass filter with the regulator's input bypass capacitor.

As shown in Figure 5, 0.1 µF bypass capacitors (C2 and C4) should be located as close as possible to the input and output power-supply pins of the isolation amplifier (U2). The bypass capacitors are required because of the high-speed digital nature of the signals inside the isolation

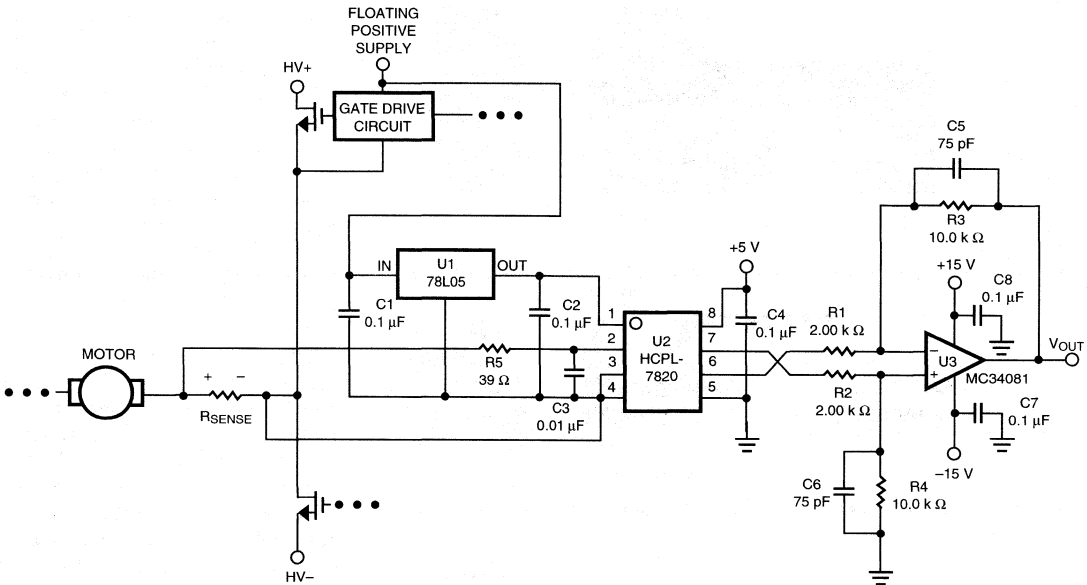


Figure 5. Recommended Application Circuit for the HCPL-7820.

amplifier. A 0.01 µF bypass capacitor (C3) is also recommended at the input pin(s) due to the switched-capacitor nature of the input circuit.

The placement of the power-supply and input bypass capacitors can change the offset at the input of the isolation amplifier. This change in offset arises from inductive coupling between the input power-supply bypass capacitor and the input circuit, which includes the input bypass capacitor and the input leads of the isolation amplifier. A portion of the high-frequency power-supply bypass current is at the sampling frequency of the input signal; induced voltages at this frequency will alias down to DC, increasing the effective offset of the isolation amplifier. Because of this effect, metallic objects in close proximity to the input circuit can also affect the offset due to the permeability of the metal changing the relevant inductances.

Several steps can be taken to minimize the mutual coupling between these two parts of the circuit, thereby improving the offset performance of the design. Separate the two bypass capacitors (C2 and C3) as much as possible (even placing them on opposite sides of the printed circuit board), while keeping the total lead lengths, including traces, of each bypass capacitor less than 20 mm. The printed circuit (PC) board traces should be made as short as possible and placed close together or over a ground plane to minimize loop area and pickup of stray magnetic fields. Avoid using sockets, as they will typically increase both loop area and inductance. Finally, using capacitors with small body size and orienting them (C2 and C3) perpendicular to each other on the PC board can also help. Figure 6 shows an example through-hole PC board layout for the isolation amplifier input circuit which illustrates some of the suggestions described above. The layout shown in Figure 6 is meant for illustrative purposes and cannot be reproduced photographically to generate a working PC board.

It is also possible to utilize this mutual coupling to advantage. For example, the layout shown in Figure 6 can be modified to enhance the inductive coupling in such a way as to minimize offset drift over temperature, as shown in Figure 7. The objective of this layout is to cancel the mutual coupling effects as much as possible. To accomplish this, the input leads cross over each other close to the package and then form a loop with the input bypass capacitor (C3). This input loop is inside of another loop formed by the power supply traces and

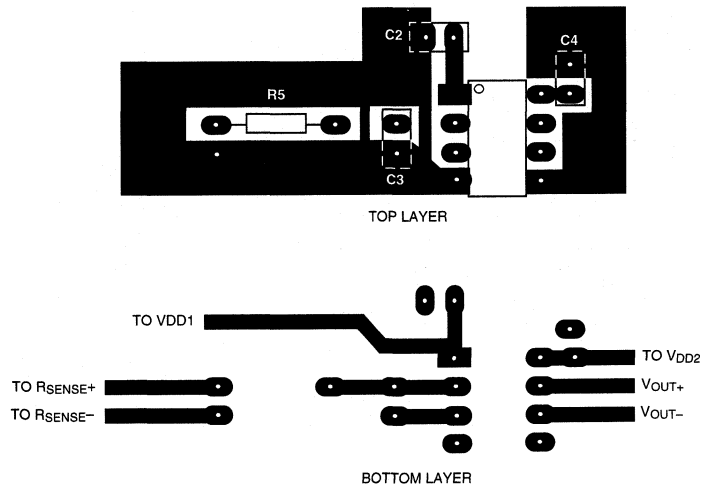


Figure 6. Example PC Board Layout for Isolation Amplifier Input Circuit.

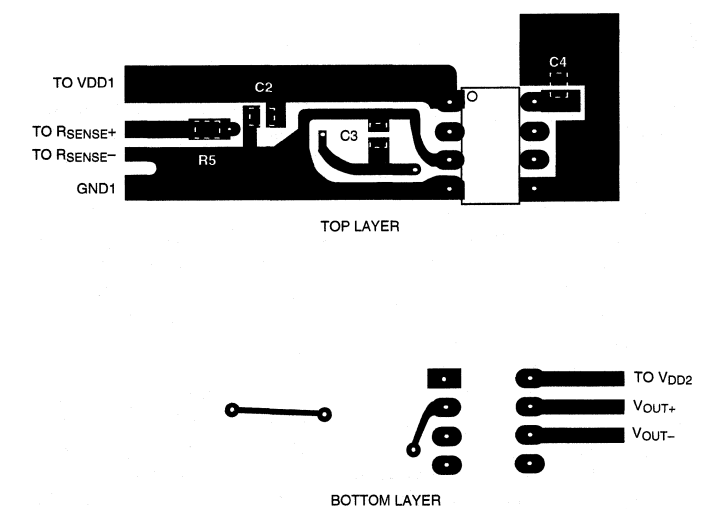


Figure 7. Example Surface-Mount PC Board Layout to Minimize Offset Tempco.

the power supply bypass capacitor (C2). The polarity of the coupling between these two loops is such that it tends to cancel the undesirable mutual coupling effects described above. By adjusting the area of the inner loop (e.g., by shifting the position of the input bypass capacitor left or right on the layout), the amount of coupling can be varied to achieve the correct amount of cancellation. This method of offset tempco cancellation can shift the mean tempco of a group of devices closer to zero, but cannot perfectly cancel the tempco for every device due to part-to-part variations. The offset tempco can typically be reduced by a factor of two or more. Unfortunately, this reduction in offset drift comes at the price of a slight increase in initial offset, on the order of 1-2 mV of additional offset for the HCPL-7820. Similar to Figure 6, the layout in Figure 7 is meant for illustrative purposes only.

Shunt Resistors

The current-sensing shunt resistor should have low resistance (to minimize power dissipation), low inductance (to minimize di/dt induced voltage spikes which could adversely affect operation), and reasonable tolerance (to maintain overall circuit accuracy). Choosing a particular value for the shunt is usually a compromise between minimizing power dissipation and maximizing accuracy. Smaller shunt resistances decrease power dissipation, while larger shunt resistances can improve circuit accuracy by utilizing the full input range of the isolation amplifier.

The first step in selecting a shunt is determining how much current the shunt will be sensing. The graph in Figure 8 shows the RMS current in each phase of a three-phase induction motor as a function of average motor output power (in horsepower, hp) and motor drive supply voltage. The maximum value of the shunt is determined by the current being measured and the maximum recommended input voltage of the isolation amplifier. The maximum shunt resistance can be calculated by taking the maximum recommended input voltage and dividing by the peak current that

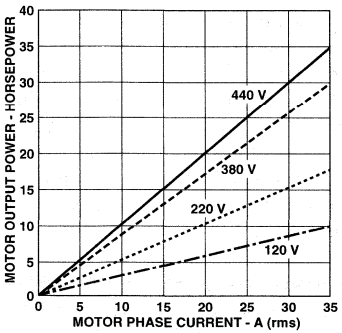


Figure 8. Motor Output Horsepower vs. Motor Phase Current and Supply Voltage.

the shunt should see during normal operation. For example, if a motor will have a maximum RMS current of 10 A and can experience up to 50% overloads during normal operation, then the peak current is 21.1 A (= 10 • 1.414 • 1.5). Assuming a maximum input voltage of 200 mV, the maximum value of shunt resistance in this case would be about 10 mΩ.

The maximum average power dissipation in the shunt can also be easily calculated by multiplying the shunt resistance times the square of the maximum RMS current, which is about 1 W in the previous example.

If the power dissipation in the shunt is too high, the resistance of the shunt can be decreased below the maximum value to decrease power dissipation. The minimum value of the shunt is limited by precision and accuracy requirements of the design. As the shunt value is reduced, the output voltage across the shunt is also reduced, which means that the offset and noise of the isolation amplifier, which are fixed, become a larger percentage of the signal amplitude.

Usually, the actual value of the shunt will fall somewhere between the minimum and maximum values, depending on the particular requirements of a specific design.

Hewlett-Packard recommends four different two-terminal shunts from Dale which can be used to sense average currents in motor drives up to 35 A and 35 hp. Table 1 shows the maximum current and horsepower range for each of the recommended LVR-series shunts. Even higher currents can be sensed with lower value four-terminal shunts available from vendors such as Dale, IRC, and Isotek (Isabellenhuette); it is also possible to make your own four-terminal shunts by stamping out an appropriate pattern from a sheet of metal alloy that has a low temperature coefficient.

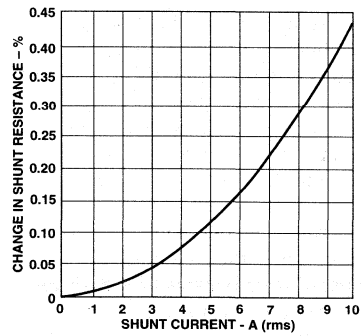


Figure 9. LVR Shunt Resistance Change vs. Shunt Current.

When sensing currents large enough to cause significant heating of the shunt, the temperature coefficient (tempco) of the shunt can introduce nonlinearity due to the signal dependent temperature rise of the shunt. For example, Figure 9 shows how the resistance of the LVR shunt resistors typically changes as a function of average current flowing through it with the shunt mounted in a typical PC board configuration. Although the effect shown in Figure 9 is relatively small, it increases as the shunt-to-ambient thermal resistance increases. This effect can be minimized either by reducing the thermal

Table 1. Current Shunt Summary.

Shunt Resistor Part Number	Shunt Resistance	Tolerance	Maximum Power Dissipation	Maximum RMS Current	Maximum Horsepower Range
LVR-3.05-1%	50 mΩ	1%	3 W	8 A	0.8 - 3.0 hp
LVR-3.02-1%	20 mΩ	1%	3 W	8 A	2.2 - 8.0 hp
LVR-3.01-1%	10 mΩ	1%	3 W	15 A	4.1 - 15 hp
LVR-5.005-1%	5 mΩ	1%	5 W	35 A	9.6 - 35 hp

resistance of the shunt or by using a shunt with a lower tempco. Lowering the thermal resistance can sometimes be as easy as repositioning the shunt on the PC board, or it might sometimes require the use of a heat sink.

As the value of shunt resistance decreases, the resistance of the shunt leads becomes a significant percentage of the total shunt resistance. This has two primary effects on shunt accuracy. First, the effective resistance of the shunt can become dependent on factors such as how long the leads are, how they are bent, how far they are inserted into the board, and how far solder wicks up the lead during assembly (these issues will be discussed in more detail shortly). Second, the leads are typically made from a material, such as copper, which has a much higher tempco than the material from which the resistive element itself is made, resulting in a higher tempco for the shunt overall.

Both of these effects are eliminated when a four-terminal shunt is used. A four-terminal shunt has two additional terminals that are Kelvin-connected directly across the resistive element itself; these two terminals are used to monitor the voltage across the resistive element while the other two terminals are used to carry the load current. Because of the Kelvin connection, any voltage drops across the leads carrying the load current will have little, if any, impact on the measured voltage.

Although four-terminal shunts can perform better than two-terminal shunts, they are more expensive, generally limiting their use to higher precision applications.

Two-terminal shunts, however, can deliver good performance when they are used properly. One of the most difficult aspects of using a two-terminal shunt is achieving an accurate, repeatable connection to the shunt, which is typically mounted on a PC board. Figure 10 shows an illustrative example of a PC board layout that can achieve good performance with two-terminal shunts with resistances down to about 5 mΩ.

There are several things to note about this layout. Two "quasi-Kelvin" connections are provided to make as close to a point contact as possible to the shunt leads where they contact the PC board. The quasi-Kelvin connections are brought together under the body of the shunt and then run very close to each other to the input of the isolation amplifier; this minimizes the loop area of the connection and reduces the possibility of stray magnetic fields (of which there are plenty in a motor drive) from interfering with the measured signal. If the shunt is not located on the same PC board as the isolation amplifier circuit, a tightly twisted pair of wires can accomplish the same thing.

Also note that both sides of the PC board are used to increase current carrying capacity. Numerous plated-through vias (shown as circles with a center cross in Figure 10) surround each terminal of the shunt to help distribute the current between the two sides of the PC board. The PC board should use 2 or 4 oz. copper for the two layers, resulting in a current carrying capacity of 10 to 20 A. Making the current carrying traces on the PC board fairly large can improve the shunt's power dissipation capability by acting

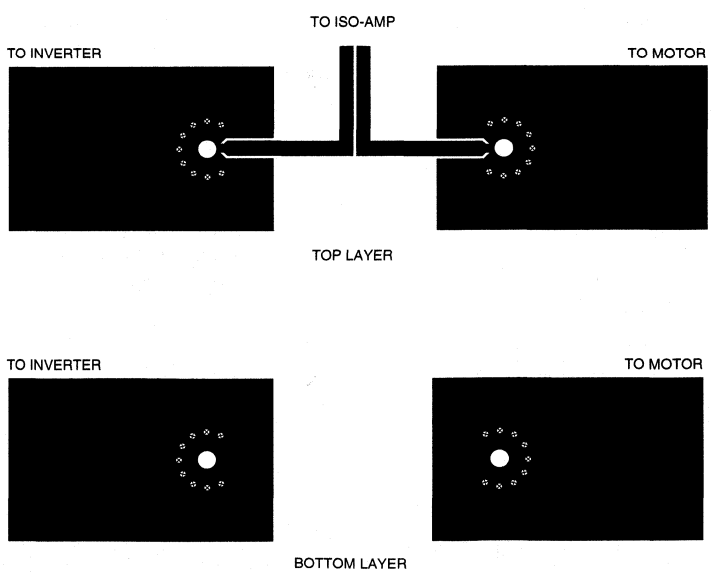


Figure 10. Example PC Board Layout for Two-Terminal Shunt.

as a heat sink. Liberal use of vias where the load current enters and exits the PC board is also recommended for the same reasons they are recommended for use at the shunt.

The final recommendation regarding the use of two-terminal shunts is to ensure that the leads of the shunt are consistently bent in the same way and inserted into the PC board the same distance every time. This is usually not a problem for automated assembly, but it could be for low-volume hand-assembled boards. For hand-assembled boards, a lead bending jig should be used and care should be taken that the shunt is inserted all the way into the board every time, minimizing any variability in the length of each shunt's leads.

An alternative to using shunts for measuring large AC currents is to use an inexpensive current transformer connected to the input of the isolation amplifier, as shown in Figure 11. Using a transformer is less invasive than a current shunt and can significantly reduce power dissipation when measuring large currents (greater than 50 A). Because the isolation amplifier is providing the primary isolation barrier, a low-cost current transformer can be used that has little or no isolation of its own.

Shunt Connections

The recommended method for connecting the isolation amplifier to the shunt resistor is shown in Figure 5. V_{IN+} (pin 2 of the HPCL-7820) is connected to the positive terminal of the shunt resistor, while V_{IN-}(pin 3) is shorted to GND1 (pin 4), with the power-supply return path functioning as the sense line to the negative terminal of the current shunt. This allows a single pair of wires or PC board traces to connect the isolation amplifier circuit to the shunt resistor. By referencing the input circuit to the negative side of the sense resistor, any load current induced noise transients on the shunt are seen as a common-mode signal and will not interfere with the current-sense signal. This is important because the large load currents flowing through the motor drive, along with the parasitic inductances inherent in the wiring of the circuit, can generate both noise spikes and offsets that are relatively large compared to the small voltages that are being measured across the current shunt.

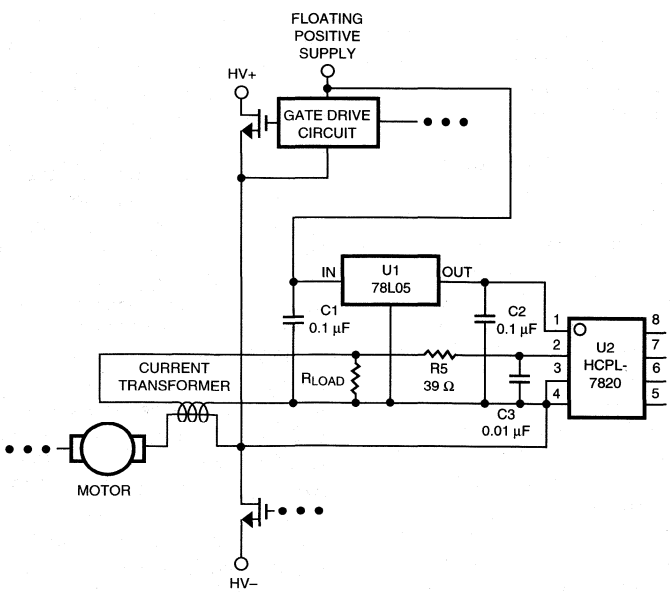


Figure 11. Using a Non-isolated Current Transformer to Measure Large AC Currents.

If the same power supply is used both for the gate drive circuit and for the current sensing circuit, it is very important that the connection from GND1 of the isolation amplifier to the sense resistor be the ***only*** return path for supply current to the gate drive power supply in order to eliminate potential ground loop problems. The only direct connection between the isolation amplifier circuit and the gate drive circuit should be the floating positive power supply line.

In some applications, however, supply currents flowing through the power-supply return path may cause offset or noise problems. In this case, better performance may be obtained by connecting V_{IN+} and V_{IN-} directly across the shunt resistor with two conductors, and connecting GND1 to the shunt resistor with a third conductor for the power-supply return path, as shown in Figure 12. When connected this way, both input

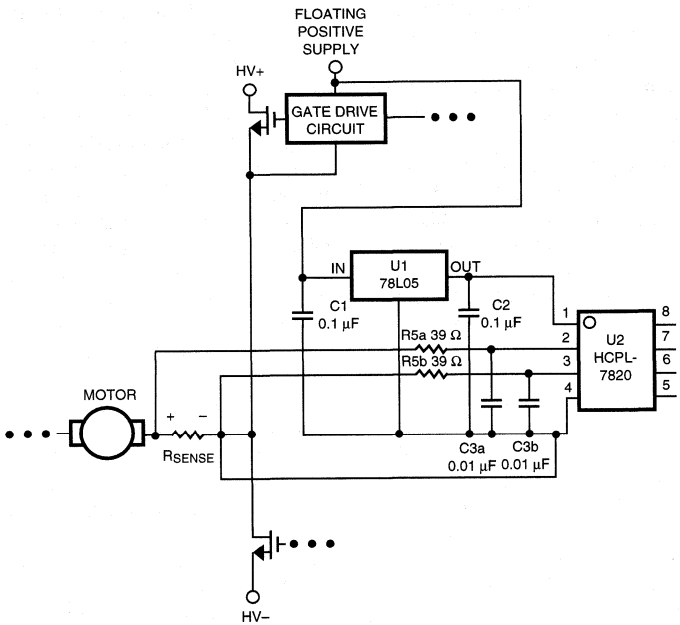


Figure 12. Schematic for Three-Conductor Shunt Connection.

pins should be bypassed. To minimize electro-magnetic interference of the sense signal, all of the conductors (whether two or three are used) connecting the isolation amplifier to the sense resistor should be either twisted pair wire or closely spaced traces on a PC board.

The 39 Ω resistor in series with the input lead (R5) forms a low-pass anti-aliasing filter with the 0.01 µF input bypass capacitor (C3) with a 400 kHz bandwidth. The resistor performs another important function as well; it dampens any ringing which might be present in the circuit formed by the shunt, the input bypass capacitor, and the inductance of wires or traces connecting the two. Undamped ringing of the input circuit near the input sampling frequency can alias into the baseband producing what might appear to be noise at the output of the device.

PC Board Layout

In addition to affecting offset, the layout of the PC board can also affect the common mode rejection (CMR) performance of the isolation amplifier, due primarily to stray capacitive coupling between the input and the output circuits. To obtain optimal CMR performance, the layout of the PC board should minimize any stray coupling by maintaining the maximum possible distance between the input and output sides of the circuit and ensuring that any ground plane on the PC board does not pass directly below or extend much wider than the body of the isolation amplifier. Using surface-mount components can help achieve many of the PC board objectives discussed in the preceding paragraphs. An example through-hole PC board layout illustrating some of the more important layout recommendations is shown in Figure 6. Note that the ground plane does not extend directly below the body of the isolation amplifier.

A surface-mount layout of the complete application circuit shown in Figure 5 is available from the Hewlett-Packard Applications Engineering Department; the size of the layout, including shunt resistor, is approximately 3 cm square. Contact your local HP sales office for more information.

Post-Amplifier Circuit

The recommended application circuit shown in Figure 5 includes a post-amplifier circuit that serves three functions: to reference the output signal to the desired level (usually ground), to amplify the signal to appropriate levels, and to help filter output noise. The particular op-amp used in the post-amplifier circuit is not critical; however, it should have low enough offset and high enough bandwidth and slew rate so that it does not adversely affect circuit performance. The maximum offset of the op-amp should be low relative to the output offset of the HCPL-7820, or less than about 5 mV. The gain is determined by resistors R1 through R4; assuming that R1 = R2 and R3 = R4, the gain of the post-amplifier is R3/R1.

To maintain the fastest overall circuit bandwidth and speed, the post-amplifier circuit should

have a bandwidth at least twice the minimum bandwidth of the isolation amplifier, or about 400 kHz; lower bandwidths can be used to decrease output noise at the expense of slower response times. If capacitors C5 and C6 are not used in the post-amplifier circuit, the post-amplifier bandwidth is determined by the gain-bandwidth product (GBW) of the op-amp. To obtain a bandwidth of 400 kHz with a gain of 5, the op-amp should have a GBW greater than 2 MHz. Using the op-amp GBW to set the overall circuit bandwidth is generally not a very good idea because the op-amp GBW is usually specified only as a typical, with no guaranteed values.

More accurate control of the post-amplifier circuit bandwidth can be achieved by using capacitors C5 and C6 to form a single-pole low-pass filter with a nominal bandwidth of $1/(2 \cdot \pi \cdot R3 \cdot C5)$, assuming that R3 = R4 and C5 = C6. These capacitors allow the bandwidth of the post-amplifier to be adjusted independently of the gain and are useful for reducing the output noise of the isolation amplifier.

To accurately set the low-pass filter frequency using C5 and C6, the op-amp should have a specified GBW greater than approximately ten times the product of the post-amplifier gain and the desired low-pass frequency; a GBW lower than that would change the low-pass frequency by more than 10 - 15%. For a post-amplifier gain of 5 and a low-pass frequency of 200 kHz, the GBW of the op-amp should be at least 7 - 10 MHz. The component values shown in Figure 5 form a differential amplifier with a gain of 5 and a cutoff frequency of approximately 200 kHz and were chosen as a compromise between low noise and fast response times. The overall recommended application circuit, including a typical isolation amplifier, has a bandwidth of about 130 kHz, a rise time of 2.6 µs and delay to 90% of 4.2 µs.

In addition to having enough bandwidth, the op-amp should have adequate slew rate to accurately reproduce large amplitude waveforms. The required slew rate can be conservatively estimated by dividing the maximum expected voltage swing at the output of the amplifier circuit by the filter time constant, which is equal to the product of R3 and C5. This estimate is more conservative at higher filter bandwidths because the overall response time of the circuit is then dominated by the response time of the isolation amplifier. For example, assuming a ± 200 mV input swing, a post-amplifier gain of 5 and a filter bandwidth of 200 kHz, the required slew rate of the op-amp is estimated to be approximately 20 V/µs, whereas less than 10V/µs is actually needed.

The gain-setting resistors in the post-amp should have a tolerance of 1% or better to ensure adequate CMRR and gain tolerance for the overall circuit. Significant mismatch of the gain-setting resistors can degrade the CMRR of the post-amplifier, contributing to offset of the circuit. Figure 13 shows how much additional offset (referred to the input of the isolation amplifier, assuming an isolation amplifier gain of 8) can be expected versus post-amplifier gain for different values of resistor tolerance. Shown in Figure 13 is the standard

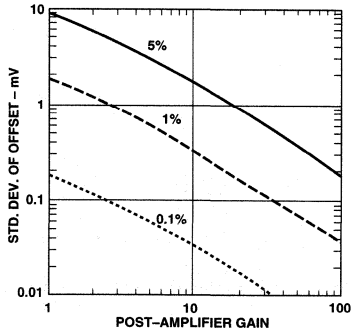


Figure 13. Standard Deviation of Post-amplifier Input-referred Offset vs. Post-amplifier Gain and Resistor Tolerance.

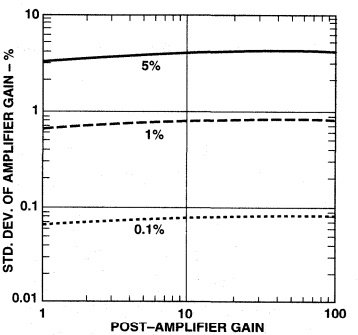


Figure 14. Standard Deviation of Post-amplifier Gain vs. Post-amplifier Gain and Resistor Tolerance.

deviation of the resulting distribution of input offsets; the mean of the distribution is zero, as would be expected from a differential amplifier circuit. In a similar way, Figure 14 shows how much additional gain tolerance the post-amplifier contributes to the overall circuit versus post-amplifier gain for different values of resistor tolerance. Figure 14 indicates the standard deviation of the resulting gain distribution of the post-amplifier circuit. The data in

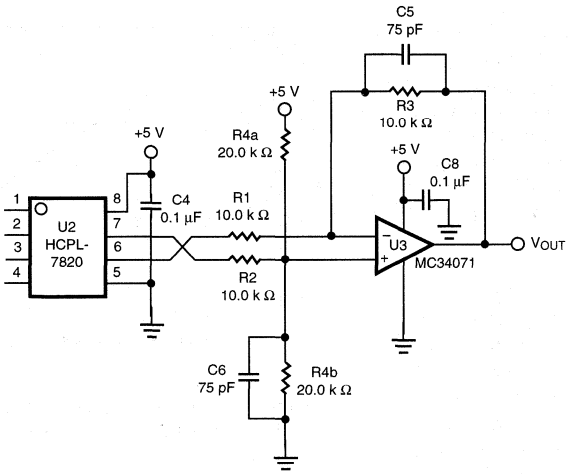


Figure 15. Single-supply Post-amplifier Circuit for HCPL-7820.

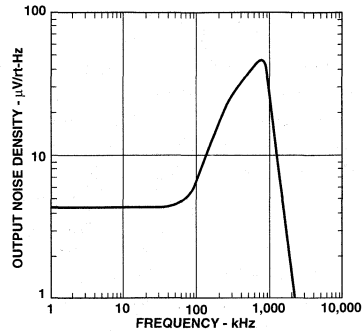


Figure 16. HCPL-7820 Output Noise Spectrum.

Figures 13 and 14 were generated by Monte Carlo simulation and conservatively assume that resistor values are uniformly distributed around their nominal value. Resistor networks with very tight ratio tolerances, from suppliers such as Dale, can be used which offer excellent performance as well as reduced component count and board space.

The post-amplifier circuit can be easily modified to allow for single-supply operation. Figure 15 shows a schematic for a post-amplifier for use in 5 V single-supply applications. One additional resistor (R4a) is needed and the gain is decreased to allow circuit operation over the full input voltage range. Adding the resistor shifts the output reference voltage from zero to one-half of the supply voltage.

Output Noise

The noise-shaping characteristic of the sigma-delta modulator results in a slightly unusual output noise spectrum, as shown in Figure 16 for the HCPL-7820. The noise spectrum is flat up to about 40 kHz, where it breaks up at 12 dB per octave. The internal filter begins to roll off the noise spectrum at about 200 kHz, with a steep drop just below 1 MHz. The shape of the noise spectrum has some implications regarding the most effective method of filtering output noise for a given signal bandwidth.

As mentioned before, reducing the bandwidth of the post-amplifier circuit reduces the amount of output noise (as well as increasing the response time). Due to the increasing noise behavior above 40 kHz, a second-order filter response can be much more effective at filtering noise than a first-order filter, depending on the particular filter bandwidth. Figure 17 shows how the output noise changes as a function of the post-amplifier bandwidth for both first- and second-order filter responses. The application circuit shown in Figure 5 exhibits a first-order low-pass filter characteristic. By adding two additional resistors and a capacitor (R1a, R2a and C9), as shown in Figure 18, a second-order filter response can be obtained. Capacitor C9 should be chosen so that the product of R1a and C9 is equal to the product of R3 and C5.

Changing the bandwidth of the post-amplifier will also affect the delay of the circuit. Figure 17 also indicates how the delay (to 90%) of the application circuit changes as a function of the post-amplifier bandwidth for both first- and second-order filter responses. From this graph it is easy to determine the trade-offs between output noise, circuit delay and amplifier bandwidth.

The output noise of the modulator is also affected by the amplitude of the input signal. Figure 19 shows the relative amplitude of the RMS output voltage versus the DC input voltage. The curve is relatively flat out to about ± 200 mV and increases rapidly for input signals larger than that. The increase in noise with amplitude is independent of the output filter bandwidth.

The statistical characteristics (probability density function) of the output noise are important when the isolation amplifier is used to sense an overload or fault condition and you need to determine how close the signal can get to the threshold before you start to get false overload indications. The output noise of the isolation amplifier is nearly gaussian when the input voltage is near zero. As the input voltage moves away from zero, the noise becomes less gaussian, with the tails of the probability distribution function lengthening in the direction of mid-scale and shortening in the direction of full-scale, as shown in Figure 20. For the HCPL-7820, Figure 21 shows how much above a particular DC input the fault detection threshold (input referred) should be for different levels of false alarm probability. For example, to limit the probability of a false alarm to 0.01% for a 200 mV input, the fault detection threshold should be at least 214 mV (a 14 mV threshold margin). The maximum recommended fault detection threshold is about 275 mV.

To reduce offset in some applications, the offset is measured by a microprocessor at power-up and then subtracted from every subsequent measurement. For

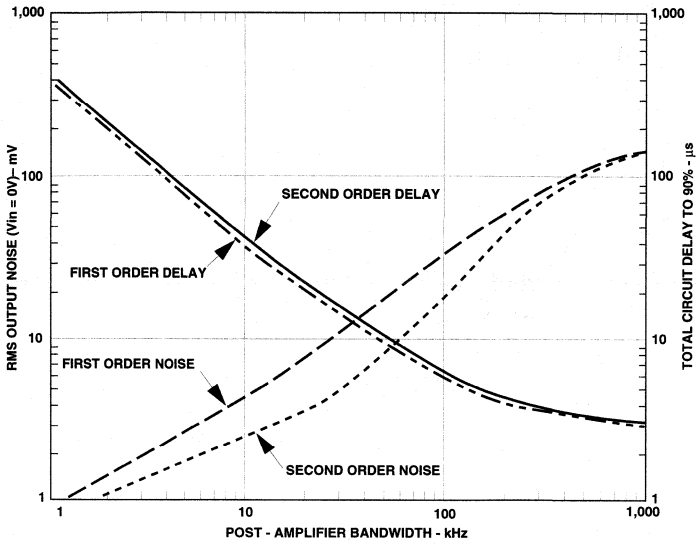


Figure 17. RMS Output Noise and Delay of the HCPL-7820 Application Circuit vs. Post-amplifier Bandwidth and Filter Order.

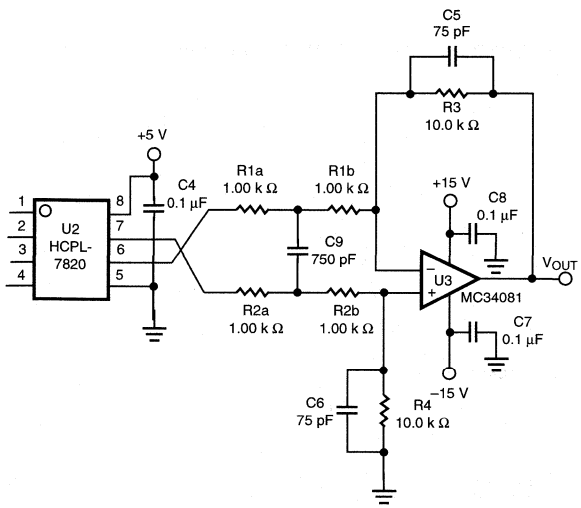


Figure 18. Post-amplifier Circuit with Second-order Filter Response.

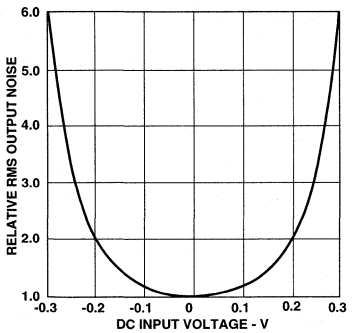


Figure 19. Relative Output Noise vs. DC Input Voltage.

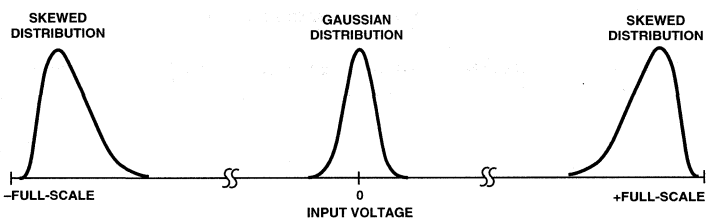


Figure 20. Noise Statistical Characteristics vs. Input Voltage.

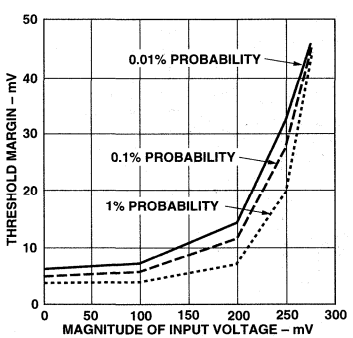


Figure 21. HCPL-7820 Threshold Detection Margin vs. Input Voltage and False Alarm Probability.

these types of auto-calibration applications, accuracy can be improved by waiting until the internal junction temperature stabilizes before measuring the offset of the isolation amplifier. For example, the HCPL-7820 has an offset drift at power-up of about 100 μV with a time constant of approximately 15 seconds when mounted on a relatively small evaluation board. Accuracy can also be improved by additional filtering or averaging of the measured signal to reduce any noise during the auto-calibration procedure.

Voltage Sensing

Hewlett-Packard isolation amplifiers can also be used to isolate signals with amplitudes larger than its recommended input range with the use of a resistive voltage divider at its input. The only restrictions are that the impedance of the divider be relatively small (less than 1 kΩ) so that the input resistance (280 kΩ) and input bias current (1 μA) of the isolation amplifier do not affect the accuracy of the measurement. An input bypass capacitor is still required, although the 39 Ω series damping resistor is not (the resistance of the voltage divider provides the same function). The low-pass filter formed by the divider resistance and the input bypass capacitor may limit the achievable bandwidth. To obtain higher bandwidths, the input bypass capacitor (C3) can be reduced, but it should not be reduced much below 1000 pF to maintain gain accuracy of the isolation amplifier.

SPICE Models

SPICE models for Hewlett-Packard isolation amplifiers are available from the HP Applications Engineering Department. Contact your local HP sales office for more information.

Thermal Data for Optocouplers

Application Note 1087

Introduction

This document contains steady state thermal models for optocouplers based on empirical data and theoretical extrapolation. Five thermal models have been chosen to suit the type of optocoupler:

- Thermal Model-A for a hermetic-package optocoupler
- Thermal Model-B for a single-channel plastic-package optocoupler
- Thermal Model-C for a single-channel HCPL-3700/60 optocoupler with a built-in buffer circuit
- Thermal Model-D for a dual-channel plastic-package optocoupler
- Thermal Model-E for HCPL-7100/1 optocoupler

The thermal data in each of these models allows the user to calculate the approximate junction temperatures at various nodes in the optocoupler. The actual semiconductor junction temperatures may vary based upon the heat flows from the surrounding components on the printed circuit board. Each of the models assumes that the optocoupler is either soldered to a printed circuit board (PCB) or placed in a socket which is soldered on a PCB. The size of the PCB is approximately 7.5 cm x 7.5 cm, unless otherwise specified. The PCB is further assumed to be in still air. In models that define the optocoupler case to be a node, the case-to-ambient thermal resistance will depend on the board design and the placement of the optocoupler. The package case temperature is measured at the center of the package bottom.

The data presented in each of these models is approximate and is meant to be an indicator, not a specification. To ensure reliability, the semiconductor junction temperatures in plastic-package optocouplers must not exceed 125 °C, and in hermetic-package optocouplers it must not exceed 175 °C unless otherwise specified.

Optocoupler Thermal Model Index.

Part Number	Thermal Model Type	Comments
4N45/6	Model-B	Approximates 6N138 data
4N55	Model-A	
6N134	Model-A	
6N135/6/7/8/9	Model-B	
6N140	Model-A	
HCNW135/6/7, HCNW4502/3, HCNW2601/11	Model-B	
HCNW138/9, 4562	Model-B	Approximates HCNW135 data

(continued on next page)

Optocoupler Thermal Model Index (continued).

Part Number	Thermal Model Type	Comments
HCNW2201, 4504, 4506	Model-B	Approximates HCNW2601 data
HCPL-0452/3, -0500/1, -0600/01/11, -0700/1	Model-B	
HCPL-0530/1/4, -0630/1, -0730/1	Model-D	Approximates HCPL-2430 data, but all thermal coefficients to be scaled up by 50%
HCPL-0201/11, -0454, -0466	Model-B	Approximates HCPL-0600 data
HCPL-1930/1	Model-A	
HCPL-2200/01/02/11/12/19	Model-B	
HCPL-2231/2	Model-D	Approximates HCPL-2430 data
HCPL-2300	Model-B	Approximates HCPL-2601 data
HCPL-2400/11	Model-B	
HCPL-2430	Model-D	
HCPL-2502/3	Model-B	Approximates 6N135 data
HCPL-2530/1/3	Model-D	Approximates HCPL-2430 data
HCPL-2601/11/12	Model-B	Approximates 6N137 data
HCPL-2630/1, -2730/1	Model-D	Approximates HCPL-2430 data
HCPL-3000, 3100/1		Refer to Application Note 1058
HCPL-3120/50		Refer to HCPL-3120/50 data sheets
HCPL-3700/60	Model-C	
HCPL-4100/4200	Model-C	Approximates HCPL-3700 data
HCPL-4502/3/4/6	Model-B	Approximates 6N135 data
HCPL-4534	Model-D	Approximates HCPL-2430 data
HCPL-4562	Model-B	Approximates 6N135 data
HCPL-4661	Model-D	Approximates HCPL-2430 data
HCPL-4701	Model-B	Approximates 6N138 data
HCPL-4731	Model-D	Approximates HCPL-2430 data
HCPL-52XX, -54XX, -55XX, -56XX, -57XX, -62XX, -64XX, -65XX	Model-A	
HCPL-7100/1	Model-E	
HCPL-7601/11	Model-B	Approximates 6N137 data
HCPL-7800/20/25/40	Model-C	Approximates HCPL-3700 data
HSSR-7110/1		Refer to HSSR-7110/1 data sheet
HSSR-8060		Refer to HSSR-8060 data sheet
HSSR-8200	Model-B	Approximates HCPL-2200 data
HSSR-8400		Refer to HSSR-8400 data sheet

Thermal Model-A for a Hermetic-Package Optocoupler

Definitions

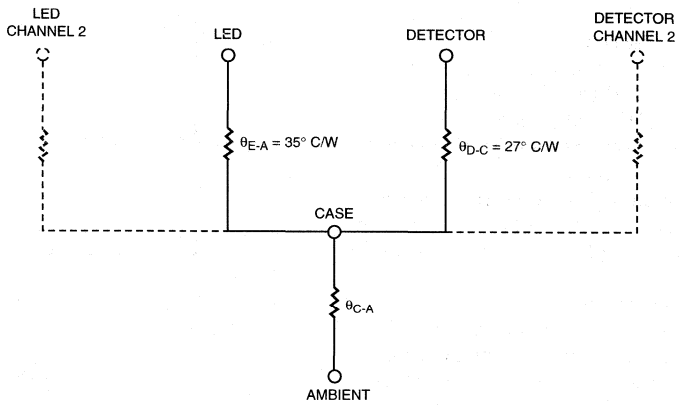
θ_{E-C}: Thermal impedance from emitter (input LED) junction to package case.

θ_{D-C}: Thermal impedance from detector (output IC) junction to package case.

θ_{C-A}: Thermal impedance from package case to ambient. The value θ_{C-A} depends on the heat flows from surrounding components, and can be estimated to be in the range of 70 °C/W to 210 °C/W (see Note 5).

Package Case Temperature: Measured at center of package bottom, with no forced air.

Ambient Temperature: Measured approximately 15 cm above the package.



Description

This thermal model assumes that an 8- or 16-pin dual-in-line package hermetic optocoupler is inserted into an IC socket which is soldered into a 7.5 cm x 7.5 cm printed circuit board (PCB). The PCB is suspended in still air. Thermal impedance values shown in the above figure can be used for calculating the temperatures at each node for a given operating condition. The thermal resistance between the LED and other internal nodes is very large in comparison with the terms shown in the figure, and is omitted for simplicity.

For optocouplers that have more than one channel, the same values for θ_{E-C} and θ_{D-C} can be assumed to be in parallel, as shown by the dotted lines, for each of the additional LED and detector. Again, the direct thermal impedance between any two LEDs, any two detectors, or an LED and a detector is very large in comparison to θ_{E-C} and θ_{D-C}, and may be omitted.

Notes:

1. Above model is applicable for HCPL-52XX, -54XX, -55XX, -56XX, -57XX, -62XX, 64XX, -65XX, -66XX, -67XX; 4N55; 6N134; and 6N140.
2. For HSSR-7100/1 thermal model, refer to its data sheet.
3. HCPL-193X and HCPL-576X have an input buffer IC. The above model may be used for these optocouplers with an assumption that the Input Buffer IC and LED are a common node. The thermal impedance of this common node to case is approximately 35 °C/W.
4. Maximum Junction Temperature for HSSR-7110/1: 150 °C; for all other hermetic optocouplers: 175 °C.
5. The thermal data in this model assumes the optocoupler is inserted into a socket. Thermal impedance θ_{C-A} is likely to be lower when the optocoupler is soldered to a printed circuit board.

Thermal Model-B for a Single-Channel Plastic-Package Optocoupler

Definitions

θ_1: Thermal impedance from LED junction to ambient

θ_2: Thermal impedance from LED to detector (output IC)

θ_3: Thermal impedance from detector (output IC) junction to ambient

Ambient Temperature: Measured approximately 1.25 cm above the optocoupler, with no forced air.

Description

This thermal model assumes that an 8-pin single-channel plastic-package optocoupler is soldered into an 8.5 cm x 8.1 cm printed circuit board (PCB). The temperature at the LED and Detector junctions of the optocoupler can be calculated using the equations below.

$$\Delta T_{EA} = A_{11}P_E + A_{12}P_D$$

$$\Delta T_{DA} = A_{21}P_E + A_{22}P_D$$

where:

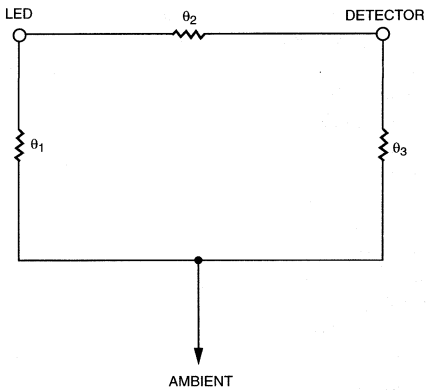
ΔT_{EA} = Temperature difference between ambient and LED

ΔT_{DA} = Temperature difference between ambient and detector

P_E = Power dissipation from LED

P_D = Power dissipation from detector

A_{11}, A_{12}, A_{21}, A_{22} thermal coefficients (units in °C/W) are functions of the thermal impedances θ_1, θ_2, θ_3 (See Note 2).



Thermal Coefficient Data (units in °C/W).

Part Number	A_{11}	A_{12} , A_{21}	A_{22}
6N135/6, HCPL-4503	323	154	225
HCNW135/6, HCNW4502/3	220	61	166
HCPL-0500/1, HCPL-0452/3	409	201	295
HCNW137, HCNW2601/11	219	51	139
HCPL-0600/01/11	455	216	308
HCPL-0700/1	396	193	290
HCPL-2200/01/02/11/12	304	149	216
HCPL-2400/11	337	139	215

Notes:

1. Maximum junction temperature for above parts: 125 °C.
2. $A_{11} = \theta_1 \,||\, (\theta_2 + \theta_3)$; $A_{12} = A_{21} = (\theta_1 \theta_2) / (\theta_1 + \theta_2 + \theta_3)$; $A_{22} = \theta_3 \,||\, (\theta_2 + \theta_3)$.

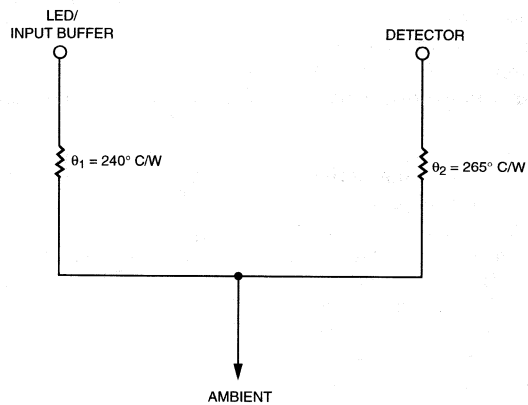
Thermal Model-C for HCPL-3700/60 Optocoupler with Input Buffer Circuit

Definitions

θ_1: Thermal impedance from LED/input-buffer IC junctions to ambient

θ_2: Thermal impedance from detector IC junction to ambient

Ambient Temperature: Measured approximately 1.25 cm above package, with no forced air.



Description

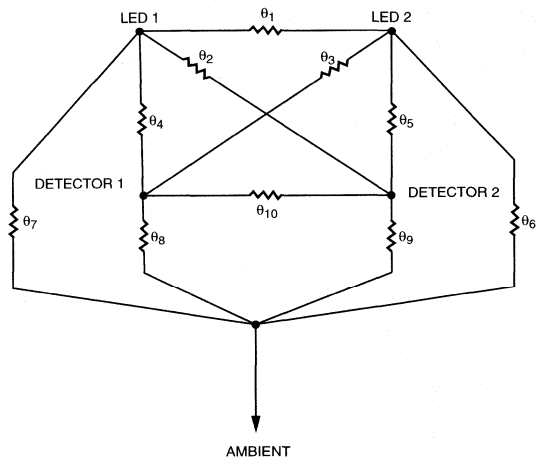
Thermal impedance values shown in the above figure can be used for calculating the temperatures at each node for a given operating condition. For simplification, the LED and the Input Buffer IC are assumed to be at the same node. Furthermore, the thermal resistance between the LED and detector are very large in comparison with the terms shown in the figure, and are omitted for simplicity.

Note: Maximum junction temperature for above part: 125 °C.

Thermal Model-D for a Dual-Channel Plastic-Package Optocoupler

Definitions

θ_1, θ_2, θ_3, θ_4, θ_5, θ_6, θ_7, θ_8, θ_9, θ_{10}: Thermal impedances between nodes as shown above.
Ambient Temperature: Measured approximately 1.25 cm above the optocoupler with no forced air.



Description

This thermal model assumes that an 8-pin dual-channel plastic-package optocoupler is soldered into an 8.5 cm x 8.1 cm printed circuit board (PCB). These optocouplers are hybrid devices with four die: two LEDs and two detectors. The temperature at the LED and the detector of the optocoupler can be calculated by using the equations below.

$$\Delta T_{E1A} = A_{11}P_{E1} + A_{12}P_{E2} + A_{13}P_{D1} + A_{14}P_{D2}$$

$$\Delta T_{E2A} = A_{21}P_{E1} + A_{22}P_{E2} + A_{23}P_{D1} + A_{24}P_{D2}$$

$$\Delta T_{D1A} = A_{31}P_{E1} + A_{32}P_{E2} + A_{33}P_{D1} + A_{34}P_{D2}$$

$$\Delta T_{D2A} = A_{41}P_{E1} + A_{42}P_{E2} + A_{43}P_{D1} + A_{44}P_{D2}$$

where:

ΔT_{E1A} = Temperature difference between ambient and LED 1
ΔT_{E2A} = Temperature difference between ambient and LED 2
ΔT_{D1A} = Temperature difference between ambient and detector 1
ΔT_{D2A} = Temperature difference between ambient and detector 2
P_{E1} = Power dissipation from LED 1;
P_{E2} = Power dissipation from LED 2;
P_{D1} = Power dissipation from detector 1;
P_{D2} = Power dissipation from detector 2
A_{xy} thermal coefficient (units in °C/W) is a function of thermal impedances θ_1 through θ_{10}.

Thermal Coefficient Data (units in °C/W).

Part Number	A_{11}, A_{22}	A_{12}, A_{21}	A_{13}, A_{24}	A_{14}, A_{23}	A_{31}, A_{42}	A_{32}, A_{41}	A_{33}, A_{44}	A_{34}, A_{43}
HCPL-2430	308	92	101	91	101	91	162	112

Note: Maximum junction temperature for above part: 125 °C.

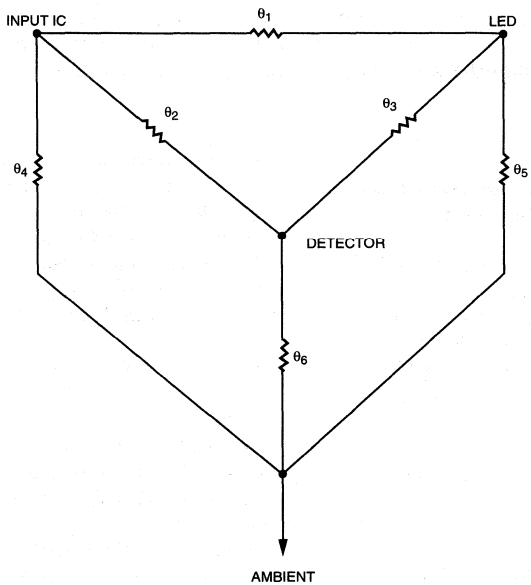
Thermal Model-E for a HCPL-7100/1 Optocoupler

Definitions

θ_1, θ_2, θ_3, θ_4, θ_5, θ_6: Thermal impedances between nodes as shown above.
Ambient Temperature: Measured approximately 1.25 cm above the optocoupler with no forced air.

Description

This thermal model assumes that the HCPL-7100/1 optocoupler is soldered into an 8.5 cm x 8.1 cm printed circuit board (PCB). The HCPL-7100/1 is a hybrid device with three die: an input IC that drives the LED, an LED, and the detector IC. The temperature at the input IC, LED, and detector of this optocoupler can be calculated be using the equations below.



$$\Delta T_{IA} = A_1P_I + A_2P_E + A_3P_D$$

$$\Delta T_{EA} = A_4P_I + A_5P_E + A_6P_D$$

$$\Delta T_{DA} = A_7P_I + A_8P_E + A_9P_D$$

where:
ΔT_{IA} = Temperature difference between ambient and input IC
ΔT_{EA} = Temperature difference between ambient and LED
ΔT_{DA} =Temperature difference between ambient and detector
P_I = Power dissipation from input IC (Typical: 25 mW)
P_E = Power dissipation from LED (Typical: 10 mW when input Logic Low; less than 0.01 mW when input Logic High)
P_D = Power dissipation from detector (Typical 30 mW)
A_1 through A_9 thermal coefficients (units in °C/W) are functions of thermal impedances θ_1, θ_2, θ_3, θ_4, θ_5, θ_6.

Part Number	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9
HCPL-7100/1	206	133	103	133	299	115	103	115	193

Note: Maximum junction temperature for above part: 125 °C.

Applications

The following abstracts represent application notes that are not published in this catalog. These application notes can be obtained from your local Hewlett-Packard sales office or authorized HP distributor or representative (see section 5).

In the US/Canada, technical literature is available from the Hewlett-Packard Components Group fax-back service at: 1-800-450-9455, or from the Components Sales Response Center at 1-800-235-0312.

AN 951-1
Applications for Low-Input-Current, High-Gain Optocouplers
Optocouplers are useful in line receivers, logic isolation, medical equipment, power lines, and telephone lines. This AN discusses the use of the 6N138/9 series of high-CTR optocouplers in each of these areas.

Publication No. 5953-7794
Document ID #55655*

AN 951-2
Linear Applications of Optocouplers
Although optocouplers are not inherently linear, the separate photodiodes used in HP devices provide better linearity as well as higher speed of response than phototransistor detectors.

Using paired optocouplers to enhance linearity is described with specific circuit examples offering dc-to-25 KHz response. These examples illustrate the relative merits of differential and servo techniques. A circuit with linear ac response to 10 MHz is also described for analog optocouplers having the photodiode terminals externally accessible.

The AN also discusses digital techniques of voltage-to-frequency conversion and pulse width modulation. Their linearity is quite independent of optocoupler linearity but requires use of high-speed optocouplers for low distortion. The AN is applicable to the HCPL-2530.

Publication No. 5954-8430

AN 1004
Threshold Sensing for Industrial Control Systems with the HCPL-3700 Interface Optocoupler
Interfacing from industrial control systems to logic systems is a necessary operation to monitor system progress. This interfacing is found in a variety of applications, including:
- Process control systems
- Programmable controllers
- Microprocessor subsystems that monitor proximity and limit switches
- Environmental sensors and ac line status
- Switching power supplies for detection of ac power loss
- Power back-up systems that need an early warning of power loss to save special microprocessor memory information or switch to battery operation, etc.

Publication No. 5953-0406

AN 1018
Designing with the HCPL-4100 and HCPL-4200 Current-Loop Optocoupler
Digital current loops provide unique advantages of large noise immunity and long-distance communication at low cost. Applications are wide and varied for current loops, but one of the critical concerns for designers of loop systems is to provide a predictable, reliable and isolated interface. The HCPL-4100 (transmitter) and HCPL-4200 (receiver) optocouplers provide easy interfacing to and from a current loop with minimal design effort.

This AN completely describes the HCPL-4100/4200 optocouplers and lists applications for digital, 20 mA, simplex, half-duplex and full-duplex loops. These loops can be either point-to-point or multidrop configurations. Factors that affect data performance are discussed. Circuit arrangements with specific data performance are given in graphical and tabular form.

Publication No. 5953-9359

*Application Notes referencing document ID number are available from Fax-Back service.

AN 1023
Radiation Immunity of Hewlett-Packard Optocouplers
This AN opens with a quotation from MIL-HDBK-279, which describes optocouplers that contain photodiodes as being superior to optocouplers that contain phototransistors.

The AN continues with a description of the properties of ionizing radiation (particles and photons) and how it affects the performance of optocouplers. Graphs show degradation of CTR (Current Transfer Ratio) in the 6N140 as a function of gamma total dose (up to 1000 rad (Si)) and as a function of total neutron fluence (up to 6×10^{12} neutrons/cm^2). A table gives radiation hardness requirements for various military applications.

Publication No. 5954-1003

AN 1024
Ring Detection with the HCPL-3700 Optocoupler
With the increased use of modems, automatic phone answering equipment, private automatic branch exchange (PABX) systems, etc., low-cost, reliable, isolated ring detection becomes important to many electronic equipment manufacturers. This AN defines the ringing requirements (U.S.A. and Europe), and the applications of the HCPL-3700 optocoupler as a simple, but effective, ring detector.

A design example is shown with calculations to illustrate proper use of the optocoupler. Features integrated into the HCPL-3700 provide predictable detection, protection and isolation with greater ease than is possible with other optocouplers.

Publication No. 5954-1006

AN 1047
Low On-Resistance Solid-State Relays for High-Reliability Applications
This AN shows the main characteristic of the HSSR-7110 Power MOSFET optocoupler and how this component operates as a low on-resistance solid-state relay. Several control drive circuits are described.

Publication No. 5091-4502E

AN 1058
Power Transistor Gate/Base Drive Optocouplers
Hewlett-Packard offers an expanded choice of optocouplers that can directly drive power MOSFETS, IGBTs, and bipolar power transistors. This application note describes the main features of the HCPL-3000, HCPL-3100 and HCPL-3101 power driver optocouplers. Also included are application guidelines for three-phase power inverters.

Publication No. 5091-6000E
Document ID #10353*

AN 1059
High-CMR Isolation Amplifier for Current-Sensing Applications
In 1992, Hewlett-Packard introduced the world's smallest isolation amplifier, the HCPL-7800. This paper describes the theory of operation for the HCPL-7800 as well as a typical application circuit for motor current sensing.

Publication No. 5091-6315E

*Application Notes referencing document ID number are available from Fax-Back service.

AN 1094

Regulatory Guide to Isolation Circuits

Optoisolator safety standards both at the component level and the equipment level are increasingly becoming the norm in the global market place. Various regions of the world have separate safety standards, safety organizations, and safety requirements.

Regulatory guide to Isolation circuits is a comprehensive handbook that details and clarifies the numerous safety standards, or regional and International safety organizations that exist today. This guide provides outstanding and exceptional information regarding the safety requirements of the optoisolator components, or the optoisolator safety requirements in equipment level applications. This guide also presents a comprehensive listing of all the optoisolator components available from Hewlett-Packard and the compliance or recognition of these optocouplers to the various regulatory and safety standards. Component level safety standard approvals or rating information, and equipment level compliance information for the optoisolators make it very convenient and useful for the designers to select the appropriate optocoupler or package style.

International and regional regulatory agencies are also discussed. IEC (International Electrotechnical Commission) provides an International umbrella for safety regulations. The charter of CENELEC (European Committee for Electrotechnical Standardization) is to Harmonize European Regulations. DKE (Deutsche Electrotechnische Kommission) addresses German Safety regulations. UL (Underwriters Laboratory) and CSA (Canadian Standards Associations) cover the US and Canadian regulations respectively. BSI (British Standards Institute) is a British regulatory agency.

Call your local HP sales representative for more information.

HEWLETT® PACKARD

Motion Sensing and Control

- **Reflective Optical Surface Mount Encoders**
- **Optical Encoder Modules**
- **Optical Encoders**
- **Rotary Pulse Generators**
- **Motion Control ICs**
- **Codewheels**

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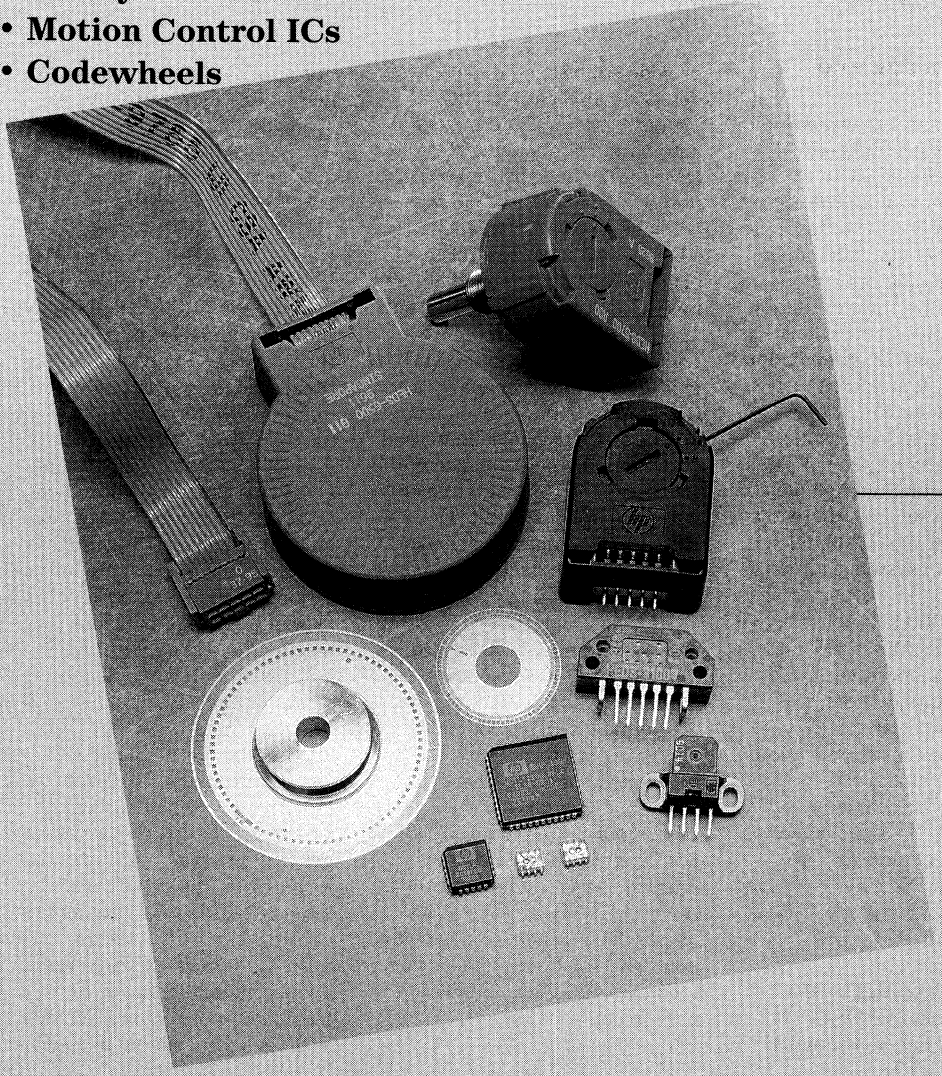

Motion Sensing and Control

Motion Sensing and Control

Hewlett-Packard's growing family of motion sensing and control products developed as an extension of our emitter/detector systems capabilities. Motion sensing products include optical shaft encoders and optical encoder modules for closed-loop servo applications, and rotary pulse generators for manual input applications. HP's optical products provide digital link converting mechanical shaft rotation into digital signals. HP's motion control ICs complement the optical products and greatly simplify the design of digital motion control systems.

The HEDR-8000 Series Reflective Optical Surface Mount Encoder is designed for modern high volume consumer equipment, such as VCRs, CD ROMs, and card readers. To fit these applications, the HEDR-8000 series is designed as a small low priced encoder. This SO-8 package uses a reflective technique to save space. The HEDR-8000 is surface mountable, enabling automated manufacturing.

The HEDS-9000, HEDS-9100, HEDS-9200, and HEDS-9700 series optical encoder modules provide sophisticated motion detection applications such as printers, plotters, and industrial automation equipment. The HEDS-9000 and HEDS-9100 are now available in three channel versions, the HEDS-9040 and 9140, which provide a third channel index pulse in addition to the standard two channel outputs. The HEDS-9200 series linear encoder module uses the same emitter/detector technology as the HEDS-9000 to sense linear position. We have also increased the resolution performance of the HEDS-9000/9100/9200 to nearly twice the previous limit. The HEDS-9700 comes in a smaller, wavesolderable package with a variety of mounting options.

The HEDS-5500, HEDS-5600, and HEDS-6500 series are complete, quick assembly, low cost optical shaft encoders. No adhesives or last minute adjustments are necessary for assembly. In addition, the HEDS-5540, HEDS-5640, and HEDS-6540 provide a third channel index pulse for home position sensing. The HEDS-5500, 5600, and 6500 series encoders offer a complete solution in industrial, medical, and office automation equipment.

For applications in noisy environments, line driver options are available on both the HEDS-9001/9100/9200 series module encoders, as well as the HEDS-5500/5600/6500 encoder kits.

Hewlett-Packard's HRPG series of low cost miniature rotary pulse generators (RPGs) use reflective optics technology for superior reliability and consistent rotational feel for more than one million revolutions. The HRPG is ideal for front panel applications such as test and measurement equipment, medical equipment, CAD/CAM systems, and audio/video equipment. The HRPG is available in a variety of configurations including smooth or detented turning, multiple terminations and mounting options, and a wide selection of shaft configurations.

To complement the motion sensing products, HP offers two motion control IC families of products. The HCTL-1100 CMOS general purpose motion control IC performs all of the time-intensive tasks of digital motion control. The HCTL-1100 controls position or velocity while using an incremental encoder for feedback information. The HCTL-1100 is also available in a surface

mount package. The HCTL-2000, HCTL-2016, and HCTL-2020 Quadrature Decoder/Counter ICs provide a one chip, easy to implement solution to interfacing the quadrature output of an encoder or RPG to a microprocessor. These CMOS ICs include a quadrature decoder, a 12 or 16 bit up/down counter, and an eight bit bus interface. In addition, the HCTL-2020 has cascade output signals as well as quadrature decoder output signals. The HCTL-2016 and HCTL-2020 are also available in surface mount packages.

New Products

Reflective Optical Surface Mount Encoder HEDR-8X00

This product will expand HP's optical encoder family into high volume and low cost applications.

2 Channel 180 LPI/500CPR Option, HEDS-9730

A higher resolution option is added to existing HEDS-9700 series.

3 Channel 2000 CPR Option, HEDS-9040

A higher resolution option is added to existing HEDS-9040 series.

3 Channel 2000 CPR Codewheel, HEDM-6140

This film codewheel is designed to work with new high resolution 3 channel option for the HEDS-9040 module.

Quick Assembly Optical Encoder, HEDS-6500 and HEDL-6500 Series Large Diameter (56 mm) Housed 2/3 Channel Optical encoder

HEWLETT® PACKARD

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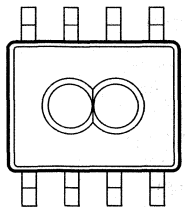
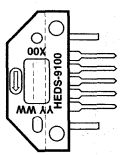
Reflective Optical Surface Mount Encoder

Package Outline Drawing	Part No.	Channels	Resolution	Page No.
	**HEDR-8000** Opt 2K0 Can be ordered in multiples of 50 units.	A, B	70-75LPI (2.76 - 2.95 lines/mm)	2-13
	HEDR-8000 Opt 2K3 Can be ordered in multiples of 100 units.	A, B		
	HEDR-8000 Opt 2K2 Designer Kit. Contains 3 encoder modules.	A, B		
	HEDR-8100 Opt 2P0 Can be ordered in multiples of 50 units	A, B	150LPI (5.91 lines/mm)	
	HEDR-8100 Opt 2P3 Can be ordered in multiples of 100 units.	A, B		
	HEDR-8100 Opt 2P2 Designer Kit. Contains 3 encoder modules.	A, B		

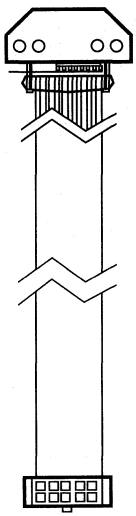
Bold type = new product

Optical Encoder Modules

Package Outline Drawing	Part No.	Channels	Resolution	Page No.
 HEDS-90XX HEDS-91XX HEDS-92XX HEDT-90XX HEDT-91XX	HEDS-9000 OPT ☐ 00	A, B	☐ A 500 CPR* B 1000 CPR*	2-40
	HEDS-9000 OPT ☐ 00 Extended Resolution		☐ T 2000 CPR U 2048 CPR	2-63
	HEDL-9000 OPT ☐ 00		☐ All	2-72
	HEDT-9000 OPT ☐ 00 125°C High Temperature		☐ A 500 CPR B 1000 CPR	2-75
	HEDS-9040 OPT ☐ 00	A, B, I	☐ B 1000 CPR* J 1024 CPR* T 2000 CPR	2-52
	HEDL-9040 OPT ☐ 00			2-72
	HEDT-9040 OPT ☐ 00 140°C High Temperature	A, B, I	☐ B 1000 CPR J 1024 CPR	2-81

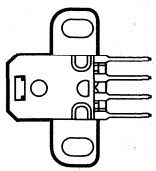
* Commonly used product with short leadtime.

Optical Encoder Modules, Continued

Package Outline Drawing	Part No.	Channels	Resolution	Page No.
 HEDL-90XX HEDL-91XX HEDL-92XX	HEDS-9100 OPT ☐ 00	A, B	☐ S 50 CPR K 96 CPR C 100 CPR*	2-40 2-72
	HEDL-9100 OPT ☐ 00		D 192 CPR E 200 CPR F 256 CPR* G 360 CPR H 400 CPR A 500 CPR* I 512 CPR* B 1000 CPR J 1024 CPR	
	HEDS-91☐☐ Special Count	A, B	☐ ☐ B A 250 CPR B B 480 CPR B C 576 CPR	2-63
	HEDT-9100 OPT ☐ 00 125°C High Temperature	A, B	K 96 CPR C 100 CPR D 192 CPR E 200 CPR F 256 CPR G 360 CPR H 400 CPR A 500 CPR I 512 CPR	2-75
	HEDS-9140 OPT ☐ 00	A, B, I	☐ S 50 CPR K 96 CPR C 100 CPR E 200 CPR F 256 CPR G 360 CPR* H 400 CPR A 500 CPR* I 512 CPR*	2-52 2-72
	HEDL-9140 OPT ☐ 00			
	HEDT-9140 OPT ☐ 00	A, B, I	☐ E 200 CPR F 256 CPR G 360 CPR A 500 CPR	2-81
	HEDS-9200 OPT ☐☐0	A, B	☐ 100 100 LPI L00 120 LPI M00 127 LPI P00 150 LPI Q00 180 LPI R00 200 LPI 300 300 LPI 360 360 LPI	2-46 2-72
	HEDL-9200 OPT ☐☐0			

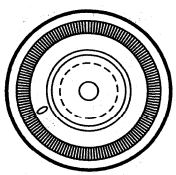
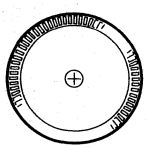
* Commonly used product with short leadtime.

Small Optical Encoder Modules–HEDS-9700 Series

Package Outline Drawing	Part No.	Lead Bend	Channels	Resolution	Mounting Options	Page No.
	HEDS-9700 OPT [1][2][2]	Straight	A, B	[1] K 96 CPR C 100 CPR*	[2][2] 50 – Standard 51 – Rounded Outline	2-20
	HEDS-9701 OPT [1][2][2]	Bent	A, B	D 192 CPR E 200 CPR F 256 CPR G 360 CPR H 400 CPR*	52 – Backplane 53 – Standard w/Posts 54 – Tabless 55 – Backplane w/Posts	
	HEDS-9720 OPT [3][2][2]	Straight	A, B	[3] L 120 LPI M 127 LPI P 150 LPI *		
	HEDS-9721 OPT [3][2][2]	Bent	A, B			
	HEDS-9730 OPT [4][2][2]	Straight	A, B	[4] A 500 CPR Q 180 LPI		2-320
	HEDS-9731 OPT [4][2][2]	Bent	A, B			

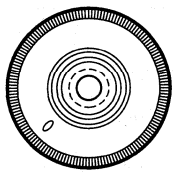
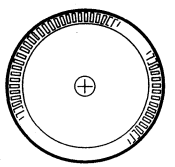
Bold type = new product

Codewheels–11.00 mm (0.433 in.) Optical Radius

Package Outline Drawing	Part No.	Matching Encoder Module	Channels	Resolution	Shaft Size	Page No.
	HEDS-5120 OPT [1][2][2]	HEDS-9100 HEDS-9700	A, B	[1] S 50 CPR K 96 CPR C 100 CPR D 192 CPR E 200 CPR F 256 CPR G 360 CPR H 400 CPR A 500 CPR* I 512 CPR	[2][2] 01 2 mm 02 3 mm 03 1/8 in. 04 5/32 in. 05 3/16 in. 06 1/4 in.* 11 4 mm* 14 5 mm 12 6 mm 13 8 mm	2-127
	HEDS-5140 OPT [3][2][2]	HEDS-9140	A, B, I	[3] S 50 CPR K 96 CPR C 100 CPR E 200 CPR F 256 CPR G 360 CPR H 400 CPR A 500 CPR* I 512 CPR		
	HEDM-5120 OPT [4][2][2]	HEDS-9100 Extended Resolution	A, B	[4] B 1000 CPR J 1024 CPR		
	HEDG-5120 OPT [4][2][2]					

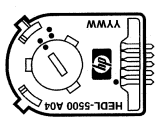
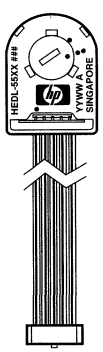
* Commonly used product with short leadtime.

Codewheels–23.36 mm (0.920 in.) Optical Radius

Package Outline Drawing	Part No.	Matching Encoder Module	Channels	Resolution	Shaft Size	Page No.
	HEDS-6100 OPT [1][2][2]	HEDS-9000	A, B	[1] A 500 CPR B 1000 CPR	[2][2] 05 3/16 in. 06 1/4 in. 07 5/16 in. 08 3/8 in. 09 1/2 in. 10 5/8 in. 11 4 mm 12 6 mm 13 8 mm	2-127
	HEDS-6140 OPT [3][2][2]	HEDS-9040	A, B, I	[3] B 1000 CPR J 1024 CPR		
	HEDM-6120 OPT [4][2][2] HEDG-6120 OPT [4][2][2]	HEDS-9000 Extended Resolution	A, B	[4] T 2000 CPR U 2048 CPR		
	HEDM-6140 OPT [5][2][2]	HEDS-9040 Extended Resolution	A, B, I	[5] T 2000 CPR		

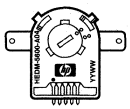
Bold type = new product

Quick Assembly Encoder–HEDS-5500 Series

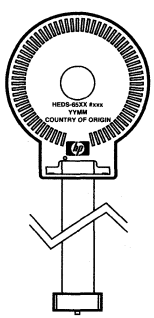
Package Outline Drawing	Part No.	Channels	Mounting Type	Through Hole	Resolution	Shaft Size	Page No.
 HEDS-55XX HEDS-56XX HEDM-550X HEDM-560X	HEDS-5500 HEDL-5500 OPT [1][2][2]	A, B	Standard	None	[1] S 50 CPR K 96 CPR C 100 CPR D 192 CPR E 200 CPR* F 256 CPR G 360 CPR H 400 CPR* A 500 CPR* I 512 CPR	[2][2] 01 2 mm 02 3 mm 03 1/8 in. 04 5/32 in. 05 3/16 in. 06 1/4 in.* 11 4 mm 14 5 mm 12 6 mm 13 8 mm	2-90 2-72
	HEDS-5505 HEDL-5505 OPT [1][2][2]	A, B	Standard	8.9 mm (0.35 in.)			2-90 2-72
	HEDS-5600 HEDL-5600 OPT [1][2][2]	A, B	External Mounting Ears	None			2-90 2-72
	HEDS-5605 HEDL-5605 OPT [1][2][2]	A, B	External Mounting Ears	8.9 mm (0.35 in.)			2-90 2-72
 HEDL-55XX HEDL-56XX	HEDS-5540 HEDL-5540 OPT [3][2][2]	A, B, I	Standard	None	[3] S 50 CPR K 96 CPR C 100 CPR E 200 CPR F 256 CPR G 360 CPR H 400 CPR A 500 CPR I 512 CPR*		2-90 2-72
	HEDS-5545 HEDL-5545 OPT [3][2][2]	A, B, I	Standard	8.9 mm (0.35 in.)			2-90 2-72
	HEDS-5640 HEDL-5640 OPT [3][2][2]	A, B, I	External Mounting Ears	None			2-90 2-72
	HEDS-5645 HEDL-5645 OPT [3][2][2]	A, B, I	External Mounting Ears	8.9 mm (0.35 in.)			2-90 2-72

*Commonly used product with short leadtime.

Quick Assembly Encoder–HEDS-5500 Series, continued

Package Outline Drawing	Part No.	Channels	Mounting Type	Through Hole	Resolution	Shaft Size	Page No.
	HEDM-5500 OPT [4][2][2]	A, B	Standard	None	B 1000 CPR J 1024 CPR		2-90
	HEDM-5505 OPT [4][2][2]	A, B	Standard	8.9 mm (0.35 in.)			
	HEDM-5600 OPT [4][2][2]	A, B	External Mounting Ears	None			
	HEDM-5605 OPT [4][2][2]	A, B	External Mounting Ears	8.9 mm (0.35 in.)			

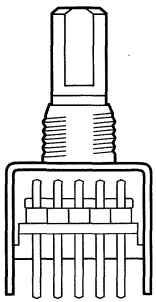
Quick Assembly Encoder–HEDS-6500 Series

Package Outline Drawing	Part No.	Channels	Through Hole	Resolution	Shaft Size	Page No.
 HEDS-650X HEDS-654X HEDL-654X HEDL-6560 HEDL-6561	**HEDS-6500** OPT [1][2][2]	A, B	None	[1] A 500 CPR B 1000 CPR* J 1024 CPR*	[2][2] 05 = 3/16 in. 06 = 1/4 in.* 07 = 5/16 in. 08 = 3/8 in. 09 = 1/2 in. 10 = 5/8 in. 11 = 4 mm* 12 = 6 mm 13 = 8 mm	2-102
	HEDS-6505 OPT [1][2][2]	A, B	13.2 mm (0.525 in.)			
	HEDS-6540 OPT [1][2][2]	A, B, I	None			
	HEDS-6545 OPT [1][2][2]	A, B, I	13.2 mm (0.525 in.)			
	HEDM-6500 OPT [1][2][2]	A, B	None	[1] T 2000 CPR U 2048 CPR		
	HEDM-6505 OPT [1][2][2]	A, B	13.2 mm (0.525 in.)			
	HEDM-6540 OPT [1][2][2]	A, B, I	None	[1] T 2000 CPR		
	HEDM-6545 OPT [1][2][2]	A, B, I	13.2 mm (0.525 in.)			
	HEDL-6500 OPT [1][2][2]	A, B	None	[1] A 500 CPR B 1000 CPR* J 1024 CPR*		
	HEDL-6505 OPT [1][2][2]	A, B	13.2 mm (0.525 in.)			
	HEDL-6540 OPT [1][2][2]	A, B, I	None			
	HEDL-6545 OPT [1][2][2]	A, B, I	13.2 mm (0.525 in.)			
	HEDL-6560 OPT [1][2][2]	A, B	None	[1] T 2000 CPR U 2048 CPR		
	HEDL-6561 OPT [1][2][2]	A, B	13.2 mm (0.525 in.)			
	HEDL-6564 OPT [1][2][2]	A, B, I	None	[1] T 2000 CPR		
	HEDL-6565 OPT [1][2][2]	A, B, I	13.2 mm (0.525 in.)			

*Commonly used product with short leadtime.

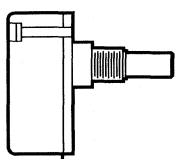
Bold type = new product

Rotary Pulse Generator–HRPG Series

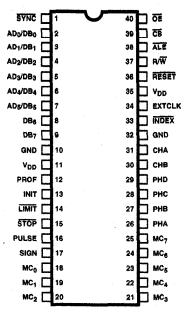
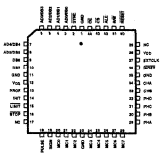
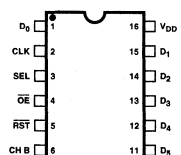
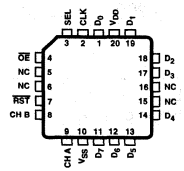
Package Outline Drawing	Part No.	Shaft Feel/Resolution	Mechanical Configuration	Termination	Page No.
	HRPG- A [1][1][1] OPT [2][2][3]	[1][1][1] S16–Smooth 16 CPR D16–Detented 16 CPR S32–Smooth 32 CPR D32–Detented 32 CPR S64–Smooth 64 CPR SCA–Smooth 120 CPR	[2][2] 11–0.3" x 0.25" 13–0.3" x 0.25" D-cut 14–0.5" x 0.25" 16–0.5" x 0.25" D-cut 17–0.8" x 0.25" 19–0.8" x 0.25" D-cut 51–7.6 mm x 6 mm 53–7.6 mm x 6 mm D-cut 54–12.7 mm x 6 mm 56–12.7 mm x 6 mm D-cut 57–20.3 mm x 6 mm 59–20.3 mm x 6 mm D-cut	[3] F–Pins Front with Bracket R–Pins Rear with Bracket C–Cable Connector with Strain Relief	2-119

* Commonly used product with short leadtime.

Rotary Pulse Generator–HEDS-5700

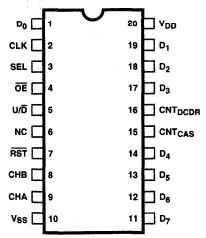
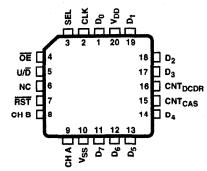
Package Outline Drawing	Part No.	Termination	Resolution	Drag Option	Shaft Configuration	Page No.
	HEDS-5700 OPT [1][2][2]	Pins	[1] K 96 CPR C 100 CPR D 192 CPR E 200 CPR F 256 CPR G 360 CPR H 400 CPR A 500 CPR I 512 CPR	[2] 0–free spinning 1–static drag	[3] 0–0.25" dia. 1–6 mm dia. 2–0.25" dia D-cut	2-116
	HEDS-5701 OPT [1][2][3]	6" Color Coded Leads				

Motion Control ICS–HCTL-XXXX Series

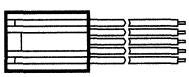
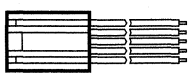
Package Outline Drawing	Part No.	Package	Description	Page No.
	HCTL-1100*	PDIP	CMOS General Purpose Motion Control IC	2-139
	HCTL-1100* OPT PLC	PLCC	CMOS General Purpose Motion Control IC	
	HCTL-2000*	PDIP	CMOS Quadrature Decoder/Counter IC, 12-bit Counter	2-178
	HCTL-2016*	PDIP	CMOS Quadrature Decoder/Counter IC, 16-bit Counter	
	HCTL-2016* OPT PLC	PLCC	CMOS Quadrature Decoder/Counter IC, 16-bit Counter	2-196

*Commonly used product with short leadtime.

Motion Control ICS–HCTL-XXXX Series, continued

Package Outline Drawing	Part No.	Package	Description	Page No.
	HCTL-2020*	PDIP	CMOS Quadrature Decoder/Counter IC, 16-bit Counter, Quadrature Decoder Output Signals, Cascade Output Signals	2-178
	HCTL-2020 OPT PLC	PLCC	CMOS Quadrature Decoder/Counter IC, 16-bit Counter, Quadrature Decoder Output Signals, Cascade Output Signals	2-196

Accessories for Encoders and Encoder Modules

Package Outline Drawing	Part No.	Description
	HEDS-8902	4-wire connector with 15.5 cm (6.1 in.) flying leads. Locks into HEDS-5500 and HEDS-5600 two channel encoders. Also fits HEDS-9000, HEDS-9100, and HEDS-9200 two channel encoder modules.
	HEDS-8903	5-wire connector with 15.5 cm (6.1 in.) flying leads. Locks into HEDS-5540 and HEDS-5640 three channel encoders. Also fits HEDS-9040 and HEDS-9140 three channel encoder modules.
	HEDS-8905	Alignment Tool for HEDS-9140
	HEDS-8906	Alignment Tool for HEDS-9040
	HEDS-8901	Gap Setting shown for film codewheels
	HEDS-8932	Gap Setting shown for glass codewheels
	HEDS-8910 OPT 0☐☐	Alignment Tool for HEDS-5540/5545 and HEDS-5640/5645. Order in appropriate shaft size.

*Commonly used product with short leadtime.

HEWLETT® PACKARD

Reflective Optical Surface Mount Encoders

Technical Data

HEDR-8000 Series
HEDR-8100 Series

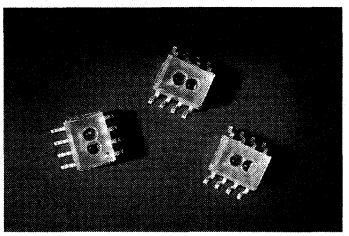
MOTION SENSING AND CONTROL

Features

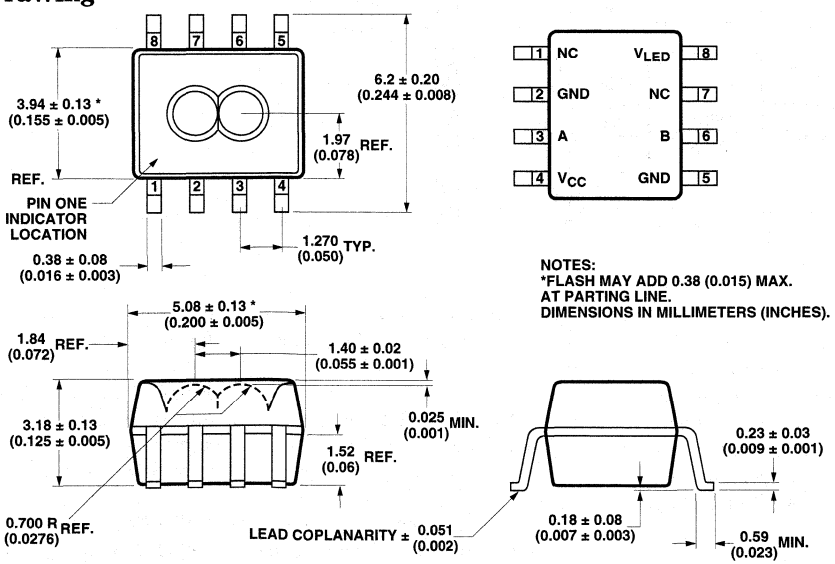
- **Reflective Technology**
- **Surface Mount SO-8 Package**
- **Two Channel Quadrature Outputs for Direction Sensing**
- **Two Encoding Resolution Options:**
  - 2.76 – 2.95 Lines/mm (70 – 75 Lines/inch)
  - 5.91 Lines/mm (150 Lines/inch)

Description

The HEDR-8000/8100 Series encoders use reflective technology to sense rotary or linear position. This sensor consists of an LED light source and a photodetector IC in a single SO-8 surface mount package. When used with a reflective codewheel or codestrip, this device can sense rotary or linear position.



Outline Drawing



ESD WARNING: NORMAL HANDLING PRECAUTIONS SHOULD BE TAKEN TO AVOID STATIC DISCHARGE.

The reflective surface mount optical encoders provide two square wave outputs in quadrature for count and direction information. These TTL compatible outputs correspond to the alternating reflective/non-reflective pattern of the codewheel or codestrip.

The HEDR-8000/8100 series encoders can be used over a range of codewheel and codestrip resolutions. The HEDR-8000/8100 reflective encoder can operate from 2.76 to 2.95 lines per mm (70 to 75 lines per inch). The HEDR-8100 can be used with a codewheel or codestrip with 150 lines per inch (5.91 lines per mm).

Applications

The HEDR-8000/8100 series provides two channel motion sensing at a very low cost, making it ideal for high volume applications. Its small size and surface mount capability make it ideal for printers, copiers, card readers, and consumer product applications.

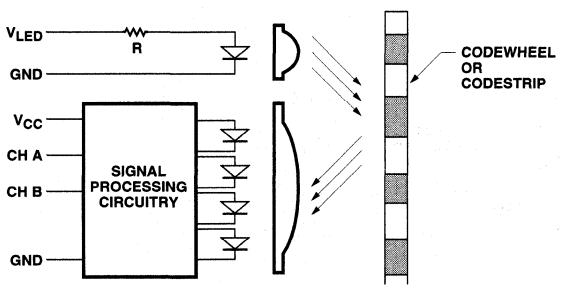
Theory of Operation

The HEDR-8000/8100 series combines an emitter and a detector in a single surface mount SO-8 package. When used with a codewheel or codestrip, the reflective sensors translates rotary or linear motion into a two channel digital output.

As seen in the block diagram, the HEDR-8000/8100 series has three key parts: a single light emitting diode (LED) light source, a photodetector IC with a set of uniquely configured photodiodes, and a pair of lenses molded into the package. The lens over the LED focuses light onto the codewheel or codestrip. Light is either reflected or not reflected back to the lens over the photodetector IC.

As the codewheel rotates or codestrip passes by, an alternating pattern of light and dark corresponding to the pattern of the codewheel falls upon the photodiodes. This light is used to produce internal signals A and $\bar{A}$, and B and $\bar{B}$. As part of this "push-pull" detector system, these signals are fed through comparators to produce the final outputs for channels A and B.

Block Diagram



Definitions

Count (N): For rotary motion, the number of bar and window pairs or counts per revolution (CPR) of the codewheel. For linear motion, the number of bar and window pairs per unit length (lines per inch [LPI] or lines per mm [LPmm]).

One Cycle (C): 360 electrical degrees (°e), 1 bar and window pair.

One Shaft Rotation: 360 mechanical degrees, N cycles (rotary motion only).

Line Density: The number of reflective and non-reflective pairs per unit length, expressed as either lines per inch (LPI) or lines per mm (LPmm).

Pulse Width (P): The number of electrical degrees that an output is high during one cycle, nominally 180°e or 1/2 a cycle.

Pulse Width Error (ΔP): The deviation in electrical degrees of the pulse width from its ideal value of 180°e.

State Width (S): The number of electrical degrees between a transition in the output of channel A and the neighboring transition in the output of channel B. There are 4 states per cycle, each nominally 90°e.

State Width Error (ΔS): The deviation in electrical degrees of each state width from its ideal value of 90°e.

Phase (ϕ): The number of electrical degrees between the center of the high state on channel A and the center of the high state on channel B. This value is nominally 90°e.

Phase Error ($\Delta\phi$): The deviation in electrical degrees of the phase from its ideal value of 90°e.

Direction of Rotation: When the codewheel or codestrip moves in the direction from pin 1 to pin 4, as viewed when looking down on the lenses, channel B will lead channel A. If the codewheel or codestrip moves in the opposite direction, channel A will lead channel B.

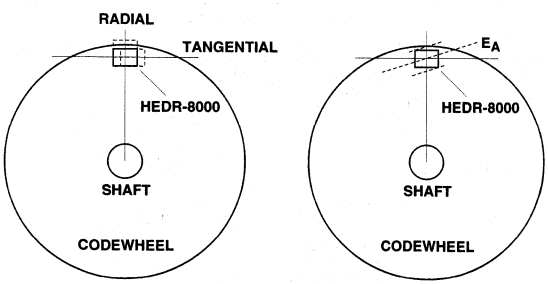
Optical Radius (Rop): For rotary motion, the distance from the codewheel's center of rotation to the center line connecting the two lenses of the encoder.

Gap (G): The distance from the top of the package to the surface of the reflective codewheel or codestrip.

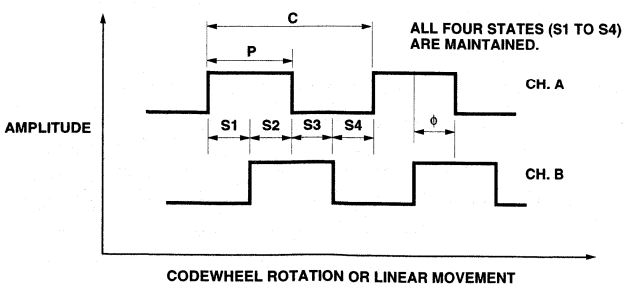
Specular Reflectance (R_f): a measure of a surface's reflective finish. This is quantified by the amount of light reflected when hit with an incident beam. A device called a scatterometer is used to quantify specular reflectance on a percent scale. (Contact factory for more information.)

Radial and Tangential Misalignment Error (E_R, E_T): For rotary motion, mechanical misalignment in the radial and tangential directions relative to the codewheel.

Angular Misalignment Error (E_A): angular misalignment of the sensor in relation to the tangential direction. This applies for both rotary and linear motion.



Output Waveforms



Absolute Maximum Ratings

Storage Temperature, T_S	-40°C to 85°C
Operating Temperature, T_A	0°C to 85°C
Supply Voltage, V_{CC}	-0.5 V to 7 V
Output Voltage, V_O	-0.5 V to V_{CC}
Output Current per Channel, I_{OUT}	-1.0 mA to 5 mA

Note: Exposure to extreme light intensity (such as from flashbulbs or spotlights) can cause permanent damage to device.

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Temperature	T_A	-10		85	°C	
Supply Voltage	V_{CC}	4.5	5.0	5.5	Volts	Ripple < 100 mVp-p
LED Current	I_{LED}	13	15	18	mA	See "Current Limiting Resistor for LED"
Load Capacitance	C_L			100	pF	2.7 KΩ Pull-Up
Count Frequency	f			15	kHz	Velocity (rpm) x N/60
Radial Misalignment	E_R			± 0.38 (± 0.015)	mm (in.)	
Tangential Misalignment	E_T			± 0.38 (± 0.015)	mm (in.)	
Angular Misalignment	E_A		0	± 1.5	deg.	
Codewheel or Codestrip Gap	G	1.52 (0.060)	2.03 (0.080)	2.54 (0.100)	mm (in.)	HEDR-8000
	G	1.02 (0.040)	1.52 (0.060)	2.03 (0.080)	mm (in.)	HEDR-8100
Codewheel or Codestrip Specular Reflectance	R_f	60%				As Measured on TMA μscan Scope (see Note 1)
Codewheel/Codestrip Tilt	C_T		0	1	deg.	
Codewheel/Codestrip Resolution	LPmm (LPI)	2.76 (70)		2.95 (75)	lines/mm (lines/in.)	HEDR-8000
	LPmm (LPI)		5.91 150		lines/mm (lines/in.)	HEDR-8100

Notes:
1. Contact factory for more information regarding measurement of specular reflectance.

Encoding Characteristics

Encoding Characteristics Over the Recommended Operating Conditions and Mounting Conditions.

Parameter	Symbol	Typical	Maximum	Units	Notes
Pulse Width Error, Channel A	ΔP	15	55	°e	HEDR-8000
Pulse Width Error	ΔP		75	°e	HEDR-8100
Phase Error	Δϕ		60	°e	HEDR-8100

Electrical Characteristics

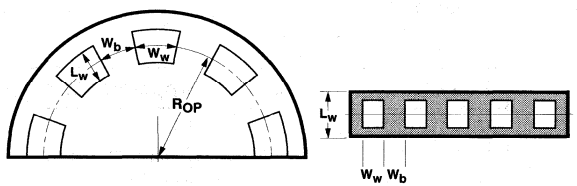
Electrical Characteristics Over Recommended Operating Conditions. Typical Values at 25°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Supply Current	I_{CC}		2.2	5.0	mA	
High Level Output Voltage	V_{OH}	2.4			V	I_{OH} = -40 µA min.
Low Level Output Voltage	V_{OL}			0.4	V	I_{OL} = 3.86 mA
Rise Time	t_r		150	200	ns	C_L = 25 pF R_L = 2.7 KΩ
Fall Time	t_f		50	60	ns	

Current Limiting Resistor for LED

A resistor to limit current to the LED is required. The recommended value is 220 Ω (± 10%) and should be placed in series between the 5 V supply and pin 8 of the device (V_{LED}). This will result in an LED current of approximately 15 mA.

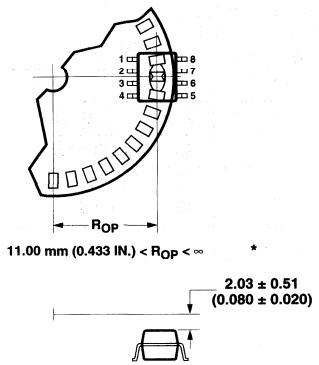
Recommended Codewheel and Codestrip Characteristics



Parameter	Symbol	Min.	Max.	Units	Notes
Window/Bar Ratio	Ww/Wb	0.9	1.1		
Specular Reflectance	R_f	60	85		Reflective Bars
		–	10		Non-reflective Bars
Line Density	LPmm (LPI)	2.76 (70)	2.95 (75)	lines/mm (lines/inch)	HEDR-8000
	LPmm (LPI)		5.91 (150)	lines/mm (lines/inch)	HEDR-8100
Window Length	Lw	1.80 (0.071)	2.31 (0.091)	mm (inches)	mm (inches)

Contact factory for further information on compatible codewheel and codestrips.

Mounting Conditions

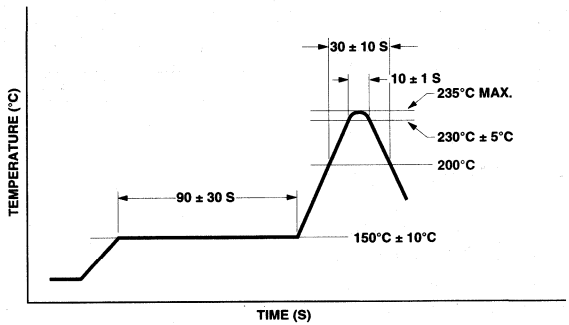


*These dimensions are for HEDR-8000. Please refer to "Recommended Operating Conditions" table for HEDR-8100.

IR Soldering Conditions

The following recommended IR soldering profile meets the specifications of the Electronic Industries Association of Japan (EIAJ):

1. 150 ± 10°C for 90 ± 30 seconds
2. Greater than 200°C for 30 ± 10 seconds
3. 230°C ± 5°C for 10 ± 1 second



Ordering Information

A. Modules

HEDR-8000# 2K☐

Low Resolution Reflective Optical Surface Mount Encoder

HEDR-8[0]00 **OPT 2☐☐**

Lines/Inch	Units in Shipping Tube*
K = 75 LPI	0 = 50 units 2 = 3 Unit (Designer's Kit) 3 = 100 Units

HEDR-8100# 2P☐

High Resolution Reflective Optical Surface Mount Encoder

HEDR-8[1]00 **OPT 2☐☐**

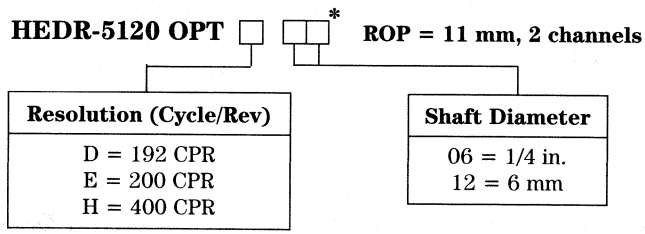
Lines/Inch	Units in Shipping Tube
P = 150 LPI	0 = 50 units 2 = 3 Unit (Designer's Kit) 3 = 100 Units

***Notes:**

1. Quantity ordered needs to be either in a multiple of 50 units or 100 units based on option part number.
2. Designer's Kit: ordering one unit will get three units of encoder modules.
3. Please contact your local HP representative for tape and reel option.

Ordering Information

B. Codewheel: reflective



*Please contact the factory for other shaft diameters.

HEWLETT® PACKARD

Small Optical Encoder Modules

Technical Data

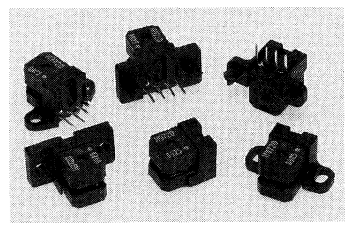
HEDS-9700 Series

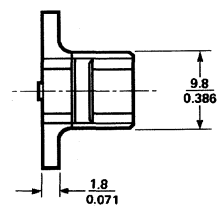
Features

- **Small Size**
- **Low Cost**
- **Multiple Mounting Options**
- **Wide Resolution Range**
- **Linear and Rotary Options Available**
- **No Signal Adjustment Required**
- **Insensitive to Radial and Axial Play**
- **-40°C to +85°C Operating Temperature**
- **Two Channel Quadrature Output**
- **TTL Compatible**
- **Single 5V Supply**
- **Wave Solderable**

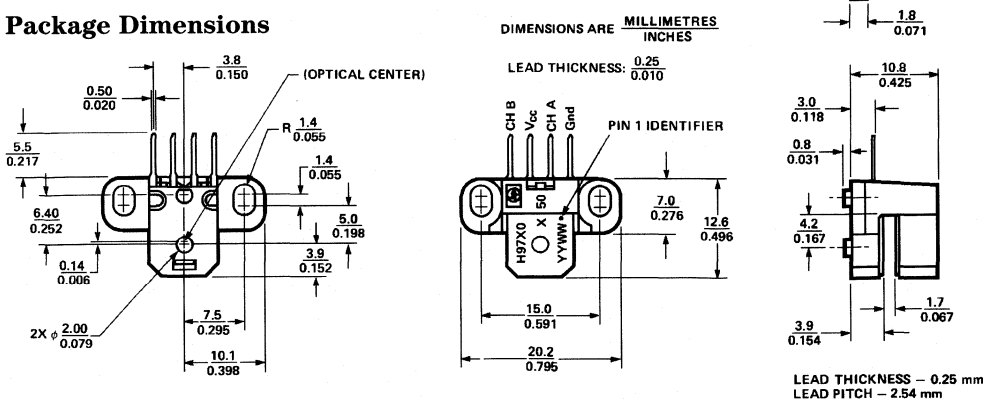
Description

The HEDS-9700 series is a high performance, low cost, optical incremental encoder module. When operated in conjunction with either a codewheel or codestrip, this module detects rotary or linear position. The





Package Dimensions



Mounting Option #50 - Standard (Baseplane Mounting) Contact Factory for Detailed Package Dimensions

ESD WARNING; NORMAL HANDLING PRECAUTIONS SHOULD BE TAKEN TO AVOID STATIC DISCHARGE.

module consists of a lensed LED source and a detector IC enclosed in a small C-shaped plastic package. Due to a highly collimated light source and a unique photodetector array, the module is extremely tolerant to mounting misalignment.

The two channel digital outputs and 5V supply input are accessed through four solder-plated leads located on 2.54 mm (0.1 inch) centers.

The standard HEDS-9700 is designed for use with an 11 mm optical radius codewheel, or linear codestrip. Other options are available. Please contact factory for more information.

Applications

The HEDS-9700 provides sophisticated motion detection at a low cost, making closed-loop control very cost-competitive! Typical applications include printers, plotters, copiers, and office automation equipment.

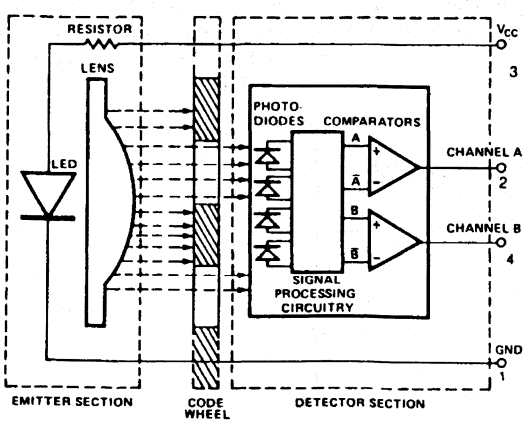
Theory of Operation

The HEDS-9700 is a C-shaped emitter/detector module. Coupled with a codewheel, it translates rotary motion into a two-channel digital output. Coupled with a codestrip, it translates linear motion into a digital output.

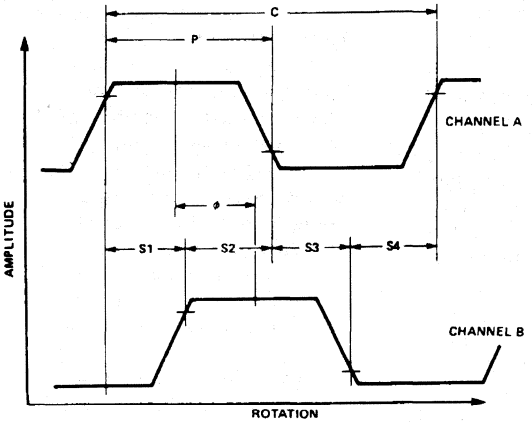
As seen in the block diagram, the module contains a single Light Emitting Diode (LED) as its light source. The light is collimated into a parallel beam by means of a single lens located directly over the LED. Opposite the emitter is the integrated detector circuit. This IC consists of multiple sets of photodetectors and the signal processing circuitry necessary to produce the digital waveforms.

The codewheel/codestrip moves between the emitter and detector, causing the light beam to be interrupted by the pattern of spaces and bars on the codewheel/codestrip. The photodiodes which detect these interruptions are arranged in a pattern that corresponds to the radius and count density of the codewheel/codestrip. These detectors are also spaced such that a light period on one pair of detectors corresponds to a dark period on the adjacent pair of detectors. The photodiode outputs are fed through the signal processing circuitry. Two comparators receive these signals and produce the final outputs for channels A and B. Due to this integrated phasing technique, the digital output of channel A is in quadrature with channel B (90 degrees out of phase).

Block Diagram



Output Waveforms



Definitions

Count (N) = The number of bar and window pairs or counts per revolution (CPR) of the codewheel, or the number of lines per inch of the codestrip (LPI).

1 Shaft Rotation = 360 mechanical degrees
= N cycles
1 cycle (c) = 360 electrical degrees (°e)
= 1 bar and window pair

Pulse Width (P): The number of electrical degrees that an output is high during one cycle. This value is nominally 180°e or 1/2 cycle.

Pulse Width Error (ΔP): The deviation, in electrical degrees, of the pulse width from its ideal value of 180°e.

State Width (S): The number of electrical degrees between a transition in the output of channel A and the neighboring transition in the output of channel B. There are 4 states per cycle, each nominally 90°e.

State Width Error (ΔS): The deviation, in electrical degrees, of each state width from its ideal value of 90°e.

Phase (ϕ): The number of electrical degrees between the center of the high state of channel A and the center of the high state of channel B. This value is nominally 90°e for quadrature output.

Phase Error (Δϕ): The deviation of the phase from its ideal value of 90°e.

Direction of Rotation: When the codewheel rotates counterclockwise, as viewed looking down on the module (so the marking is visible), channel A will lead channel B. If the codewheel rotates in the opposite direction, channel B will lead channel A.

Optical Radius (Rop): The distance from the codewheel's center of rotation to the optical center (O.C.) of the encoder module.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Notes
Storage Temperature	T_S	-40	85	°C	See Note
Operating Temperature	T_A	-40	85	°C	See Note
Supply Voltage	V_{CC}	-0.5	7	V	
Output Voltage	V_O	-0.5	V_{CC}	V	
Output Current per Channel	I_O	-1.0	5	mA	
Soldering Temperature			260	°C	t ≤ 5 sec.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Notes
Temperature	T	–40	85	°C	
Supply Voltage	V_{CC}	4.5	5.5	V	Ripple < 100 mV_{p-p}
Load Capacitance	C_L		100	pF	3.2 kΩ pull-up
Count Frequency			20	kHz	(Velocity (rpm) x N)/60

Note: The module performance is guaranteed to 20 kHz but can operate at higher frequencies. Contact factory for more information.

Encoding Characteristics

Encoding Characteristics over Recommended Operating Range and Recommended Mounting Tolerances. These characteristics do not include codewheel/codestrip contributions.

Parameter	Symbol	Typ.	Case 1 Max.	Case 2 Max.	Units	Notes
Pulse Width Error	ΔP	7	30	40	°e	
Logic State Width Error	ΔS	5	30	40	°e	
Phase Error	Δϕ	2	10	15	°e	

Case 1: Module mounted on tolerances of ± 0.13 mm (0.005"). Case 2: Module mounted on tolerances of ± 0.25 mm (0.010")

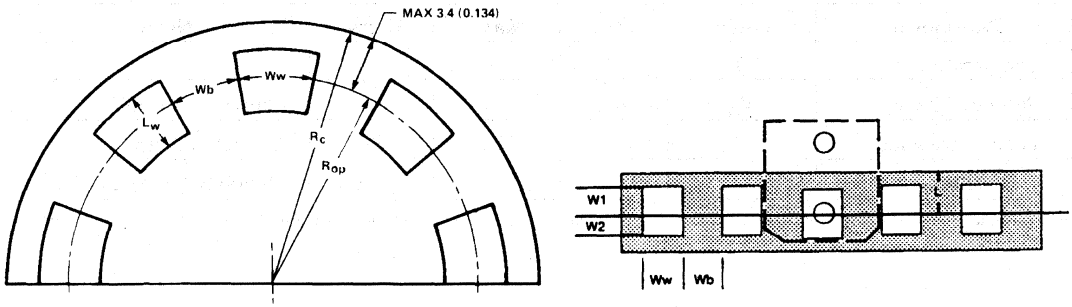
Note: See Figures in Mounting Considerations for details on Case 1 and Case 2 mounting tolerances.

Electrical Characteristics

Electrical Characteristics over Recommended Operating Range, Typical at 25°C.

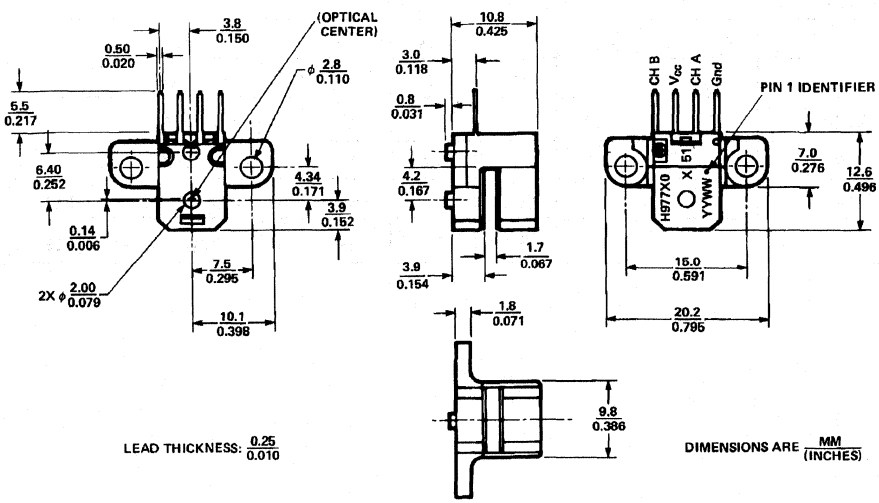
Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Supply Current	I_{CC}		17	40	mA	
High Level Output Voltage	V_{OH}	2.4			V	I_{OH} = -40 µA
Low Level Output Voltage	V_{OL}			0.4	V	I_{OL} = 3.2 mA
Rise Time	t_r		200		ns	C_L = 25 pF, R_L = 11 kΩ
Fall Time	t_f		50		ns	C_L = 25 pF, R_L = 11 kΩ

Recommended Codewheel and Codestrip Characteristics



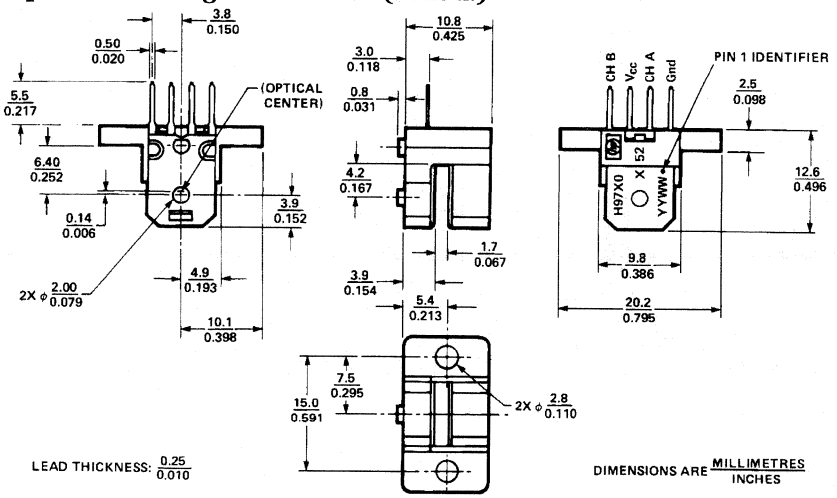
Parameter	Symbol	Min.	Max.	Units	Notes
Window/Bar Ratio	Ww/Wb	0.7	1.4		
Window Length (Rotary)	Lw	1.80 (0.071)	2.30 (0.091)	mm (inch)	
Absolute Maximum Codewheel Radius (Rotary)	Rc		Rop + 3.40 (Rop + 0.134)	mm (inch)	Includes eccentricity errors
Center of Post to Inside Edge of Window	W1	1.04 (0.041)		mm (inch)	
Center of Post to Outside Edge of Window	W2	0.76 (0.030)		mm (inch)	
Center of Post to Inside Edge of Codestrip	L		3.60 (0.142)	mm (inch)	

Optional Packages Available

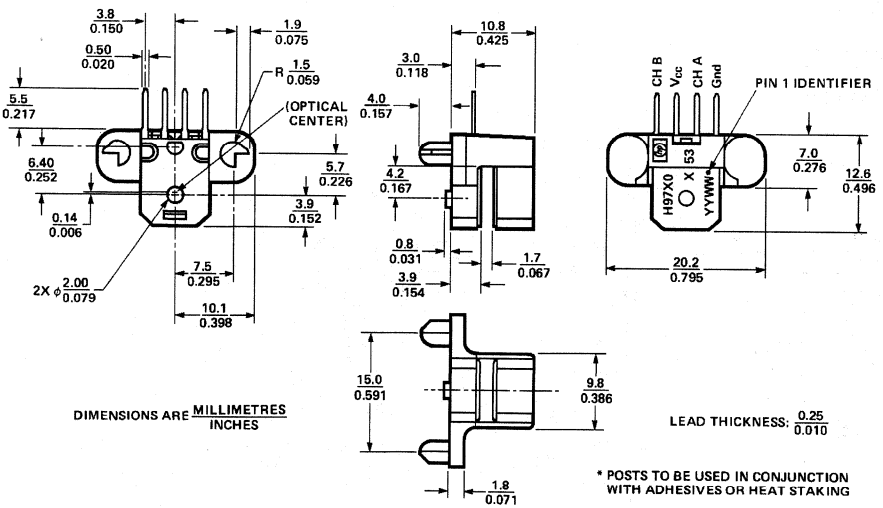


Mounting Option #51 – Rounded Outline (Baseplane Mounting)

Optional Packages Available (cont'd.)

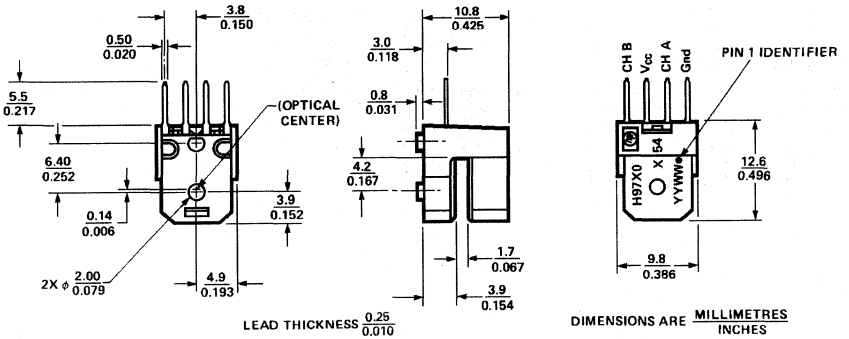


Mounting Option #52 – Backplane (Backplane Mounting)

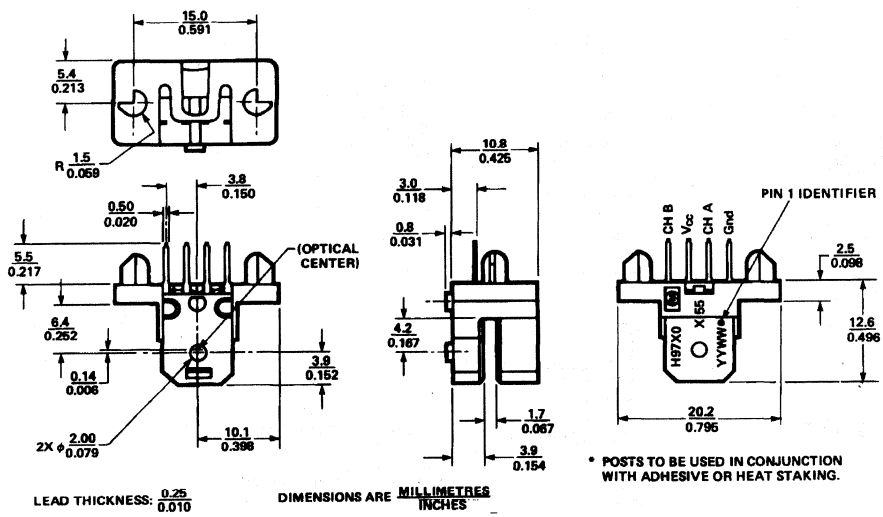


Mounting Option #53 – Standard with Posts (Baseplane Mounting)

Optional Packages Available (cont'd.)

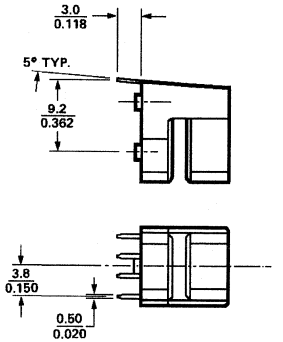


Mounting Option #54 – Tabless (Baseplane Mounting)



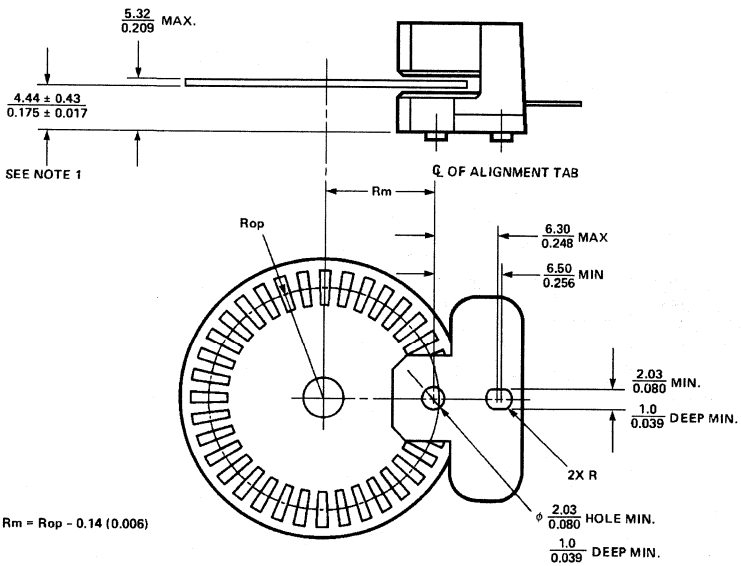
Mounting Option #55 – Backplane with Posts (Backplane Mounting)

Bent Lead Option



DIMENSIONS ARE MILLIMETERS / INCHES

Mounting Considerations



Note: These dimensions include shaft end play and codewheel warp.

All dimensions for mounting the module and codewheel/codestrip should be measured with respect to the two mounting posts, shown above.

Mounting Tolerances

Case 1 and Case 2 specify the mounting tolerances required on Rm in order to achieve the respective encoding characteristics shown on page 4. The mounting tolerances are as follows:

Case 1: Rm ± 0.13 mm (.005 inches)
Case 2: Rm ± 0.25 mm (.010 inches)

Recommended Screw Size: M2.5 x 0.45 or 2-56

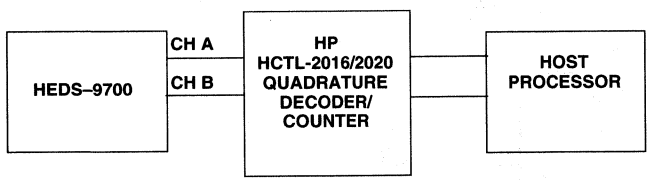
Wave Solder Conditions

Flux – RMA Water Soluble (per MIL-F-14256D)

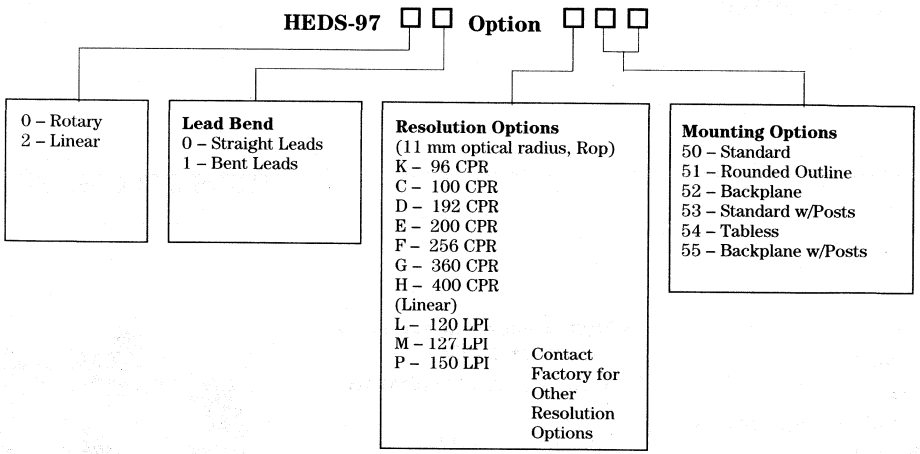
Process Parameters

1. Flux
2. Pre-heat 60 seconds total
   PCB top side @ 230°C
   PCB bottom side @ 260°C
3. Wave solder 255°C, 1.2 meters/min line speed
4. Hot Water Wash
   1st: 30°C 45 seconds
   2nd: 70°C 90 seconds
5. Rinse
   1st: 23°C 45 seconds
   2nd: 23°C 45 seconds
6. Dry
   1st: 80°C 105 seconds
   2nd: 95°C 105 seconds

Typical Interface



Ordering Information



Note: Please contact factory for codewheel and codestrip information.

HEWLETT® PACKARD

Small Optical Encoder Modules

Technical Data

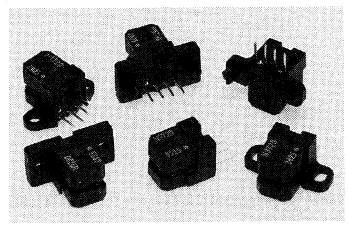
HEDS-973X Series

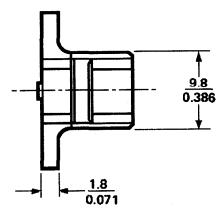
Features

- **Small Size**
- **Low Cost**
- **Multiple Mounting Options**
- **Wide Resolution Range**
- **Linear and Rotary Options Available**
- **No Signal Adjustment Required**
- **Insensitive to Radial and Axial Play**
- **-40°C to +85°C Operating Temperature**
- **High Resolution Version of the HEDS-970X**
- **Two Channel Quadrature Output**
- **TTL Compatible**
- **Single 5 V Supply**
- **Wave Solderable**

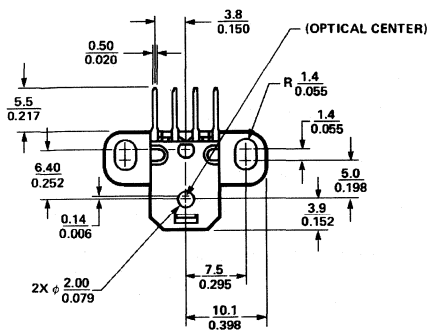
Description

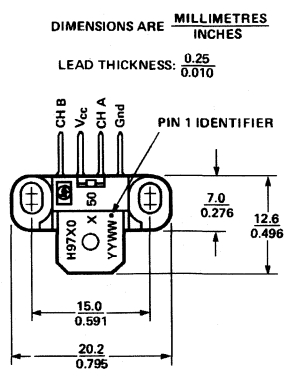
The HEDS-9730 series is a high performance, low cost, optical incremental encoder module. When operated in conjunction

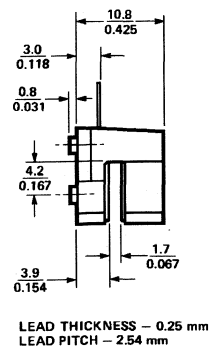




Package Dimensions







Mounting Option #50 - Standard (Baseplane Mounting) Contact Factory for Detailed Package Dimensions

ESD WARNING: NORMAL HANDLING PRECAUTIONS SHOULD BE TAKEN TO AVOID STATIC DISCHARGE.

with either a codewheel or codestrip, this module detects rotary or linear position. The module consists of a lensed LED source and a detector IC enclosed in a small C-shaped plastic package. Due to a highly collimated light source and a unique photodetector array, the module is extremely tolerant to mounting misalignment.

The two channel digital outputs and 5V supply input are accessed through four solder-plated leads located on 2.54 mm (0.1 inch) centers.

The standard HEDS-9730 is designed for use with an 11 mm optical radius codewheel, or linear codestrip. Other options are available. Please contact factory for more information.

Applications

The HEDS-9730 provides sophisticated motion detection at a low cost, making closed-loop control very cost-competitive! Typical applications include printers, plotters, copiers, and office automation equipment.

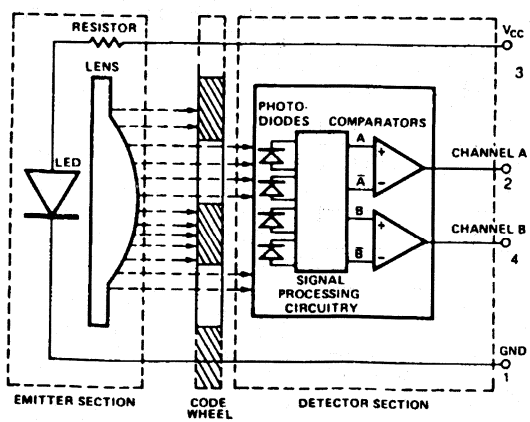
Theory of Operation

The HEDS-9730 is a C-shaped emitter/detector module. Coupled with a codewheel, it translates rotary motion into a two-channel digital output. Coupled with a codestrip, it translates linear motion into a digital output.

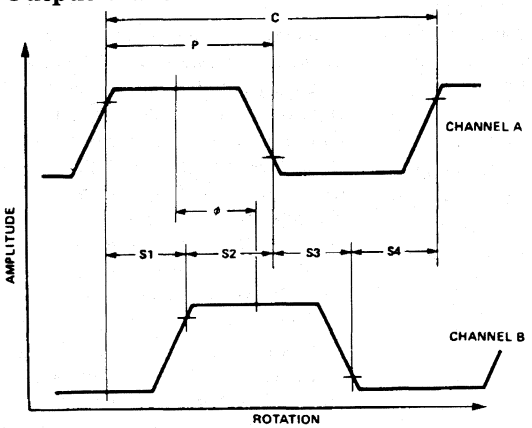
As seen in the block diagram, the module contains a single Light Emitting Diode (LED) as its light source. The light is collimated into a parallel beam by means of a single lens located directly over the LED. Opposite the emitter is the integrated detector circuit. This IC consists of multiple sets of photodetectors and the signal processing circuitry necessary to produce the digital waveforms.

The codewheel/codestrip moves between the emitter and detector, causing the light beam to be interrupted by the pattern of spaces and bars on the codewheel/codestrip. The photodiodes which detect these interruptions are arranged in a pattern that corresponds to the radius and count density of the codewheel/codestrip. These detectors are also spaced such that a light period on one pair of detectors corresponds to a dark period on the adjacent pair of detectors. The photodiode outputs are fed through the signal processing circuitry. Two comparators receive these signals and produce the final outputs for channels A and B. Due to this integrated phasing technique, the digital output of channel A is in quadrature with channel B (90 degrees out of phase).

Block Diagram



Output Waveforms



Definitions

Count (N) = The number of bar and window pairs or counts per revolution (CPR) of the codewheel, or the number of lines per inch of the codestrip (LPI).

1 Shaft Rotation = 360 mechanical degrees
= N cycles
1 cycle (c) = 360 electrical degrees (°e)
= 1 bar and window pair

Pulse Width (P): The number of electrical degrees that an output is high during one cycle. This value is nominally 180°e or 1/2 cycle.

Pulse Width Error (ΔP): The deviation, in electrical degrees, of the pulse width from its ideal value of 180°e.

State Width (S): The number of electrical degrees between a transition in the output of channel A and the neighboring transition in the output of channel B. There are 4 states per cycle, each nominally 90°e.

State Width Error (ΔS): The deviation, in electrical degrees, of each state width from its ideal value of 90°e.

Phase (ϕ): The number of electrical degrees between the center of the high state of channel A and the center of the high state of channel B. This value is nominally 90°e for quadrature output.

Phase Error (Δϕ): The deviation of the phase from its ideal value of 90°e.

Direction of Rotation: When the codewheel rotates counterclockwise, as viewed looking down on the module (so the marking is visible), channel A will lead channel B. If the codewheel rotates in the opposite direction, channel B will lead channel A.

Optical Radius (Rop): The distance from the codewheel's center of rotation to the optical center (O.C.) of the encoder module.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Notes
Storage Temperature	T_S	-40	85	°C	See Note
Operating Temperature	T_A	-40	85	°C	See Note
Supply Voltage	V_{CC}	-0.5	7	V	
Output Voltage	V_O	-0.5	V_{CC}	V	
Output Current per Channel	I_O	-1.0	5	mA	
Soldering Temperature			260	°C	t ≤ 5 sec.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Notes
Temperature	T	-40	85	°C	
Supply Voltage	V_{CC}	4.5	5.5	V	Ripple < 100 mV_{p-p}
Load Capacitance	C_L		100	pF	3.2 kΩ pull-up
Count Frequency			20	kHz	(Velocity (rpm) x N)/60

Note: The module performance is specified at 20 kHz but can operate at higher frequencies. Contact factory for more information.

Electrical Characteristics

Electrical Characteristics over Recommended Operating Range, Typical at 25°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Supply Current	I_{CC}		17	40	mA	
High Level Output Voltage	V_{OH}	2.4			V	I_{OH} = -200 µA
Low Level Output Voltage	V_{OL}			0.4	V	I_{OL} = 3.86 mA
Rise Time	t_r		180		ns	C_L = 25 pF, R_L = 3.3 kΩ pull-up
Fall Time	t_f		40		ns	

Encoding Characteristics

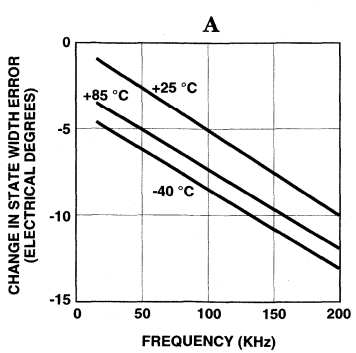
Encoding Characteristics over Recommended Operating Range and Recommended Mounting Tolerances. These characteristics do not include codewheel/codestrip contribution. The Typical Values are averages over the full rotation of the codewheel. For operation above 20 kHz, see frequency derating curves.

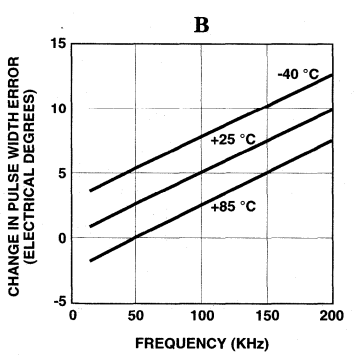
Parameter	Symbol	Typical	Maximum	Units
Pulse Width Error	ΔP	5	45	°e
Logic State Width Error	ΔS	3	45	°e
Phase Error	Δϕ	2	15	°e

Note: Module mounted on tolerances of ± 0.13 mm (± 0.005") radius referenced from centerline of codewheel shaft to alignment tabs. 3.3 kΩ pull-up resistors used on all encoder module outputs.

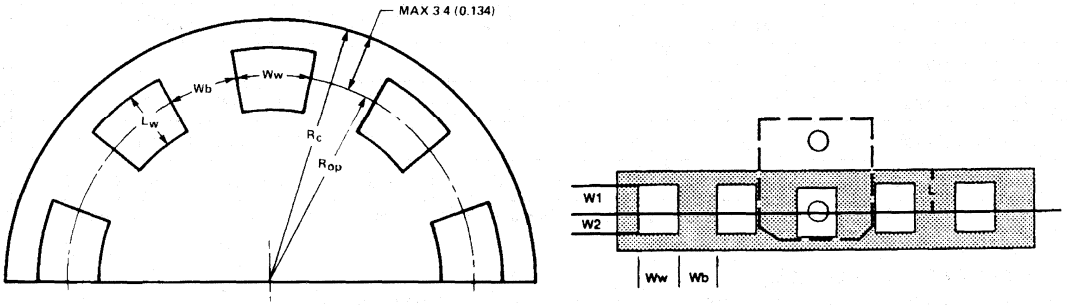
Frequency Derating Curves

Typical performance over extended operating range. These curves were derived using a 25 pF load with a 3.3 k pull-up resistor. Greater load capacitances will cause more error than shown in these graphs.



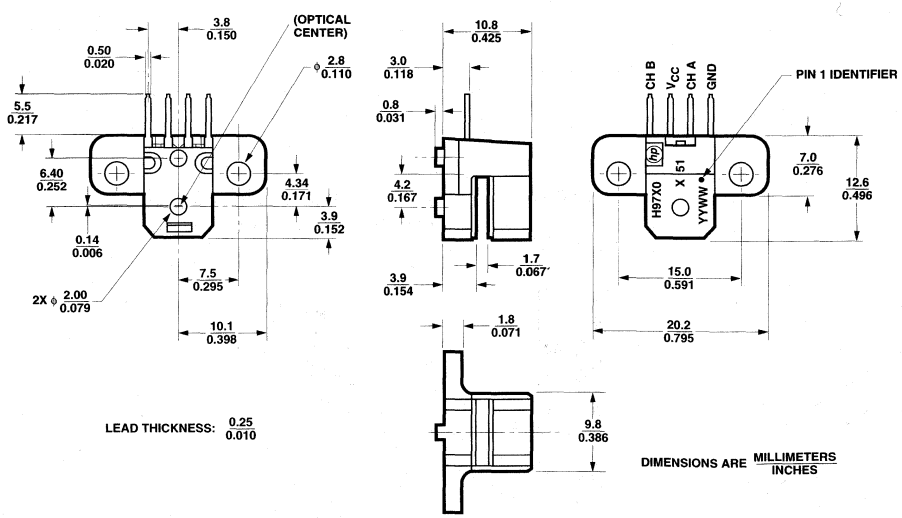


Recommended Codewheel and Codestrip Characteristics



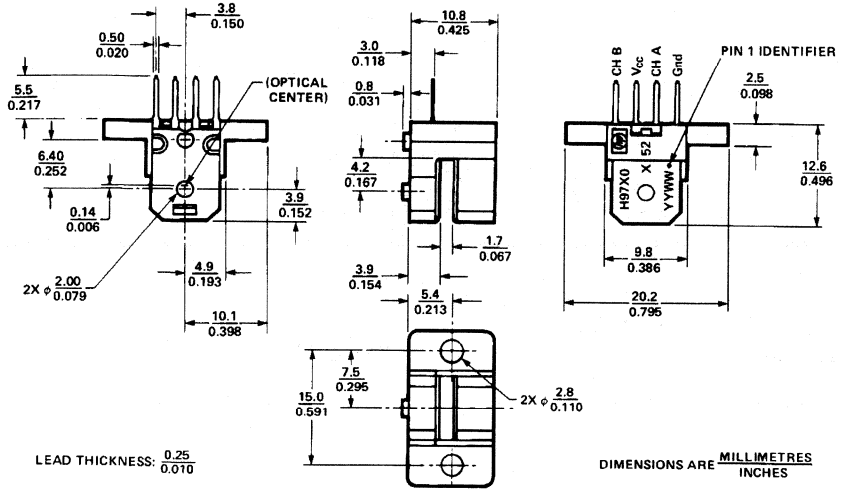
Parameter	Symbol	Min.	Max.	Units	Notes
Window/Bar Ratio	Ww/Wb	0.7	1.4		
Window Length (Rotary)	Lw	1.80 (0.071)	2.30 (0.091)	mm (inch)	
Absolute Maximum Codewheel Radius (Rotary)	Rc		Rop + 3.40 (Rop + 0.134)	mm (inch)	Includes eccentricity errors
Center of Post to Inside Edge of Window	W1	1.04 (0.041)		mm (inch)	
Center of Post to Outside Edge of Window	W2	0.76 (0.030)		mm (inch)	
Center of Post to Inside Edge of Codestrip	L		3.60 (0.142)	mm (inch)	

Optional Packages Available

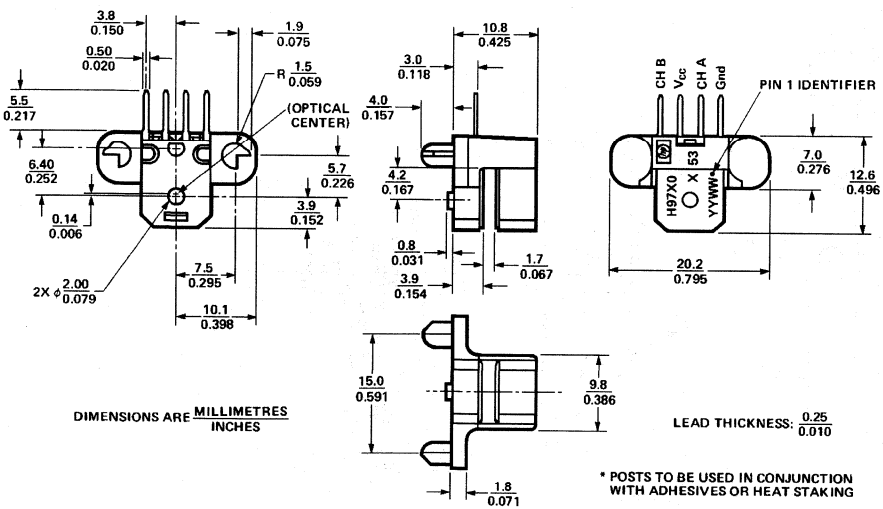


Mounting Option #51 – Rounded Outline (Baseplane Mounting)

Optional Packages Available (cont'd.)

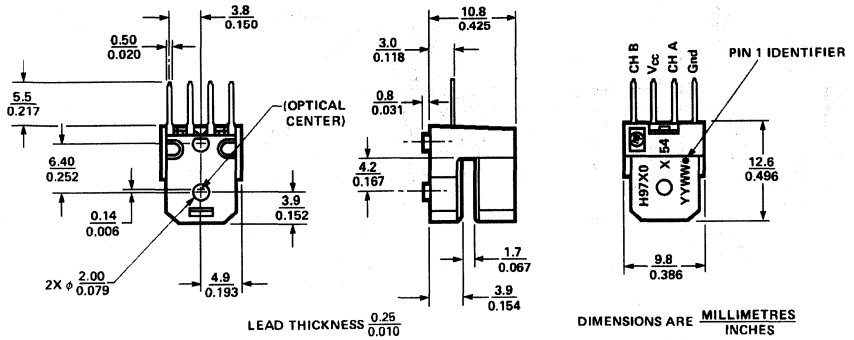


Mounting Option #52 – Backplane (Backplane Mounting)

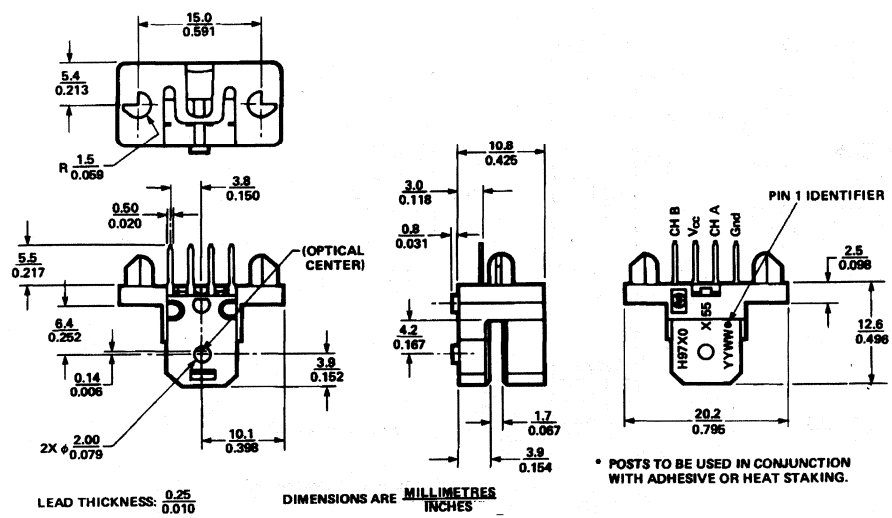


Mounting Option #53 – Standard with Posts (Baseplane Mounting)

Optional Packages Available (cont'd.)

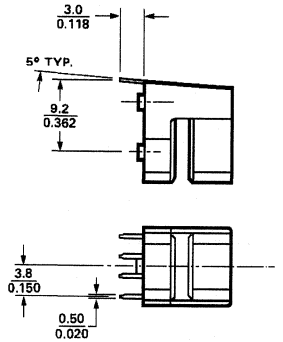


Mounting Option #54 – Tabless (Baseplane Mounting)



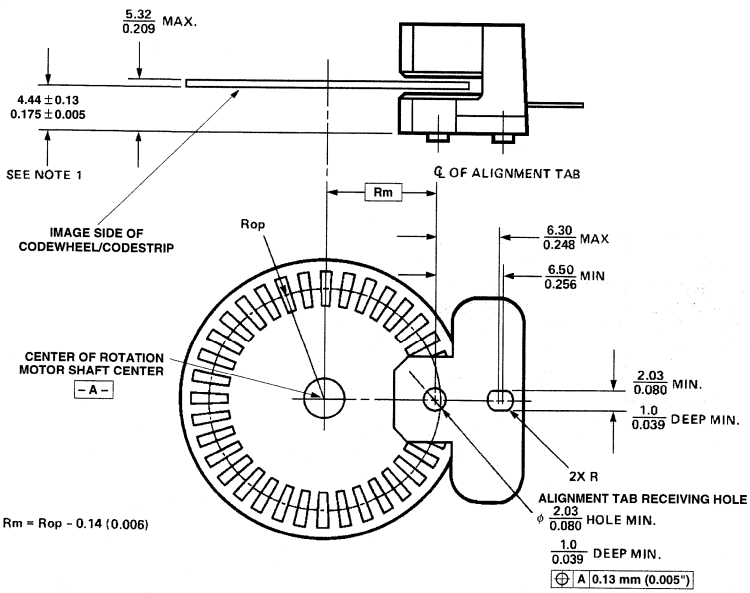
Mounting Option #55 – Backplane with Posts (Backplane Mounting)

Bent Lead Option



DIMENSIONS ARE MILLIMETERS / INCHES

Mounting Considerations



Note: These dimensions include shaft end play and codewheel warp.

All dimensions for mounting the module and codewheel/codestrip should be measured with respect to the two mounting posts, shown above.

Mounting Tolerances

Case 1 specifies the mounting tolerances required on Rm in order to achieve the respective encoding characteristics shown on page 4. The mounting tolerances are as follows:

Case 1: Rm True Position ± 0.13 mm (.005 inches)

Recommended Screw Size: M2.5 x 0.45 or 2-56

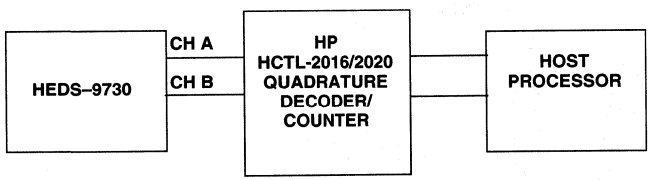
Wave Solder Conditions

Flux – RMA Water Soluble (per MIL-F-14256D)

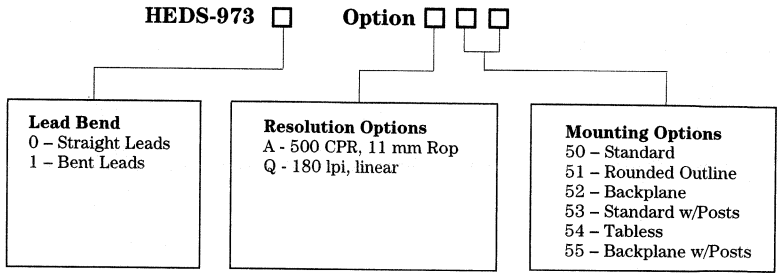
Process Parameters

1. Flux
2. Pre-heat 60 seconds total
   PCB top side @ 230°C
   PCB bottom side @ 260°C
3. Wave solder 255°C, 1.2 meters/min line speed
4. Hot Water Wash
   1st: 30°C 45 seconds
   2nd: 70°C 90 seconds
5. Rinse
   1st: 23°C 45 seconds
   2nd: 23°C 45 seconds
6. Dry
   1st: 80°C 105 seconds
   2nd: 95°C 105 seconds

Typical Interface



Ordering Information



Note: Please contact factory for codewheel and codestrip information.

HEWLETT® PACKARD

Two Channel Optical Incremental Encoder Modules

Technical Data

HEDS-9000
HEDS-9100

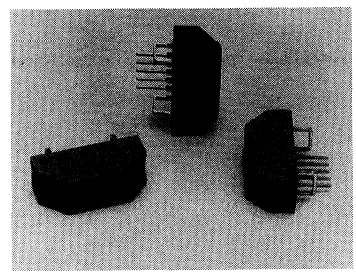
Features

- **High Performance**
- **High Resolution**
- **Low Cost**
- **Easy to Mount**
- **No Signal Adjustment Required**
- **Small Size**
- **-40°C to 100 °C Operating Temperature**
- **Two Channel Quadrature Output**
- **TTL Compatible**
- **Single 5 V Supply**

Description

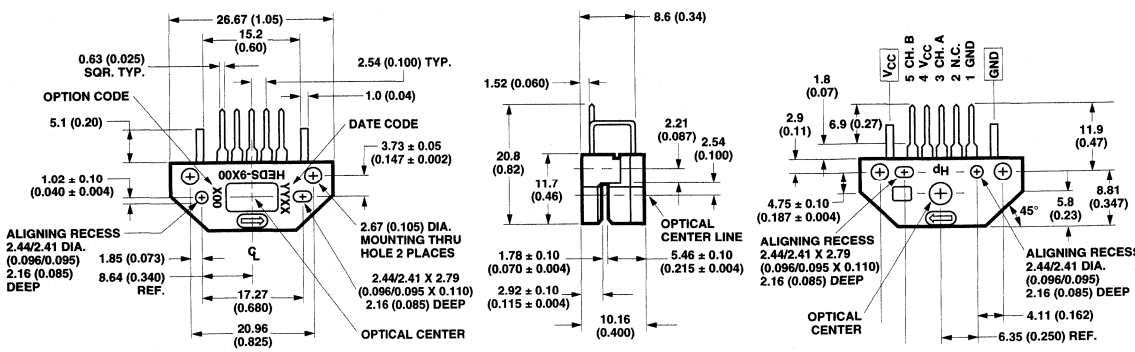
The HEDS-9000 and the HEDS-9100 series are high performance, low cost, optical incremental encoder modules. When used with a codewheel, these modules detect rotary position. The modules consist of a lensed (LED) source and a detector IC enclosed in a small C-shaped plastic package. Due to a highly collimated light source and unique photodetector array, these modules are extremely tolerant to mounting misalignment.

The two channel digital outputs and the single 5 V supply input are accessed through five 0.025 inch square pins located on 0.1 inch centers.



Standard resolutions for the HEDS-9000 are 500 CPR and 1000 CPR for use with a HEDS-6100 codewheel or equivalent.

Package Dimensions



ESD WARNING: NORMAL HANDLING PRECAUTIONS SHOULD BE TAKEN TO AVOID STATIC DISCHARGE.

5965-5887E

For the HEDS-9100, standard resolutions between 96 CPR and 512 CPR are available for use with a HEDS-5120 codewheel or equivalent.

Applications

The HEDS-9000 and 9100 provide sophisticated motion detection at a low cost, making them ideal for high volume applications. Typical applications include printers, plotters, tape drives, and factory automation equipment.

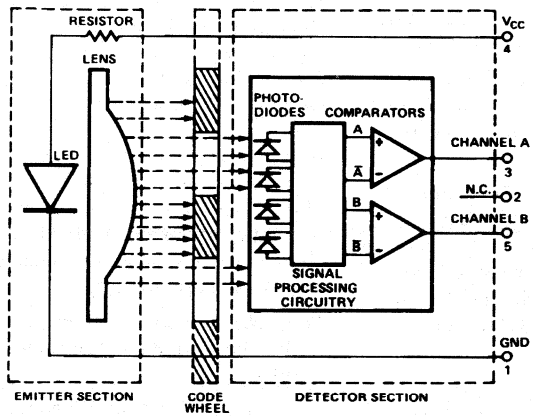
Theory of Operation

The HEDS-9000 and 9100 are C-shaped emitter/detector modules. Coupled with a codewheel, they translate the rotary motion of a shaft into a two-channel digital output.

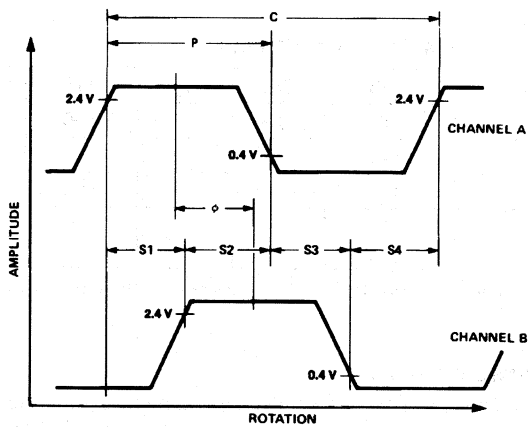
As seen in the block diagram, each module contains a single Light Emitting Diode (LED) as its light source. The light is collimated into a parallel beam by means of a single polycarbonate lens located directly over the LED. Opposite the emitter is the integrated detector circuit. This IC consists of multiple sets of photodetectors and the signal processing circuitry necessary to product the digital waveforms.

The codewheel rotates between the emitter and detector, causing the light beam to be interrupted by the pattern of spaces and bars on the codewheel. The photodiodes which detect these interruptions are arranged in a pattern that corresponds to the radius and design of the ode-wheel. These detectors are also spaced such that a light period on one pair of detectors corresponds to a dark period on the adjacent pair of detectors. The photodiode outputs are then fed through the signal processing circuitry resulting in A, A, B, and B. Two comparators receive these signals and produce the final outputs for channels A and B. Due to this integrated phasing technique, the digital output of channel A is in quadrature with that of channel B (90 degrees out of phase).

Block Diagram



Output Waveforms



Definitions

Count (N): The number of bar and window pairs or counts per revolution (CPR) of the codewheel.

1 Shaft Rotation = 360 mechanical degrees,
= N cycles.

1 cycle (C) = 360 electrical degrees (°e),
= 1 bar and window pair.

Pulse Width (P): The number of electrical degrees that an output is high during 1 cycle. This value is nominally 180°e or 1/2 cycle.

Pulse Width Error (ΔP): The deviation, in electrical degrees of the pulse width from its ideal value of 180°e.

State Width (S): The number of electrical degrees between a transition in the output of channel A and the neighboring transition in the output of channel B. There are 4 states per cycle, each nominally 90°e.

State Width Error (ΔS): The deviation, in electrical degrees, of each state width from its ideal value of 90°e.

Absolute Maximum Ratings

Storage Temperature, T_S ..... -40°C to 100°C
Operating Temperature, T_A ..... -40°C to 100°C
Supply Voltage, V_{CC} ..... -0.5 V to 7 V
Output Voltage, V_O ..... -0.5 V to V_{CC}
Output Current per Channel, I_{out} ..... -1.0 mA to 5 mA

Phase (ϕ): The number of electrical degrees between the center of the high state of channel A and the center of the high state of channel B. This value is nominally 90°e for quadrature output.

Phase Error ($\Delta\phi$): The deviation of the phase from its ideal value of 90°e.

Direction of Rotation: When the codewheel rotates in the direction of the arrow on top of the module, channel A will lead channel B. If the codewheel rotates in the opposite direction, channel B will lead channel A.

Optical Radius (R_{op}): The distance from the codewheel's center of rotation to the optical center (O.C.) of the encoder module.

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Temperature	T	-40		100	°C	
Supply Voltage	V_{CC}	4.5		5.5	Volts	Ripple < 100 mV_{p-p}
Load Capacitance	C_L			100	pF	3.3 kW pull-up resistor
Count Frequency	f			100	kHz	$\frac{\text{Velocity (rpm) x N}}{60}$

Note: The module performance is guaranteed to 100 kHz but can operate at higher frequencies.

Encoding Characteristics

Encoding Characteristics over Recommended Operating Range and Recommended Mounting Tolerances. These Characteristics do not include codewheel/codestrip contribution.

Description	Sym.	Typ.	Case 1 Max.	Case 2 Max.	Units	Notes
Pulse Width Error	ΔP	30	40		°e	
Logic State Width Error	ΔS	30	40		°e	
Phase Error	$\Delta\phi$	2	10	105	°e	

Case 1: Module mounted on tolerance circle of ± 0.13 mm (± 0.005 in.).
Case 2: HEDS-9000 mounted on tolerances of ± 0.50 mm (0.020").
HEDS-9100 mounted ontolerances of ± 0.38 mm (0.015").

Electrical Characteristics

Electrical Characteristics over Recommended Operating Range, typical at 25°C.

Parameter	Symbol	Min.	Typical	Max.	Units	Notes
Supply Current	I_{CC}		17	40	mA	
High Level Output Voltage	V_{OH}	2.4			Volts	I_{OH} = -40 µA max.
Low Level Output Voltage	V_{OL}			0.4	Volts	I_{OL} = 3.2 mA
Rise Time	t_r		200		ns	C_L = 25 pF R_L = 11 kΩ pull-up
Fall Time	t_f		50		ns	

Recommended Codewheel Characteristics

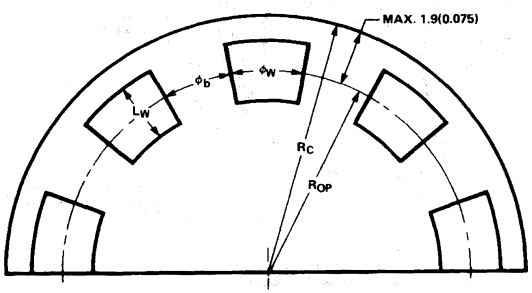


Figure 1. Codestrip Design

Codewheel Options

HEDS Series	CPR (N)	Option	Optical Radius mm (in.)
5120	96	K	11.00 (0.433)
5120	100	C	11.00 (0.433)
5120	192	D	11.00 (0.433)
5120	200	E	11.00 (0.433)
5120	256	F	11.00 (0.433)
5120	360	G	11.00 (0.433)
5120	400	H	11.00 (0.433)
5120	500	A	11.00 (0.433)
5120	512	I	11.00 (0.433)
6100	500	A	23.36 (0.920)
6100	1000	B	23.36 (0.920)

Parameter	Symbol	Minimum	Maximum	Units	Notes
Window/Bar Ratio	ϕ_w/ϕ_b	0.7	1.4		
Window Length	L_W	1.8 (0.071)	2.3 (0.09)	mm (inch)	
Absolute Maximum Codewheel Radius	R_C		R_{OP} + 1.9 (0.0075)	mm (inch)	Includes eccentricity errors

Mounting Considerations

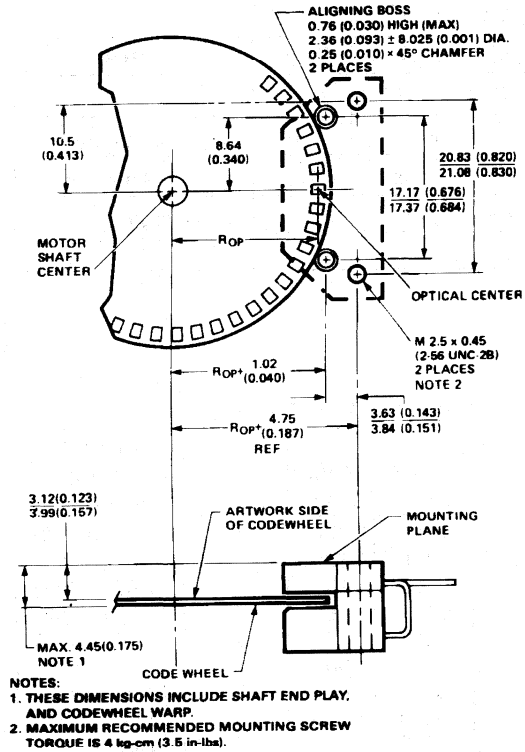


Figure 2. Mounting Plane Side A.

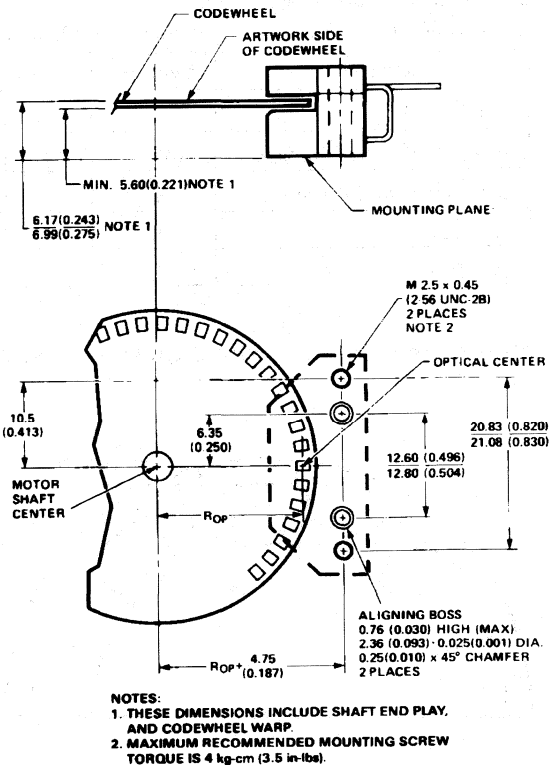


Figure 3. Mounting Plane Side B.

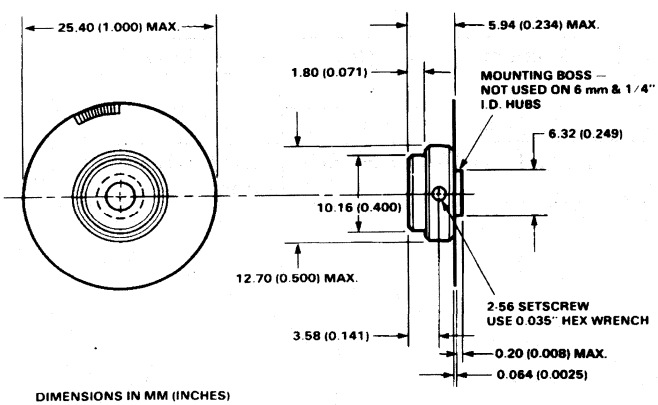


Figure 4. Mounting as Referenced to Side A.

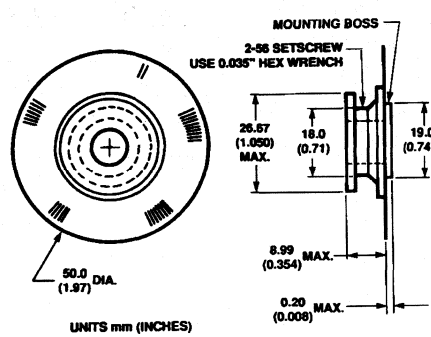


Figure 5. Mounting as Referenced to Side B.

Connectors

Manufacturer	Part Number	Mounting Surface
AMP	1203686-4 640442-5	Both Side B
DuPont	65039-032 with 4825X-000 term.	Both
HP	HEDS-8902 with 4-wire leads	Side B (see Fig. 6)
Molex	2695 series with 2759 series term.	Side B

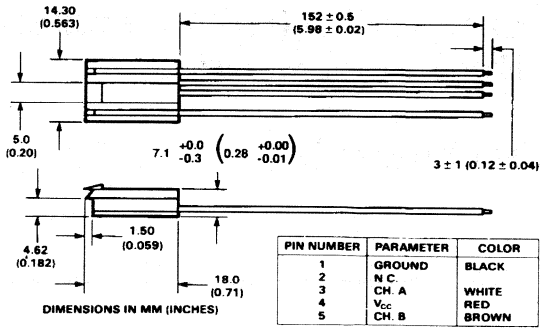


Figure 6. HEDS-8902 Connector.

Ordering Information

HEDS-9000 Option ☐ 0 0 **HEDS-6100 Option** ☐ ☐ ☐

Resolution (Cycles/Rev)
A - 500 CPR
B - 1000 CPR
T = 2000 CPR*
U = 2048 CPR*

Shaft Diameter	
05 - 3/16 in.	10 - 5/8 in.
06 - 1/4 in.	11 - 4 mm
07 - 5/16 in.	12 - 6 mm
08 - 3/8 in.	13 - 8 mm
09 - 1/2 in.	

HEDS-9100 Option ☐ 0 0 **HEDS-5120 Option** ☐ ☐ ☐

Resolution (Cycles/Rev)	
S - 50 CPR	G - 360 CPR
K - 96 CPR	H - 400 CPR
C - 100 CPR	A - 500 CPR
D - 192 CPR	I - 512 CPR
E - 200 CPR	B - 1000 CPR*
F - 256 CPR	J - 1024 CPR*

Shaft Diameter	
01 - 2 mm	11 - 4 mm
02 - 3 mm	14 - 5 mm
03 - 1/8 in.	12 - 6 mm
04 - 5/32 in.	13 - 8 mm
05 - 3/16 in.	
06 - 1/4 in.	

HEDS-91 ☐ ☐

Resolution (Cycles/Rev)
BA - 250 CPR
BB - 480 CPR
BC - 576 CPR

*Please refer to separate HEDS-9000/9100/9200 Extended Resolution series data sheet for detailed information and Codewheel selection.

HEWLETT® PACKARD

Linear Optical Incremental Encoder Modules

Technical Data

HEDS-9200 Series

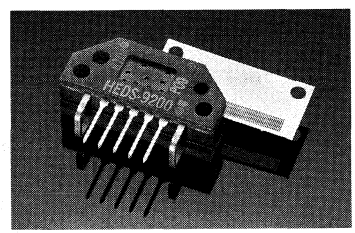
Features

- **High Performance**
- **High Resolution**
- **Low Cost**
- **Easy to Mount**
- **No Signal Adjustment Required**
- **Insensitive to Mechanical Disturbances**
- **Small Size**
- **-40°C to 100°C Operating Temperature**
- **Two Channel Quadrature Output**
- **TTL Compatible**
- **Single 5 V Supply**

Description

The HEDS-9200 series is a high performance, low cost, optical incremental encoder module. When operated in conjunction with a codestrip, this module detects linear position. The module consists of a lensed LED source and a detector IC enclosed in a small C-shaped plastic package. Due to a highly collimated light source and a unique photodetector array, the module is extremely tolerant to mounting misalignment.

The two channel digital outputs and the single 5 V supply input

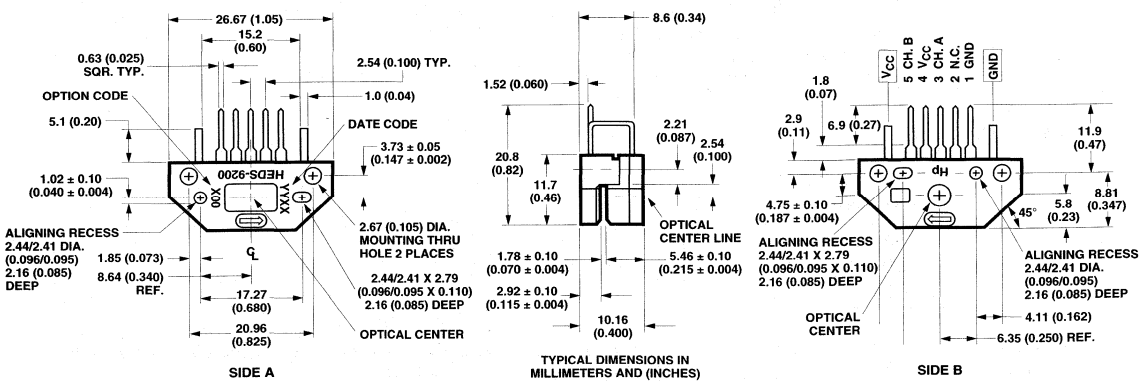


Note: Codestrip not included with HEDS-9200

are accessed through four 0.025 inch square pins located on 0.1 inch centers.

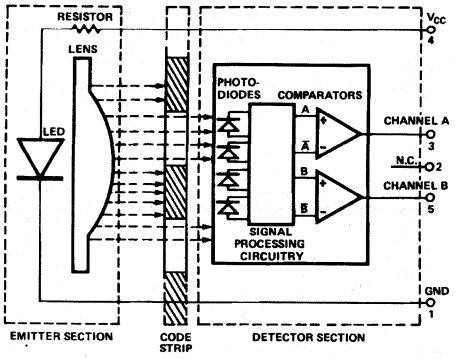
Five standard resolutions between 4.72 counts per mm (120 counts

Package Dimensions

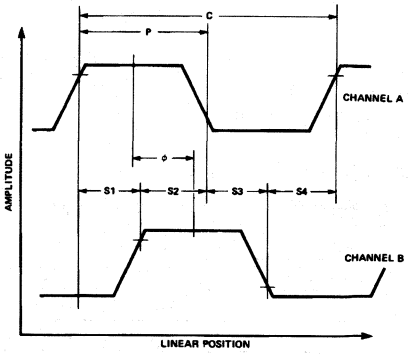


ESD WARNING: NORMAL HANDLING PRECAUTIONS SHOULD BE TAKEN TO AVOID STATIC DISCHARGE.

Block Diagram



Output Waveforms



per inch) and 7.87 counts per mm (200 counts per inch) are available. Consult local Hewlett-Packard sales representatives for other resolutions ranging from 1.5 to 7.87 counts per mm (40 to 200 counts per inch).

Applications

The HEDS-9200 provides sophisticated motion detection at a low cost, making it ideal for high volume applications. Typical applications include printers, plotters, tape drives, and factory automation equipment.

Theory of Operation

The HEDS-9200 is a C-shaped emitter/detector module. Coupled with a codestrip it translates linear motion into a two-channel digital output.

As seen in the block diagram, the module contains a single Light Emitting Diode (LED) as its light source. The light is collimated into a parallel beam by means of a single polycarbonate lens located directly over the LED. Opposite the emitter is the integrated detector circuit. This IC consists of multiple sets of photodetectors and the signal processing circuitry necessary to produce the digital waveforms.

The codestrip moves between the emitter and detector, causing the light beam to be interrupted by the pattern of spaces and bars on the codestrip. The photodiodes which detect these interruptions are arranged in a pattern that corresponds to the count density of the codestrip. These detectors are also spaced such that a light period on one pair of detectors corresponds to a dark period on the adjacent pair of detectors. The photodiode outputs are then fed through the signal processing circuitry resulting in A, $\overline{A}$, B and $\overline{B}$. Two comparators receive these signals and produce the final outputs for channels A and B. Due to this integrated phasing technique, the digital output of channel A is in quadrature with that of channel B (90 degrees out of phase) .

Definitions

Count density (D): The number of bar and window pairs per unit length of the codestrip.

Pitch: 1/D, The unit length per count.

Electrical degree (°e): Pitch/360, The dimension of one bar and window pair divided by 360.

1 cycle (C): 360 electrical degrees, 1 bar and window pair.

Pulse Width (P): The number of electrical degrees that an output is high during 1 cycle. This value is nominally 180°e or 1/2 cycle.

Pulse Width Error (ΔP): The deviation, in electrical degrees, of the pulse width from its ideal value of 180°e.

State Width (S): The number of electrical degrees between a transition in the output of channel A and the neighboring transition in the output of channel B. There are 4 states per cycle, each nominally 90°e.

State Width Error (ΔS): The deviation, in electrical degrees, of each state width from its ideal value of 90°e.

Phase (ϕ): The number of electrical degrees between the center of the high state of channel A and the center of the high state of channel B. This value is nominally 90°e for quadrature output.

Phase Error ($\Delta\phi$): The deviation of the phase from its ideal value of 90°e.

Direction of Movement: When the codestrip moves, relative to the module, in the direction of the arrow on top of the module, channel A will lead channel B. If the codestrip moves in the opposite direction, channel B will lead channel A.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Storage Temperature	T_S	-40		100	°C	
Operating Temperature	T_A	-40		100	°C	
Supply Voltage	V_{CC}	-0.5		7	Volts	
Output Voltage	V_O	-0.6		V_{CC}	Volts	
Output Current per Channel	I_O	-10		5	mA	

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Temperature	T	-40		100	°C	
Supply Voltage	V_{CC}	4.5		5.5	Volts	Ripple < 100 m Vp-p
Load Capacitance	C_L			100	pF	3.2 KΩ Pull-Up Resistor
Count Frequency	f			100	kHz	Velocity $\left(\frac{\text{inch}}{\text{sec}} \times \frac{\text{Counts}}{\text{inch}}\right)$

Note: The module performance is guaranteed to 100 kHz but can operate at higher frequencies.

Encoding Characteristics

Encoding Characteristics Over Recommended Operating Range and Recommended Mounting Tolerances. These Characteristics Do Not Include Codestrip Defects.

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Pulse Width Error	ΔP		7	35	elec. deg.	
Logic State Width Error	ΔS		5	35	elec. deg.	
Phase Error	$\Delta\phi$		2	13	elec. deg.	

Electrical Characteristics

Electrical Characteristics Over Recommended Operating Range, Typical at 25°C

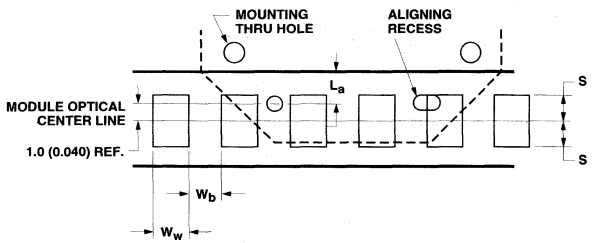
Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Supply Current	I_{CC}		17	40	mA	
High Level Output Voltage	V_{OH}	2.4			Volts	I_{OH} = -40 µA Max.
Low Level Output Voltage	V_{OL}			0.4	Volts	I_{OL} = 3.2 mA
Rise Time	t_r		200		ns	C_L = 25 pF R_L = 11 KΩ Pull-Up
Fall Time	t_f		50		ns	

Note:
1. For improved performance in noisy environments or high speed applications, a 3.3 kΩ pull-up resistor is recommended.

Recommended Codestrip Characteristics

Codestrip design must take into consideration mounting as referenced to either side A or side B (see Figure 4).

Mounting as Referenced to Side A



Mounting as Referenced to Side B

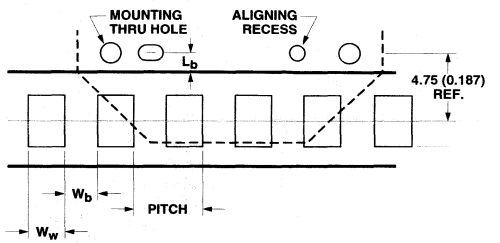


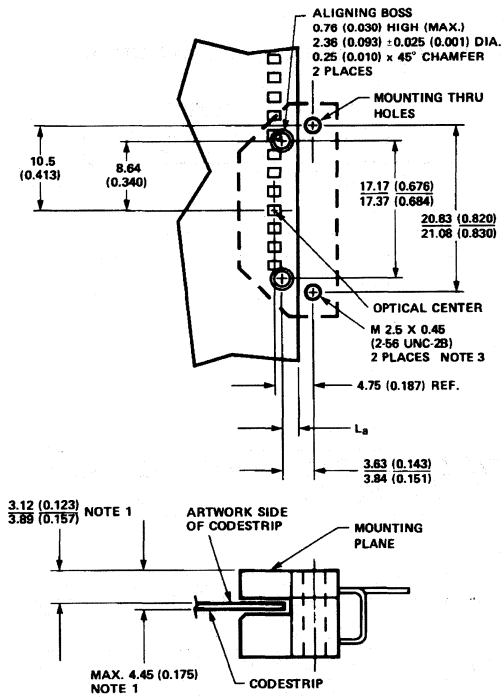
Figure 1. Codestrip Design.

STATIC CHARGE WARNING: LARGE STATIC CHARGE ON CODESTRIP MAY HARM MODULE. PREVENT ACCUMULATION OF CHARGE.

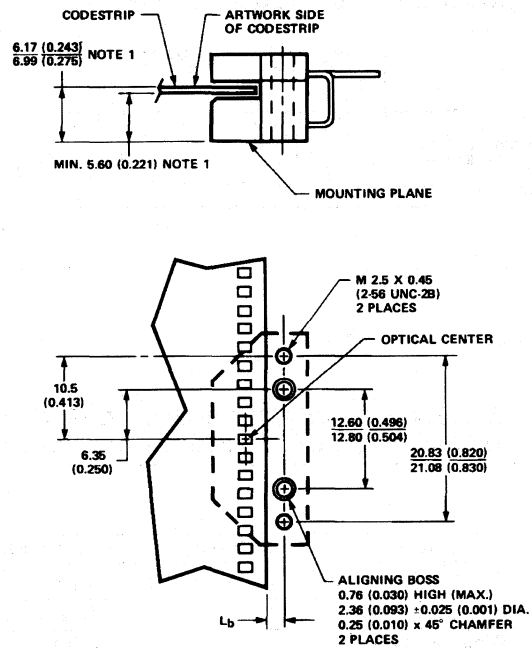
Parameter	Symbol	Mounting Ref. Side A	Mounting Ref. Side B	Units
Window/Bar Ratio	W_w/W_b	0.7 min., 1.4 max.	0.7 min., 1.4 max.	
Mounting Distance	L	$L_a \leq 0.51$ (0.020)	$L_b \geq 3.23$ (0.127)	mm (inch)
Window Edge to Module Opt Center Line	S	0.90 (0.035) min.	0.90 (0.035) min.	mm (inch)
Parallelism Module to Codestrip	α	1.3 max.	1.3 max.	deg.

Note: All parameters and equations must be satisfied over the full length of codestrip travel including maximum codestrip runout.

Mounting Considerations



MOUNTING PLANE SIDE A



MOUNTING PLANE SIDE B

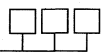
Notes:

1. These dimensions include codestrip warp.
2. Reference definitions of L_a and L_b on page 4.
3. Maximum recommended mounting screw torque is 4 kg-cm (3.5 in-lbs).

Connectors

Manufacturer	Part Number	Mounting Surface
AMP	103686-4	Both
	640442-5	Side B
DuPont	65039-032 with 4825X-000 Term.	Both
HP	HEDS-8902 with 4-wire Leads	Side B
Molex	2695 Series with 2759 Series Term.	Side B

Ordering Information

HEDS-9200 Option 

Resolution Counts per mm (inch)	Pitch mm (inch) per count
100 - 3.937 (100)	0.254 (0.0100)
L00 - 4.72 (120)	0.212 (0.0083)
M00 - 5.00 (127)	0.200 (0.0079)
P00 - 5.91 (150)	0.169 (0.0067)
Q00 - 7.09 (180)	10.141 (0.0056)
R00 - 7.87 (200)	0.127 (0.0050)
300 - 11.81 (300)*	0.085 (0.0033)*
360 - 14.17 (360)*	0.071 (0.0028)*

Consult local Hewlett-Packard sales representatives for other resolutions.

*Please refer to separate HEDS-9000/9100/9200 Extended Resolution Series data sheet for detailed information.

HEWLETT® PACKARD

Three Channel Optical Incremental Encoder Modules

Technical Data

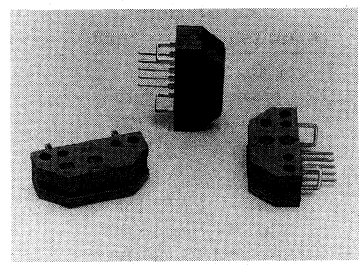
HEDS-9040
HEDS-9140

Features

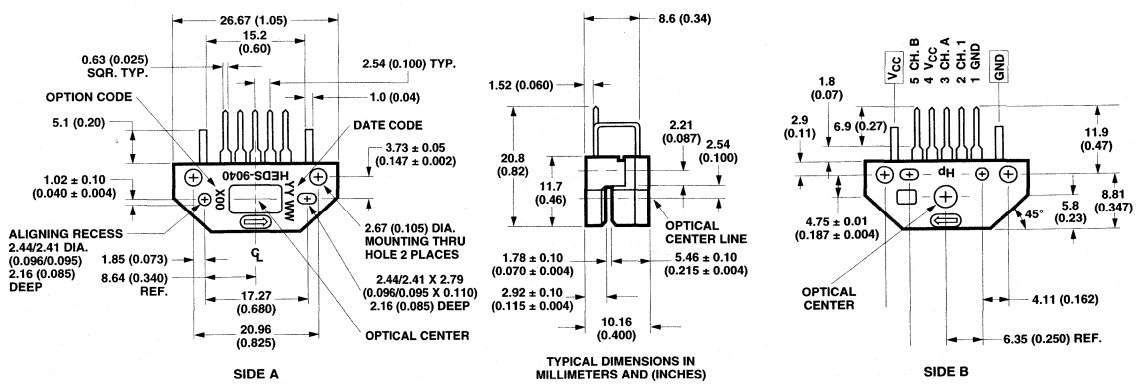
- **Two Channel Quadrature Output with Index Pulse**
- **Resolution Up to 2000 CPR Counts Per Revolution**
- **Low Cost**
- **Easy to Mount**
- **No Signal Adjustment Required**
- **Small Size**
- **-40°C to 100°C Operating Temperature**
- **TTL Compatible**
- **Single 5 V Supply**

Description

The HEDS-9040 and HEDS-9140 series are three channel optical incremental encoder modules. When used with a codewheel, these low cost modules detect rotary position. Each module consists of a lensed LED source and a detector IC enclosed in a small plastic package. Due to a highly collimated light source and a unique photodetector array, these modules provide the same high performance found in the HEDS-9000/9100 two channel encoder family.



Package Dimensions



ESD WARNING: NORMAL HANDLING PRECAUTIONS SHOULD BE TAKEN TO AVOID STATIC DISCHARGE.

The HEDS-9040 and 9140 have two channel quadrature outputs plus a third channel index output. This index output is a 90 electrical degree high true index pulse which is generated once for each full rotation of the codewheel.

The HEDS-9040 is designed for use with a HEDX-614X codewheel which has an optical radius of 23.36 mm (0.920 inch). The HEDS-9140 is designed for use with a HEDS-5140 codewheel which has an optical radius of 11.00 mm (0.433 inch).

The quadrature signals and the index pulse are accessed through five 0.025 inch square pins located on 0.1 inch centers.

Standard resolutions between 256 and 2000 counts per revolution are available. Consult local Hewlett-Packard sales representatives for other resolutions.

Applications

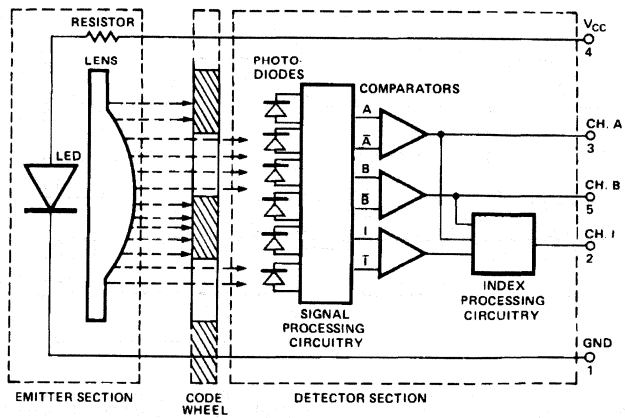
The HEDS-9040 and 9140 provide sophisticated motion control detection at a low cost, making them ideal for high volume applications. Typical applications include printers, plotters, tape drives, and industrial and factory automation equipment.

Theory of Operation

The HEDS-9040 and 9140 are emitter/detector modules. Coupled with a codewheel, these modules translate the rotary motion of a shaft into a three-channel digital output.

As seen in the block diagram, the modules contain a single Light

Block Diagram

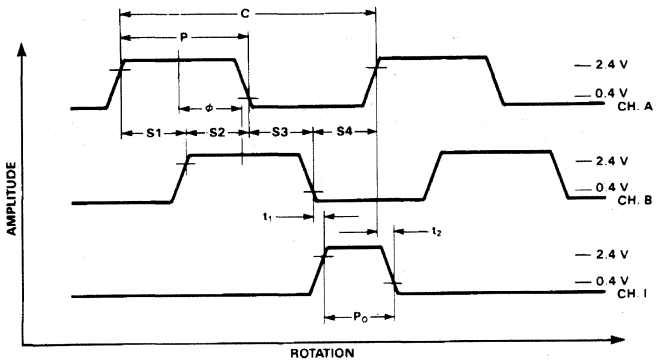


Emitting Diode (LED) as its light source. The light is collimated into a parallel beam by means of a single polycarbonate lens located directly over the LED. Opposite the emitter is the integrated detector circuit. This IC consists of multiple sets of photodetectors and the signal processing circuitry necessary to produce the digital waveforms.

The codewheel rotates between the emitter and detector, causing the light beam to be interrupted by the pattern of spaces and bars on the codewheel. The photodiodes which detect these interruptions are arranged in a pattern that corresponds to the radius and design of the codewheel. These detectors are also spaced such that a light period on one pair of detectors corresponds to a dark period on the adjacent pair of detectors. The photodiode outputs are then fed through the signal processing circuitry resulting in A, $\overline{A}$, B, $\overline{B}$, I and $\overline{I}$. Comparators receive these signals and produce the final outputs for channels A and B. Due to this integrated phasing technique, the digital output of channel A is in quadrature with that of channel B (90 degrees out of phase).

The output of the comparator for I and $\overline{I}$ is sent to the index processing circuitry along with the outputs of channels A and B. The final output of channel I is an index pulse P_O which is generated once for each full rotation of the codewheel. This output P_O is a one state width (nominally 90 electrical degrees), high true index pulse which is coincident with the low states of channels A and B.

Output Waveforms



Definitions

Count (N): The number of bar and window pairs or counts per revolution (CPR) of the codewheel.

One Cycle (C): 360 electrical degrees (°e), 1 bar and window pair.

One Shaft Rotation: 360 mechanical degrees, N cycles.

Position Error ($\Delta\Theta$): The normalized angular difference between the actual shaft position and the position indicated by the encoder cycle count.

Cycle Error (ΔC): An indication of cycle uniformity. The difference between an observed shaft angle which gives rise to one electrical cycle, and the nominal angular increment of 1/N of a revolution.

Pulse Width (P): The number of electrical degrees that an output is high during 1 cycle. This value is nominally 180°e or 1/2 cycle.

Pulse Width Error (ΔP): The deviation, in electrical degrees, of the pulse width from its ideal value of 180°e.

State Width (S): The number of electrical degrees between a transition in the output of channel A and the neighboring transition in the output of channel B. There are 4 states per cycle, each nominally 90°e.

State Width Error (ΔS): The deviation, in electrical degrees, of each state width from its ideal value of 90°e.

Phase (ϕ): The number of electrical degrees between the center of the high state of channel A and the center of the high state of channel B. This value is nominally 90°e for quadrature output.

Phase Error ($\Delta\phi$): The deviation of the phase from its ideal value of 90°e.

Direction of Rotation: When the codewheel rotates in the direction of the arrow on top of the module, channel A will lead channel B. If the codewheel rotates in the opposite direction, channel B will lead channel A.

Optical Radius (R_{OP}): The distance from the codewheel's center of rotation to the optical center (O.C.) of the encoder module.

Index Pulse Width (P_O): The number of electrical degrees that an index is high during one full shaft rotation. This value is nominally 90°e or 1/4 cycle.

Absolute Maximum Ratings

Storage Temperature, T_S	-40°C to +100°C
Operating Temperature, T_A	-40°C to +100°C
Supply Voltage, V_{CC}	-0.5 V to 7 V
Output Voltage, V_O	-0.5 V to V_{CC}
Output Current per Channel, I_{OUT}	-1.0 mA to 5 mA
Shaft Axial Play	± 0.25 mm (± 0.010 in.)
Shaft Eccentricity Plus Radial Play	0.1 mm (0.004 in.) TIR
Velocity	30,000 RPM[1]
Acceleration	250,000 rad/sec²[1]

Note:

1. Absolute maximums for HEDS-5140/6140 codewheels only.

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Temperature	T_A	-40		100	°C	
Supply Voltage	V_{CC}	4.5	5.0	5.5	Volts	Ripple < 100 mV_{p-p}
Load Capacitance	C_L			100	pF	2.7 kΩ pull-up
Count Frequency	f			100	kHz	Velocity (rpm) x N/60
Shaft Perpendicularity Plus Axial Play				± 0.25 (± 0.010)	mm (in.)	6.9 mm (0.27 in.) from mounting surface
Shaft Eccentricity Plus Radial Play				0.04 (0.0015)	mm (in.) TIR	6.9 mm (0.27 in.) from mounting surface

Note: The module performance is guaranteed to 100 kHz but can operate at higher frequencies. For the HEDS-9040 #T00 for operation below 0°C and greater than 50 kHz the maximum Pulse Width and Logic State Width errors are 60°e.

Encoding Characteristics
HEDS-9040 (except #T00), HEDS-9140

Encoding Characteristics over Recommended Operating Range and Recommended Mounting Tolerances unless otherwise specified. Values are for the worst error over the full rotation of HEDS-5140 and HEDS-6140 codewheels.

Parameter		Symbol	Min.	Typ.[1]	Max.	Units
Cycle Error		ΔC		3	5.5	°e
Pulse Width Error		ΔP		7	30	°e
Logic State Width Error		ΔS		5	30	°e
Phase Error		Δϕ		2	15	°e
Position Error		ΔΘ		10	40	min. of arc
Index Pulse Width		P_0	60	90	120	°e
CH. I rise after CH. B or CH. A fall	-25°C to +100°C	t_1	10	100	250	ns
	-40°C to +100°C	t_1	-300	100	250	ns
CH. I fall after CH. A or CH. B rise	-25°C to +100°C	t_2	70	150	300	ns
	-40°C to +100°C	t_2	70	150	1000	ns

Note:
1. Module mounted on tolerance circle of ± 0.13 mm (± 0.005 in.) radius referenced from module Side A aligning recess centers. 2.7 kΩ pull-up resistors used on all encoder module outputs.

Encoding Characteristics
HEDS-9040 #T00

Encoding Characteristics over Recommended Operating Range and Recommended Mounting Tolerances unless otherwise specified. Values are for the worst error over the full rotation of HEDM-614X Option TXX codewheel.

Parameter		Symbol	Min.	Typ.[1]	Max.	Units
Cycle Error		ΔC		3	7.5	°e
Pulse Width Error		ΔP		7	50	°e
Logic State Width Error		ΔS		5	50	°e
Phase Error		$\Delta\phi$		2	15	°e
Position Error		$\Delta\Theta$		2	20	min. of arc
Index Pulse Width		P_O	40	90	140	°e
CH. I rise after CH. B or CH. A fall	-40°C to +100°C	t_1	10	450	1500	ns
CH. I fall after CH. A or CH. B rise	-40°C to +100°C	t_2	10	250	1500	ns

Note:
1. Module mounted on tolerance circle of ± 0.13 mm (± 0.005 in.) radius referenced from module Side A aligning recess centers. 2.7 kΩ pull-up resistors used on all encoder module outputs.

Electrical Characteristics

Electrical Characteristics over Recommended Operating Range.

Parameter	Symbol	Min.	Typ.[1]	Max.	Units	Notes
Supply Current	I_{CC}	30	57	85	mA	
High Level Output Voltage	V_{OH}	2.4			V	I_{OH} = -200 µA max.
Low Level Output Voltage	V_{OL}			0.4	V	I_{OL} = 3.86 mA
Rise Time	t_r		180[2]		ns	C_L = 25 pF R_L = 2.7 kΩ pull-up
Fall Time	t_f		49[2]		ns	

Notes:
1. Typical values specified at V_{CC} = 5.0 V and 25°C.
2. t_r and t_f 80 nsec for HEDS-9040 #T00.

Electrical Interface

To insure reliable encoding performance, the HEDS-9040 and 9140 three channel encoder modules require 2.7 kΩ (± 10%) pull-up resistors on output pins 2, 3, and 5 (Channels I, A and B) as shown in Figure 1. These pull-up resistors should be located as close to the encoder module as possible (within 4 feet). Each of the three encoder module outputs can drive a single TTL load in this configuration.

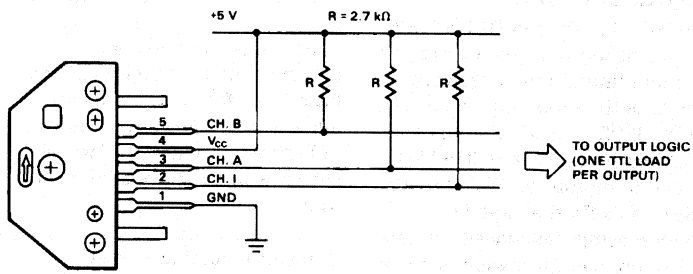


Figure 1. Pull-up Resistors on HEDS-9X40 Encoder Module Outputs.

Mounting Considerations

Figure 2 shows a mounting tolerance *requirement* for proper operation of the HEDS-9040 and HEDS-9140. The Aligning Recess Centers must be located within a tolerance circle of 0.005 in. radius from the nominal locations. This tolerance must be maintained whether the module is mounted with side A as the mounting plane using aligning pins (see Figure 5), or mounted with Side B as the mounting plane using an alignment tool (see Figures 3 and 4).

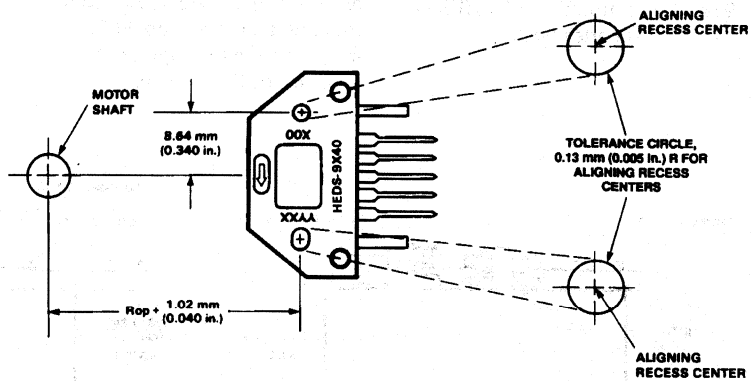


Figure 2. HEDS-9X40 Mounting Tolerance.

Mounting with an Alignment Tool

The HEDS-8905 and HEDS-8906 alignment tools are recommended for mounting the modules with Side B as the mounting plane. The HEDS-8905 is used to mount the HEDS-9140, and the HEDS-8906 is used to mount the HEDS-9040. These tools fix the module position using the codewheel hub as a reference. They will not work if Side A is used as the mounting plane.

The following assembly procedure uses the HEDS-8905/8906 alignment tool to mount a HEDS-9140/9040 module and a HEDS-5140/6140 codewheel:

Instructions:

1. Place codewheel on shaft.

2. Set codewheel height by placing alignment tool on motor base (pins facing up) flush up against the codewheel as shown in Figure 3. Tighten codewheel setscrew and remove alignment tool.

3. Insert mounting screws through module and thread into the motor base. Do not tighten screws.

4. Slide alignment tool over codewheel hub and onto module as shown in Figure 4. The pins of the alignment tool should fit snugly inside the alignment recesses of the module.

5. While holding alignment tool in place, tighten screws down to secure module.

6. Remove alignment tool.

Mounting with Aligning Pins

The HEDS-9040 and HEDS-9140 can also be mounted using aligning pins on the motor base. (Hewlett-Packard does not provide aligning pins.) For this configuration, Side A must be used as the mounting plane. The aligning recess centers must be located within the 0.005 in. R Tolerance Circle as explained above. Figure 5 shows the necessary dimensions.

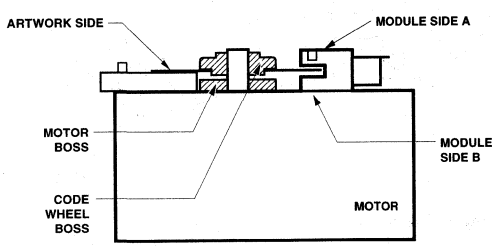
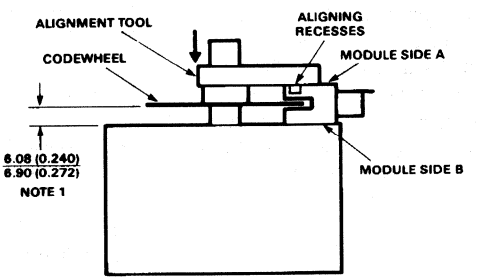


Figure 3. Alignment Tool is Used to Set Height of Codewheel.



NOTE 1: THIS DIMENSION IS FROM THE MOUNTING PLANE TO THE NON-HUB SIDE OF THE CODEWHEEL.

Figure 4. Alignment Tool is Placed over Shaft and onto Codewheel Hub. Alignment Tool Pins Mate with Aligning Recesses on Module.

Mounting with Aligning Pins

The HEDS-9040 and HEDS-9140 can also be mounted using aligning pins on the motor base. (Hewlett-Packard does not provide aligning pins.) For this configuration, Side A *must* be used as the mounting plane. The aligning recess centers must be located within the 0.005 in. Radius Tolerance Circle as explained in "Mounting Considerations." Figure 5 shows the necessary dimensions.

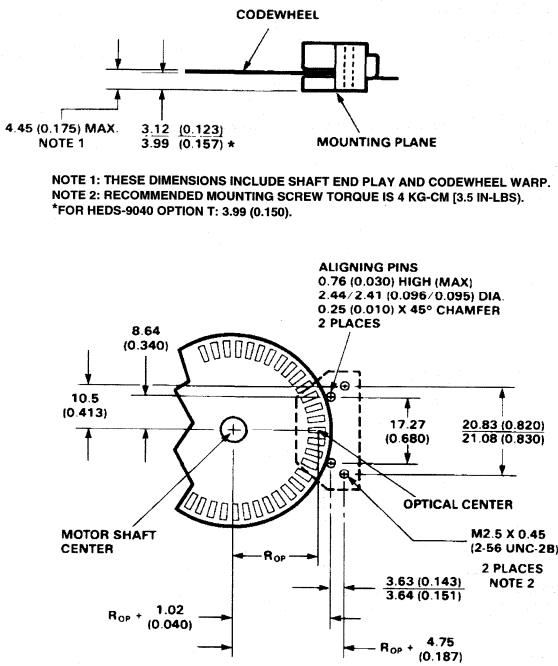


Figure 5. Mounting Plane Side A.

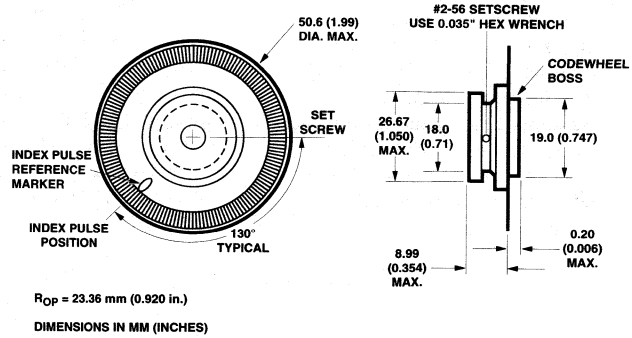


Figure 6a. HEDS-6140 Codewheel Used with HEDS-9040.

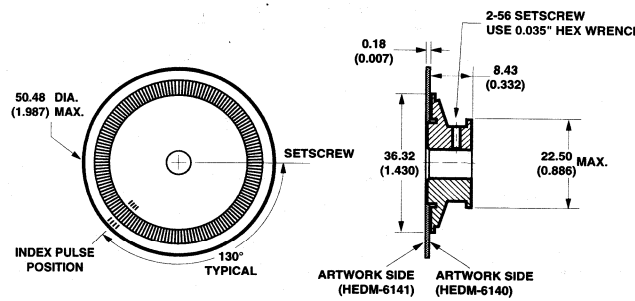


Figure 6b. HEDM-614X Series Codewheel used with HEDS-9040 #T00.

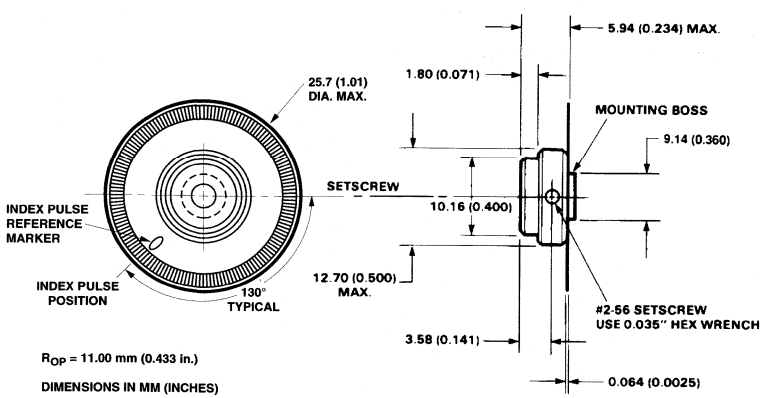


Figure 7. HEDS-5140 Codewheel Used with HEDS-9140.

Orientation of Artwork for HEDS-9040 Option T00 (2000 CPR, 23.36 mm Rop)

The Index area on the HEDS-9040 Option T00, 2000 CPR Encoder Module has a non-symmetrical pattern as does the mating Codewheel. In order for the Index to operate, the "Right-reading" side of the Codewheel disk (the "Artwork Side") must point toward "Side A" of the Module (the side with the connecting pins).

Because the Encoder Module may be used with either "Side A" or with "Side B" toward the Mounting Surface, Hewlett-Packard supplies two versions of Film Codewheels for use with the Option T00 3-channel Module: Codewheel HEDM-6140 Option TXX has the Artwork Side on the "Hub Side" of the Codewheel/hub assembly and works with "Side B" of the Module on the user's mounting surface. Codewheel HEDM-6141 Option TXX has the Artwork Side opposite the "Hub Side" and works with "Side A" of the Module on the mounting surface. For the Index to operate, these parts must be oriented as shown in Figure 7a and 7b.

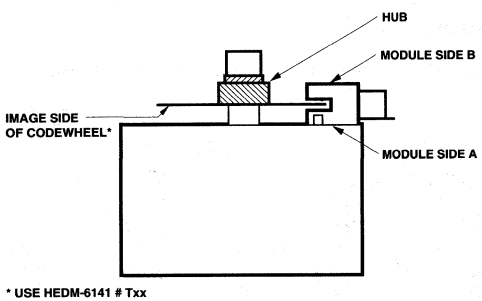


Figure 7a.

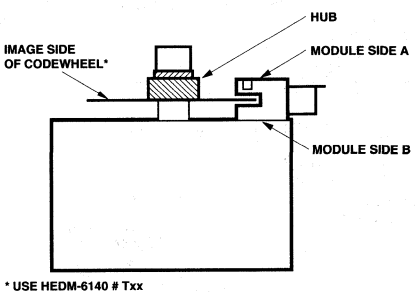


Figure 7b.

*Please note that the image side of the codewheel must always be facing the module Side A.

Connectors

Manufacturer	Part Number	Mounting Surface
AMP	103686-4	Both
	640442-5	Side B
DuPont	65039-032 with 4825X-000 term	Both
HP	HEDS-8903 with 5-wire leads	Side B (see Figure 8)
Molex	2695 series with 2759 series term	Side B

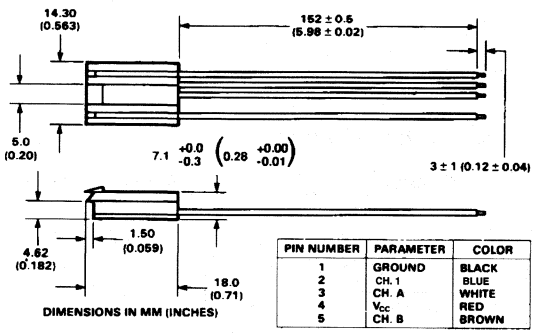
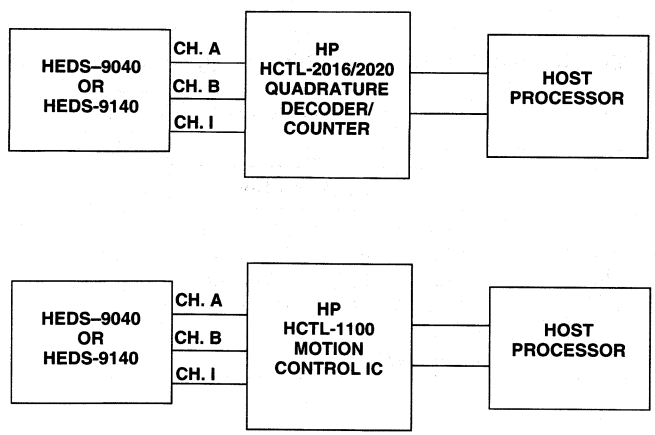


Figure 8. HEDS-8903 Connector.

Typical Interfaces



Ordering Information

Three Channel Encoder Modules and Codewheels, 23.36 mm Optical Radius

HEDS-9040 Option ☐ 0 0 **HEDS-6140 Option** ☐ ☐☐

Assembly Tool

HEDS-8906

Resolution (Cycles/Rev)
B - 1000 CPR
J - 1024 CPR

Shaft Diameter	
05 - 3/16 in.	11 - 4 mm
06 - 1/4 in.	12 - 6 mm
07 - 5/16 in.	13 - 8 mm
08 - 3/8 in.	
09 - 1/2 in.	
10 - 5/8 in.	

Three Channel Encoder Modules and Codewheels, 23.36 mm Optical Radius

HEDS-9040 Option ☐ 0 0 **HEDM-614** ☐ **Option** ☐☐

Assembly Tool

HEDS-8906

Resolution (Cycles/Rev)
T - 2000 CPR

Artwork Orientation*
0 - Artwork on hub side (use when module Side B is down)
1 - Artwork opposite hub side (use when Module Side A is down)

Shaft Diameter	
05 - 3/16 in.	11 - 4 mm
06 - 1/4 in.	12 - 6 mm
07 - 5/16 in.	13 - 8 mm
08 - 3/8 in.	
09 - 1/2 in.	
10 - 5/8 in.	

*Index will not work if wrong orientation is used. Hub side of codewheel must point away from mounting surface. See Figure 7.

Three Channel Encoder Modules and Codewheels, 11.00 mm Optical Radius

HEDS-9140 Option ☐ 0 0 **HEDS-5140 Option** ☐ ☐☐

Assembly Tool

HEDS-8905

Resolution (Cycles/Rev)	
S - 50 CPR	G - 360 CPR
K - 96 CPR	H - 400 CPR
C - 100 CPR	A - 500 CPR
E - 200 CPR	I - 512 CPR
F - 256 CPR	

Shaft Diameter	
01 - 2 mm	11 - 4 mm
02 - 3 mm	14 - 5 mm
03 - 1/8 in.	12 - 6 mm
04 - 5/32 in.	13 - 8 mm
05 - 3/16 in.	
06 - 1/4 in.	

Accessories

Please refer to the codewheel data sheet for information on alignment (centering and gap-setting) tools for the module.

Two Channel High Resolution Optical Incremental Encoder Modules

Technical Data

HEDS-9000/9100/9200 Extended Resolution Series

Features

- **High Resolution: Up to 2048 Cycles per Revolution**
- **Up to 8192 Counts per Revolution with 4X Decoding**
- **Two Channel Quadrature Output**
- **Low Cost**
- **Easy to Mount**
- **No Signal Adjustment Required**
- **Small Size**
- **-40°C to 100 °C Operating Temperature**
- **TTL Compatible**
- **Single 5 V Supply**

Description

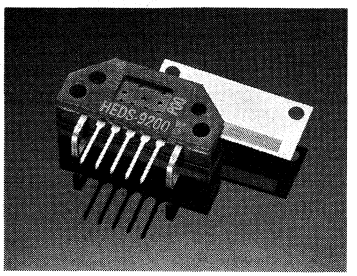
The HEDS-9000 Options T and U and the HEDS-9100 Options B and J are high resolution two channel rotary incremental encoder modules. These options are an extension of our popular HEDS-9000 and HEDS-9100 series. When used with a codewheel, these modules detect relative rotary position. The HEDS-9200 Option 300 and 360 are high resolution linear encoder modules. When used with a codestrip, these modules detect relative linear position.

These modules consist of a lensed Light Emitting Diode (LED) source and detector IC enclosed in a small C shaped plastic package. Due to a highly collimated light source and unique photodetector array, these modules provide a highly reliable quadrature output.

The HEDS-9000 and HEDS-9100 are designed for use with codewheels which have an optical radius of 23.36 mm and 11 mm respectively. The HEDS-9200 is designed for use with a linear codestrip.

These components produce a two channel quadrature output which can be accessed through five 0.025 inch square pins located on 0.1 inch centers.

The resolution of the HEDS-9000 Options T and U are 2000 and 2048 counts per revolution respectively. The HEDS-9100 Options B and J are 1000 and 1024 counts per revolution



respectively. The HEDS-9200 Option 300 and 360 linear encoder modules have resolutions of 300 and 360 lines per inch.

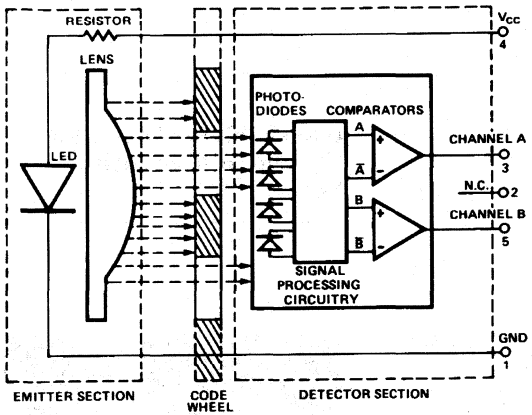
Consult local Hewlett-Packard sales representatives for other resolutions.

Theory of Operation

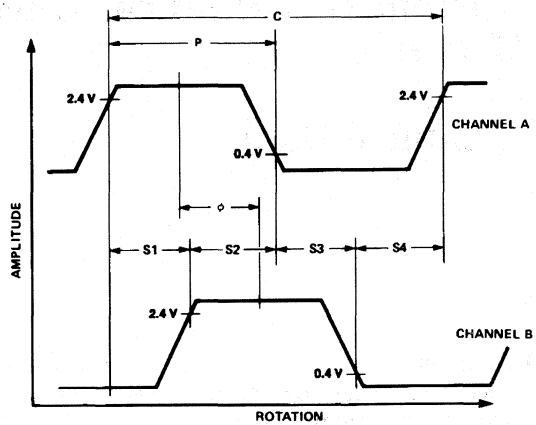
The diagram shown on the following page is a block diagram of the encoder module. As seen in this block diagram, the module contains a single LED as its light source. The light is collimated into a parallel beam by means of a single polycarbonate lens located directly over the LED. Opposite the emitter is the integrated detector circuit. This IC consists

ESD WARNING: NORMAL HANDLING PRECAUTIONS SHOULD BE TAKEN TO AVOID STATIC DISCHARGE.

Block Diagram



Output Waveforms



of multiple sets of photodetectors and the signal processing circuitry necessary to produce the digital waveforms.

The codewheel/codestrip passes between the emitter and detector, causing the light beam to be interrupted by the pattern of spaces and bars on the codewheel. The photodiodes which detect these interruptions are arranged in a pattern that corresponds to the codewheel/codestrip. These detectors are also spaced such that a light period on one pair of detectors corresponds to a dark period on the adjacent pair of detectors. The photodiode outputs are then fed through the signal processing circuitry resulting in A, $\overline{A}$, B, and $\overline{B}$. Comparators receive these signals and produce the final outputs for channels A and B. Due to this integrated phasing technique, the digital output of channel A is in quadrature with that of channel B (90 degrees out of phase).

Definitions

Count (N): The number of bar and window pairs or counts per revolution (CPR) of the codewheel.

1 cycle (C): 360 electrical degrees (°e), 1 bar and window pair.

1 Shaft Rotation: 360 mechanical degrees, N cycles.

Pulse Width (P): The number of electrical degrees that an output is high during 1 cycle. This value is nominally 180°e or 1/2 cycle.

Pulse Width Error (ΔP): The deviation, in electrical degrees of the pulse width from its ideal value of 180°e.

State Width (S): The number of electrical degrees between a transition in the output of channel A and the neighboring transition in the output of channel B. There are 4 states per cycle, each nominally 90°e.

State Width Error (ΔS): The deviation, in electrical degrees, of each state width from its ideal value of 90°e.

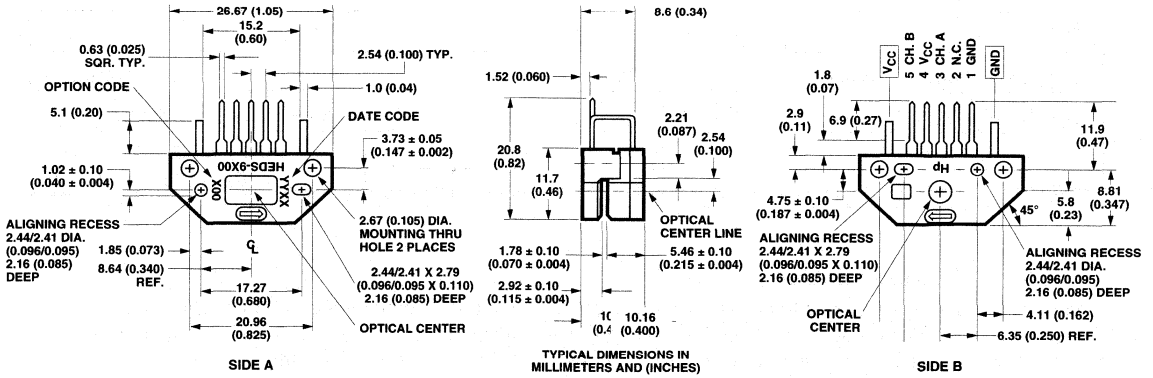
Phase (ϕ): The number of electrical degrees between the center of the high state of channel A and the center of the high state of channel B. This value is nominally 90°e for quadrature output.

Phase Error ($\Delta\phi$): The deviation of the phase from its ideal value of 90°e.

Direction of Rotation: When the codewheel rotates in the direction of the arrow on top of the module, channel A will lead channel B. If the codewheel rotates in the opposite direction, channel B will lead channel A.

Optical Radius (R_{op}): The distance from the codewheel's center of rotation to the optical center (O.C.) of the encoder module.

Package Dimensions



Absolute Maximum Ratings

Storage Temperature, T_S ..... -40°C to 100°C
Operating Temperature, T_A ..... -40°C to 100°C
Supply Voltage, V_{CC} ..... -0.5 V to 7 V
Output Voltage, V_O ..... -0.5 V to V_{CC}
Output Current per Channel, I_{out} ..... -1.0 mA to 5 mA

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Temperature	T_A	-40		100	°C	
Supply Voltage	V_{CC}	4.5	5.0	5.5	Volts	Ripple < 100 mV_{p-p}
Load Capacitance	C_L			100	pF	3.3 kΩ pull-up resistor
Count Frequency	f			100	kHz	Velocity (rpm) x N/60
Shaft Axial Play				± 0.125 ± 0.005	mm in.	

Note: The module performance is guaranteed to 100 kHz but can operate at higher frequencies. For frequencies above 100 kHz it is recommended that the load capacitance not exceed 25 pF and the pull up resistance not exceed 3.3 kΩ. For typical module performance above 100 kHz please see derating curves.

Electrical Characteristics

Electrical Characteristics over Recommended Operating Range, typical at 25°C.

Parameter	Symbol	Min.	Typical	Max.	Units	Notes
Supply Current	I_{CC}	30	57	85	mA	
High Level Output Voltage	V_{OH}	2.4			Volts	I_{OH} = -200 µA max.
Low Level Output Voltage	V_{OL}			0.4	Volts	I_{OL} = 3.86 mA
Rise Time	t_r		180		ns	C_L = 25 pF R_L = 3.3 kΩ pull-up
Fall Time	t_f		40		ns	

Encoding Characteristics

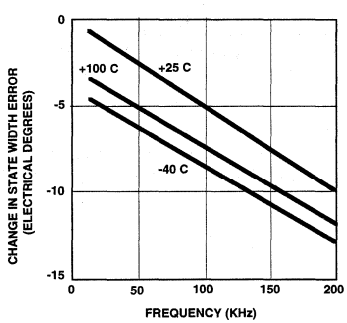
Encoding Characteristics over Recommended Operating Range and Recommended Mounting Tolerances. These Characteristics do not include codewheel/codestrip contribution. The Typical Values are averages over the full rotation of the codewheel. For operation above 100 kHz, see frequency derating curves.

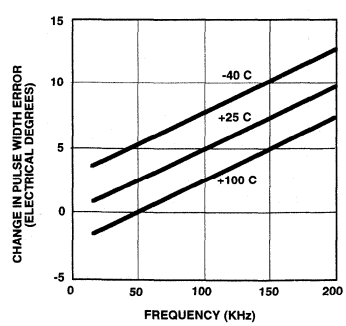
Description	Symbol	Typical	Maximum	Units
Pulse Width Error	ΔP	5	45	°e
Logic State Width Error	ΔS	3	45	°e
Phase Error	Δϕ	2	15	°e

Note: Module mounted on tolerance circle of ± 0.13 mm (± 0.005 in.) radius referenced from module Side A aligning recess centers. 3.3 kΩ pull-up resistors used on all encoder module outputs.

Frequency Derating Curves

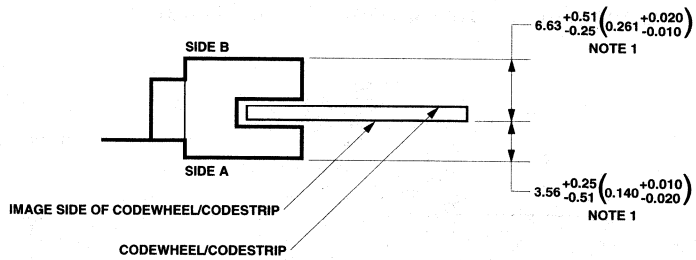
Typical performance over extended operating range. These curves were derived using a 25 pF load with a 3.3 k pull-up resistor. Greater load capacitances will cause more error than shown in these graphs.





Gap Setting for Rotary and Linear Modules

Gap is the distance between the image side of the codewheel and the detector surface of the module. This gap dimension must always be met and codewheel warp and shaft end play must stay within this range. This dimension is shown in Figure 1.



NOTES: 1. THESE DIMENSIONS INCLUDE CODEWHEEL/CODESTRIP WARP AND SHAFT END PLAY.
2. DIMENSIONS IN MILLIMETERS AND (INCHES).

Figure 1. Module Gap Setting.

Mounting Considerations for Rotary Modules

Figure 2 shows a mounting tolerance *requirement* for proper operation of the high resolution rotary encoder modules. The Aligning Recess Centers must be located within a tolerance circle of 0.13 mm (0.005 in.) radius from the nominal locations. This tolerance must be maintained whether the module is mounted with side A as the mounting plane using aligning pins (see Figure 3), or mounted with Side B as the mounting plane using an alignment tool.

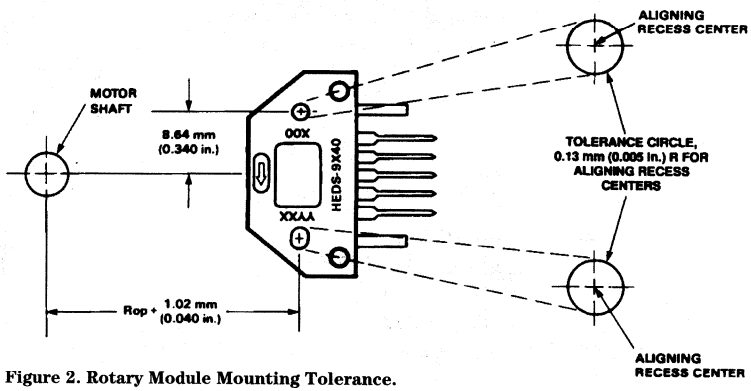
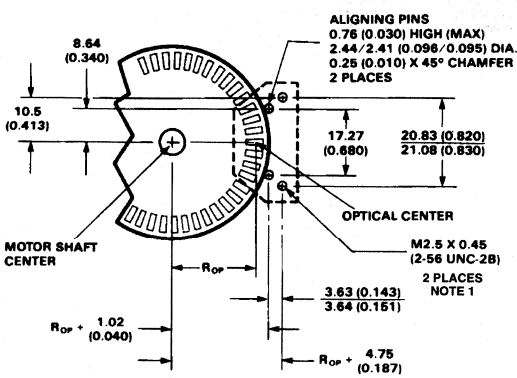


Figure 2. Rotary Module Mounting Tolerance.

Mounting with Aligning Pins

The high resolution rotary encoder modules can be mounted using aligning pins on the motor base. (HP does not provide aligning pins.) For this configuration, Side A *must* be used as the mounting plane. The Aligning Recess Centers must be located within the 0.13 mm (0.005 in.) R Tolerance Circle as explained above. Figure 3 shows the necessary dimensions.



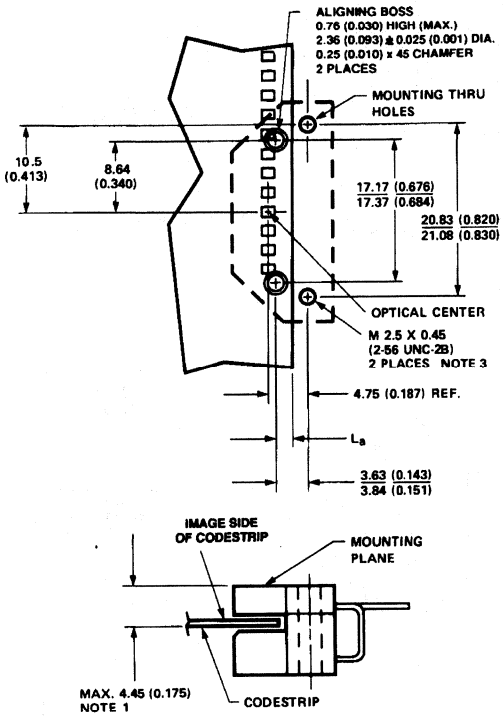
NOTE 1: RECOMMENDED MOUNTING SCREW TORQUE IS 4 KG-CM (3.5 IN-LBS).

Figure 3. Mounting Plane Side A.

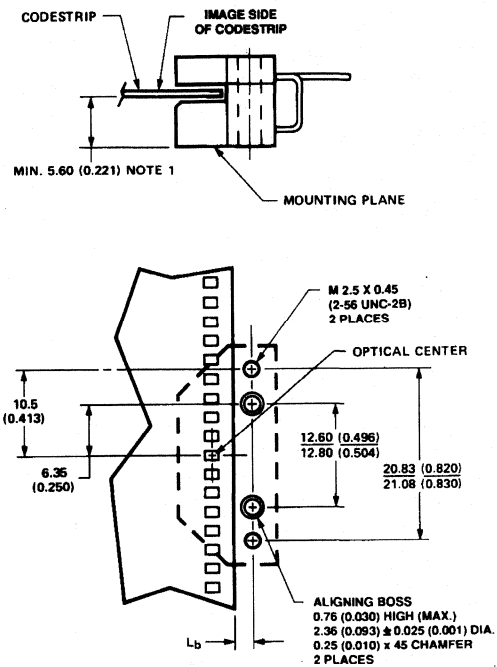
Mounting with HP Alignment Tools

HP offers alignment tools for mounting HP encoder modules in conjunction with HP codewheels, using side B as the mounting plane. Please refer to the HP codewheel data sheet for more information.

Mounting Considerations for Linear Modules



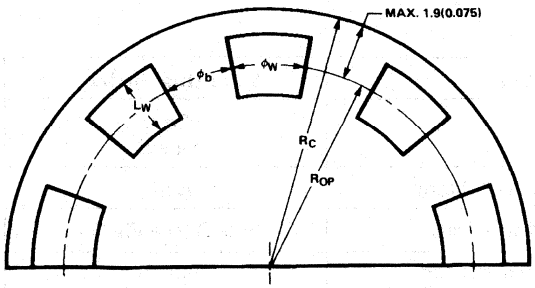
Mounting Plane Side A



Mounting Plane Side B

NOTES:
1. THESE DIMENSIONS INCLUDE CODESTRIP WARP.
2. REFERENCE DEFINITIONS OF L_a AND L_b ON THE FOLLOWING PAGE.
3. MAXIMUM RECOMMENDED MOUNTING SCREW TORQUE IS 4 kg-cm (3.5 in-lbs).

Recommended Codewheel Characteristics

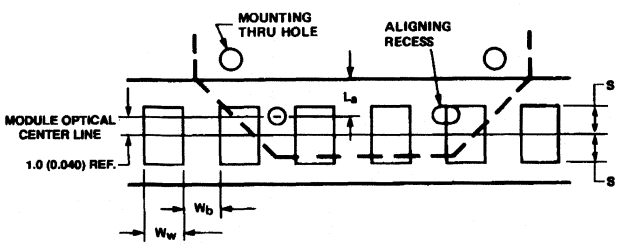


Parameter	Symbol	Minimum	Maximum	Units	Notes
Window/Bar Ratio	ϕ_w/ϕ_b	0.7	1.4		
Window Length	L_w	1.8 (0.07)		mm (inch)	
Absolute Maximum Codewheel Radius	R_c		R_{op} 1.9 (0.075) +	mm (inch)	Includes eccentricity errors

Recommended Codestrip Characteristics and Alignment

Codestrip design must take into consideration mounting as referenced to either side A *or* side B (see Figure 4).

Mounting as Referenced to Side A



Mounting as Referenced to Side B

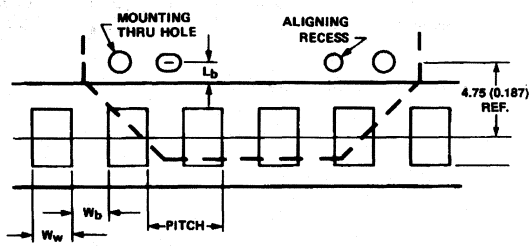


Figure 4. Codestrip Design

STATIC CHARGE WARNING: LARGE STATIC CHARGE ON CODESTRIP MAY HARM MODULE. PREVENT ACCUMULATION OF CHARGE.

Parameter	Symbol	Mounting Ref. Side A	Mounting Ref. Side B	Units
Window/Bar Ratio	W_w/W_b	0.7 min., 1.4 max.	0.7 min., 1.4 max.	
Window Distance	L	$L_a \leq 0.51$ (0.020)	$L_b \geq 3.23$ (0.127)	mm (inch)
Window Edge to Module Opt Center Line	S	0.90 (0.035) min.	0.90 (0.035) min.	mm (inch)
Parallelism Module to Codestrip	α	1.3 max.	1.3 max.	deg.

Note: All parameters and equations must be satisfied over the full length of codestrip travel including maximum codestrip runout.

Connectors

Manufacturer	Part Number	Mounting Surface
AMP	103686-4 640442-5	Both Side B
DuPont	65039-032 with 4825X-000 term.	Both
HP	HEDS-8902 with 4-wire leads	Side B (see Fig. 7)
Molex	2695 series with 2759 series term.	Side B

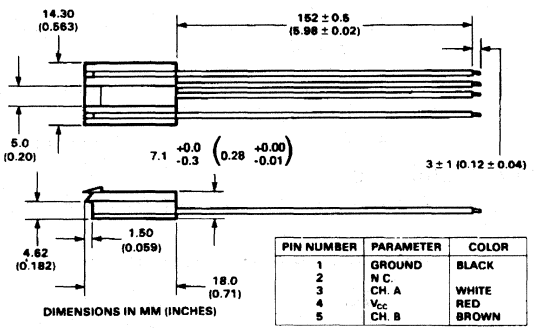


Figure 7. HEDS-8902 Connector.

Ordering Information

Two Channel Encoder Modules with a 23.36 mm Optical Radius

HEDS-9000 Option □ 0 0 *

Resolution (Cycles/Rev)
T - 2000 CPR
U - 2048 CPR

Two Channel Encoder Modules with an 11.00 mm Optical Radius

HEDS-9100 Option □ 0 0 *

Resolution (Cycles/Rev)
B - 1000 CPR
J - 1024 CPR

Two Channel Linear Encoder Module

HEDS-9200 Option □□□

Resolution (Cycles/Rev)
300 - 300 LPI
360 - 360 LPI

Note: For lower resolutions, please refer to HEDS-9000/9100 and HEDS-9200 data sheets for detailed information.

*Codewheel Information

For information on matching codewheels and accessories for use with HP rotary encoder modules, please refer to the HP Codewheel Data sheet HEDS-5120/6100, HEDG-5120/6120, HEDM-5120/6120

HEWLETT® PACKARD

Encoder Line Drivers

Technical Data

HEDL-550X/554X
HEDL-556X/557X
HEDL-560X/564X
HEDL-9000/9100/9200
HEDL-9040/9140
HEDL-9060/9160/9260
HEDL-9061/9161

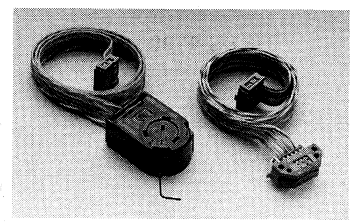
Features

- **Available on Both Encoder Modules (HEDS-9000 Series) and Encoder Kit Housings (HEDS-5500 Series)**
- **Complementary Outputs**
- **Industry Standard Line Driver IC**
- **Single 5 V Supply**
- **Onboard Bypass Capacitor**
- **70°C and 100°C Versions Available**

Description

Line Drivers are available for the HEDS-55XX/56XX series and the HEDS-9000/9100/9200/9040/9140 series encoders. The line driver offers enhanced performance when the encoder is used in noisy environments, or when it is required to drive long distances.

The 70°C version utilizes an industry standard line driver IC (26LS31) which provides complementary outputs for each encoder channel. The 100°C version utilizes an industry standard line driver IC, 26C31, which provides complementary outputs for each encoder channel. Thus, the output of the line driver encoder is A, $\overline{A}$, B, $\overline{B}$ and I/$\overline{I}$ for three channel versions. Suggested line receivers are 26LS32 and 26LS33.



For additional information, please refer to:
HEDS-5500/5540/5600/5640 data sheet,
HEDS-90X0/91X0/92X0 data sheets,
HEDS-9000 series extended resolution data sheet, and
26LS31 data sheet.

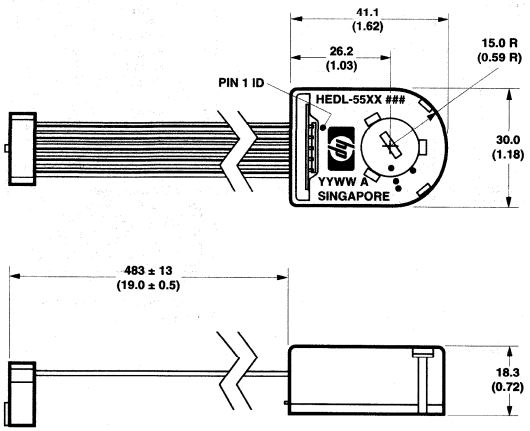
Device Characteristics

Parameter	Characteristic	Notes
Termination	10 conductor ribbon cable with 10 position IDC Berg connector	See pinout
Electrical Outputs	Complementary outputs: A, $\overline{A}$, B, $\overline{B}$, I, $\overline{I}$	I and $\overline{I}$ available only on three channel encoders
Line Driver Components	26LS31 line driver IC, decoupling capacitor on PC board.	
Operating Temperature Range	0°C to 70°C	70°C Series
	0°C to 100°C	100°C Series
Storage Temperature	-40°C to 70°C	70°C Series
	-40°C to 100°C	100°C Series

ESD WARNING: NORMAL HANDLING PRECAUTIONS SHOULD BE TAKEN TO AVOID STATIC DISCHARGE.

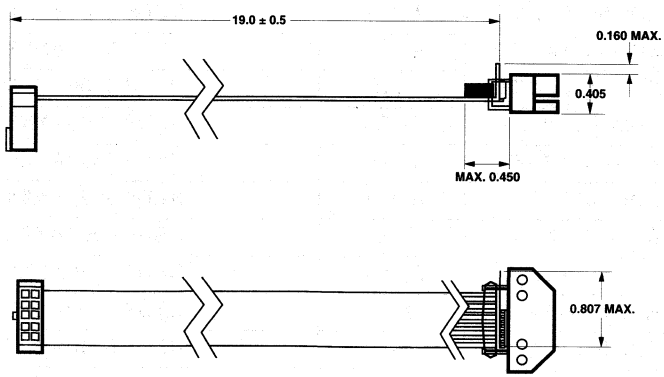
Line Driver Package Dimensions

For Detailed Dimensions on encoder packages, please refer to the respective data sheets.



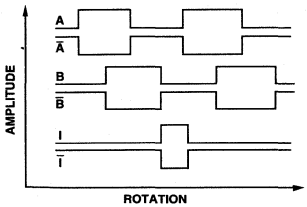
HEDL-550X/554X/560X/564X
HEDL-556X/557X

NOTE: DIMENSIONS IN MILLIMETERS (INCHES)

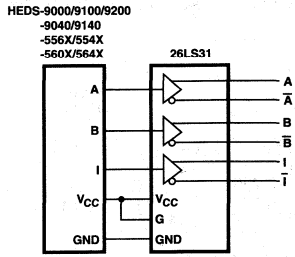


HEDL-9000/9100/9200/9040/9140
HEDL-9060/9160/9260/9061/9161

Waveforms



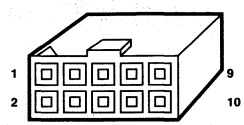
Block Diagram



Pinouts

10-PIN CONNECTOR

NO.	COLOR	PARAMETER
1	BROWN	NC
2	RED	V_{CC} (+ 5 V)
3	ORANGE	GND
4	YELLOW	NC
5	GREEN	$\overline{A}$
6	BLUE	A
7	VIOLET	$\overline{B}$
8	GREY	B
9	WHITE	$\overline{I}$ ($\overline{INDEX}$)



10 POSITION IDC CONNECTOR
CENTER POLARIZED.

Note: I/$\overline{I}$ only available on three channel encoders.

Line Driver Base Parts Available:

70°C Line Driver Base Part	100°C Line Driver Base Part	Channels	Refer to the following encoder data sheet for additional information and option codes (XXX = resolution and/or shaft size)
HEDL-5500#XXX	HEDL-5568#XXX	A, B	HEDS-5500#XXX
HEDL-5505#XXX	HEDL-5569#XXX	A, B	HEDS-5505#XXX
HEDL-5540#XXX	HEDL-5570#XXX	A, B, I	HEDS-5540#XXX
HEDL-5545#XXX	HEDL-5571#XXX	A, B, I	HEDS-5545#XXX
HEDL-5600#XXX	HEDL-5572#XXX	A, B	HEDS-5600#XXX
HEDL-5605#XXX	HEDL-5573#XXX	A, B	HEDS-5605#XXX
HEDL-5640#XXX	HEDL-5574#XXX	A, B, I	HEDS-5640#XXX
HEDL-5645#XXX	HEDL-5575#XXX	A, B, I	HEDS-5645#XXX
HEDL-9000#XXX	HEDL-9060#XXX	A, B	HEDS-9000#XXX
HEDL-9040#XXX	HEDL-9061#XXX	A, B, I	HEDS-9040#XXX
HEDL-9100#XXX	HEDL-9160#XXX	A, B	HEDS-9100#XXX
HEDL-9140#XXX	HEDL-9161#XXX	A, B, I	HEDS-9140#XXX
HEDL-9200#XXX	HEDL-9260#XXX	A, B	HEDS-9200#XXX

Ordering Information:

For option code selection, refer to the data sheet for the corresponding "HEDS" part number (see right column).

HEWLETT® PACKARD

High Temperature 125°C Two Channel Optical Incremental Encoder Modules

Technical Data

HEDT-9000
HEDT-9100

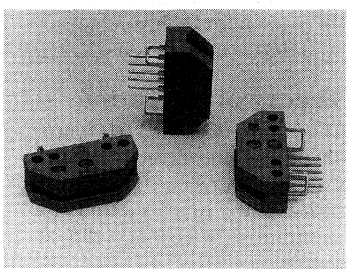
MOTION SENSING AND CONTROL

Features

- **High Performance**
- **High Resolution**
- **Low Cost**
- **Easy to Mount**
- **No Signal Adjustment Required**
- **Insensitive to Radial and Axial Play**
- **Small Size**
- **-40°C to 125°C Operating Temperature**
- **Two Channel Quadrature Output**
- **TTL Compatible**
- **Single 5 V Supply**

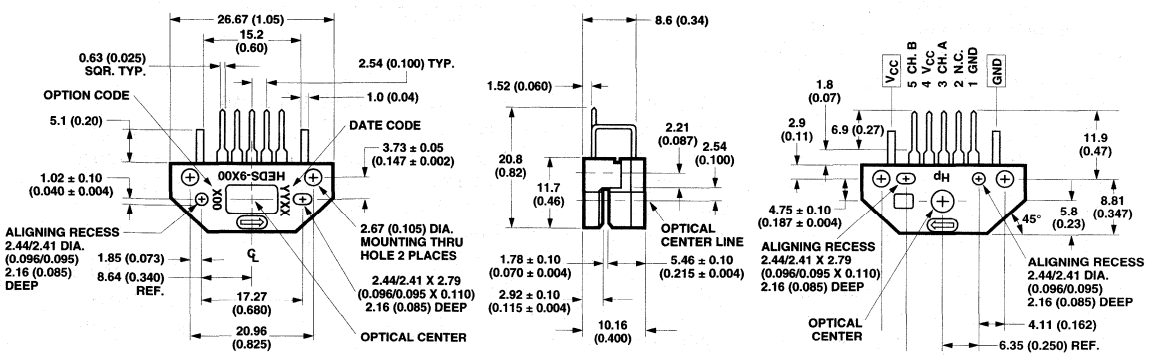
Description

The HEDT-9000 and the HEDT-9100 series are high performance, low cost, optical incremental encoder modules that operate to 125°C. When used with a codewheel, these modules detect rotary position. The modules consist of a lensed (LED) source and a detector IC enclosed in a small C-shaped plastic package. Due to a highly collimated light source and unique photodetector array, these modules are extremely tolerant to mounting misalignment.



The two channel digital outputs and the single 5 V supply input are accessed through five 0.025 inch square pins located on 0.1 inch centers.

Package Dimensions



ESD WARNING: NORMAL HANDLING PRECAUTIONS SHOULD BE TAKEN TO AVOID STATIC DISCHARGE.

Standard resolutions for the HEDT-9000 are 500 CPR and 1000 CPR for use with a HEDS-6100 codewheel or equivalent. For the HEDT-9100, standard resolutions between 96 CPR and 512 CPR are available for use with a HEDS-5120 codewheel or equivalent.

Applications

The HEDT-9000 and 9100 provide sophisticated motion detection at a low cost, at temperatures to 125°C, making them ideal for high volume automotive applications.

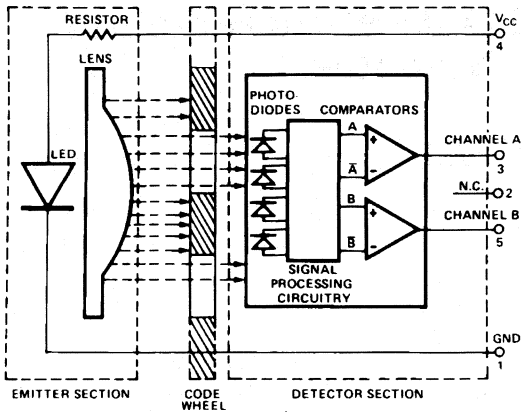
Theory of Operation

The HEDT-9000 and 9100 are C-shaped emitter/detector modules. Coupled with a codewheel, they translate the rotary motion of a shaft into a two-channel digital output.

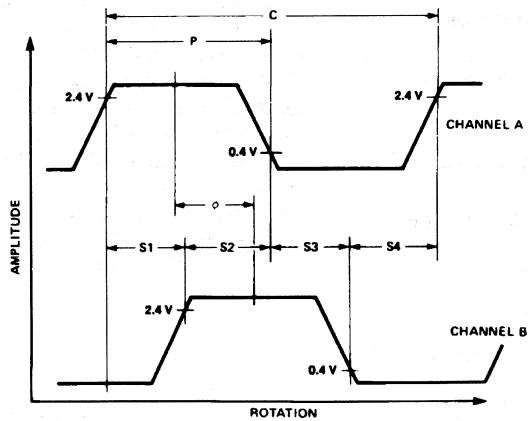
As seen in the block diagram, each module contains a single Light Emitting Diode (LED) as its light source. The light is collimated into a parallel beam by means of a single polyetherimide lens located directly over the LED. Opposite the emitter is the integrated detector circuit. This IC consists of multiple sets of photodetectors and the signal processing circuitry necessary to product the digital waveforms.

The codewheel rotates between the emitter and detector, causing the light beam to be interrupted by the pattern of spaces and bars on the codewheel. The photodiodes which detect these interruptions are arranged in a pattern that corresponds to the radius and design of the code-wheel. These detectors are also spaced such that a light period on one pair of detectors corresponds to a dark period on the adjacent pair of detectors. The photodiode outputs are then fed through the signal processing circuitry resulting in A, $\overline{A}$, B, and $\overline{B}$. Two comparators receive these signals and produce the final outputs for channels A and B. Due to this integrated phasing technique, the digital output of channel A is in quadrature with that of channel B (90 degrees out of phase).

Block Diagram



Output Waveforms



Definitions

Count (N): The number of bar and window pairs or counts per revolution (CPR) of the codewheel.

1 Shaft Rotation = 360 mechanical degrees,
= N cycles.

1 cycle (C) = 360 electrical degrees (°e),
= 1 bar and window pair.

Pulse Width (P): The number of electrical degrees that an output is high during 1 cycle. This value is nominally 180°e or 1/2 cycle.

Pulse Width Error (ΔP): The deviation, in electrical degrees of the pulse width from its ideal value of 180°e.

State Width (S): The number of electrical degrees between a transition in the output of channel A and the neighboring transition in the output of channel B. There are 4 states per cycle, each nominally 90°e.

State Width Error (ΔS): The deviation, in electrical degrees, of each state width from its ideal value of 90°e.

Absolute Maximum Ratings

Storage Temperature, T_S ..... -40°C to 125°C
Operating Temperature, T_A ..... -40°C to 125°C
Supply Voltage, V_{CC} ..... -0.5 V to 7 V
Output Voltage, V_O ..... -0.5 V to V_{CC}
Output Current per Channel, I_{out} ..... -1.0 mA to 5 mA

Phase (ϕ): The number of electrical degrees between the center of the high state of channel A and the center of the high state of channel B. This value is nominally 90°e for quadrature output.

Phase Error (Δϕ): The deviation of the phase from its ideal value of 90°e.

Direction of Rotation: When the codewheel rotates in the direction of the arrow on top of the module, channel A will lead channel B. If the codewheel rotates in the opposite direction, channel B will lead channel A.

Optical Radius (R_{op}): The distance from the codewheel's center of rotation to the optical center (O.C.) of the encoder module.

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Temperature	T	-40		125	°C	
Supply Voltage	V_{CC}	4.5		5.5	Volts	Ripple < 100 mV_{p-p}
Load Capacitance	C_L			100	pF	3.3 kΩ pull-up resistor
Count Frequency	f			100	kHz	$\frac{\text{Velocity (rpm) x N}}{60}$

Note: The module performance is guaranteed to 100 kHz but can operate at higher frequencies.

Encoding Characteristics

Encoding Characteristics over Recommended Operating Range and Recommended Mounting Tolerances. These Characteristics do not include codewheel/codestrip contributions.

Description	Sym.	Typ.	Case 1 Max.	Case 2 Max.	Units	Notes
Pulse Width Error	ΔP	7	35	45	°e	
Logic State Width Error	ΔS	5	35	45	°e	
Phase Error	Δϕ	2	15	20	°e	

Case 1: Module mounted on tolerance circle of ± 0.13 mm (± 0.005 in.).
Case 2: HEDT-9000 mounted on tolerances of ± 0.50 mm (0.020").
HEDT-9100 mounted ontolerances of ± 0.38 mm (0.015").

Electrical Characteristics

Electrical Characteristics over Recommended Operating Range, typical at 25°C.

Parameter	Symbol	Min.	Typical	Max.	Units	Notes
Supply Current	I_{CC}		17	40	mA	
High Level Output Voltage	V_{OH}	2.4			Volts	I_{OH} = -40 µA max.
Low Level Output Voltage	V_{OL}			0.4	Volts	I_{OL} = 3.2 mA
Rise Time	t_r		200		ns	C_L = 25 pF R_L = 11 kΩ pull-up
Fall Time	t_f		50		ns	

Recommended Codewheel Characteristics

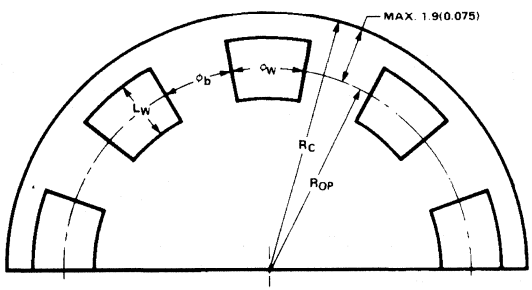


Figure 1. Codestrip Design.

Codewheel Options

HEDS Series	CPR (N)	Option	Optical Radius mm (in.)
5120	96	K	11.00 (0.433)
5120	100	C	11.00 (0.433)
5120	192	D	11.00 (0.433)
5120	200	E	11.00 (0.433)
5120	256	F	11.00 (0.433)
5120	360	G	11.00 (0.433)
5120	400	H	11.00 (0.433)
5120	500	A	11.00 (0.433)
5120	512	I	11.00 (0.433)
6100	500	A	23.36 (0.920)
6100	1000	B	23.36 (0.920)

Parameter	Symbol	Minimum	Maximum	Units	Notes
Window/Bar Ratio	ϕ_w/ϕ_b	0.7	1.4		
Window Length	L	1.8 (0.07)	2.3 (0.09)	mm (inch)	
Absolute Maximum Codewheel Radius	R_C		R_{OP} + 1.9 (0.075)	mm (inch)	Includes eccentricity errors

Mounting Considerations

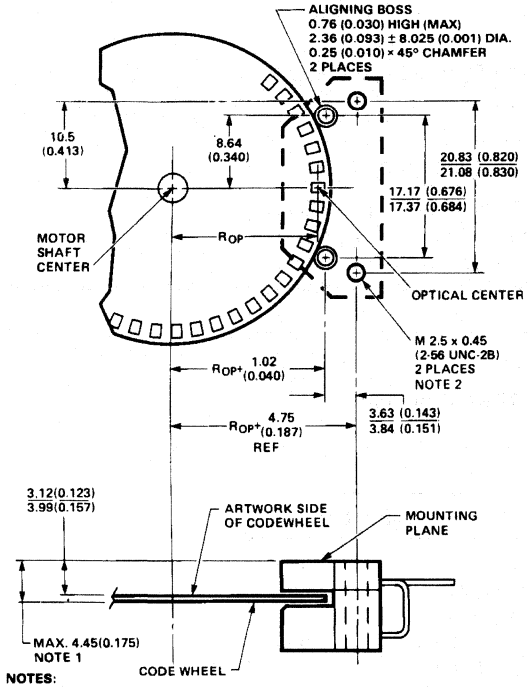


Figure 2. Mounting Plane Side A.

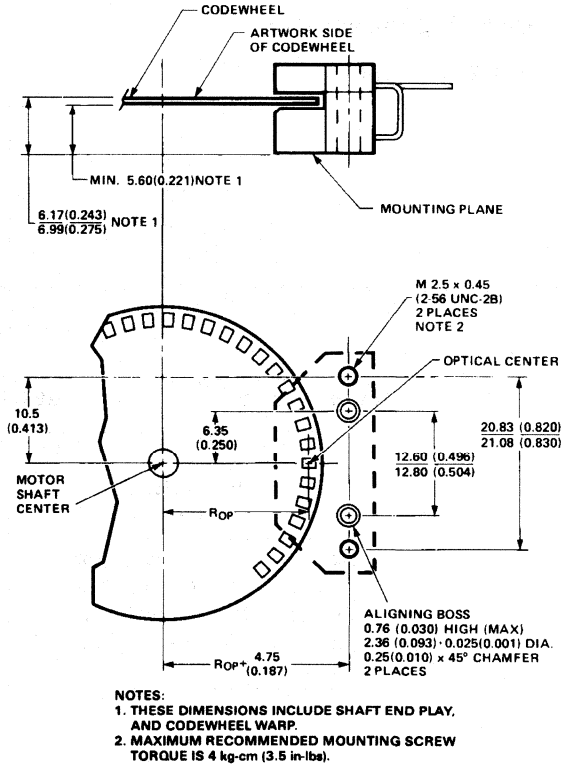


Figure 3. Mounting Plane Side B.

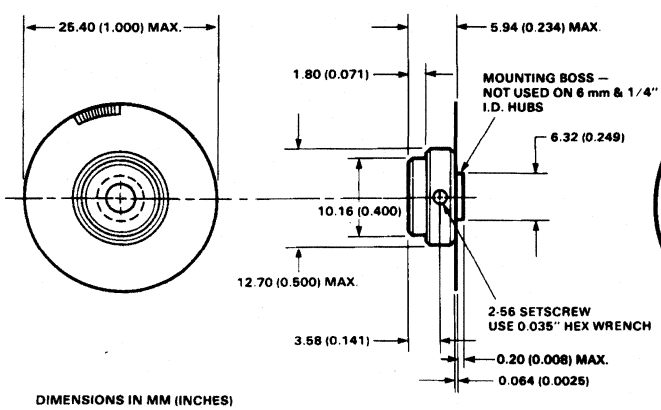


Figure 4. HEDS-5120 Codewheel.

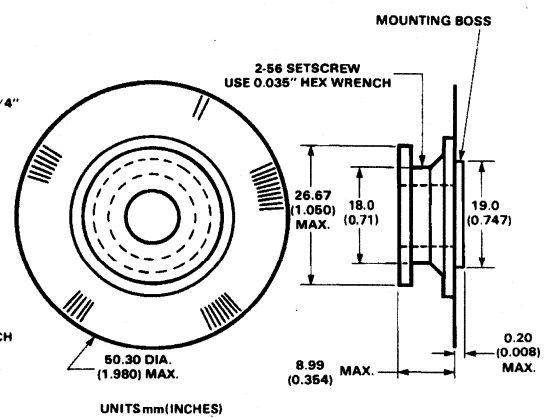


Figure 5. HEDS-6100 Codewheel.

Ordering Information

HEDT-9000 Option □ 0 0 **HEDS-6100 Option** □ □ □

Resolution (Cycles/Rev)
A - 500 CPR
B - 1000 CPR

Shaft Diameter	
05 - 3/16 in.	10 - 5/8 in.
06 - 1/4 in.	11 - 4 mm
07 - 5/16 in.	12 - 6 mm
08 - 3/8 in.	13 - 8 mm
09 - 1/2 in.	

HEDT-9100 Option □ 0 0 **HEDS-5120 Option** □ □ □

Resolution (Cycles/Rev)	
K - 96 CPR	G - 360 CPR
C - 100 CPR	H - 400 CPR
D - 192 CPR	A - 500 CPR
E - 200 CPR	I - 512 CPR
F - 256 CPR	

Shaft Diameter	
01 - 2 mm	11 - 4 mm
02 - 3 mm	14 - 5 mm
03 - 1/8 in.	12 - 6 mm
04 - 5/32 in.	13 - 8 mm
05 - 3/16 in.	
06 - 1/4 in.	

High Temperature 140°C Three Channel Optical Incremental Encoder Modules

Technical Data

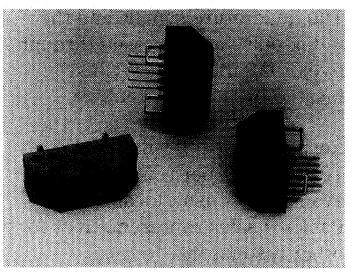
HEDT-9040
HEDT-9140

Features

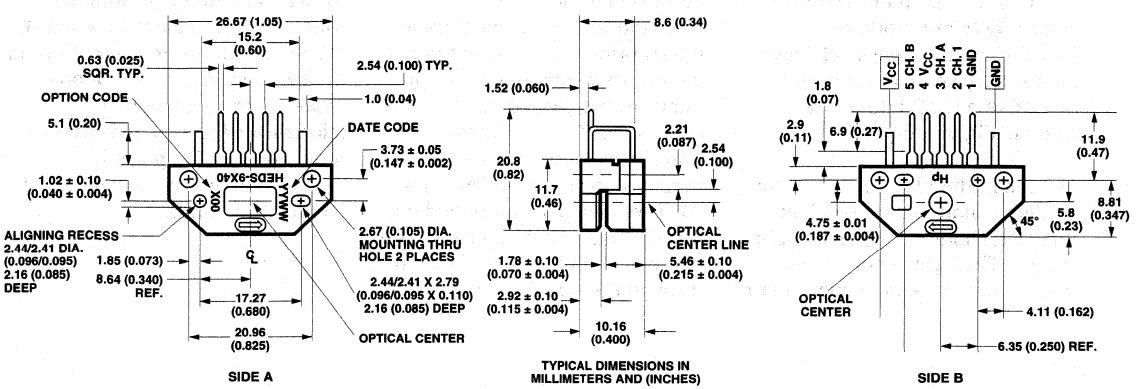
- **-40°C to 140°C Operating Temperature**
- **Two Channel Quadrature Output with Index Pulse**
- **Suitable for Automotive Applications**
- **Resolution up to 1024 Counts per Revolution**
- **Low Cost**
- **Easy to Mount**
- **No Signal Adjustment Required**
- **Small Size**

Description

The HEDT-9040 and HEDT-9140 are high temperature three channel optical incremental encoder modules. When used with a codewheel, these low cost modules detect rotary position. Each module consists of a lensed LED source and a detector IC enclosed in a small plastic package. Due to a highly collimated light source and a unique photodetector array, these modules provide the same high performance found in the HEDS-9040/9140 three channel encoders.



Package Dimensions



ESD WARNING: NORMAL HANDLING PRECAUTIONS SHOULD BE TAKEN TO AVOID STATIC DISCHARGE.

The HEDT-9040 and 9140 have two channel quadrature outputs plus a third channel index output. This index output is a 90 electrical degree high true index pulse.

The HEDT-9040 is designed for codewheels which have an optical radius of 23.36 mm (0.920 in.). The HEDT-9140 is designed for codewheels which have an optical radius of 11.00 mm (0.433 in.).

The quadrature signals and the index pulse are accessed through five 0.025 inch square pins located on 0.1 inch centers.

Resolutions between 360 and 1024 counts per revolution are available. Consult local Hewlett-Packard sales representatives for other resolutions.

Applications

The HEDT-9040 and 9140 provide high temperature motion control detection at a low cost, making them suitable for automotive and industrial applications.

Theory of Operation

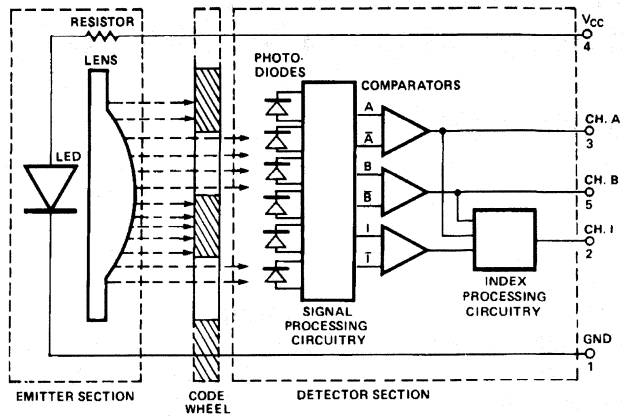
The HEDT-9040 and 9104 are emitter/detector modules. Coupled with a codewheel, these modules translate the rotary motion of a shaft into a three-channel digital output.

As seen in the block diagram, the module contains a single Light Emitting Diode (LED) as its light source. The light is collimated into a parallel beam by means of a single lens located directly over the LED. Opposite the emitter is the integrated detector circuit. This IC consists of multiple sets of photodetectors and the signal processing circuitry necessary to produce the digital waveforms.

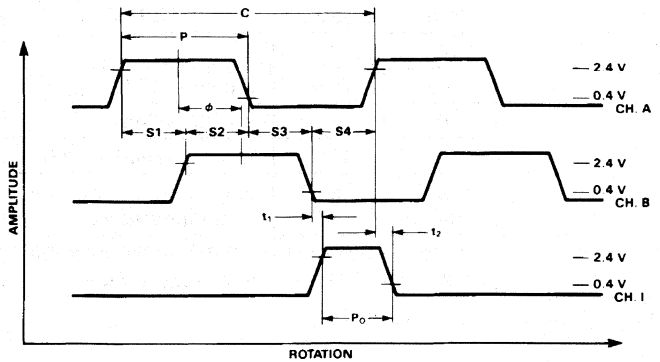
The codewheel rotates between the emitter and detector, causing the light beam to be interrupted by the pattern of spaces and bars on the codewheel. The photodiodes which detect these interruptions are arranged in a pattern that corresponds to the radius and design of the codewheel. These detectors are also spaced such that a light period on one pair of detectors corresponds to a dark period on the adjacent pair of detectors. The photodiode outputs are then fed through the signal processing circuitry resulting in A, $\overline{A}$, B, $\overline{B}$, I and $\overline{I}$. Comparators receive these signals and produce the final outputs for channels A and B. Due to this integrated phasing technique, the digital output of channel A is in quadrature with that of channel B (90 degrees out of phase).

The output of the comparator for I and $\overline{I}$ is sent to the index processing circuitry along with the outputs of channels A and B. The final output of channel I is an index pulse Po which is a one state width (nominally 90 electrical degrees), high true index pulse. This pulse is coincident with the low states of channels A and B.

Block Diagram



Output Waveforms



Definitions

Count (N): The number of bar and window pairs or counts per revolution (CPR) of the codewheel.

One Cycle (C): 360 electrical degrees (°e), 1 bar and window pair.

One Shaft Rotation: 360 mechanical degrees, N cycles.

Position Error ($\Delta\Theta$): The normalized angular difference between the actual shaft position and the position indicated by the encoder cycle count.

Cycle Error (ΔC): An indication of cycle uniformity. The difference between an observed shaft angle which gives rise to one electrical cycle, and the nominal angular increment of 1/N of a revolution .

Pulse Width (P): The number of electrical degrees that an output is high during 1 cycle. This value is nominally 180°e or 1/2 cycle.

Pulse Width Error (ΔP): The deviation, in electrical degrees, of the pulse width from its ideal value of 180°e.

State Width (S): The number of electrical degrees between a transition in the output of channel A and the neighboring transition in the output of channel B. There are 4 states per cycle, each nominally 90°e.

State Width Error (ΔS): The deviation, in electrical degrees, of each state width from its ideal value of 90°e.

Phase (ϕ): The number of electrical degrees between the center of the high state of channel A and the center of the high state of channel B. This value is nominally 90°e for quadrature output.

Phase Error ($\Delta\phi$): The deviation of the phase from its ideal value of 90°e.

Direction of Rotation: When the codewheel rotates in the direction of the arrow on top of the module, channel A will load channel B. If the codewheel rotates in the opposite direction, channel B will lead channel A.

Optical Radius (R_{OP}): The distance from the codewheel's center of rotation to the optical center (O.C.) of the encoder module.

Index Pulse Width (P_o): The number of electrical degrees that an index is high during one full shaft rotation. This value is nominally 90°e or 1/4 cycle.

Absolute Maximum Ratings

Storage Temperature, T_S	-40°C to 140°C
Operating Temperature, T_A	-40°C to 140°C
Supply Voltage, V_{CC}	-0.5 V to 7 V
Output Voltage, V_O	-0.5 V to V_{CC}
Output Current per Channel, I_{OUT}	-1.0 mA to 5 mA
Shaft Axial Play	± 0.25 mm (± 0.010 in.)
Shaft Eccentricity Plus Radial Play	0.1 mm (0 004 in.) TIR
Velocity	30,000 RPM[1]
Acceleration	250,000 rad/sec^2[1]

Note:
1. Absolute maximums for HEDS-5140 codewheel only.

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Temperature	T_A	-40		140	°C	
Supply Voltage	V_{CC}	4.5	5.0	5.5	Volts	Ripple < 100 mV_{p-p}
Load Capacitance	C_L			100	pF	2.7 kΩ pull-up
Count Frequency	f			50	kHz	Velocity (rpm) x N/60
Shaft Perpendicularity Plus Axial Play				± 0.25 (± 0.010)	mm (in.)	6.9 mm (0.27 in.) from mounting surface
Shaft Eccentricity Plus Radial Play				0.04 (0.0015)	mm (in.) TIR	6.9 mm (0.27 in.) from mounting surface

Note: The module performance is guaranteed to 50 kHz but can operate at higher frequencies.

Encoding Characteristics

Encoding Characteristics over Recommended Operating Range and Recommended Mounting Tolerances unless otherwise specified. Values are for the worst error over the full rotation of HEDS-514X and HEDS-6145 codewheels.

Parameter	Symbol	Min.	Typ.*	Max.	Units
Cycle Error	ΔC		5	10	°e
Pulse Width Error	ΔP		7	30	°e
Logic State Width Error	ΔS		5	30	°e
Phase Error	Δϕ		2	15	°e
Position Error	ΔΘ		10	40	min. of arc
Index Pulse Width	P_O	60	90	120	°e
CH. I rise after CH. B or CH. A fall	t_1	20	430	1490	ns
CH. I fall after CH. A or CH. B rise	t_2	40	250	620	ns

Note: Module mounted on tolerance circle of ± 0.13 mm (± 0.005 in.) radius referenced from module Side A aligning recess centers. 2.7 kΩ pull-up resistors used on all encoder module outputs.

Electrical Characteristics

Electrical Characteristics over Recommended Operating Range.

Parameter	Symbol	Min.	Typ.*	Max.	Units	Notes
Supply Current	I_{CC}	30	57	85	mA	
High Level Output Voltage	V_{OH}	2.4			V	I_{OH} = -100 μA min.
Low Level Output Voltage	V_{OL}			0.4	V	I_{OL} = 3.86 mA max.
Rise Time	t_r		90		ns	C_L = 25 pF
Fall Time	t_f		80		ns	R_L = 2.7 kΩ pull-up

*Typical values specified at V_{CC} = 5.0 V and 25°C.

Mechanical Characteristics

Part No.	Parameter	Dimension	Tolerance	Units
HEDS-5140 11.00 mm optical radius codewheel	Codewheel Available to Fit These Standard Shaft Diameters	2 3 4 5 6 8	+0.000 -0.015	mm
		5/32 1/8 3/16 1/4	+0.000 -0.0007	in.
	Moment of Inertia	0.6 (8.0 x 10^{-6})		g-cm^2 (oz-in-s^2)

Note: The tolerance requirements are on the mating shaft, not on the codewheel.

Electrical Interface

To insure reliable encoding performance, the HEDT-9040 and 9140 three channel encoder modules require 2.7 kΩ (± 10%) pull-up resistors on output pins 2, 3, and 5 (Channels I, A, and B) as shown in Figure 1. These pull-up resistors should be located in close proximity of the encoder module (within 4 feet). Each of the three encoder module outputs can drive a single TTL load in this configuration.

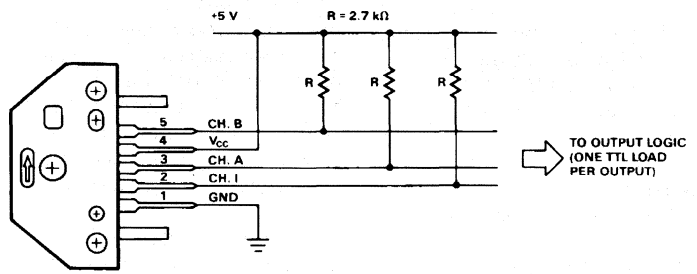


Figure 1. Pull-up Resistors on HEDT-9X40 Encoder Module Outputs.

Mounting Considerations

Figure 2 shows a mounting tolerance requirement for proper operation of the HEDT-9040 and HEDT-9140. The Aligning Recess Centers must be located within a tolerance circle of 0.13 mm (0.005 in.) radius from the nominal locations. This tolerance must be maintained whether the module is mounted with Side A as the mounting plane using aligning pins (see Figure 5), or mounted with Side B as the mounting plane using an alignment tool (see Figures 3 and 4).

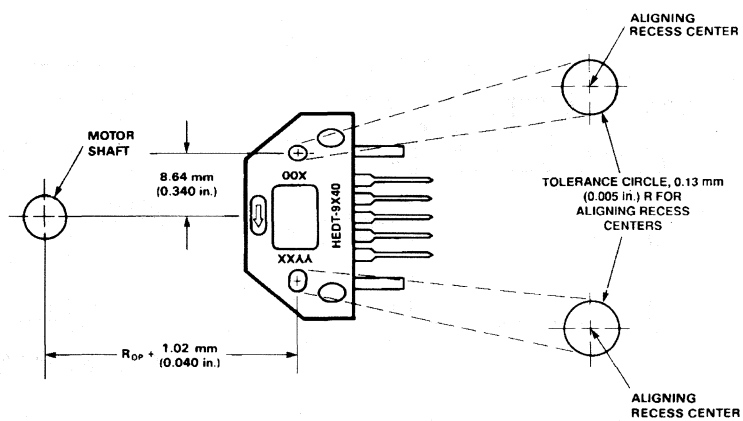


Figure 2. HEDT-9X40 Mounting Tolerance.

Mounting the HEDT-9140 with an Alignment Tool

The HEDS-8905 alignment tool is recommended for mounting the HEDT-9140 module with Side B as the mounting plane. This tool can only be used when the HEDT-9140 module is mounted with the HEDS-5140 (codewheel with hub). The HEDS-8905 tool fixes the module position using the codewheel hub as a reference. It will not work if Side A is used as the mounting plane.

The following assembly procedure uses the HEDS-8905 alignment tool to mount an HEDT-9140 module and an HEDS-5140 codewheel:

Instructions:

1. Place codewheel on shaft.

2. Set codewheel height: (a) place alignment tool on motor base (pins facing up) flush up against the motor shaft as shown in Figure 3. (b) Push codewheel down against alignment tool. The codewheel is now at the proper height. (c) Tighten codewheel setscrew and remove alignment tool.

Some motors have a boss around the shaft that extends above the mounting plane. In this case, the alignment tool cannot be used as a gage block to set the codewheel height as described in 2(a), (b), and (c). *If boss is above mounting plane:* Slide module onto motor base, adjusting height of codewheel so that it sits approximately in the middle of module slot. Lightly tighten setscrew. The codewheel height will be more precisely set in step 5.

3. Insert mounting screws through module and thread into the motor base. Do not tighten screws.

4. Slide alignment tool over codewheel hub and onto module as shown in Figure 4. The pins of the alignment tool should fit snugly inside the alignment recesses of the module.

If boss is above mounting plane: The pins of the tool may not mate properly because the codewheel is too high on the shaft. Loosen codewheel setscrew and lower codewheel slightly. Retighten setscrew lightly and attempt this step again.

5. While holding alignment tool in place, tighten screws down to secure module.

If boss is above mounting plane: Push codewheel up flush against alignment tool to set codewheel height. Tighten codewheel setscrew.

6. Remove alignment tool.

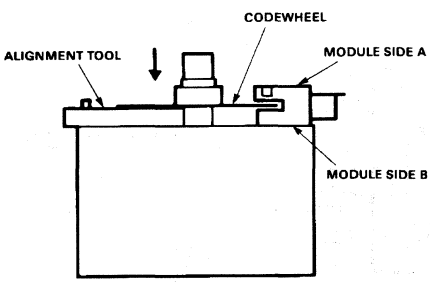


Figure 3. Alignment Tool is Used to Set Height of Codewheel.

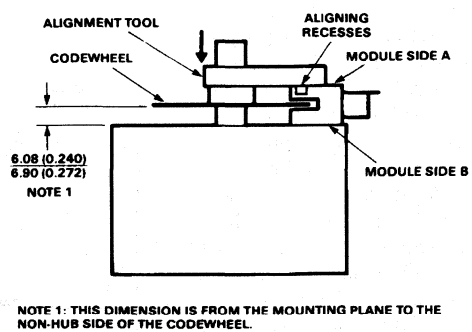
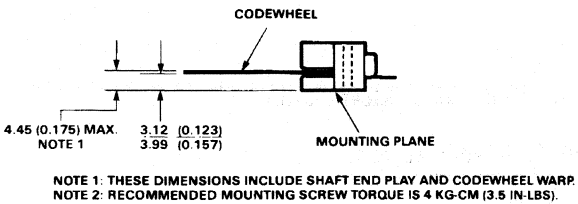


Figure 4. Alignment Tool is Placed over Shaft and onto Codewheel Hub. Alignment Tool Pins Mate with Aligning Recesses on Module.

Mounting with Aligning Pins
The HEDT-9040 and HEDT-9140 can also be mounted using aligning pins on the mounting surface. (Hewlett-Packard does not provide aligning pins.) For this configuration, Side A *must* be used as the mounting plane. The aligning recess centers must be located within the 0.13 mm (0.005 in.) Radius Tolerance Circle as explained in "Mounting Considerations." Figure 5 shows the necessary dimensions.



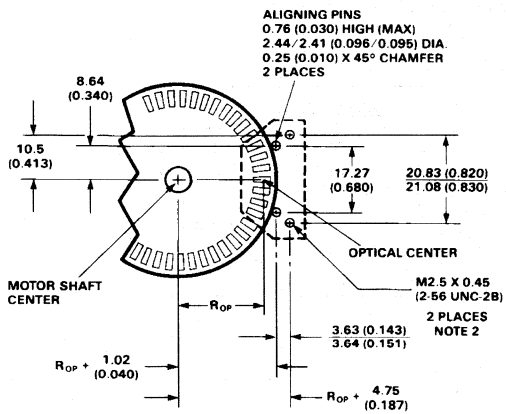


Figure 5. Mounting Plane Side A.

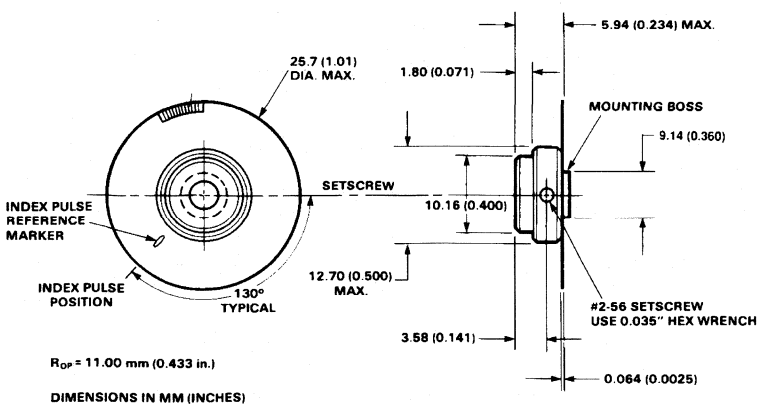
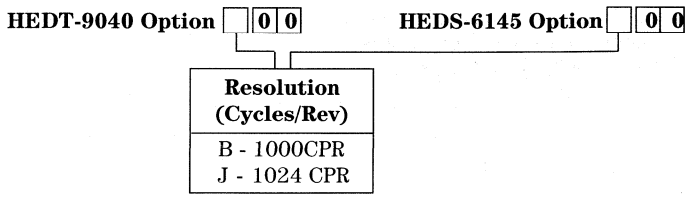


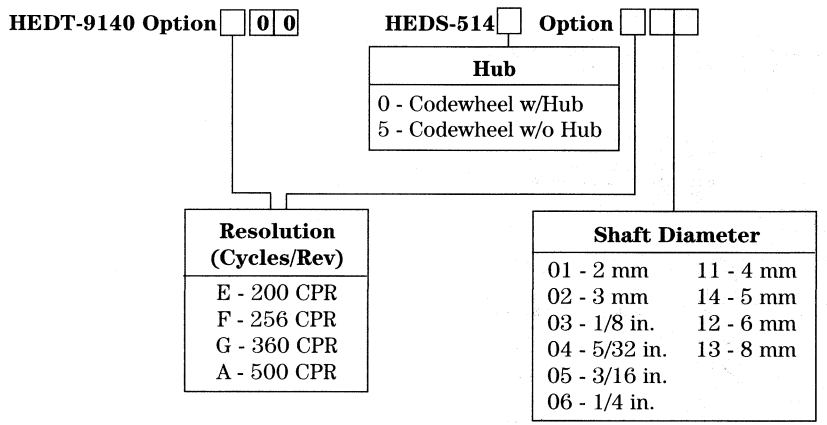
Figure 6. HEDS-5140 Codewheel Used with HEDT-9140.

Ordering Information

Three Channel Encoder Modules and Bare Codewheels, 23.36 mm Optical Radius



Three Channel Encoder Modules and Codewheels, 11.00 mm Optical Radius



Accessories

HEDS-8905
Alignment Tool for mounting the HEDT-9140.

Using Multiple Index Pulses

The third channel index (Channel I) is not limited to occurring just once per revolution. Index pulses may be placed arbitrarily over a full codewheel rotation. This is done by altering only the pattern of the codewheel with no modifications necessary to the HEDT-9X40 module. The only restriction is that, depending on the CPR of the codewheel, consecutive index pulses may have to be separated by at least 10 full cycles.

Multiple index pulses can provide more precise absolute position information. By strategically placing the index pulses, a unique index series can be created for a particular angular position. This leads to the idea of the "quasi-absolute" encoder in which only a partial turning of the codewheel is required to determine the absolute position.

A special codewheel is required to accomplish a multiple index pattern. The standard HEDS-5140, 5145, and 6145 codewheels have one index pulse per full revolution. Please consult a local HP sales representative for further information.

HEWLETT® PACKARD

Quick Assembly Two and Three Channel Optical Encoders

Technical Data

HEDM-550X/560X
HEDS-550X/554X
HEDS-560X/564X

Features

- **Two Channel Quadrature Output with Optional Index Pulse**
- **Quick and Easy Assembly**
- **No Signal Adjustment Required**
- **External Mounting Ears Available**
- **Low Cost**
- **Resolutions Up to 1024 Counts Per Revolution**
- **Small Size**
- **-40°C to 100°C Operating Temperature**
- **TTL Compatible**
- **Single 5 V Supply**

Description

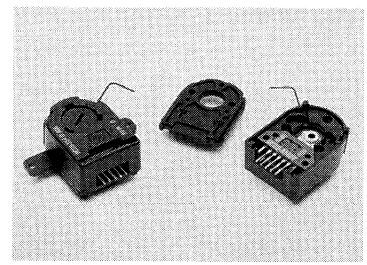
The HEDS-5500/5540, HEDS-5600/5640, and HEDM-5500/5600 are high performance, low cost, two and three channel optical incremental encoders. These encoders emphasize high reliability, high resolution, and easy assembly.

Each encoder contains a lensed LED source, an integrated circuit with detectors and output circuitry, and a codewheel which rotates between the emitter and detector IC. The outputs of the HEDS-5500/5600 and HEDM-5500/ 5600 are two square waves in quadrature. The HEDS-5540 and 5640 also have a third channel index output in addition to the two channel quadrature. This index output is a 90 electrical degree, high true index pulse which is generated once for each full rotation of the codewheel.

The HEDS series utilizes metal codewheels, while the HEDM series utilizes a film codewheel allowing for resolutions to 1024 CPR. The HEDM series is nont available with a third channel index.

These encoders may be quickly and easily mounted to a motor. For larger diameter motors, the HEDM-5600, and HEDS-5600/5640 feature external mounting ears.

The quadrature signals and the index pulse are accessed through



five 0.025 inch square pins located on 0.1 inch centers.

Standard resolutions between 96 and 1024 counts per revolution are presently available. Consult local Hewlett-Packard sales representatives for other resolutions.

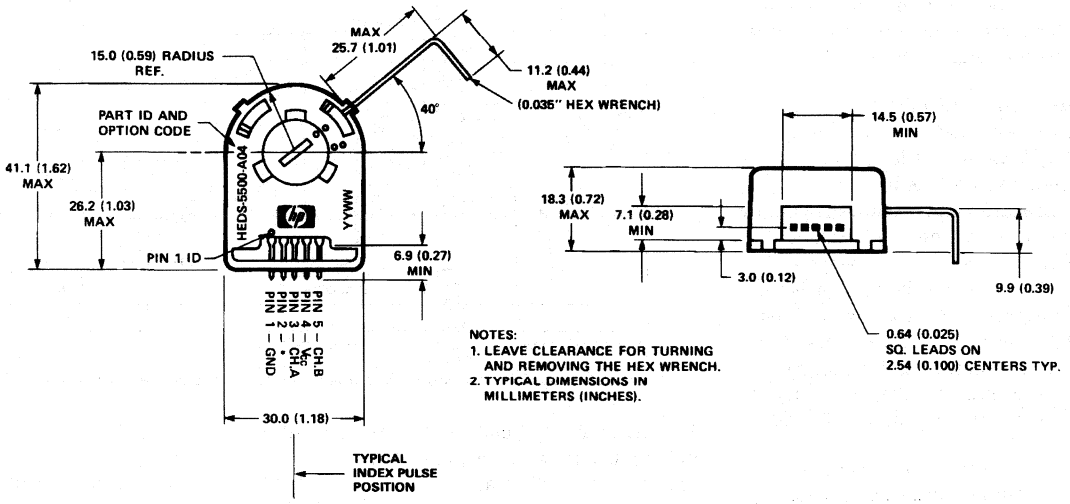
Applications

The HEDS-5500, 5540, 5600, 5640, and the HEDM-5500, 5600 provide motion detection at a low cost, making them ideal for high volume applications. Typical applications include printers, plotters, tape drives, positioning tables, and automatic handlers.

ESD WARNING: NORMAL HANDLING PRECAUTIONS SHOULD BE TAKEN TO AVOID STATIC DISCHARGE.

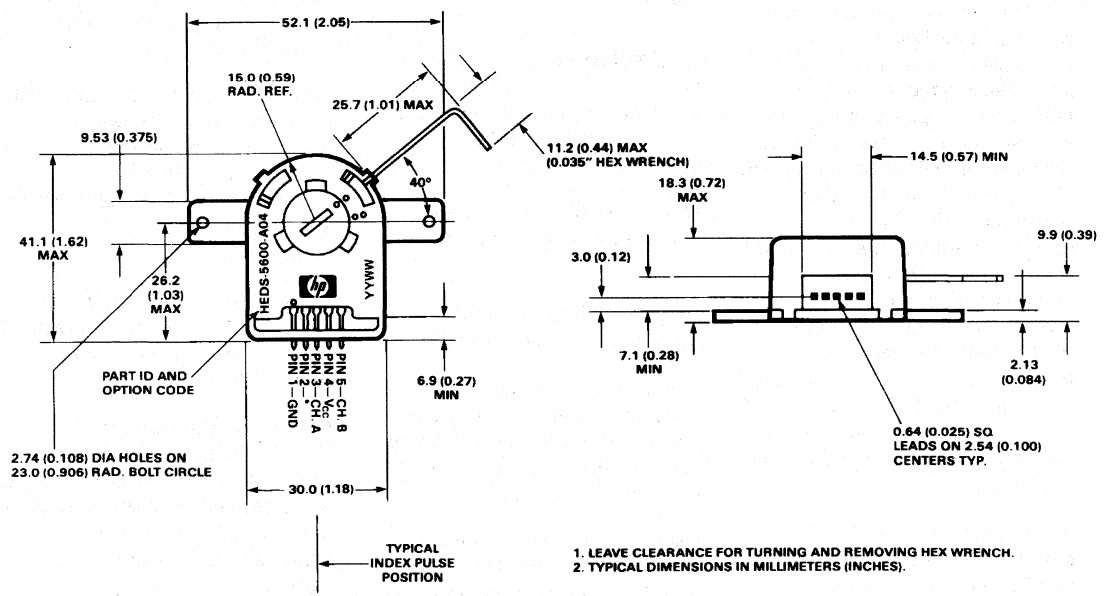
Package Dimensions

HEDS-5500/5540, HEDM-5500



***Note:** For the HEDS-5500 and HEDM-5500, Pin #2 is a No Connect. For the HEDS-5540, Pin #2 is CH. I, the index output.

HEDS-5600/5640, HEDM-5600



***Note:** For the HEDS-5600 and HEDM-5600, Pin #2 is a No Connect. For the HEDS-5640, Pin #2 is CH. I, the index output.

Theory of Operation

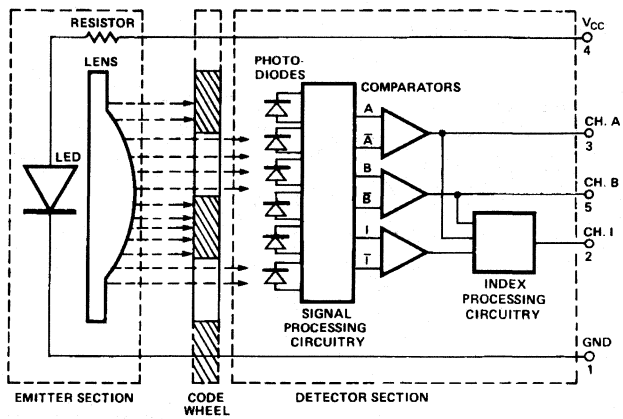
The HEDS-5500, 5540, 5600, 5640, and HEDM-5500, 5600 translate the rotary motion of a shaft into either a two- or a three-channel digital output.

As seen in the block diagram, these encoders contain a single Light Emitting Diode (LED) as its light source. The light is collimated into a parallel beam by means of a single polycarbonate lens located directly over the LED. Opposite the emitter is the integrated detector circuit. This IC consists of multiple sets of photodetectors and the signal processing circuitry necessary to produce the digital waveforms.

The codewheel rotates between the emitter and detector, causing the light beam to be interrupted by the pattern of spaces and bars on the codewheel. The photodiodes which detect these interruptions are arranged in a pattern that corresponds to the radius and design of the codewheel. These detectors are also spaced such that a light period on one pair of detectors corresponds to a dark period on the adjacent pair of detectors. The photodiode outputs are then fed through the signal processing circuitry resulting in A, $\overline{A}$, B and $\overline{B}$ (also I and $\overline{I}$ in the HEDS-5540 and 5640). Comparators receive these signals and produce the final outputs for channels A and B. Due to this integrated phasing technique, the digital output of channel A is in quadrature with that of channel B (90 degrees out of phase).

In the HEDS-5540 and 5640, the output of the comparator for I and $\overline{I}$ is sent to the index processing circuitry along with the outputs of channels A and B.

Block Diagram



NOTE: CIRCUITRY FOR CH. I IS ONLY IN HEDS-5540 AND 5640 THREE CHANNEL ENCODERS.

The final output of channel I is an index pulse P_0 which is generated once for each full rotation of the codewheel. This output P_0 is a one state width (nominally 90 electrical degrees), high true index pulse which is coincident with the low states of channels A and B.

Definitions

Count (N): The number of bar and window pairs or counts per revolution (CPR) of the codewheel.

One Cycle (C): 360 electrical degrees (°e), 1 bar and window pair.

One Shaft Rotation: 360 mechanical degrees, N cycles.

Position Error ($\Delta\Theta$): The normalized angular differencc between the actual shaft position and the position indicated by the encoder cycle count.

Cycle Error (ΔC): An indication of cycle uniformity. The difference between an observed shaft angle which gives rise to one electrical cycle, and the nominal angular increment of 1/N of a revolution.

Pulse Width (P): The number of electrical degrees that an output is high during 1 cycle. This value is nominally 180°e or 1/2 cycle.

Pulse Width Error (ΔP): The deviation, in electrical degrees, of the pulse width from its ideal value of 180°e.

State Width (S): The number of electrical degrees between a transition in the output of channel A and the neighboring transition in the output of channel B. There are 4 states per cycle, each nominally 90°e.

State Width Error (ΔS): The deviation, in electrical degrees, of each state width from its ideal value of 90°e.

Phase (ϕ): The number of electrical degrees between the center of the high state of channel A and the center of the high state of channel B. This value is nominally 90°e for quadrature output.

Phase Error ($\Delta\phi$): The deviation of the phase from its ideal value of 90°e.

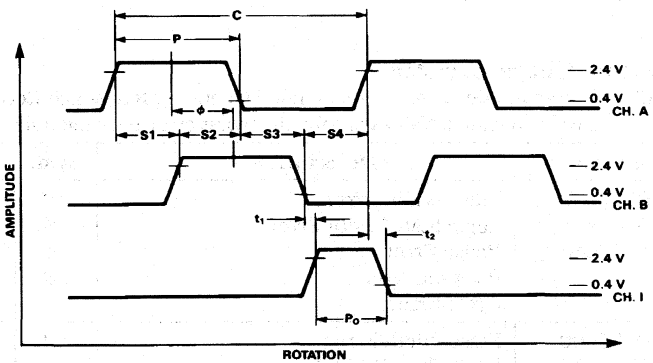
Absolute Maximum Ratings

Parameter	HEDS-55XX/56XX	HEDM-550X/560X
Storage Temperature, T_S	-40°C to 100°C	-40°C to +70°C
Operating Temperature, T_A	-40°C to 100°C	-40°C to +70°C
Supply Voltage, V_{CC}	-0.5 V to 7 V	-0.5 V to 7 V
Output Voltage, V_O	-0.5 V to V_{CC}	-0.5 V to V_{CC}
Output Current per Channel, I_{OUT}	-1.0 mA to 5 mA	-1.0 mA to 5 mA
Vibration	20 g, 5 to 1000 Hz	20 g, 5 to 1000 Hz
Shaft Axial Play	± 0.25 mm (± 0.010 in.)	± 0.175 mm (± 0.007 in.)
Shaft Eccentricity Plus Radial Play	0.1 mm (0.004 in.) TIR	0.04 mm (0.0015 in.) TIR
Velocity	30,000 RPM	30,000 RPM
Acceleration	250,000 rad/sec^2	250,000 rad/sec^2

Direction of Rotation: When the codewheel rotates in the counter-clockwise direction (as viewed from the encoder end of the motor), channel A will lead channel B. If the codewheel rotates in the clockwise direction, channel B will lead channel A.

Index Pulse Width (P_O): The number of electrical degrees that an index output is high during one full shaft rotation. This value is nominally 90°e or 1/4 cycle.

Output Waveforms



Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Temperature HEDS Series	T_A	-40		100	°C	
Temperature HEDM Series	T_A	-40		70	°C	non-condensing atmosphere
Supply Voltage	V_{CC}	4.5	5.0	5.5	Volts	Ripple < 100 mV_{p-p}
Load Capacitance	C_L			100	pF	2.7 kΩ pull-up
Count Frequency	f			100	kHz	Velocity (rpm) x N/60
Shaft Perpendicularity Plus Axial Play (HEDS Series)				± 0.25 (± 0.010)	mm (in.)	6.9 mm (0.27 in.) from mounting surface
Shaft Eccentricity Plus Radial Play (HEDS Series)				0.04 (0.0015)	mm (in.) TIR	6.9 mm (0.27 in.) from mounting surface
Shaft Perpendicularity Plus Axial Play (HEDM Series)				± 0.175 (± 0.007)	mm (in.)	6.9 mm (0.27 in.) from mounting surface
Shaft Eccentricity Plus Radial Play(HEDM Series)				0.04 (0.0015)	mm (in.) TIR	6.9 mm (0.27 in.) from mounting surface

Note: The module performance is guaranteed to 100 kHz but can operate at higher frequencies. 2.7 kΩ pull-up resistors required for HEDS-5540 and 5640.

Encoding Characteristics

Encoding Characteristics over Recommended Operating Range and Recommended Mounting Tolerances unless otherwise specified. Values are for the worst error over the full rotation.

Part No.	Description		Sym.	Min.	Typ.*	Max.	Units
HEDS-5500 HEDS-5600 (Two Channel)	Pulse Width Error		ΔP		7	45	°e
	Logic State Width Error		ΔS		5	45	°e
	Phase Error		Δϕ		2	20	°e
	Position Error		ΔΘ		10	40	min. of arc
	Cycle Error		ΔC		3	5.5	°e
HEDM-5500 HEDM-5600 (Two Channel)	Pulse Width Error		ΔP		10	45	°e
	Logic State Width Error		ΔS		10	45	°e
	Phase Error		Δϕ		2	15	°e
	Position Error		ΔΘ		10	40	min. of arc
	Cycle Error		ΔC		3	7.5	°e
HEDS-5540 HEDS-5640 (Three Channel)	Pulse Width Error		ΔP		5	35	°e
	Logic State Width Error		ΔS		5	35	°e
	Phase Error		Δϕ		2	15	°e
	Position Error		ΔΘ		10	40	min. of arc
	Cycle Error		ΔC		3	5.5	°e
	Index Pulse Width		P_O	55	90	125	°e
	CH. I rise after	-25°C to +100°C	t_1	10	100	250	ns
	CH. A or CH. B fall	-40°C to +100°C	t_1	-300	100	250	ns
	CH. I fall after	-25°C to +100°C	t_2	70	150	300	ns
	CH. B or CH. A rise	-40°C to +100°C	t_2	70	150	1000	ns

Note: See Mechanical Characteristics for mounting tolerances.
*Typical values specified at V_{CC} = 5.0 V and 25°C.

Electrical Characteristics

Electrical Characteristics over Recommended Operating Range.

Part No.	Parameter	Sym.	Min.	Typ.*	Max.	Units	Notes
HEDS-5500 HEDS-5600	Supply Current	I_{CC}		17	40	mA	
	High Level Output Voltage	V_{OH}	2.4			V	I_{OH} = -40 µA max.
	Low Level Output Voltage	V_{OL}			0.4	V	I_{OL} = 3.2 mA
	Rise Time	t_r		200		ns	C_L = 25 pF
	Fall Time	t_f		50		ns	R_L = 11 kΩ pull-up
HEDS-5540 HEDS-5640 HEDM-5500 HEDM-5600	Supply Current	I_{CC}	30	57	85	mA	
	High Level Output Voltage	V_{OH}	2.4			V	I_{OH} = -200 µA max.
	Low Level Output Voltage	V_{OL}			0.4	V	I_{OL} = 3.86 mA
	Rise Time	t_r		180		ns	C_L = 25 pF
	Fall Time	t_f		40		ns	R_L = 2.7 kΩ pull-up
HEDM-5500 HEDM-5600	Supply Current	I_{CC}	30	57	85	mA	
	High Level Output Voltage	V_{OH}	2.4			V	I_{OH} = -40 µA max.
	Low Level Output Voltage	V_{OL}			0.4	V	I_{OL} = 3.86 mA
	Rise Time	t_r		180		ns	C_L = 25 pF
	Fall Time	t_f		40		ns	R_L = 3.2 kΩ pull-up

*Typical values specified at V_{CC} = 5.0 V and 25°C.

Mechanical Characteristics

Parameter	Symbol	Dimension	Tolerance[1]	Units
Codewheel Fits These Standard Shaft Diameters		2 3 4 5 6 8	+0.000 -0.015	mm
		5/32 1/8 3/16 1/4	+0.0000 -0.0007	in
Moment of Inertia	J	0.6 (8.0 x 10^{-6})		g-cm^2 (oz-in-s^2)
Required Shaft Length[2]		14.0 (0.55)	± 0.5 (± 0.02)	mm (in.)
Bolt Circle[3]	2 screw mounting	19.05 (0.750)	± 0.13 (± 0.005)	mm (in.)
	3 screw mounting	20.90 (0.823)	± 0.13 (± 0.005)	mm (in.)
	external mounting ears	46.0 (1.811)	± 0.13 (± 0.005)	mm (in.)
Mounting Screw Size[4]	2 screw mounting	M 2.5 or (2-56)		mm (in.)
	3 screw mounting	M 1.6 or (0-80)		mm (in.)
	external mounting ears	M 2.5 or (2-56)		mm (in.)
Encoder Base Plate Thickness		0.33 (0.130)		mm (in.)
Hub Set Screw		(2-56)		(in.)

Notes:
1. These are tolerances required of the user.
2. The HEDS-55X5 and 56X5, HEDM-5505, 5605 provide an 8.9 mm (0.35 inch) diameter hole through the housing for longer motor shafts. See Ordering Information.
3. The HEDS-5540 and 5640 must be aligned using the aligning pins as specified in Figure 3, or using the alignment tool as shown in "Encoder Mounting and Assembly". See also "Mounting Considerations."
4. The recommended mounting screw torque for 2 screw and external ear mounting is 1.0 kg-cm (0.88 in-lbs). The recommended mounting screw torque for 3 screw mounting is 0.50 kg-cm (0.43 in-lbs).

Electrical Interface

To insure reliable encoding performance, the HEDS-5540 and 5640 three channel encoders require 2.7 kΩ (± 10%) pull-up resistors on output pins 2, 3, and 5 (Channels I, A, and B) as shown in Figure 1. These pull-up resistors should be located as close to the encoder as possible (within 4 feet). Each of the three encoder outputs can drive a single TTL load in this configuration.

The HEDS-5500, 5600, and HEDM-5500, 5600 two channel encoders do not normally require pull-up resistors. However, 3.2 kΩ pull-up resistors on output pins 3 and 5 (Channels A and B) are recommended to improve rise times, especially when operating above 100 kHz frequencies.

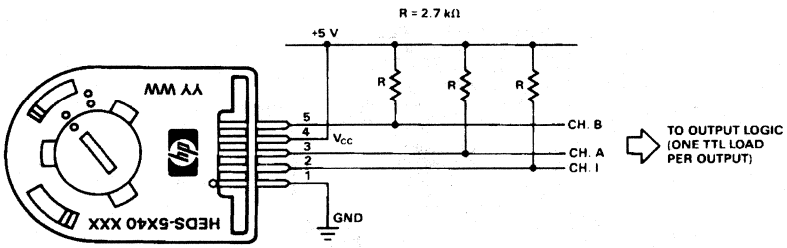


Figure 1. Pull-up Resistors on HEDS-5X40 Encoder Outputs.

Mounting Considerations

The HEDS-5540 and 5640 three channel encoders and the HEDM Series high resolution encoders must be aligned using the aligning pins as specified in Figure 3, or using the HEDS-8910 Alignment Tool as shown in Encoder Mounting and Assembly.

The use of aligning pins or alignment tool is recommended but not required to mount the HEDS-5500 and 5600. If these two channel encoders are attached to a motor with the screw sizes and mounting tolerances specified in the mechanical characteristics section without any additional mounting bosses, the encoder output errors will be within the maximums specified in the encoding characteristics section.

The HEDS-5500 and 5540 can be mounted to a motor using either the two screw or three screw mounting option as shown in Figure 2. The optional aligning pins shown in Figure 3 can be used with either mounting option.

The HEDS-5600, 5640, and HEDM-5600 have external mounting ears which may be used for mounting to larger motor base plates. Figure 4 shows the necessary mounting holes with optional aligning pins and motor boss.

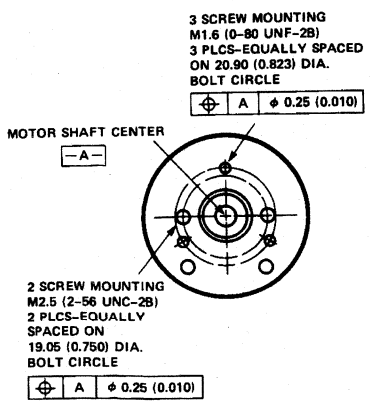


Figure 2. Mounting Holes.

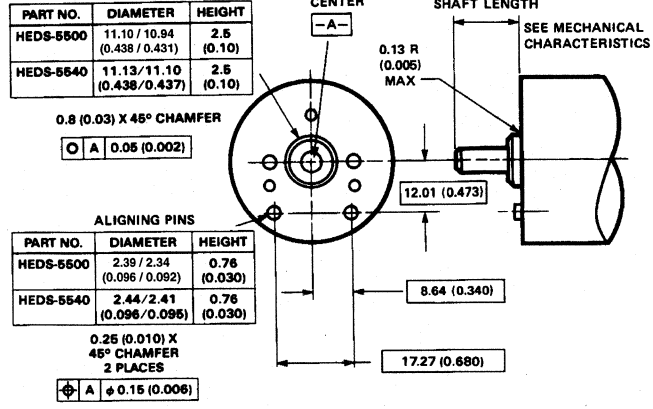


Figure 3. Optional Mounting Aids.

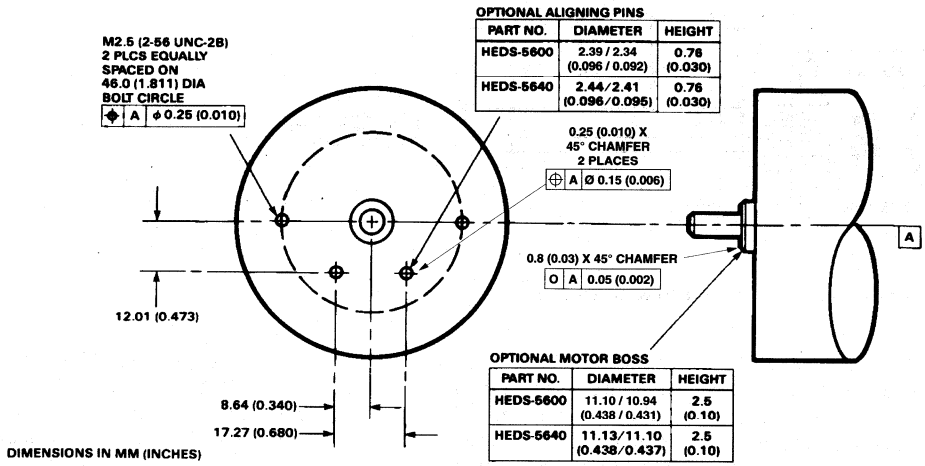
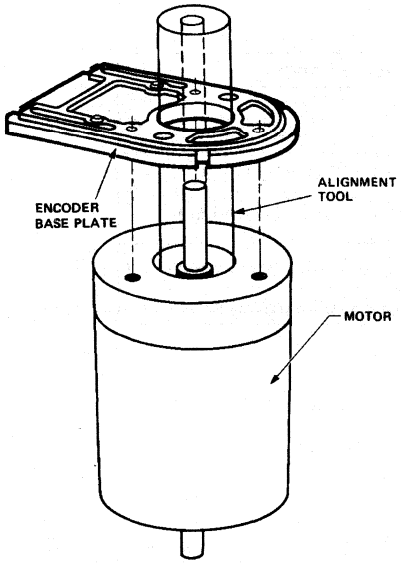


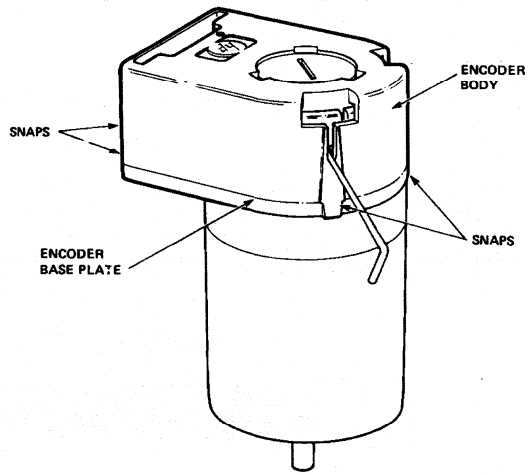
Figure 4. Mounting with External Ears.

Encoder Mounting and Assembly

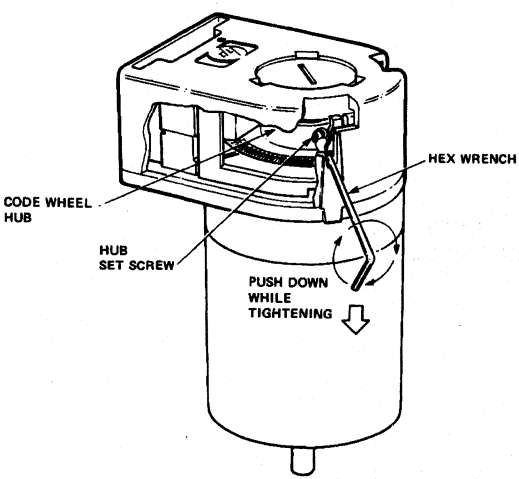


1. For HEDS-5500 and 5600: Mount encoder base plate onto motor. Tighten screws. Go on to step 2.

1a. For HEDS-5540, 5640 and HEDM-5500, 5600: Slip alignment tool onto motor shaft. With alignment tool in place, mount encoder baseplate onto motor as shown above. Tighten screws. Remove alignment tool.



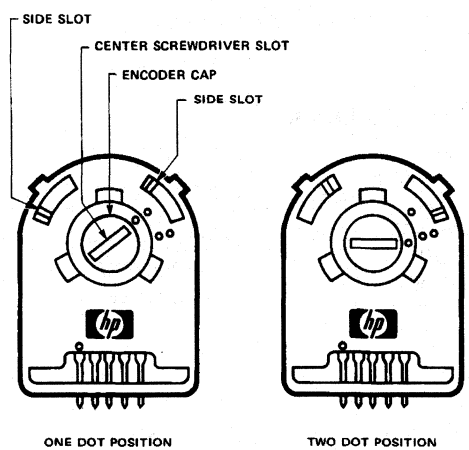
2. Snap encoder body onto base plate locking all 4 snaps.



3a. Push the hex wrench into the body of the encoder to ensure that it is properly seated into the code wheel hub set screws. Then apply a downward force on the end of the hex wrench. This sets the code wheel gap by levering the code wheel hub to its upper position.

3b. While continuing to apply a downward force, rotate the hex wrench in the clockwise direction until the hub set screw is tight against the motor shaft. The hub set screw attaches the code wheel to the motor's shaft.

3c. Remove the hex wrench by pulling it straight out of the encoder body.

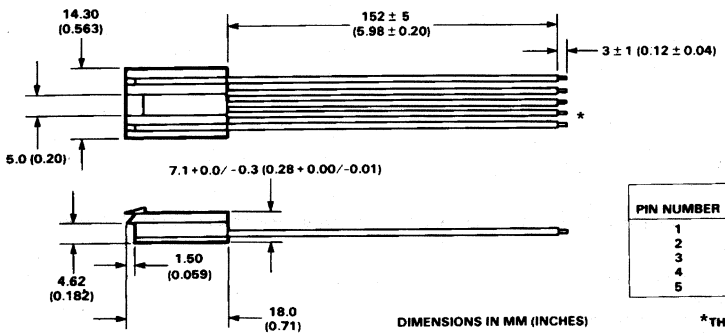


4. Use the center screwdriver slot, or either of the two side slots, to rotate the encoder cap dot clockwise from the one dot position to the two dot position. Do not rotate the encoder cap counterclockwise beyond the one dot position.

The encoder is ready for use!

Connectors

Manufacturer	Part Number
AMP	103686-4 640442-5
Dupont/Berg	65039-032 with 4825X-000 term.
HP (designed to mechanically lock into the HEDS-5XXX, HEDM-5X0X Series)	HEDS-8902 (2 ch.) with 4-wire leads
	HEDS-8903 (3 ch.) with 5-wire leads
Molex	2695 series with 2759 series term.

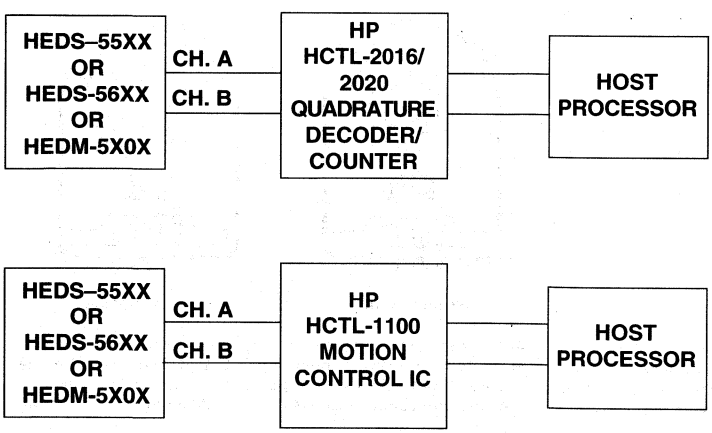


PIN NUMBER	PARAMETER	HEDS-8902 COLORS	HEDS-8903 COLORS
1	GROUND	BLACK	BLACK
2	CH. I	N/A*	BLUE
3	CH. A	WHITE	WHITE
4	V_{CC}	RED	RED
5	CH. B	BROWN	BROWN

*THIS WIRE IS NOT ON HEDS-8902.

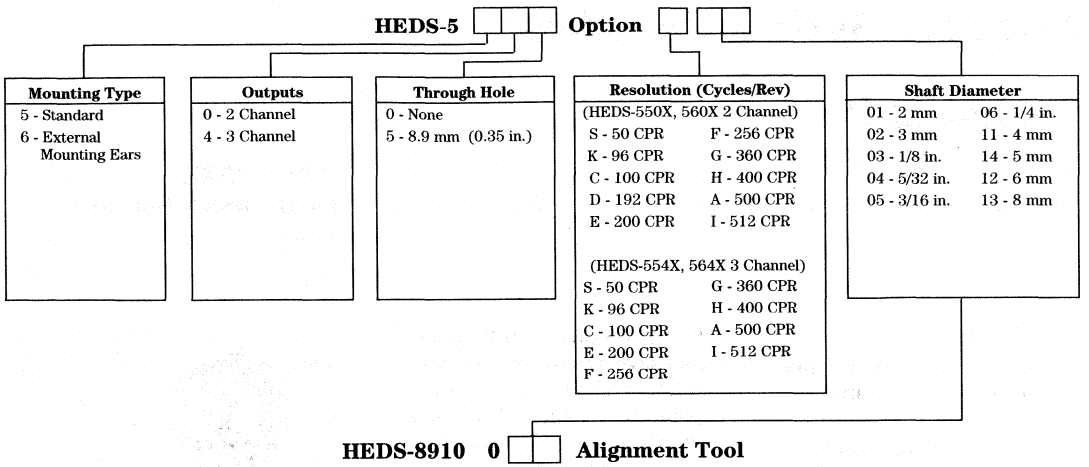
Figure 5. HEDS-8902 and 8903 Connectors.

Typical Interfaces



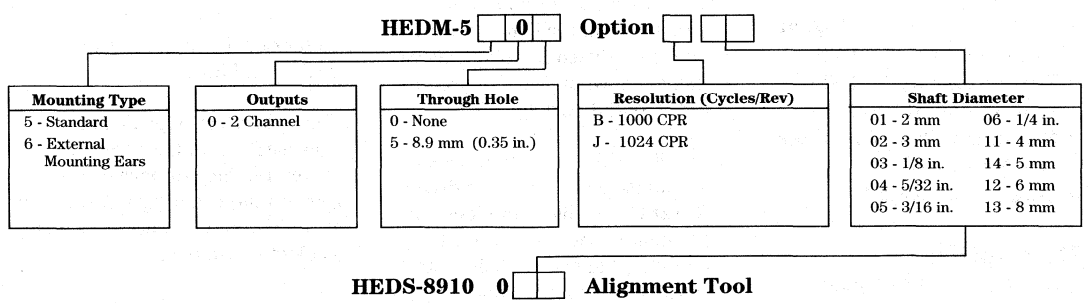
Ordering Information

Encoders with Metal Codewheels



(Included with each order of HEDS-554X/564X three channel encoders)

Encoders with Film Codewheels



(Included with each order of HEDM-550X/560X two channel encoders)

HEWLETT® PACKARD

Large Diameter (56mm), Housed Two and Three Channel Optical Encoders

Technical Data

HEDL-65XX, HEDS-65XX Series

Features:

- **Two Channel Quadrature Output with Optional Index Pulse**
- **TTL Compatible Single Ended Outputs on HEDS Series**
- **100°C Operating Temperature**
- **Industry Standard 26C31 CMOS Line Driver IC on HEDL Series**
- **Easy Assembly, No Signal Adjustment Necessary**
- **Resolutions up to 1024 Counts Per Revolution**
- **Maximum Shaft Diameter of 5/8 Inches**
- **Single +5 V Supply**

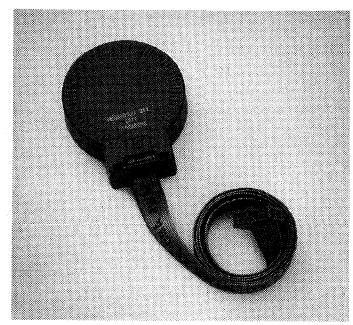
Description

The HEDS-65XX/HEDL-65XX are high performance two and three channel optical incremental encoders. These encoders emphasize high reliability, high resolution, and easy assembly. Each encoder contains a lensed LED source (emitter), an integrated circuit with detectors and output circuitry, and a codewheel which rotates between the emitter and detector integrated circuit. The outputs of the HEDS-6500 are two single ended square waves in quadrature. The HEDL-65XX outputs are differential.

The HEDS-6540 / HEDL-6540 also have a third channel index output in addition to the two quadrature outputs. This index is an active high pulse that occurs once every full rotation of the codewheel. Resolutions up to 1024 Counts Per Revolution are available in the two and three channel versions.

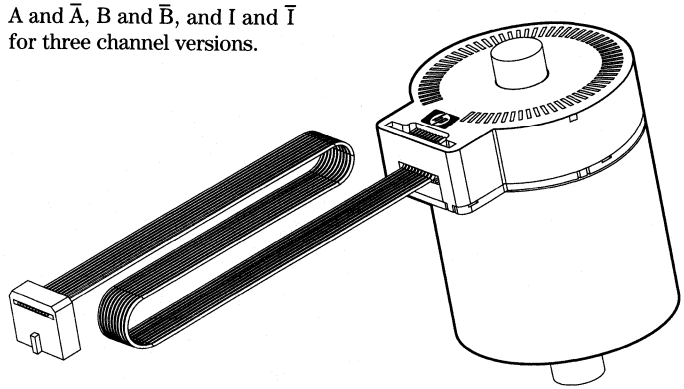
The line driver option offers enhanced performance when the encoder is used in noisy environments, or when it is required to drive long distances.

The line driver option utilizes an industry standard line driver IC (26C31) which provides complementary outputs for each encoder channel. Thus the outputs of the line driver encoder are A and $\overline{A}$, B and $\overline{B}$, and I and $\overline{I}$ for three channel versions.



Suggested line receivers are 26C32 and 26C33.

The quadrature signals are accessed through a cable and 10-pin female connector. Please refer to the ordering information at the end of this data sheet for a selection matrix.

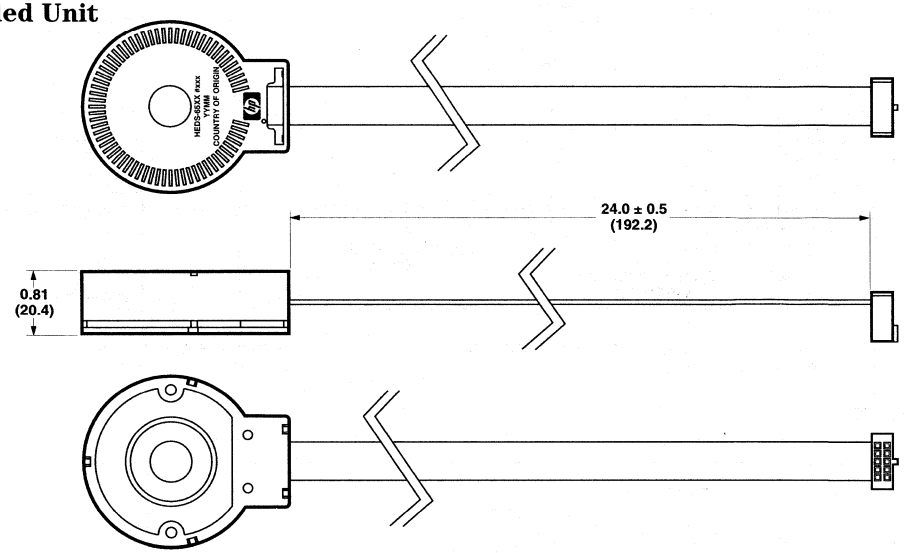


5965-2745E

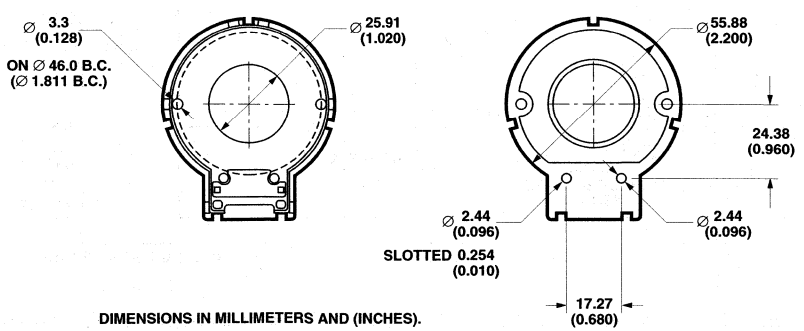
Applications

The HEDS-65XX / HEDL-65XX provide motion detection to a very high resolution and accept a variety of shaft sizes up to a maximum of 5/8 inches. Typical applications include printers, plotters, tape drives, positioning tables, and automatic handlers.

Assembled Unit

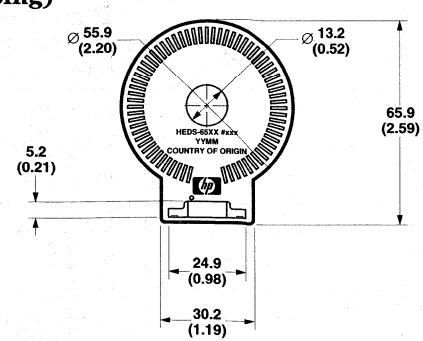


Base Plate



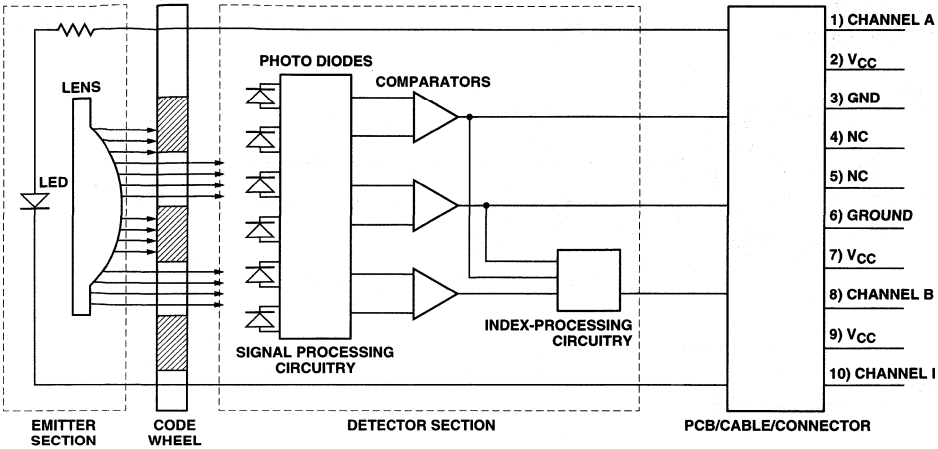
DIMENSIONS IN MILLIMETERS AND (INCHES).

Top Cover (Housing)

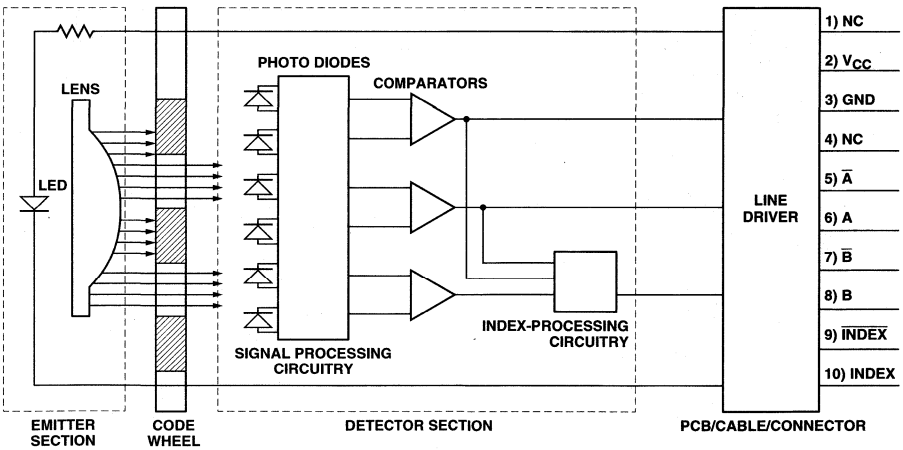


DIMENSIONS IN MILLIMETERS AND (INCHES).

Pinout A

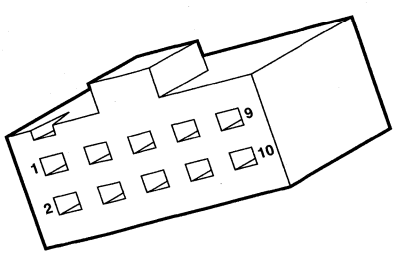


Pinout B



There are two different connector pin-out configurations used with the HEDS-65XX / HEDL-65XX series of encoders. The table below relates the part to its connector pin-out.

Connector Pin-out



Pinout A

HEDS-65XX CONNECTOR PIN OUT
1 Channel A
2 Vcc
3 GND
4 NC
5 NC
6 GND
7 Vcc
8 Channel B
9 Vcc
10 Channel I

Pinout B

HEDL-65XX CONNECTOR PIN OUT
1 NC
2 Vcc
3 GND
4 NC
5 $\overline{A}$
6 A
7 $\overline{B}$
8 B
9 $\overline{I}$ ($\overline{INDEX}$)
10 I (INDEX)

Theory of Operation

The HEDS-65XX / HEDL-65XX translate the rotary motion of a shaft into either a two or three channel digital output.

The HEDS-65XX uses one of the standard HEDS-9000 or HEDS-9040 modules for encoding purposes. The HEDL-654X uses the standard HEDL-9040 for encoding purposes.

As seen in the block diagram, these modules contain a single Light Emitting Diode (LED) as their light source (emitter). The light is collimated into a single parallel beam by means of a plastic lens located directly over the LED. Opposite the emitter is the integrated detector circuit (detector). This circuit consists of multiple sets of photodetectors and the signal processing circuitry necessary to produce the digital waveforms.

The codewheel rotates between the emitter and detector, causing the light beam to be interrupted by a pattern of spaces and bars on the codewheel. The photodiodes which detect these interruptions are arranged in a pattern that corresponds to the radius and design of the codewheel. These detectors are also spaced such that a light period on one pair of detectors corresponds to a dark period on the adjacent pair of detectors. The photodiode outputs are then fed into the signal processing circuitry resulting in A, $\overline{A}$, B, and $\overline{B}$ (I and $\overline{I}$ also in the three channel encoders).

Comparators receive these signals and produce the final outputs for channels A and B. Due to this integrated phasing technique, the digital output of channel A is in quadrature with that of channel B (90 degrees out of phase).

In the HEDS-6540 / HEDL-6540 the output of the comparator for the index pulse is combined with that of the outputs of channel A and channel B to produce the final index pulse. The index pulse is generated once every rotation of the codewheel and is a one state width (nominally 90 electrical degrees), true high index pulse. It is coincident with the low states on channels A and B.

Definitions

Count (N): The number of bar and window pairs or counts per revolution (CPR) of the codewheel.

One Cycle (C): 360 electrical degrees (e), 1 bar and window pair.

One Shaft Rotation: 360 mechanical degrees, N cycles.

Position Error ($\Delta\Theta$): The normalized angular difference between the actual shaft position and the position indicated by the encoder cycle count.

Cycle Error (ΔC): An indication of cycle uniformity. The difference between an observed shaft angle which gives rise to one electrical cycle, and the nominal angular increment of 1/N of a revolution.

Pulse Width (P): The number of electrical degrees that an output is high during one cycle. This value is nominally 180 e or 1/2 cycle.

Pulse Width Error (ΔP): The deviation, in electrical degrees, of the pulse width from its ideal value of 180 e.

State Width (S): The number of electrical degrees between a transition in the output of channel A and the neighboring transition in the output of channel B. There are 4 states per cycle, each nominally 90 e.

State Width Error (ΔS): the deviation, in electrical degrees, of each state width from its ideal value of 90 e.

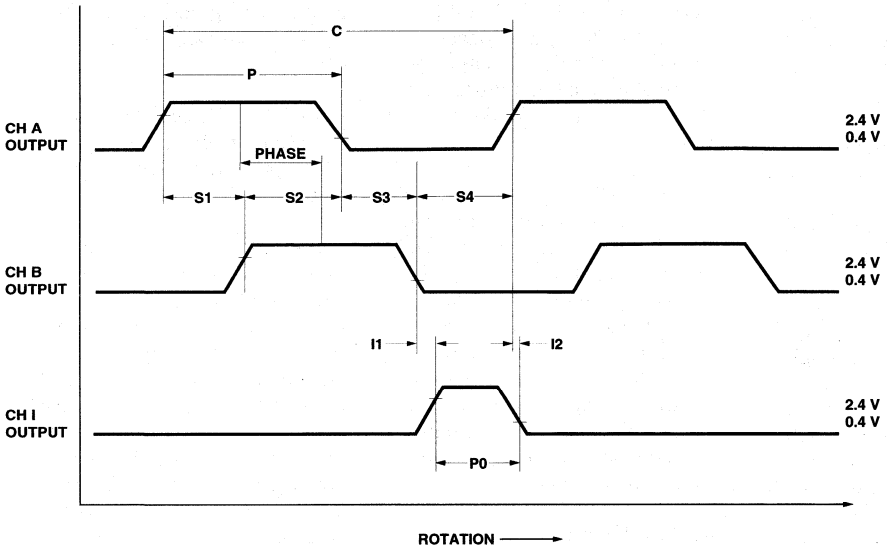
Phase (Φ): the number of electrical degrees between the center of high state on channel A and the center of the high state on channel B. This value is nominally 90 e for quadrature output.

Phase Error ($\Delta\Phi$): The deviation of the phase from its ideal value of 90 e.

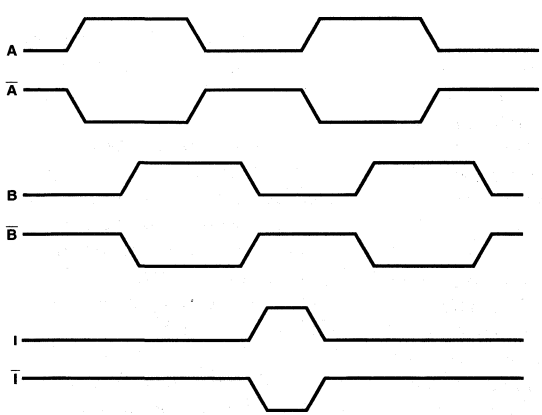
Direction of Rotation: When the codewheel rotates in a counterclockwise direction (when viewed from the encoder end of the motor) channel A will lead channel B. If the codewheel rotates in the clockwise direction channel B will lead channel A.

Index Pulse Width (P0): The number of electrical degrees that an index output is high during one full shaft rotation. This value is nominally 90 e or 1/4 cycle.

Output Waveforms



Waveforms for Encoders without Line Drivers.



Waveforms for Encoders with Line Drivers.
(Meets all requirements of EIA-422.)

Absolute Maximum Ratings

Parameter	HEDS-6500	HEDS-6540	HEDL-6540	HEDL-6545	
Storage Temperature	-40 to +100	-40 to +100	-40 to +100	-40 to +100	Celsius
Operating Temperature	-40 to +100	-40 to +100	-40 to +100	-40 to +100	Celsius
Supply Voltage	-.5 to +7	-.5 to +7	-.5 to +7	-.5 to +7	Volts
Output Voltage	-.6 to V_{CC}	-.6 to V_{CC}	-.6 to V_{CC}	-.6 to V_{CC}	Volts
Output Current Per Channel	-1 to 5	-1 to 5			mA
Velocity	30,000	30,000	30,000	30,000	RPM
Vibration	20	20	20	20	Gs
Shaft Axial Play	5	5	5	5	Inch/1000
Radial Play & Eccentricity	2	2	2	2	Inch/1000

Recommended Operating Conditions

Parameter	HEDS-6500	HEDS-6540	HEDL-6540	HEDL-6545	
Temperature	-40 to +100	-40 to +100	-40 to +100	-40 to +100	Celsius
Supply Voltage	4.5 to 5.5	4.5 to 5.5	4.5 to 5.5	4.5 to 5.5	Volts
Load Capacitance	100	100	100	100	pF
Count Frequency	100	100	100	100	kHz
Shaft Eccentricity Plus Radial Play	± .05 (± .002)	± .05 (± .002)	± .05 (± .002)	± .05 (± .002)	mm (Inch/1000)

Note: The HEDS-65XX performance is guaranteed to 100 kHz but can operate at higher frequencies. For frequencies above 100 kHz it is recommended that the load capacitance not exceed 25 pF and pull up resistors of 3.3 kΩ between the output channels and V_{CC} are included.

Encoding Characteristics

Encoding Characteristics over Recommended Operating Range and Recommended Mounting Tolerances unless otherwise specified. Values are for the worst error in the full rotation.

Part Number	Description	Symbol	Min.	Typ.*	Max.	Units
HEDS-6500***	Pulse Width Error	ΔP		5	35	e
	Logic State Width Error	ΔS		5	35	e
	Phase Error	ΔΦ		2	15	e
	Position Error	ΔΘ		7	20	min. of arc
	Cycle Error	ΔC		5	5.5	e
HEDS-6540**	Pulse Width Error	ΔP		5	35	e
	Logic State Width Error	ΔS		5	35	e
	Phase Error	ΔΦ		2	15	e
	Position Error	ΔΘ		7	20	min. of arc
	Cycle Error	ΔC		5	5.5	e
	Index Pulse Width	ΔP0	55	90	125	e
	CH I fall after CH B or CH A fall					
	-25°C to +100°C	t1	10	100	250	ns
	-40°C to +100°C	t1	-300	100	250	ns
	CH I rise after CH B or CH A rise					
	-25°C to +100°C	t2	70	150	300	ns
	-40°C to +100°C	t2	70	150	1000	ns
HEDL-654X	Pulse Width Error	ΔP		5	35	e
	Logic State Width Error	ΔS		5	35	e
	Phase Error	ΔΦ		2	15	e
	Position Error	ΔΘ		7	20	min. of arc
	Cycle Error	ΔC		5	5.5	e
	Index Pulse Width	ΔP0		90		e

*Typical values specified at V_{CC} = 5.0 V and 25°C.

**HEDS-6540 – Active high Index part. Pull-up of 2.7 kΩ used on all outputs of modules that do not have a line driver.

***HEDS-6500 – 3.3 kΩ pull-up resistors used on all encoder module outputs.

Electrical Characteristics

Electrical Characteristics over Recommended Operating Range, typical at 25°C.

Part Number	Symbol*	Min.	Typ.	Max.	Units	Notes
HEDS-6500	I_{CC}		17	40	mA	
	V_{OH}	2.4			V	I_{OH} = -40 µA max
	V_{OL}			0.4	V	I_{OL} = 3.2 mA
	t_r		200		ns	C_L = 25 pF, R_L = 11 kΩ pull-up.
	t_f		50		ns	
HEDS-6540	I_{CC}	30	57	85	mA	
	V_{OH}	2.4			V	I_{OH} = -200 µA max
	V_{OL}			0.4	V	I_{OL} = 3.86 mA
	t_r		180		ns	C_L = 25 pF, R_L = 3.3 kΩ pull-up.
	t_f		40		ns	

*Explanation for symbols.

I_{CC} – Supply current, V_{OH} – High Level Output Voltage, V_{OL} – Low Level Output Voltage, t_r – Rise Time, t_f – Fall Time.

Electrical Interfaces

To insure reliable encoding performance, the HEDS-6540 three channel encoder requires 2.7 kΩ pull-up resistors to the supply voltage on each of the three output lines Ch. A, Ch. B, and Ch. I located as close as possible to the encoder (less than 4 feet).

Mechanical Characteristics

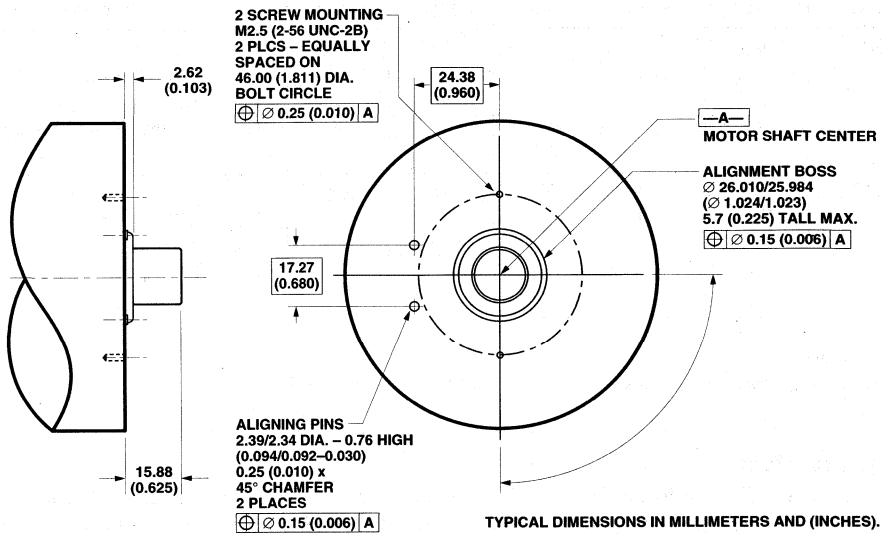
Parameter	Symbol	Dimensions	Tolerances [1]	Units
Moment Of Inertia	J	7.7 (110 x 10^{-6})		gcm^2 ($oz\text{-}in\text{-}s^2$)
Required Shaft Length [2]		15.9 (0.625)	± 0.6 (.024)	mm (inches)
Bolt Circle [3]		46.0 (1.811)	± 0.13 (.005)	mm (inches)
Mounting Screw Size [4]		2.5 x 0.45 x 5		mm
Pan Head Style		#2-56 x 3/16		Inches
Encoder Base Plate Thickness		3.04 (120)		mm (inches)
Mounting Screw Torque		1.0 (0.88)		Kg (in-lbs)
Hub Set Screw		UNC #2-56		Hex head set screw

Notes:

1. These are tolerances required of the user.
2. Through hole in the encoder housing are also available, for longer shafts.
3. The HEDL-65X0 must be aligned using the aligning pins as specified in the section on "MOUNTING CONSIDERATIONS."
4. The recommended mounting screw torque for 2 screws is 1.0 Kg (0.88 in-lbs).

Mounting Considerations

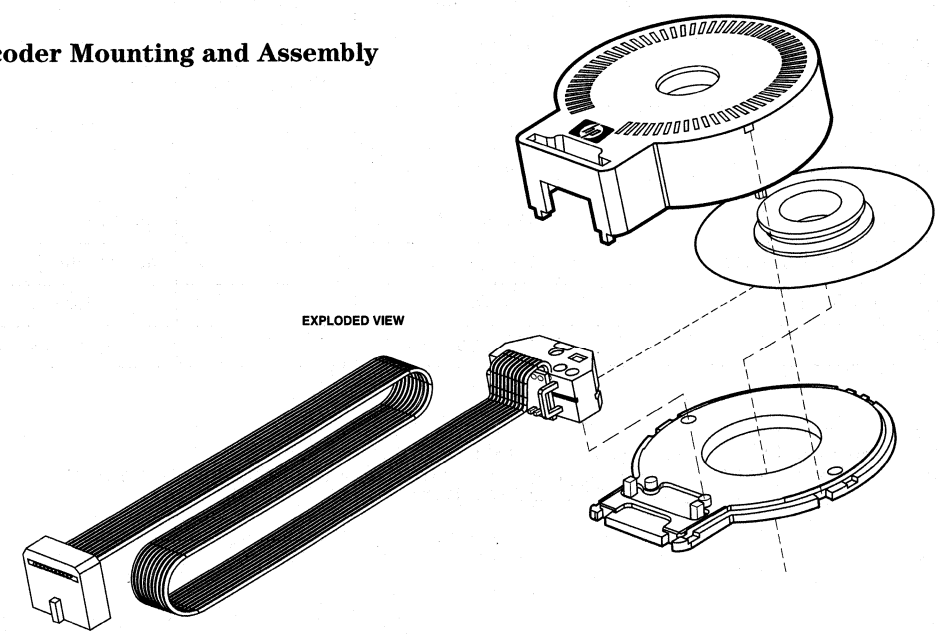
The HEDS-654X/HEDL-654X must be aligned with respect to the optical center (codewheel shaft) as indicated in the following figure.



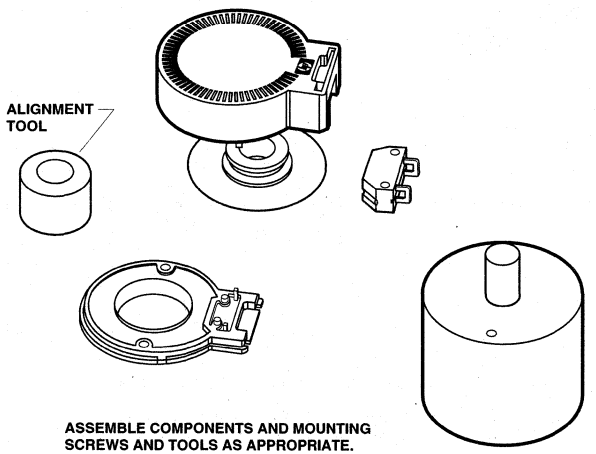
If neither locating pins nor locating boss are available, then a centering tool supplied by HP can be used (HEDS-6510).

The following figure shows how the main encoder components are organized.

Encoder Mounting and Assembly

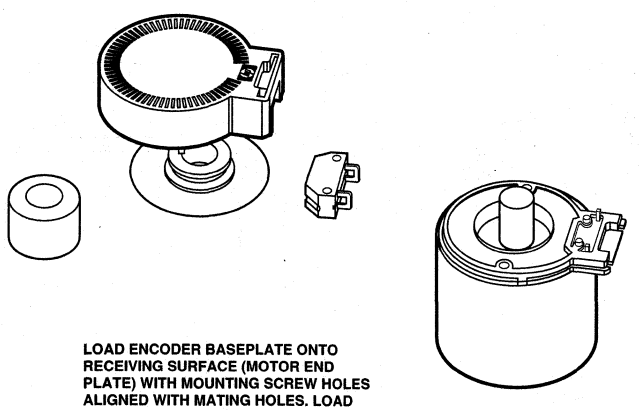


1



ASSEMBLE COMPONENTS AND MOUNTING SCREWS AND TOOLS AS APPROPRIATE.

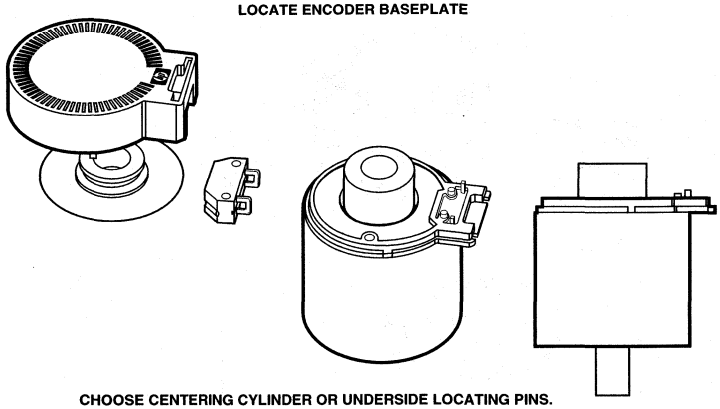
2



LOAD ENCODER BASEPLATE ONTO RECEIVING SURFACE (MOTOR END PLATE) WITH MOUNTING SCREW HOLES ALIGNED WITH MATING HOLES. LOAD MOUNTING SCREWS AND LEAVE SLIGHTLY LOOSE.

3

LOCATE ENCODER BASEPLATE



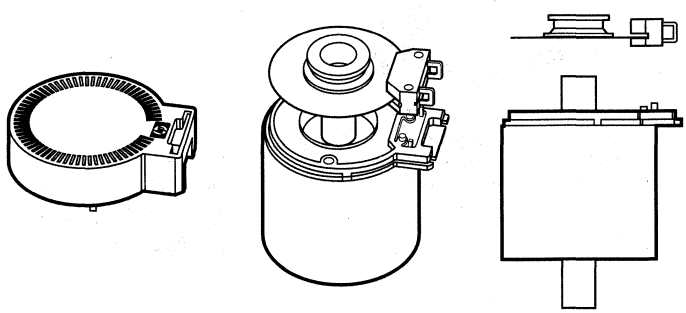
CHOOSE CENTERING CYLINDER OR UNDERSIDE LOCATING PINS.

CENTERING CYLINDER: LOCATE ENCODER BASEPLATE WITH CENTERING CYLINDER. WHEN IN PLACE, TIGHTEN MOUNTING SCREWS.

LOCATING PINS: WITH LOCATING PINS PROPERLY SEATED IN CORRESPONDING RECEIVING HOLES IN ENCODER BASEPLATE, TIGHTEN MOUNTING SCREWS.

4

LOCATE ENCODER MODULE AND CODEWHEEL

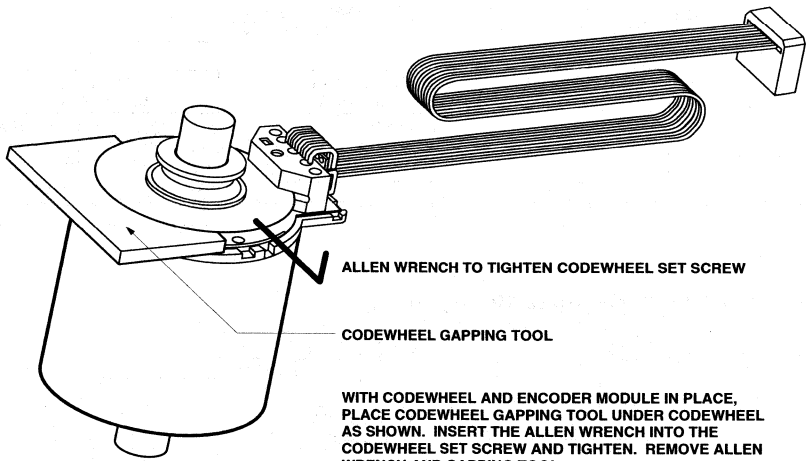


ALIGN ENCODER MODULE AND CODEWHEEL AS SHOWN.
BE CAREFUL NOT TO DAMAGE THE ENCODER INTERNAL COMPONENTS WITH THE CODEWHEEL.

BRING THE ENCODER MODULE AND CODEWHEEL DOWN SUCH THAT THE ENCODER MODULE LOCATING HOLES (ON ITS UNDERSIDE) MATE WITH THE BASEPLATE ROUND PINS. THE BASEPLATE SQUARE PINS SHOULD SEAT INTO THE ENCODER MODULE MOUNTING THRU HOLES.

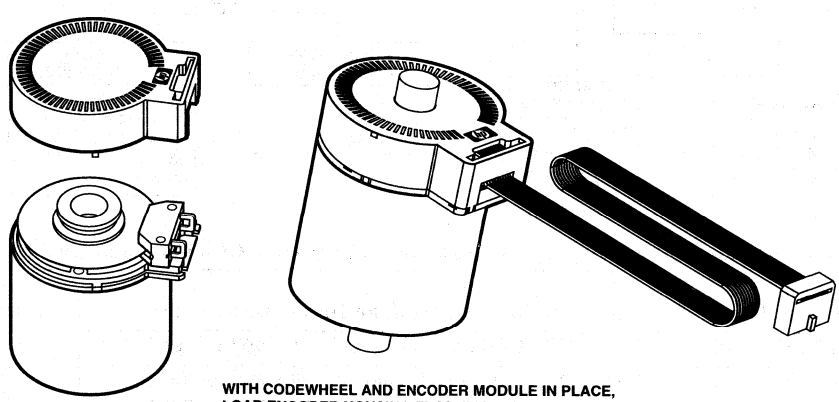
CONCURRENTLY, BRING THE CODEWHEEL DOWN ONTO THE MATING SHAFT.

5



WITH CODEWHEEL AND ENCODER MODULE IN PLACE, PLACE CODEWHEEL GAPPING TOOL UNDER CODEWHEEL AS SHOWN. INSERT THE ALLEN WRENCH INTO THE CODEWHEEL SET SCREW AND TIGHTEN. REMOVE ALLEN WRENCH AND GAPPING TOOL.

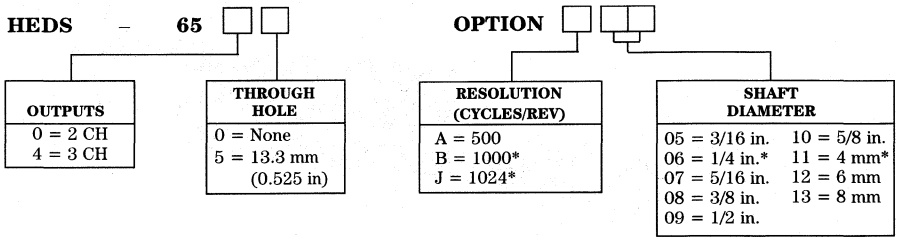
6



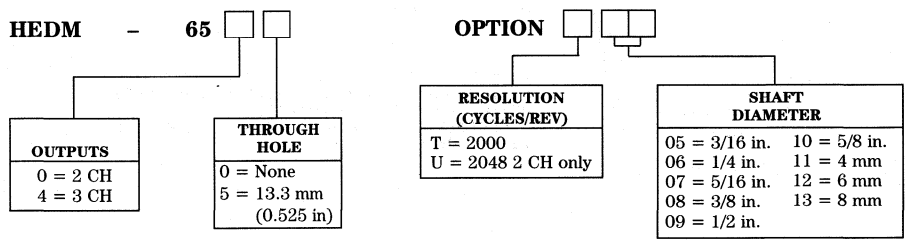
WITH CODEWHEEL AND ENCODER MODULE IN PLACE, LOAD ENCODER HOUSING FROM TOP INTO "SNAPPED" POSITION. INSURE THAT ANY CABLES FROM THE ENCODER MODULE ARE FOLDED DOWN SUCH THAT THEY EMERGE FROM THE BOTTOM OF THE HOUSING'S REAR RECTANGULAR PORT.

Ordering Information for 2CH and 3CH Encoder Modules

Encoders with Metal Codewheels (up to 100 Degree C.)

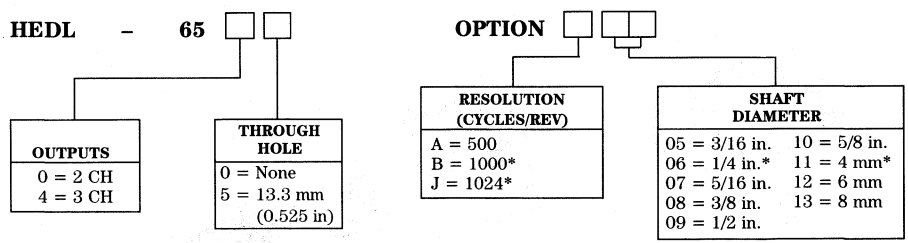


Encoders with Film Codewheels (up to 70 Degree C.)



Ordering Information for 2CH and 3CH Encoders Module with Line Driver

Encoders with Metal Codewheels (up to 100 Degree C.)



Encoders with Film Codewheels (up to 70 Degree C.) for 2000 CPR and 2048 CPR

Part Number	Encoder Module with Line Driver Description	Available Shaft Diameter
HEDL-6560#TXX	2 Ch. 2000 CPR encoder module with no through hole	Please refer to HEDS-65XX data sheet
HEDL-6561#TXX	2 ch. 2000 CPR encoder module with through hole	
HEDL-6560#UXX	2 ch, 2048 CPR encoder module with no through hole	
HEDL-6561#UXX	2 ch. 2048 CPR encoder module with through hole	
HEDL-6564#TXX	3 ch. 2000 CPR encoder module with no through hole	
HEDL-6565#TXX	3 ch. 2000 CPR encoder module with through hole	

*This is a popular option with short lead time.

Ordering Information for HEDS-65XX Centering Tools

HEDS–6510 OPTION 0 ☐☐

SHAFT DIAMETER	
05 = 3/16 in.	10 = 5/8 in.
06 = 1/4 in.	11 = 4 mm
07 = 5/16 in.	12 = 6 mm
08 = 3/8 in.	13 = 8 mm
09 = 1/2 in.	

Ordering Information for HEDS-65XX Codewheel

Gapping Tool

HEDS-6511

HEWLETT® PACKARD

Panel Mount Optical Encoders

Technical Data

HEDS-5700 Series

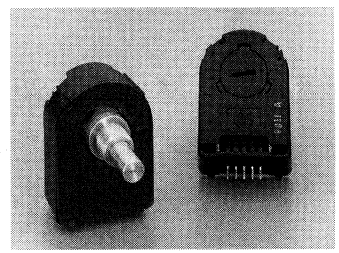
Features

- **Two Channel Quadrature Output with Optional Index Pulse**
- **Available with or without Static Drag for Manual or Mechanized Operation**
- **High Resolution – Up to 512 CPR**
- **Long Rotational Life, >1 Million Revolutions**
- **-20 to 85°C Operating Temperature Range**
- **TTL Quadrature Output**
- **Single 5 V Supply**
- **Available with Color Coded Leads**

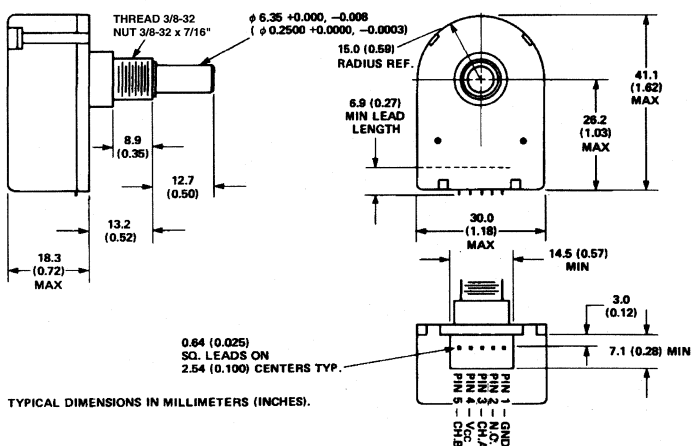
Description

The HEDS-5700 series is a family of low cost, high performance, optical incremental encoders with mounted shafts and bushings. The HEDS-5700 is available with tactile feedback for hand operated panel mount applications, or with a free spinning shaft for applications requiring a pre-assembled encoder for position sensing.

The encoder contains a collimated LED light source and special detector circuit which allows for high resolution, excellent encoding performance, long rotational life, and increased reliability. The unit outputs two digital waveforms which are 90 degrees out of phase to provide position and direction information. The HEDS-5740 Series provides a third Index Channel.

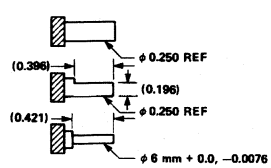


Package Dimensions



TYPICAL DIMENSIONS IN MILLIMETERS (INCHES).

SHAFT OPTIONS



OPTIONAL WIRING COLOR CODE TABLE	
COLOR	OUTPUT
WHITE	A
BROWN	B
RED	V_{CC}
BLACK	GND
BLUE (THREE CHANNEL)	I

*Note: For the HEDS-5700, Pin #2 is a No Connect. For the HEDS-5740, Pin #2 is Channel I, the index output.

The HEDS-5700 is quickly and easily mounted to a front panel using the threaded bushing, or it can be directly coupled to a motor shaft (or gear train) for position sensing applications.

Applications

The HEDS-5700 with the static drag option is best suited for applications requiring digital information from a manually operated knob. Typical front panel applications include instruments, CAD/CAM systems, and audio/video control boards.

The HEDS-5700 without static drag (free spinning) is best suited for low speed, mechanized operations. Typical applications are copiers, X-Y tables, and assembly line equipment.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Notes
Storage Temperature	T_s	-40	+85	°C	
Operating Temperature	T_a	-20	+85	°C	
Vibration			20	g	20 Hz - 2 kHz
Supply Voltage	V_{CC}	-0.5	7	V	
Output Voltage	V_O	-0.5	V_{CC}	V	
Output Current per Channel	I_O	-1	5	mA	
Shaft Load – Axial			1	lb	
– Radial			1	lb	

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Notes
Temperature	T	-20	+85	°C	Noncondensing Atmosphere
Supply Voltage	V_{CC}	4.5	5.5	V	Ripple <100 mV_{p-p}
Rotational Speed – Drag			300	RPM	
– Free Spinning			2000	RPM	

Electrical Characteristics Over Recommended Operating Range, Typical at 25°C

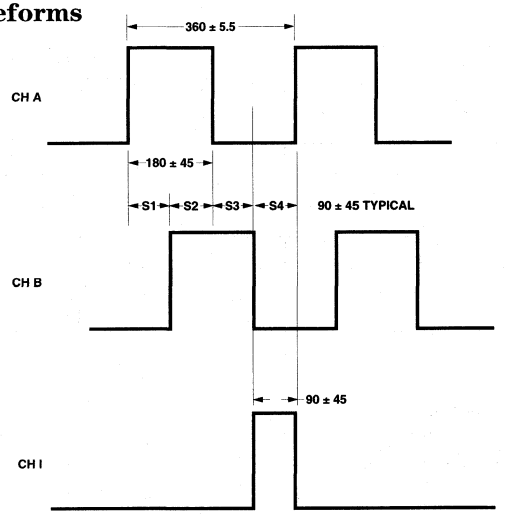
Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Supply Current	I_{CC}		17	40	mA	Two Channel
			57	85		Three Channel
High Level Output Voltage	V_{OH}	2.4			V	I_{OH} = -40 µA Max.
Low Level Output Voltage	V_{OL}			0.4	V	I_{OL} = 3.2 mA

Note: If more source current is required, use a 3.2 K pullup resistor on each output.

Mechanical Characteristics

Parameter		Min.	Typ.	Max.	Units	Notes
Starting Torque	– Static Drag		0.47		oz in	
	– Free Spinning			0.14	oz in	
Dynamic Drag	– Static Drag		1.1		oz in	100 RPM
	– Free Spinning		0.70		oz in	2000 RPM
Rotational Life	– Static Drag	1×10^6			Revolutions	1 lb Load
	– Free Spinning	12×10^6			Revolutions	4 oz Radial Load
Mounting Torque of Nut				13	lb in	

Output Waveforms



NOTE:
ALL VALUES ARE IN ELECTRICAL DEGREES, WHERE 360° e = 1 CYCLE OF RESOLUTION.
ERRORS ARE WORST CASE OVER ONE REVOLUTION.
CH B LEADS CH A FOR COUNTERCLOCKWISE ROTATION.
CH A LEADS CH B FOR CLOCKWISE ROTATION.

Ordering Information

HEDS-57□□-□□□

Outputs
0 - 2 Channel
4 - 3 Channel

Mechanical Configuration
0 - Pins
1 - 6" Coded Leads

Resolutions (Cycles Per Revolution)

HEDS-570X 2 Channel

K - 96 CPR	G - 360 CPR
C - 100 CPR	H - 400 CPR
D - 192 CPR	A - 500 CPR
E - 200 CPR	I - 512 CPR
F - 256 CPR	

HEDS-574X Three Channel*

F - 256 CPR	A - 500 CPR
G - 360 CPR	I - 512 CPR

Drag Option
0 - Free Spining
1 - Static Drag

Shaft Configuration
0 - 1/4" dia. with no flat
1 - 6 mm dia. with no flat
2 - 1/4" dia. with flat

*Please contact factory for other resolutions.

HEWLETT® PACKARD

Miniature Panel Mount Optical Encoders

Technical Data

MOTION SENSING AND CONTROL

HRPG Series

Features

- **Miniature Size**
- **Smooth Turning and Detented Options**
- **Multiple Mounting Bracket Options**
- **Uses Optical Reflective Technology**
- **Quadrature Digital Output**
- **Small Footprint for Versatile Mounting**
- **TTL Compatible**

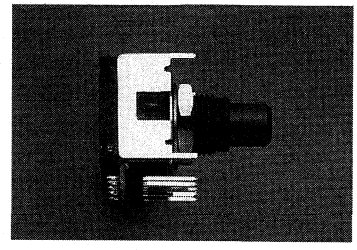
Description

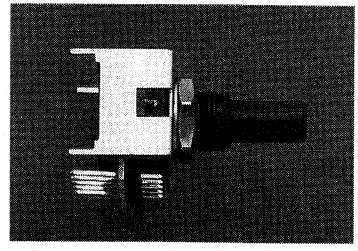
The HRPG series is a family of miniature panel mount optical encoders, also known as Rotary Pulse Generators (RPG) and digital potentiometers. The HRPG is designed to be mounted on a front panel and used as a rotary, data-entry device. The HRPG is very flexible for numerous applications due to the many configuration options available. These options include detents or smooth, multiple terminations, versatile mounting capabilities, and different shaft configurations.

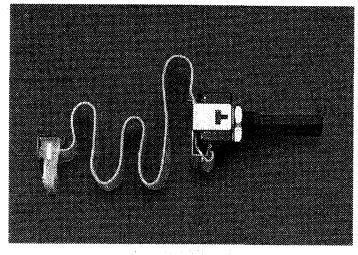
The HRPG uses optical reflective technology providing accuracy and reliability to the encoder. An LED emits a beam of light onto the specular codewheel surface. When the light strikes the surface, it projects the image of the codewheel back on the photodetector, causing the output to change. The entire detector circuit is on one IC, thus the part is less sensitive to temperature and other environmental variations.

Applications

Typical applications for the Rotary Pulse Generator include front panel instruments, audio/visual boards, and other devices requiring digital output from a turning knob.







Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Notes
Storage Temperature	T_S	-40	+85	°C	
Operating Temperature	T_A	0	+70	°C	
Vibration			20	g	20 Hz to 2 kHz
Supply Voltage	V_{CC}	-0.5	7	V	
Output Voltage	V_O	-0.5	V_{CC}	V	
Output Current Per Channel	I_O	-1	5	mA	
Shaft Load – Axial			4.0	N	10^6 Revolutions
Shaft Load – Radial			0.1	Nm	10^6 Revolutions
Revolution Life		10^6		Rev	At Maximum Loads

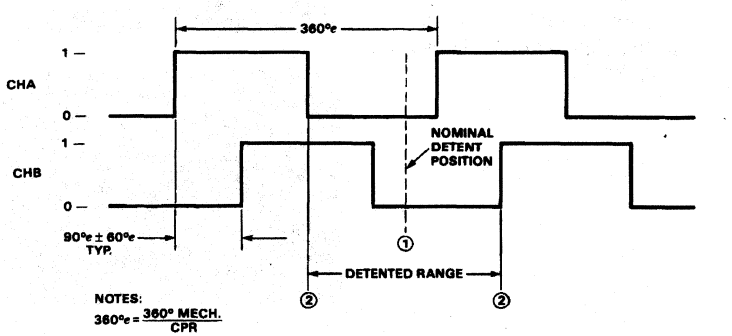
Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Notes
Temperature	T	0	+70	°C	Noncondensing Atmosphere
Supply Voltage	V_{CC}	4.5	5.5	V	Ripple < 100 mV_{P-P}
Rotation Speed – Detented			200	RPM	
– Smooth			300	RPM	

Electrical Characteristics
Over Recommended Operating Range

Parameter	Symbol	Min.	Max.	Units	Notes
Supply Current	I_{CC}		40	mA	
High Level Output Voltage	V_{OH}	2.4		V	I_{OH} = -40 µA Max.
Low Level Output Voltage	V_{OL}		0.4	V	I_{OL} = 3.2 mA

Output Waveforms



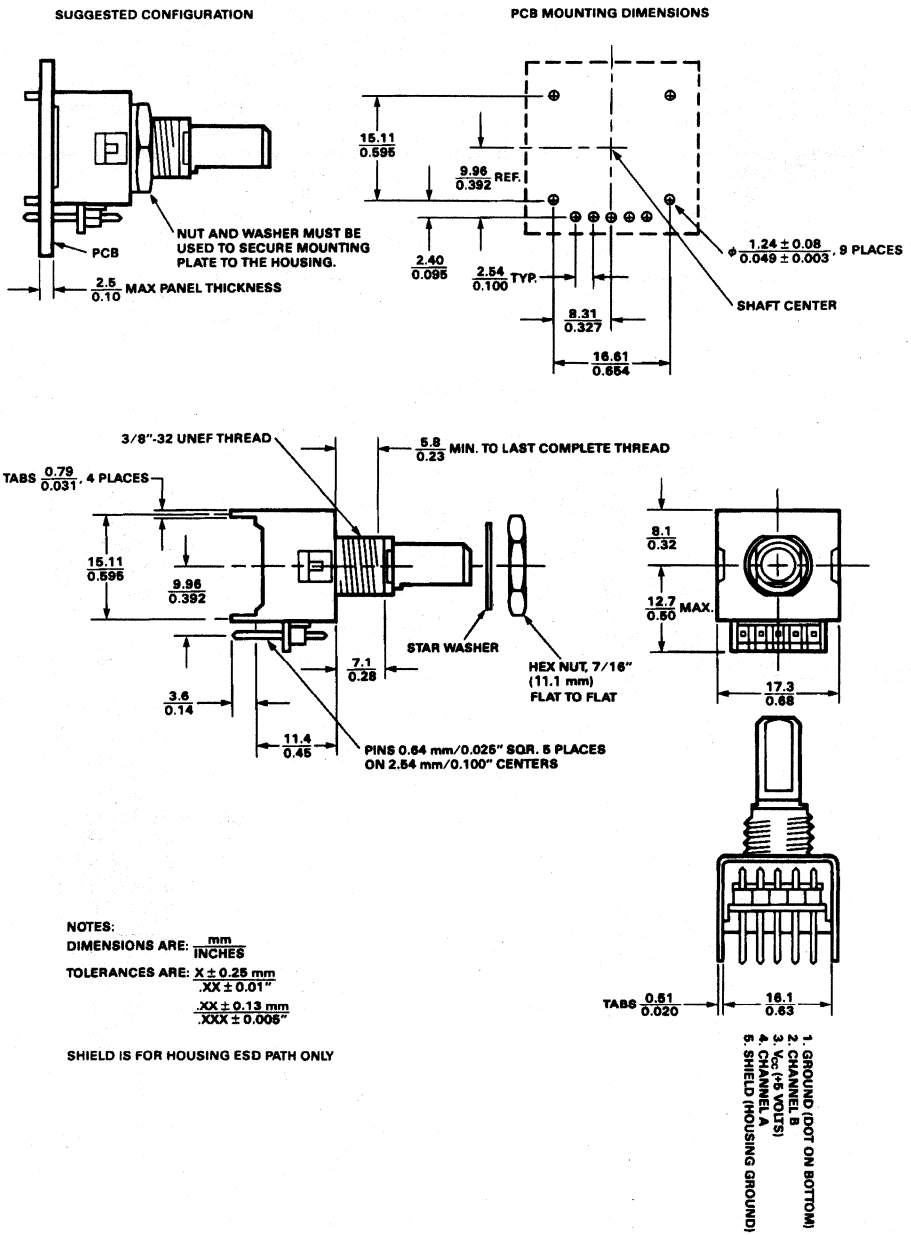
NOTES:
$360°e = \frac{360° \text{ MECH.}}{CPR}$

CHANNEL A LEADS CHANNEL B FOR CLOCKWISE ROTATION
CHANNEL B LEADS CHANNEL A FOR COUNTERCLOCKWISE ROTATION
1. FOR HRPG-ADXX #XXX THE NOMINAL DETENT POSITION IS CENTERED AROUND LOW-LOW STATE (CHA = 0, CHB = 0).
2. DETENT POSITION WILL LIE WITHIN THESE BOUNDARIES, NEVER IN HIGH-HIGH STATE (CHA = 1, CHB = 1).

Mechanical Configurations

Termination Options

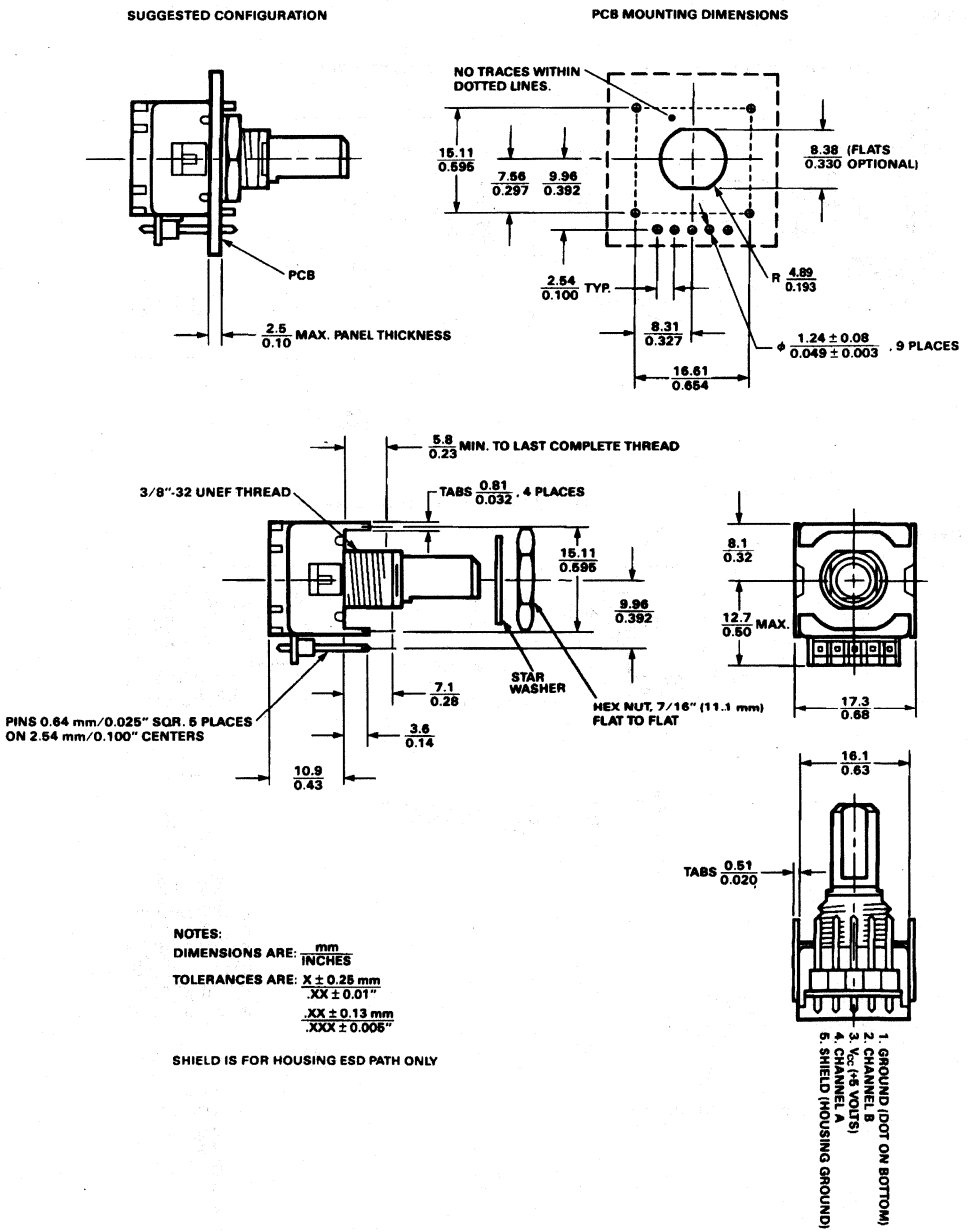
Option R – Pins Rear with Bracket
HRPG-AXXX#XXR



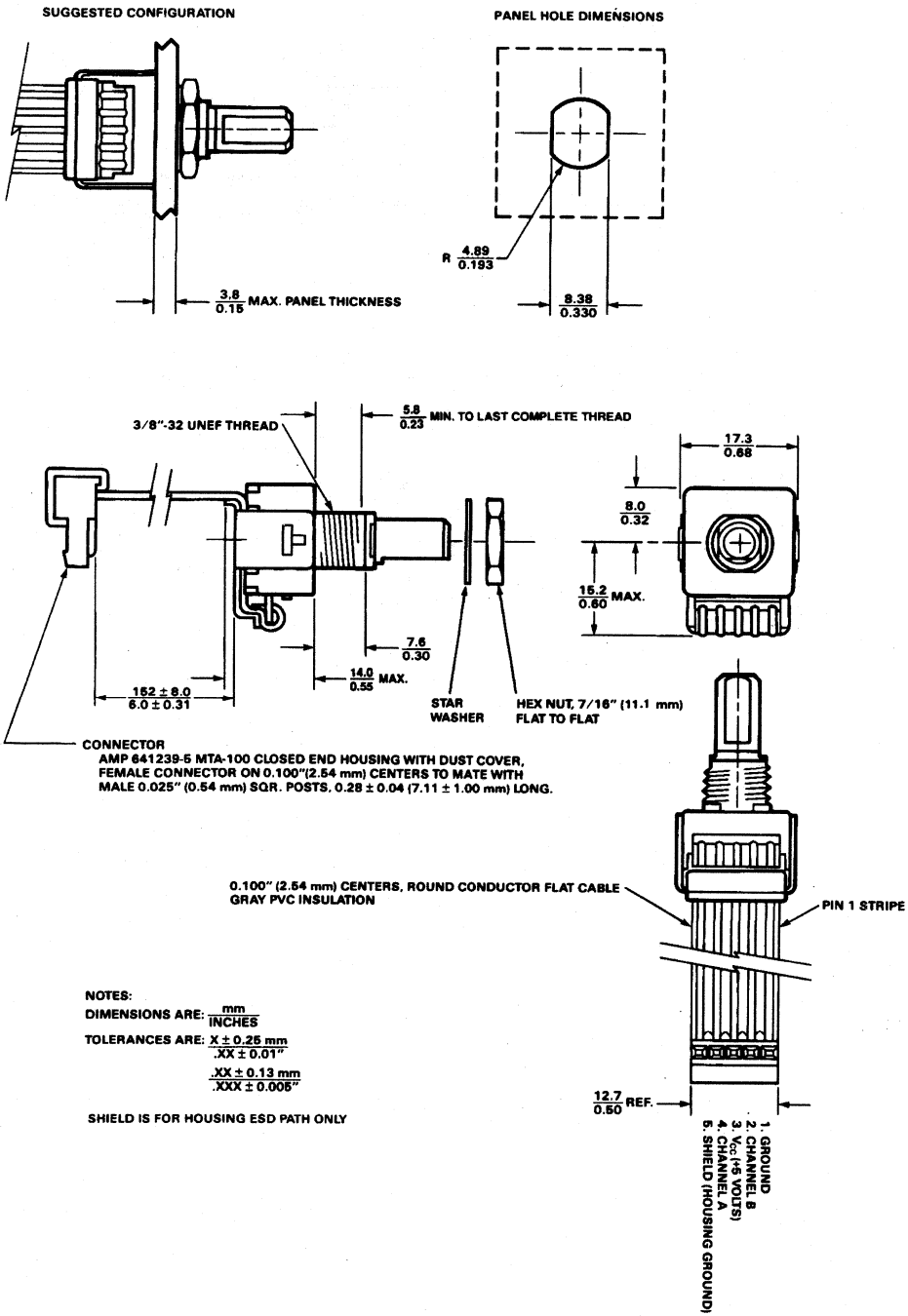
NOTES:
DIMENSIONS ARE: mm / INCHES
TOLERANCES ARE: X ± 0.25 mm / .XX ± 0.01"
.XX ± 0.13 mm / .XXX ± 0.005"

SHIELD IS FOR HOUSING ESD PATH ONLY

Option F – Pins Front with Bracket
HRPG-AXXX#XXF



Option C – Cable Connector with Strain Relief
HRPG-AXXX#XXC

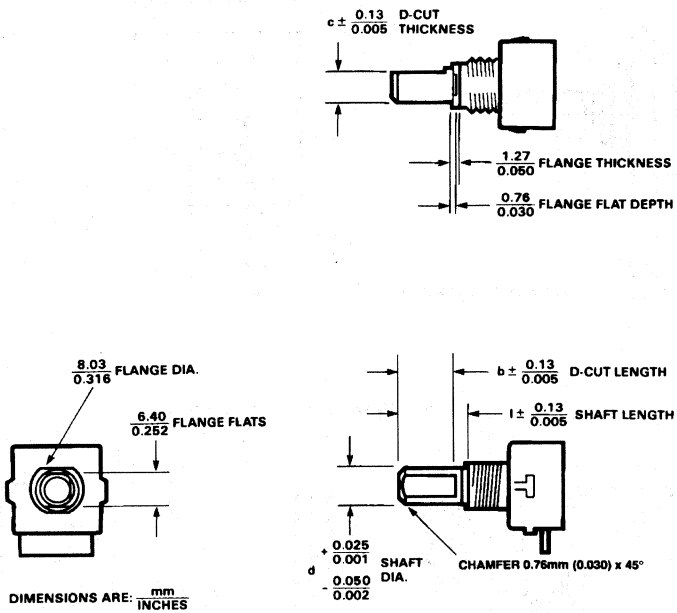


NOTES:
DIMENSIONS ARE: mm / INCHES
TOLERANCES ARE: X ± 0.25 mm / .XX ± 0.01"
.XX ± 0.13 mm / .XXX ± 0.005"

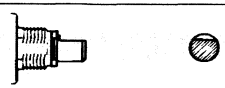
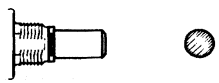
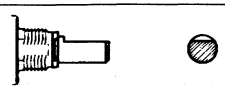
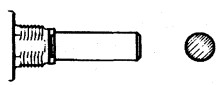
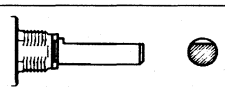
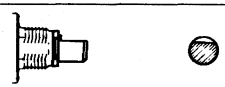
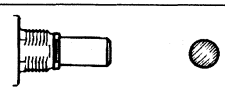
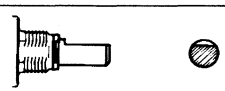
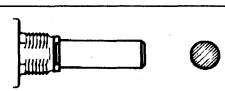
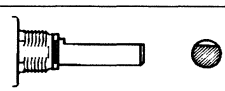
SHIELD IS FOR HOUSING ESD PATH ONLY

Shaft Configurations

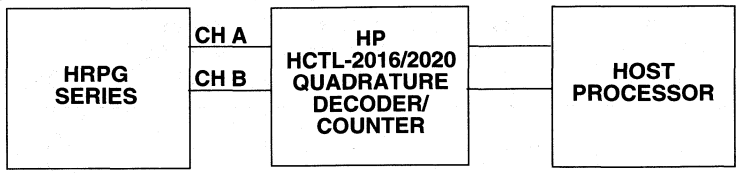
Shaft Dimensions (D-cut shown also)



Shaft Options Available

Option #	Shaft Length (l)	Shaft Diameter (d)	D-Cut Thickness (c)	D-Cut Length (b)	Sketch (not to scale)
11	0.30"	0.251"	–	–	
13	0.30"	0.250"	0.225"	0.230"	
14	0.50"	0.251"	–	–	
16	0.50"	0.250"	0.225"	0.400"	
17	0.80"	0.251"	–	–	
19	0.80"	0.250"	0.225"	0.700"	
51	7.6 mm	6.02 mm	–	–	
53	7.6 mm	6.00 mm	5.33 mm	5.84 mm	
54	12.7 mm	6.02 mm	–	–	
56	12.7 mm	6.00 mm	5.33 mm	10.16 mm	
57	20.32 mm	6.02 mm	–	–	
59	20.32 mm	6.00 mm	5.33 mm	17.78 mm	

Typical Interface



Ordering Information

HRPG - A ☐☐☐ **#** ☐☐☐

Shaft Feel / Resolution

S16 – Smooth 16CPR
D16 – Detented 16CPR*
S32 – Smooth 32CPR
D32 – Detented 32CPR*
S64 – Smooth 64CPR
SCA – Smooth 120CPR

Mechanical Configuration

11 – 0.3" long, 0.25" dia.
13 – 0.3" long, 0.25" dia. D-cut
14 – 0.5" long, 0.25" dia.
16 – 0.5" long, 0.25" dia. D-cut
17 – 0.8" long, 0.25" dia.
19 – 0.8" long, 0.25" dia. D-cut
51 – 7.6 mm long, 6 mm dia.
53 – 7.6 mm long, 6 mm dia. D-cut
54 – 12.7 mm long, 6 mm dia.
56 – 12.7 mm long, 6 mm dia. D-cut
57 – 20.3 mm long, 6 mm dia.
59 – 20.3 mm long, 6 mm dia. D-cut

Termination

F – Pins Front with Bracket
R – Pins Rear with Bracket
C – Cable Connector with Strain Relief
L - Flying Leads with Strain Relief

*Note: When ordering detented versions, a D-cut shaft is recommended.

HEWLETT® PACKARD

Two and Three Channel Codewheels for use with HP Optical Encoder Modules

Technical Data

HEDS-51X0/61X0 Series
HEDG-512X/612X Series
HEDM-512X/61XX Series

Features:

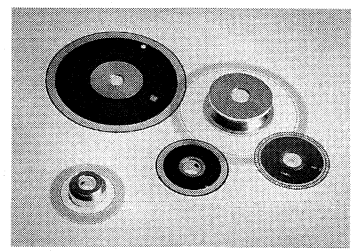
- **Codewheels Available in Glass, Film, and Metal**
- **Available in Two Standard Diameters**
- **Cost Effective**
- **Resolutions from 96 CPR to 2048 CPR**
- **For Use with HEDS-90XX/ 91XX Series Two and Three Channel Encoders**

Description

Hewlett-Packard offers a wide variety of codewheels for use with Hewlett-Packard's HEDS-9000, HEDS-9100, HEDS-9040, and HEDS-9140 series Encoder Modules. Designed for many environments, applications, and budgets, HP codewheels are available in Glass, Film, and Metal. These codewheels are available in resolutions from 96 Counts Per Revolution (CPR) to 1024 CPR on an 11 mm optical radius and 500 to 2048 CPR on a 23.36 mm optical radius.

Each of the three codewheel materials offers a certain advantage. Metal codewheels are the most versatile, with a temperature rating up to 100°C, resolution to 512 CPR (28 mm diameter), as well as 2 and 3 channel outputs. Film codewheels offer higher resolution (up to 1024 CPR on a 28 mm diameter) with an operating temperature of 70°C. Glass codewheels combine the best of film and metal, offering a temperature rating of 100°C and resolutions to 1024 CPR on a 28 mm diameter.

In addition, each material offers a specific reliability rating. It is important to consider the specific application operating environment, long term operating conditions, and temperature ranges when choosing a codewheel material.



Also See:

- HEDS-9000/HEDS-9100 Encoder Module Data Sheet
- HEDS-9000/9100/9200 Extended Resolution Encoder Module Data Sheet
- HEDS-9040/9140 Three Channel Encoder Module Data Sheet
- HEDS-9700 Small Encoder Module Data Sheet

Absolute Maximum Ratings

It is important to consider the environment in which the codewheels will be used when selecting a codewheel material. In brief, metal codewheels are rugged, but do not offer higher resolution capabilities. Film codewheels allow higher resolution, but cannot endure the same temperatures and high humidity as metal. Glass codewheels offer both high temperature and higher resolution, but are also more expensive. Consider the following rating table when choosing a codewheel material.

Parameter	Symbol	HEDS-XXXX Metal Codewheels	HEDM-XXXX Film Codewheels	HEDG-XXXX Glass Codewheels
Storage Temperature	T_S	-40°C to +100°C	-40°C to +70°C	-40°C to +100°C
Operating Temperature	T_A	-40°C to +100°C	-40°C to +70°C	-40°C to +100°C
Humidity			non condensing	
Velocity		30,000 RPM	30,000 RPM	12,000 RPM
Shaft Axial Play		± 0.25 mm (± 0.010 in)	± 0.175 mm (± 0.007 in)	± 0.175 mm (± 0.007 in)
Shaft Eccentricity Plus Radial Play		± 0.1 mm (± 0.004 in) TIR	± 0.04 mm (± 0.0015 in) TIR	± 0.04 mm (± 0.0015 in) TIR
Acceleration		250,000 Rad/Sec^2	250,000 Rad/Sec^2	100,000 Rad/Sec^2

Recommended Operating Conditions

Parameter	HEDS-XXXX Metal Codewheels	HEDM-XXXX Film Codewheels	HEDG-XXXX Glass Codewheels
Maximum Count Frequency	100 kHz	200 kHz*	200 kHz
Shaft Perpendicularity Plus Axial Play	± 0.25 mm (± 0.010 in)	± 0.175 mm (± 0.007 in)	± 0.175 mm (± 0.007 in)
Shaft Eccentricity Plus Radial Play	± 0.1 mm (± 0.004 in) TIR	± 0.04 mm (± 0.0015 in) TIR	± 0.04 mm (± 0.0015 in) TIR

Note: HP Encoder Modules are guaranteed to 100 kHz, but can operate at higher frequencies. See Encoder Module Data Sheet for specifications and output load recommendations.

*HEDM-6140 is guaranteed to 100 kHz with the HEDS-9040 #T00 module.

Encoding Characteristics

Encoding characteristics over recommended operating range and recommended mounting tolerances unless otherwise specified. Values are for worst error over a full rotation. Please refer to Encoder Module Data Sheet for definitions of Encoding characteristics.

Part Number	Description	Symbol	Min.	Typ.	Max.	Units
HEDS-51XX	Cycle Error Position Error	ΔC Δθ		3 10	5.5 40	°e min. of arc
HEDS-61XX	Cycle Error Position Error	ΔC Δθ		3 7	5.5 20	°e min. of arc
HEDM-512X	Cycle Error Position Error	ΔC Δθ		3 4	7.5 40	°e min. of arc
HEDM-61XX	Cycle Error Position Error	ΔC Δθ		3 2	7.5 20	°e min. of arc
HEDG-512X	Cycle Error Position Error	ΔC Δθ		3 4	7.5 30	°e min. of arc
HEDG-612X	Cycle Error Position Error	ΔC Δθ		3 2	7.5 15	°e min. of arc

Reliability

In addition to the absolute maximum specifications of codewheels, the environment characteristics of the application are also important. For example, consistent, large temperature swings over the life of the product will affect the codewheel performance characteristics depending on the material. The following reliability table shows results of lifetests under varying conditions of temperature and humidity.

Glass Codewheel Tests

Test	Duration	Number of Parts	Number of Failures
Storage at 100°C	1000 hours	44	0
Rotating at 100°C	500 hours	10	0
Temperature Cycle: -40°C to +100°C	500 cycles	98	0
Temperature/Humidity: 85°C/85% R.H.	500 hours	43	0

Film Codewheel Tests

Test	Duration	Number of Parts	Number of Failures
Storage at 70°C	1000 hours	118	0
Rotating at 70°C	500 hours	10	0
Temperature Cycle: -40°C to +70°C	500 cycles	66	0
Temperature Cycle: +20°C to +40°C	1000 cycles	64	0
Temperature Cycle: +20°C to +55°C	1000 cycles	46	0
Temperature Cycle: +20°C to +70°C	500 cycles	50	0

Mounting Rotary Encoders with Codewheels

There are two orientations for mounting the HP encoder module and HP codewheel. Figure 1a shows mounting the module with side A as the mounting plane.

Figure 1b shows mounting the module with side B as the mounting plane. When assembling the encoder and codewheel, it is important to maintain the tolerances of Side A of the module, and the image side of the codewheel. See module Data Sheets for these tolerances.

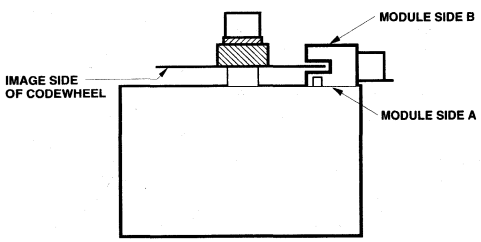


Figure 1a.

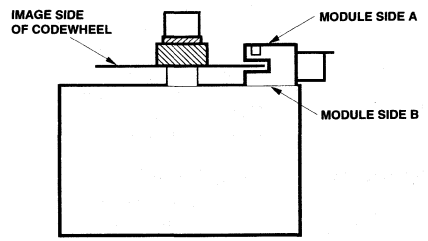


Figure 1b.

*Please note that the image side of the codewheel must always be facing the module Side A.

Mounting with Module Side A as the Mounting Plane

Mounting a high resolution or three channel encoder with Module Side A as the mounting plane requires alignment pins in the motor base. These alignment pins provide the necessary centering of the module with respect to the center of the motor shaft. In addition to centering, the codewheel gap is also important. Please refer to the respective encoder data sheet for necessary mounting information.

Mounting with Module Side B as the Mounting Plane, using HP Assembly Tools

Hewlett-Packard offers centering tools and gap setting tools only for the case when the module is mounted with Side B down. Please refer to the Ordering Information Table to choose the correct assembly tools.

Assembly Instructions Using HP Assembly Tools

Instructions

1. Place codewheel on shaft.
2. Set codewheel height:
   (a) Place the correct gap setting tool (per Ordering Information Table) on motor base, flush up against the motor shaft as shown in Figure 2. The shim has two different size steps. Choose the one that most closely matches the width of the codewheel boss. The shim should not contact the codewheel boss.
   (b) Push codewheel down against gap setting shim. The codewheel is now at the proper height.
   (c) Tighten codewheel setscrew.
3. Insert mounting screws through module and thread into the motor base. Do not tighten screws.
4. Slide the HEDS-8905 or HEDS-8906 centering tool over codewheel hub and onto module as shown in Figure 3. The pins of the alignment tool should fit snugly inside the alignment recesses of the module.
5. While holding alignment tool in place, tighten screws down to secure module.
6. Remove alignment tools.

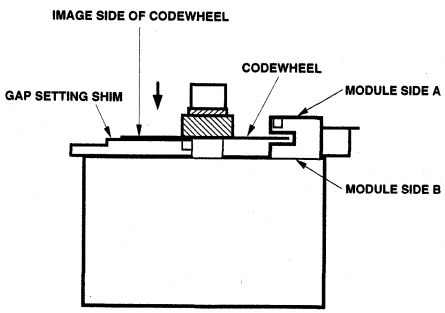


Figure 2. Alignment Tool is Used to Set Height of Codewheel.

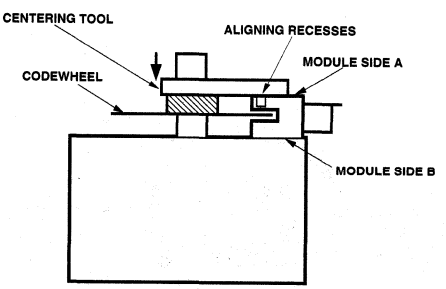


Figure 3. Alignment Tool is Placed over Shaft and onto Codewheel Hub. Alignment Tool Pins Mate with Aligning Recesses on Module.

Mechanical Drawings

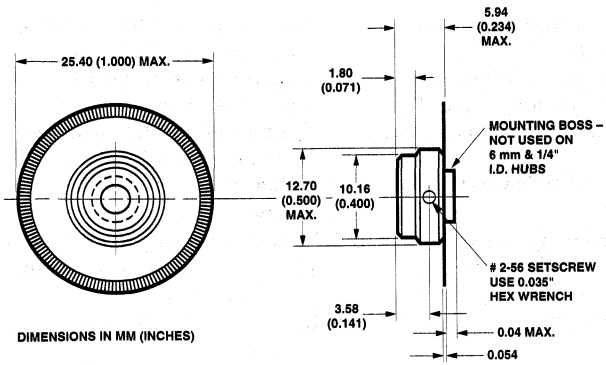


Figure 4. HEDS-5120 Codewheel.

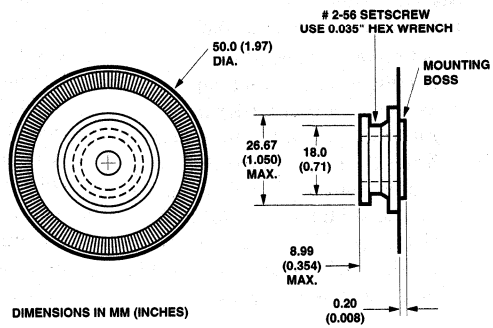


Figure 5. HEDS-6100 Codewheel.

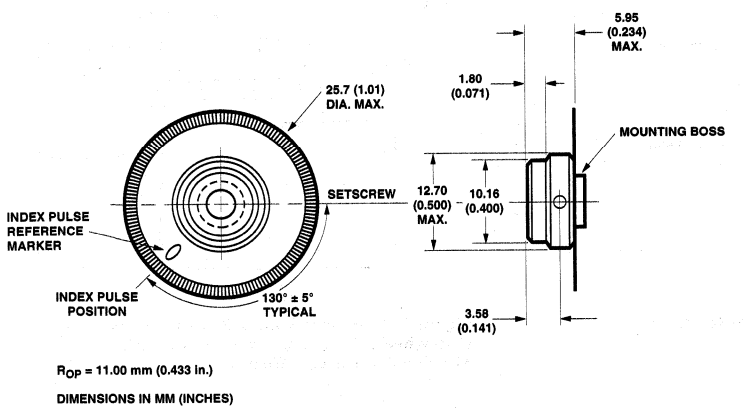


Figure 6. HEDS-5140 Codewheel Used with HEDS-9140.

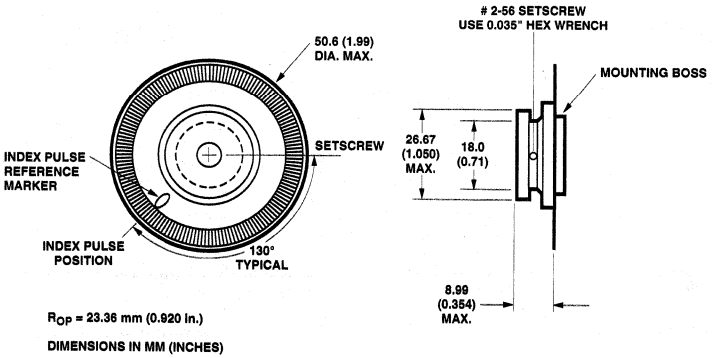


Figure 7. HEDS-6140 Codewheel Used with HEDS-9040.

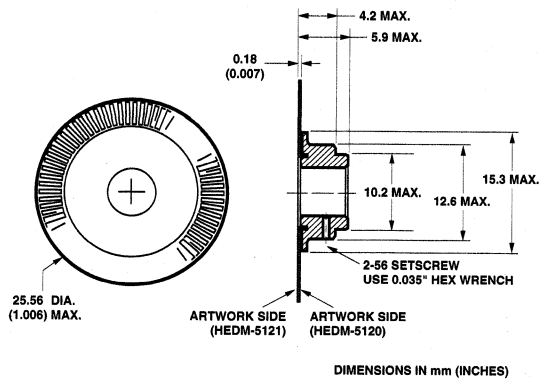


Figure 8. HEDM-5120 Codewheel/HEDM-5121 Codewheel.

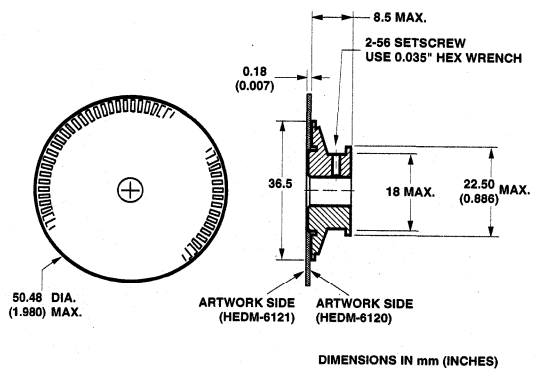


Figure 9. HEDM-6120 Codewheel/HEDM-6121 Codewheel.

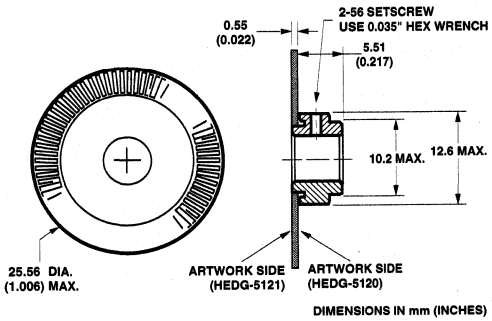


Figure 10. HEDG-5120 Codewheel/HEDG-5121 Codewheel.

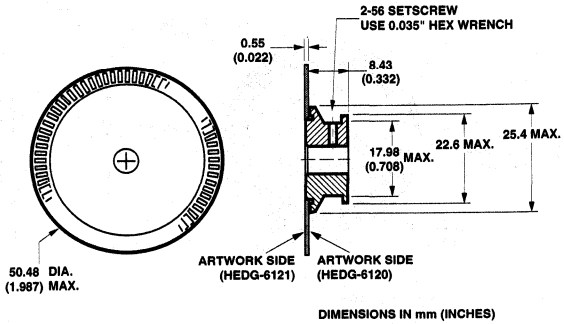


Figure 11. HEDG-6120 Codewheel/HEDG-6121 Codewheel.

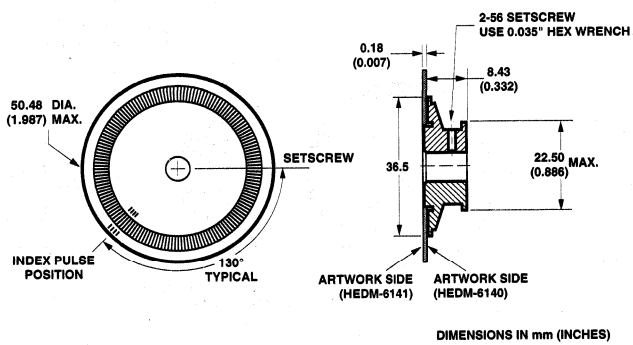


Figure 12. HEDM-6140 Codewheel/HEDM-6141 Codewheel.

Ordering Information Encoder Modules, Codewheel and Assembly Tools

Metal Codewheels

HEDS-9100 option modules □ 0 0 **HEDS-5120 codewheels** **Option** □ □□ **Rop = 11 mm, 2 channels**

Resolution (Cycles/Rev)
S - 50 CPR
K - 96 CPR
C - 100 CPR
D - 192 CPR
E - 200 CPR
F - 256 CPR
G - 360 CPR
H - 400 CPR
A - 500 CPR
I - 512 CPR

Shaft Diameter
01 - 2 mm
02 - 3 mm
03 - 1/8 in.
04 - 5/32 in.
05 - 3/16 in.
06 - 1/4 in.
11 - 4 mm
14 - 5 mm
12 - 6 mm
13 - 8 mm

Assembly Tools	
Centering	Gap-Setting
HEDS-8905	HEDS-8901

HEDS-9140 option modules □ 0 0 **HEDS-5140 codewheels** **Option** □ □□ **Rop = 11 mm, 3 channels**

Resolution (Cycles/Rev)
S - 50 CPR
K - 96 CPR
C - 100 CPR
E - 200 CPR
F - 256 CPR
G - 360 CPR
H - 400 CPR
A - 500 CPR
I - 512 CPR

Shaft Diameter
01 - 2 mm
02 - 3 mm
03 - 1/8 in.
04 - 5/32 in.
05 - 3/16 in.
06 - 1/4 in.
11 - 4 mm
14 - 5 mm
12 - 6 mm
13 - 8 mm

Assembly Tools	
Centering	Gap-Setting
HEDS-8905	HEDS-8905

HEDS-9000 option modules □ 0 0 **HEDS-6100 codewheels** **Option** □ □□ **Rop = 23 mm, 2 channels**

Resolution (Cycles/Rev)
A - 500 CPR
B - 1000 CPR

Shaft Diameter
05 - 3/16 in.
06 - 1/4 in.
07 - 5/16 in.
08 - 3/8 in.
09 - 1/2 in.
10 - 5/8 in.
11 - 4 mm
12 - 6 mm
13 - 8 mm

Assembly Tools	
Centering	Gap-Setting
HEDS-8906	HEDS-8901

Ordering Information (Cont'd.)

HEDS-9040 option modules □ 0 0 **HEDS-6140 codewheels** **Option** □ □□ **Rop = 23 mm, 3 channels**

Resolution (Cycles/Rev)
B - 1000 CPR
J - 1024 CPR

Shaft Diameter
05 - 3/16 in.
06 - 1/4 in.
07 - 5/16 in.
08 - 3/8 in.
09 - 1/2 in.
10 - 5/8 in.
11 - 4 mm
12 - 6 mm
13 - 8 mm

Assembly Tools	
Centering	Gap-Setting
HEDS-8906	HEDS-8906

Note:
1. For the lower resolution, two channel encoders, (11 mm ≤ 512 CPR; 23 mm ≤ 1024 CPR) the centering tool and gap-settting shim are not necessary, but sometimes helpful in an assembly process.

Film Codewheels

HEDS-9100 modules option □ 0 0 **HEDM-512 codewheels option** □ □□ **Rop = 11 mm, 2 channels**

Resolution (Cycles/Rev)
B - 1000 CPR
J - 1024 CPR

Artwork Orientation
0 - Artwork on hub side (Use when module side B is down)
1 - Artwork opposite hub side (use when module side A is down)

Shaft Diameter
01 - 2 mm
02 - 3 mm
03 - 1/8 in.
04 - 5/32 in.
05 - 3/16 in.
06 - 1/4 in.
11 - 4 mm
14 - 5 mm
12 - 6 mm
13 - 8 mm

Assembly Tools	
Centering	Gap-Setting
HEDS-8905	HEDS-8901

Ordering Information (Cont'd.)

HEDS-9000 modules option ☐ 0 0

HEDM-612 codewheels option ☐ ☐☐

Rop = 23 mm, 2 channels

Assembly Tools

Centering	Gap-Setting
HEDS-8906	HEDS-8906

Resolution (Cycles/Rev)	Artwork Orientation	Shaft Diameter
T - 2000 CPR U - 2048 CPR	0 - Artwork on hub side (Use when module side B is down) 1 - Artwork opposite hub side (use when module side A is down)	05 - 3/16 in. 06 - 1/4 in. 07 - 5/16 in. 08 - 3/8 in. 09 - 1/2 in. 10 - 5/8 in. 11 - 4 mm 12 - 6 mm 13 - 8 mm

HEDS-9040 modules option ☐ 0 0

HEDM-614 codewheels option ☐ ☐☐

Rop = 23 mm, 3 channels

Assembly Tools

Centering	Gap-Setting
HEDS-8906	HEDS-8906

Resolution (Cycles/Rev)	Artwork Orientation*	Shaft Diameter
T - 2000 CPR	0 - Artwork on hub side (Use when module side B is down) 1 - Artwork opposite hub side (use when module side A is down)	05 - 3/16 in. 06 - 1/4 in. 07 - 5/16 in. 08 - 3/8 in. 09 - 1/2 in. 10 - 5/8 in. 11 - 4 mm 12 - 6 mm 13 - 8 mm

*Index will not work if wrong orientation is used.

Ordering Information (Cont'd.)

Glass Codewheels

HEDS-9100 modules option □ 0 0

HEDG-512 codewheels option □ □□

Rop = 11 mm, 2 channels

Assembly Tools

Centering	Gap-Setting
HEDS-8905	HEDS-8932

Resolution (Cycles/Rev)	Artwork Orientation	Shaft Diameter
B - 1000 CPR J - 1024 CPR	0 - Artwork on hub side (Use when module side B is down) 1 - Artwork opposite hub side (use when module side A is down)	01 - 2 mm 02 - 3 mm 03 - 1/8 in. 04 - 5/32 in. 05 - 3/16 in. 06 - 1/4 in. 11 - 4 mm 14 - 5 mm 12 - 6 mm 13 - 8 mm

HEDS-9000 modules option □ 0 0

HEDG-612 codewheels option □ □□

Rop = 23 mm, 2 channels

Assembly Tools

Centering	Gap-Setting
HEDS-8906	HEDS-8932

Resolution (Cycles/Rev)	Artwork Orientation	Shaft Diameter
T - 2000 CPR U - 2048 CPR	0 - Artwork on hub side (Use when module side B is down) 1 - Artwork opposite hub side (use when module side A is down)	05 - 3/16 in. 06 - 1/4 in. 07 - 5/16 in. 08 - 3/8 in. 09 - 1/2 in. 10 - 5/8 in. 11 - 4 mm 12 - 6 mm 13 - 8 mm

HEWLETT® PACKARD

General Purpose Motion Control ICs

Technical Data

HCTL-1100 Series

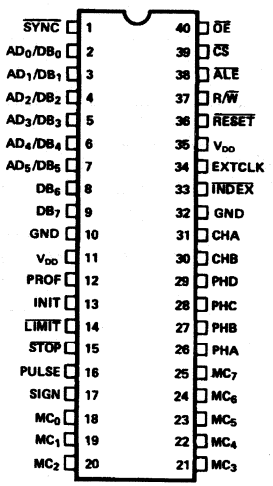
Features

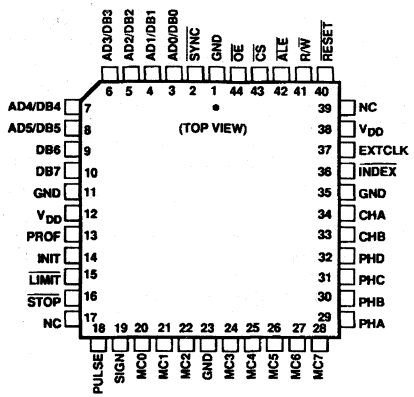
- **Low Power CMOS**
- **PDIP and PLCC Versions Available**
- **Enhanced Version of the HCTL-1000**
- **DC, DC Brushless, and Step Motor Control**
- **Position and Velocity Control**
- **Programmable Digital Filter and Commutator**
- **8-Bit Parallel, and PWM Motor Command Ports**
- **TTL Compatible**
- **SYNC Pin for Coordinating Multiple HCTL-1100 ICs**
- **100 kHz to 2 MHz Operation**
- **Encoder Input Port**

Description

The HCTL-1100 series is a high performance, general purpose motion control IC, fabricated in HP CMOS technology. It frees the host processor for other tasks by performing all the time-intensive functions of digital motion control. The programmability of all control parameters provides maximum flexibility and quick design of control systems with a minimum number of components. In addition to the HCTL-1100, the complete control system consists of a host processor to specify commands, an amplifier, and a motor with an incremental encoder (such as the HP HEDS-5XXX, -6XXX, -9XXX series). No analog compensation or velocity feedback is necessary.

Pinouts





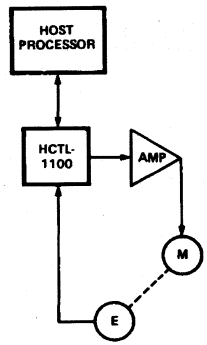
ESD WARNING: NORMAL HANDLING PRECAUTIONS SHOULD BE TAKEN TO AVOID STATIC DISCHARGE.

Applications

Typical applications for the HCTL-1100 include printers, medical instruments, material handling machines, and industrial automation.

HCTL-1100 vs. HCTL-1000

The HCTL-1100 is designed to replace the HCTL-1000. Some differences exist, and some enhancements have been added.

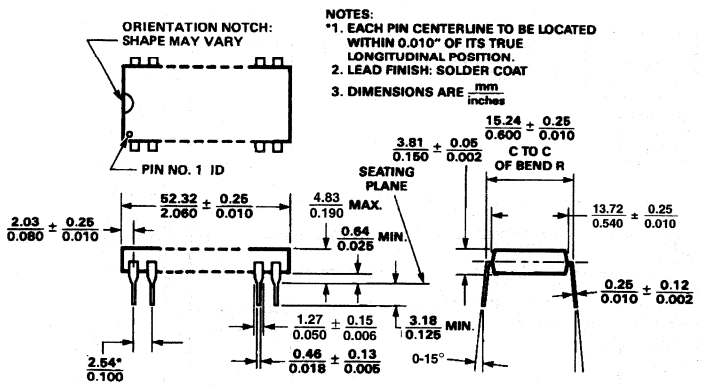


System Block Diagram

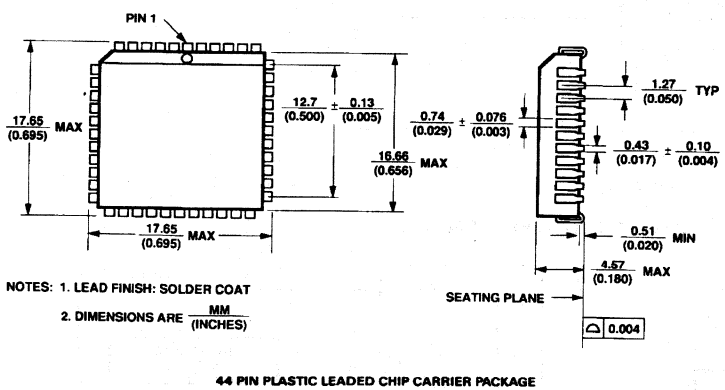
Comparison of HCTL-1100 and HCTL-1000

Description	HCTL-1100	HCTL-1000
Max. Supply Current	30 mA	180 mA
Max. Power Dissipation	165 mW	950 mW
Max. Tri-State Output Leakage Current	150 nA	10 µA
Operating Frequency	100 kHz-2 MHz	1 MHz-2 MHz
Operating Temperature Range	-20°C to +85°C	0°C to 70°C
Storage Temperature Range	-55°C to +125°C	-40°C to +125°C
Synchronize 2 or More ICs	Yes	–
Preset Actual Position Registers	Yes	–
Read Flag Register	Yes	–
Limit and Stop Pins	Must be pulled up to V_{DD} if not used.	Can be left floating if not used.
Hard Reset	Required	Recommended
PLCC Package Available	Yes	–

Package Dimensions



40-PIN PLASTIC DUAL INLINE PACKAGE



44 PIN PLASTIC LEADED CHIP CARRIER PACKAGE

Theory of Operation

The HCTL-1100 is a general purpose motor controller which provides position and velocity control for DC, DC brushless and stepper motors. The internal block diagram of the HCTL-1100 is shown in Figure 1. The HCTL-1100 receives its input commands from a host processor and position feedback from an incremental encoder with quadrature output. An 8-bit bi-directional multiplexed address/data bus interfaces the HCTL-1100 to the host processor. The encoder feedback is decoded into quadrature counts and a 24-bit counter keeps track of position. The HCTL-1100 executes any one of four control algorithms selected by the user. The four control modes are:

- Position Control
- Proportional Velocity Control
- Trapezoidal Profile Control for point to point moves
- Integral Velocity Control with continuous velocity profiling using linear acceleration

The resident Position Profile Generator calculates the necessary profiles for Trapezoidal Profile Control and Integral Velocity Control. The HCTL-1100 compares the desired position (or velocity) to the actual position (or velocity) to compute compensated motor commands using a programmable digital filter D(z). The motor command is externally available at the Motor Command port as an 8-bit byte and at the PWM port as a Pulse Width Modulated (PWM) signal.

The HCTL-1100 has the capability of providing electronic commutation for DC brushless and stepper motors. Using the encoder position information, the motor phases are enabled in the correct sequence. The commutator is fully programmable to encompass most motor/encoder combinations. In addition, phase overlap and phase advance can be programmed to improve torque ripple and high speed performance. The HCTL-1100 contains a number of flags including two externally available flags, Profile and Initialization, which allow the user to see or check the status of the controller. It also has two emergency inputs, Limit and Stop, which allow operation of the HCTL-1100 to be interrupted under emergency conditions.

The HCTL-1100 controller is a digitally sampled data system. While information from the host processor is accepted asynchronously with respect to the control functions, the motor command is computed on a discrete sample time basis. The sample timer is programmable.

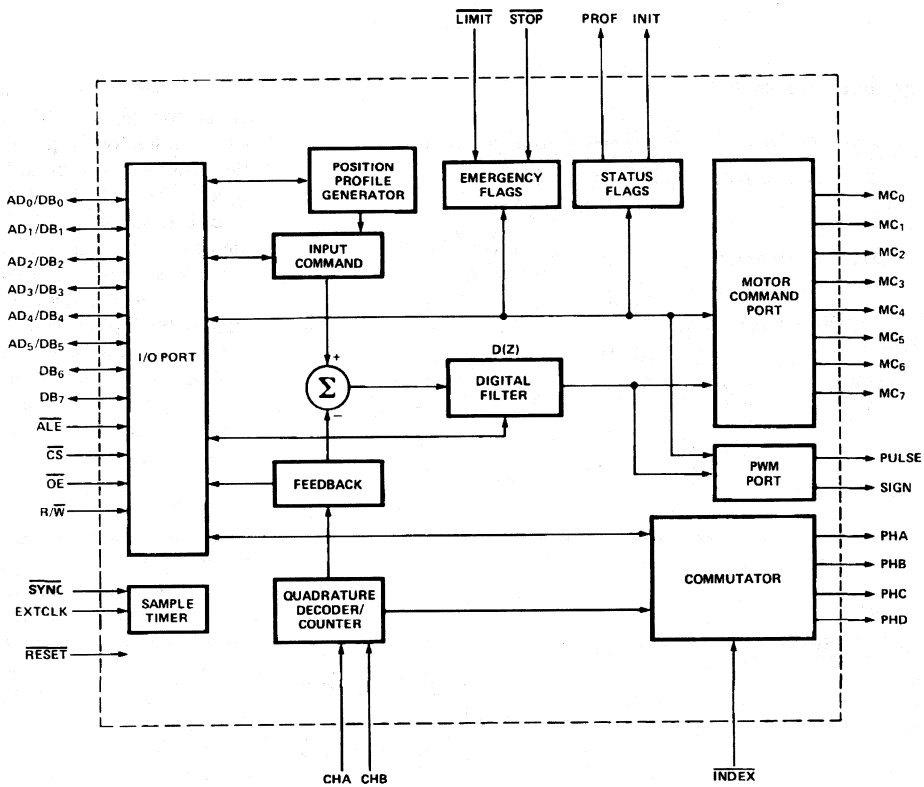


Figure 1. Internal Block Diagram.

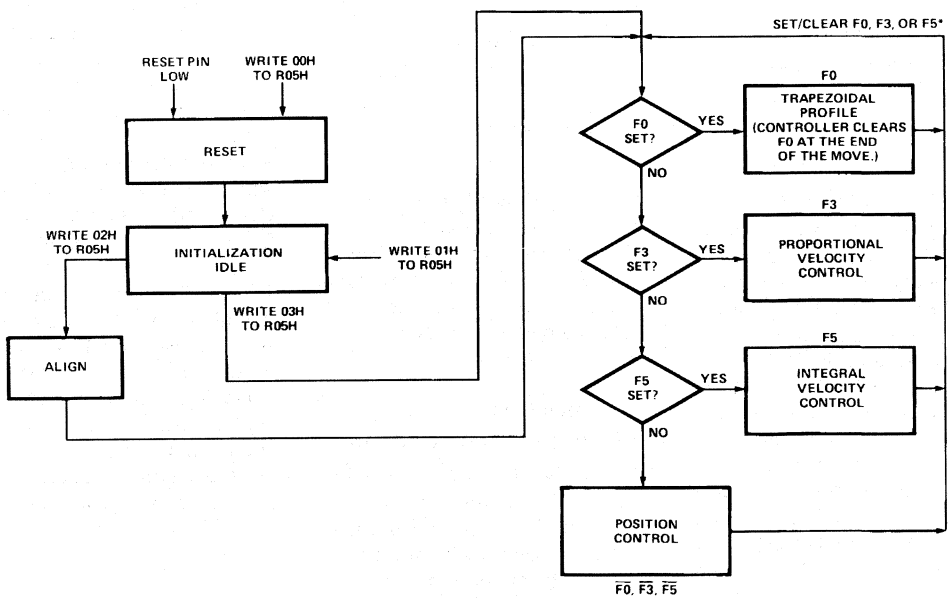


Figure 2. Operating Mode Flowchart.

Electrical Specifications

Absolute Maximum Ratings

Operating Temperature, T_A ..... -20°C to 85°C
Storage Temperature, T_S ..... -55°C to 125°C
Supply Voltage, V_{DD} ..... -0.3 V to 7 V
Input Voltage, V_{IN} ..... -0.3 V to V_{DD} +0.3 V
Maximum Operating Clock Frequency, f_{CLK} ..... 2 MHz

DC Electrical Characteristics

V_{DD} = 5 V ± 5%; T_A = -20°C to +85°C

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Supply Voltage	V_{DD}	4.75	5.00	5.25	V	
Supply Current	I_{DD}		15	30	mA	
Input Leakage Current	I_{IN}		10	100	nA	V_{IN} = 0.00 and 5.25 V
Input Pull-Up Current						
SYNC PIN	I_{PU}		- 40	± 150	µA	V_{IN} = 0.00 V
Tristate Output Leakage Current	I_{OZ}		10	-150	nA	Sync, LIMIT, STOP pin #35 (PDIP) V_{OUT} = -0.3 to 5.25 V pin #38 (PLCC)
Input Low Voltage	V_{IL}	-0.3		0.8	V	
Input High Voltage	V_{IH}	2.0		V_{DD}	V	
Output Low Voltage	V_{OL}	-0.3		0.4	V	I_{OL} = 2.2 mA
Output High Voltage	V_{OH}	2.4		V_{DD}	V	I_{OH} = -200 µA
Power Dissipation	P_D		75	165	mW	
Input Capacitance	C_{IN}			20	pF	
Output Capacitance	C_{OUT}		100		pF	

AC Electrical Characteristics

V_{DD} = 5 V ± 5%; T_A = -20°C to +85°C; Units = nsec

ID #	Signal	Symbol	Clock Frequency				Formula*	
			2 MHz		1 MHz			
			Min.	Max.	Min.	Max.	Min.	Max.
1	Clock Period (clk)	t_{CPER}	500		1000			
2	Pulse Width, Clock High	t_{CPWH}	230		300			
3	Pulse Width, Clock Low	t_{CPWL}	200		200		200	
4	Clock Rise and Fall Time	t_{CR}		50		50		50
5	Input Pulse Width $\overline{\text{Reset}}$	t_{IRST}	2500		5000		5 clk	
6	Input Pulse Width $\overline{\text{Stop}}$, $\overline{\text{Limit}}$	t_{IP}	600		1100		1 clk + 100 ns	
7	Input Pulse Width $\overline{\text{Index}}$, Index	t_{IX}	1600		3100		3 clk + 100 ns	
8	Input Pulse Width CHA, CHB	t_{IAB}	1600		3100		3 clk + 100 ns	
9	Delay CHA to CHB Transition	t_{AB}	600		1100		1 clk + 100 ns	
10	Input Rise/Fall Time CHA, CHB, Index	t_{IABR}		450		900		900 (clk < 1 MHz)
11	Input Rise/Fall Time $\overline{\text{Reset}}$, $\overline{\text{ALE}}$, $\overline{\text{CS}}$, $\overline{\text{OE}}$, Stop, Limit	t_{IR}		50		50		50
12	Input Pulse Width $\overline{\text{ALE}}$, $\overline{\text{CS}}$	t_{IPW}	80		80		80	
13	Delay Time, $\overline{\text{ALE}}$ Fall to $\overline{\text{CS}}$ Fall	t_{AC}	50		50		50	
14	Delay Time, $\overline{\text{ALE}}$ Rise to $\overline{\text{CS}}$ Rise	t_{CA}	50		50		50	
15	Address Setup Time Before $\overline{\text{ALE}}$ Rise	t_{ASR1}	20		20		20	
16	Address Setup Time Before $\overline{\text{CS}}$ Fall	t_{ASR}	20		20		20	
17	Write Data Setup Time Before $\overline{\text{CS}}$ Rise	t_{DSR}	20		20		20	
18	Address/Data Hold Time	t_H	20		20		20	
19	Setup Time, R/$\overline{\text{W}}$ Before $\overline{\text{CS}}$ Rise	t_{WCS}	20		20		20	
20	Hold Time, R/$\overline{\text{W}}$ After $\overline{\text{CS}}$ Rise	t_{WH}	20		20		20	
21	Delay Time, Write Cycle, $\overline{\text{CS}}$ Rise to $\overline{\text{ALE}}$ Fall	t_{CSAL}	1700		3400		3.4 clk	
22	Delay Time, Read/Write, $\overline{\text{CS}}$ Rise to $\overline{\text{CS}}$ Fall	t_{CSCS}	1500		3000		3 clk	
23	Write Cycle, $\overline{\text{ALE}}$ Fall to $\overline{\text{ALE}}$ Fall For Next Write	t_{WC}	1830		3530		3.7 clk	

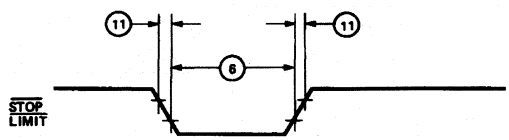
AC Electrical Characteristics (continued).

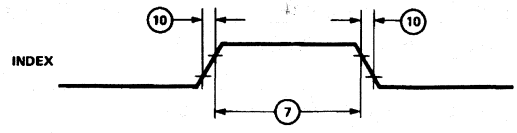
ID #	Signal	Symbol	Clock Frequency				Formula*	
			2 MIIz		1 MHz			
			Min.	Max.	Min.	Max.	Min.	Max.
24	Delay Time, $\overline{CS}$ Rise to $\overline{OE}$ Fall	t_{CSOE}	1700		3200		3 clk + 200 ns	
25	Delay Time, $\overline{OE}$ Fall to Data Bus Valid	t_{OEDB}	100		100		100	
26	Delay Time, $\overline{CS}$ Rise to Data Bus Valid	t_{CSDB}	1800		3300		3 clk + 300 ns	
27	Input Pulse Width $\overline{OE}$	t_{IPWOE}	100		100		100	
28	Hold Time, Data Held After $\overline{OE}$ Rise	t_{DOEH}	20		20		20	
29	Delay Time, Read Cycle, $\overline{CS}$ Rise to $\overline{ALE}$ Fall	t_{CSALR}	1820		3320		3 clk + 320 ns	
30	Read Cycle, $\overline{ALE}$ Fall to $\overline{ALE}$ Fall For Next Read	t_{RC}	1950		3450		3 clk + 450 ns	
31	Output Pulse Width, PROF, INIT, Pulse, Sign, PHA-PHD, MC Port	t_{OF}	500		1000		1 clk	
32	Output Rise/Fall Time, PROF, INIT, Pulse, Sign, PHA-PIID, MC Port	t_{OR}	20	150	20	150	20	150
33	Delay Time, Clock Rise to Output Rise	t_{EP}	20	300	20	300	20	300
34	Delay Time, $\overline{CS}$ Rising to MC Port Valid	t_{CSMC}		1600		3200		3.2 clk
35	Hold Time, $\overline{ALE}$ High After $\overline{CS}$ Rise	t_{ALH}	100		100		100	
36	Pulse Width, $\overline{ALE}$ High	t_{ALPWH}	100		100		100	
37	Pulse Width, $\overline{SYNC}$ Low	t_{SYNC}	9000		18000		18 clk	

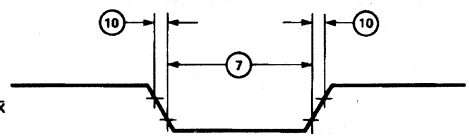
*General formula for determining AC characteristics for other clock frequencies (clk), between 100 kHz and 2 MHz.

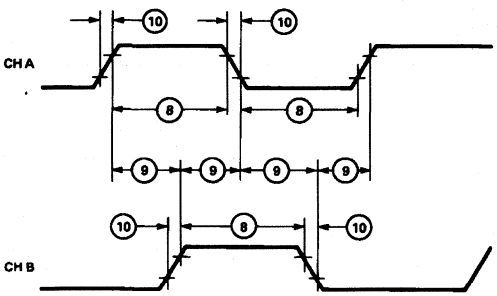
HCTL-1100 I/O Timing Diagrams

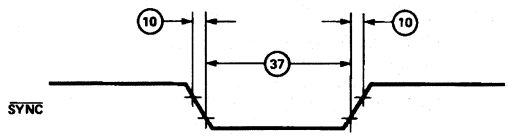
Input logic level values are the TTL Logic levels V_{IL} = 0.8 V and V_{IH} = 2.0 V. Output logic levels are V_{OL} = 0.4 V and V_{OH} = 2.4 V.

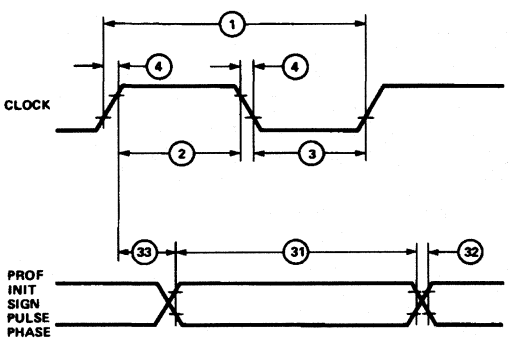


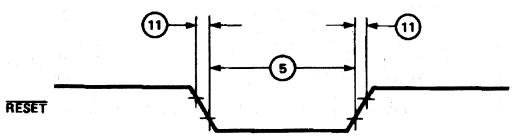










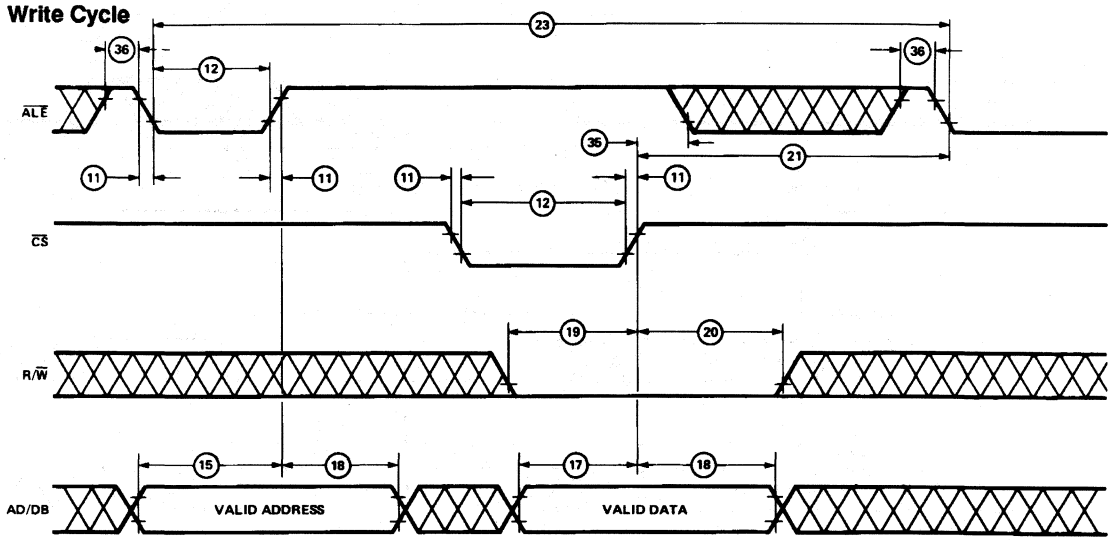


HCTL-1100 I/O Timing Diagrams

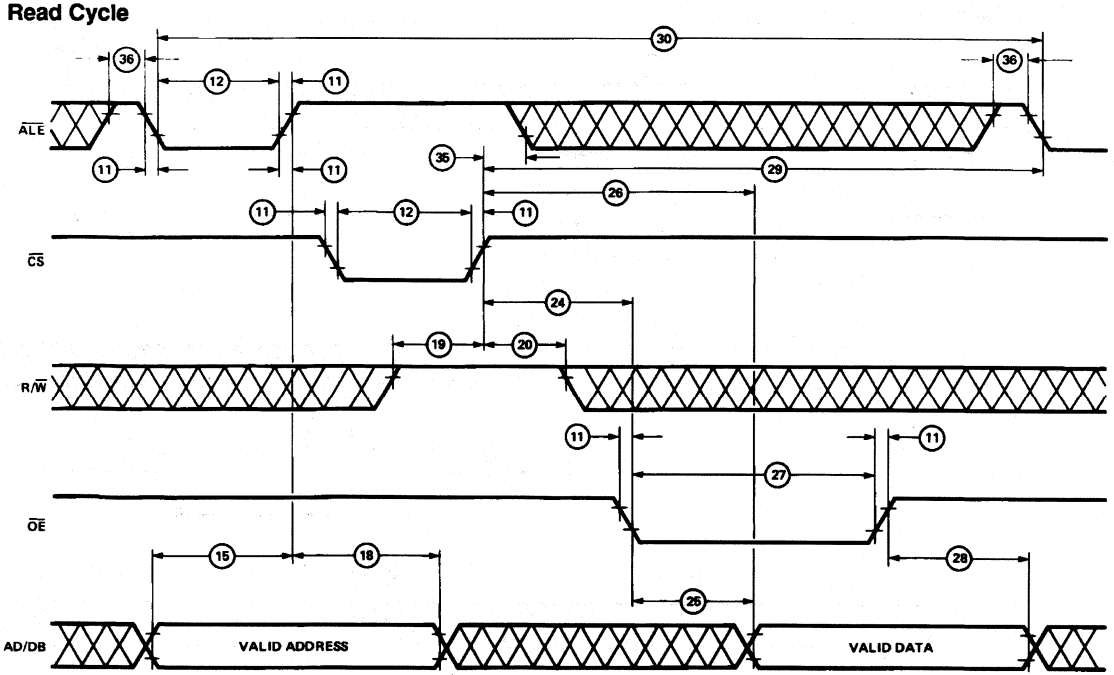
There are three different timing configurations which can be used to give the user flexibility to interface the HCTL-1100 to most microprocessors. See the I/O interface section for more details.

$\overline{ALE}/\overline{CS}$ NON OVERLAPPED

Write Cycle



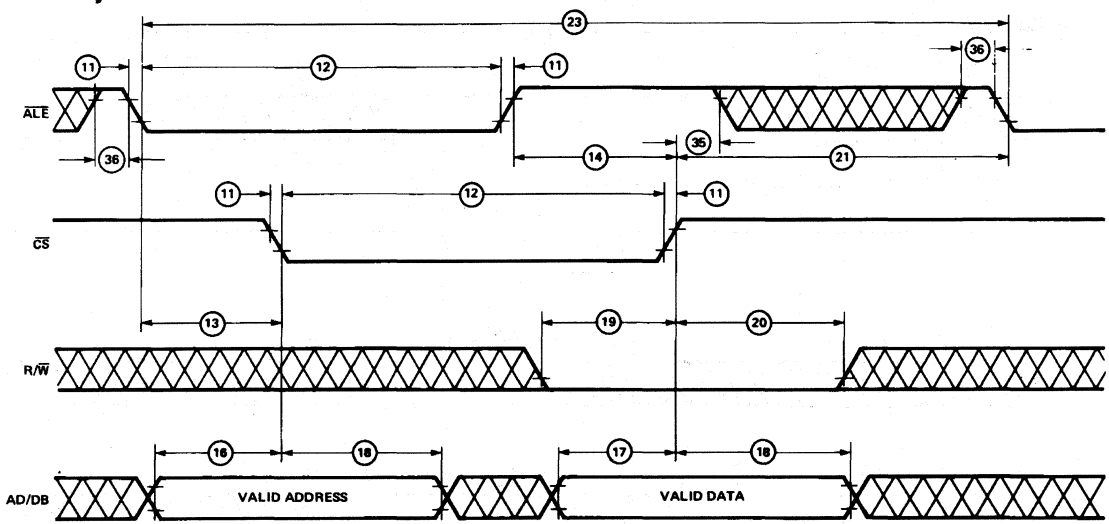
Read Cycle



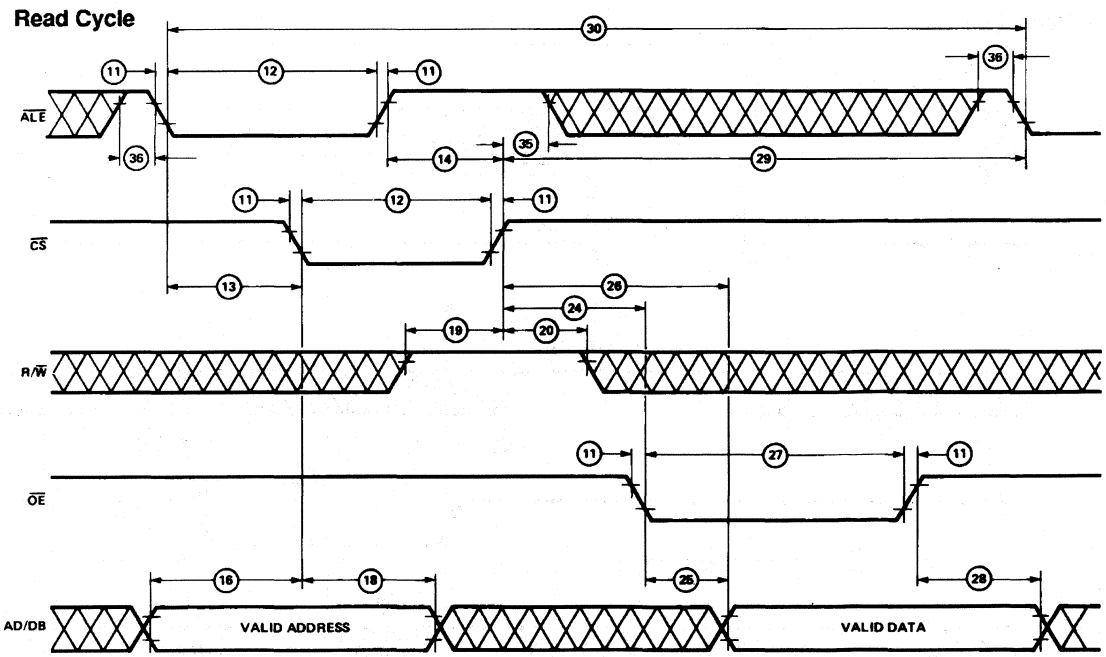
HCTL-1100 I/O Timing Diagrams

$\overline{ALE}/\overline{CS}$ OVERLAPPED

Write Cycle



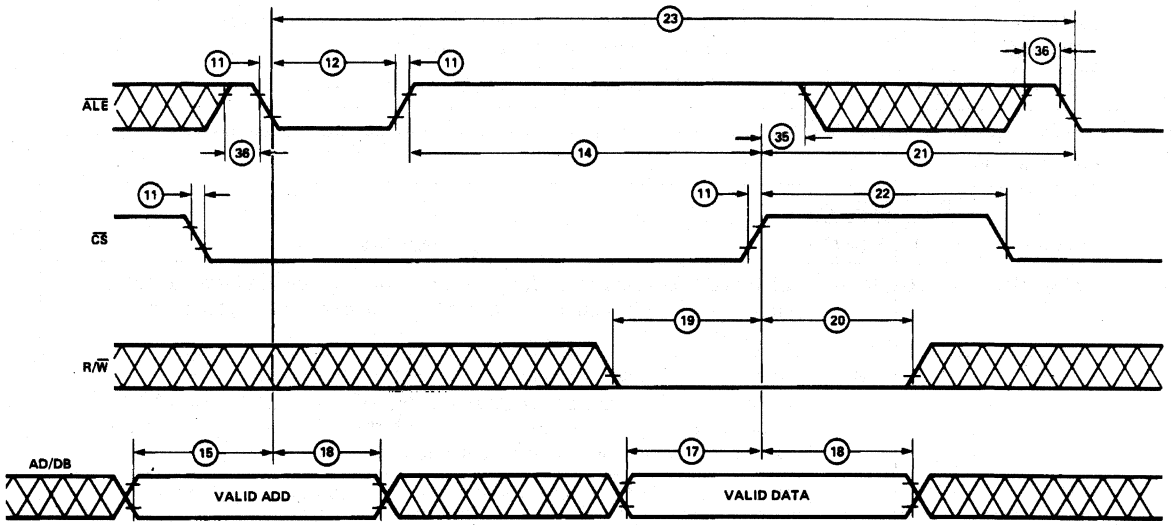
Read Cycle



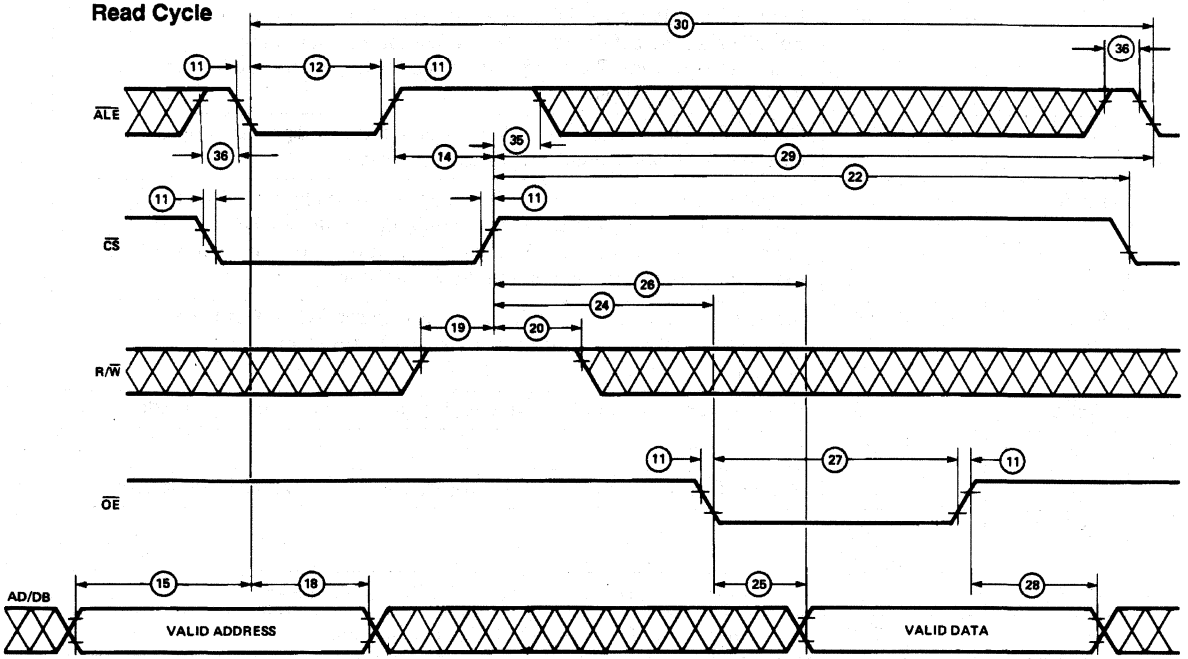
HCTL-1100 I/O Timing Diagrams

$\overline{ALE}$ WITHIN $\overline{CS}$

Write Cycle



Read Cycle



Pin Descriptions and Functions

Input/Output Pins

Symbol	Pin Number		Description
	PDIP	PLCC	
AD0/DB0-AD5/DB5	2-7	3-8	Address/Data Bus – Lower 6 bits of 8-bit I/O port which are multiplexed between address and data.
DB6, DB7	8, 9	9, 10	Data bus – Upper 2 bits of 8-bit I/O port used for data only.

Input Signals

Symbol	Pin Number		Description
	PDIP	PLCC	
CHA/CHB	31, 30	34, 33	Channel A, B – Input pins for position feedback from an incremental shaft encoder. Two channels, A and B, 90 degrees out of phase are required.
Index	33	36	Index Pulse – Input from the reference or index pulse of an incremental encoder. Used only in conjunction with the Commutator. Either a low or high true signal can be used with the Index pin. See Timing Diagrams and Encoder Interface section for more detail.
R/W	37	41	Read/Write – Determines direction of data exchange for the I/O port.
ALE	38	42	Address Latch Enable – Enables lower 6 bits of external data bus into internal address latch.
CS	39	43	Chip Select – Performs I/O operation dependent on status of R/W line. For a Write, the external bus data is written into the internal addressed location. For Read, data is read from an internal location into an internal output latch.
OE	40	44	Output Enable – Enables the data in the internal output latch onto the external data bus to complete a Read operation.
Limit	14	15	Limit Switch – An internal flag which when externally set, triggers an unconditional branch to the Initialization/Idle mode before the next control sample is executed. Motor Command is set to zero. Status of the Limit flag is monitored in the Status register.
Stop	15	16	Stop Flag – An internal flag that is externally set. When flag is set during Integral Velocity Control mode, the Motor Command is decelerated to a stop.
$\overline{\text{Reset}}$	36	40	Reset – A hard reset of internal circuitry and a branch to Reset mode.
ExtClk	34	37	External Clock
V_{DD}	11, 35	12, 38	Voltage Supply – Both V_{DD} pins must be connected to a 5.0 volt supply.
GND	10, 32	1, 11, 23, 35	Circuit Ground
SYNC	1	2	Used to synchronize multiple HCTL-1100 sample timers.
NC	–	17, 39	Not connected. These pins should be left floating.

Output Pins

Symbol	Pin Number		Description
	PDIP	PLCC	
MC0-MC7	18-25	20-22, 24-28	Motor Command Port – 8-bit output port which contains the digital motor command adjusted for easy bipolar DAC interfacing. MC7 is the most significant bit (MSB).
Pulse	16	18	Pulse – Pulse width modulated signal whose duty cycle is proportional to the Motor Command magnitude. The frequency of the signal is External Clock/100 and pulse width is resolved into 100 external clocks.
Sign	17	19	Sign – Gives the sign/direction of the pulse signal.
PHA-PHD	26-29	29-32	Phase A, B, C, D – Phase Enable outputs of the Commutator.
Prof	12	13	Profile Flag – Status flag which indicates that the controller is executing a profiled position move in the Trapezoidal Profile Control mode.
Init	13	14	Initialization/Idle Flag – Status flag which indicates that the controller is in the Initialization/Idle mode.

Pin Functionality

$\overline{\text{SYNC}}$ Pin

The $\overline{\text{SYNC}}$ pin is used to synchronize two or more ICs. It is only valid in the INIT/IDLE mode (see Operating the HCTL-1100). When this pin is pulled low, the internal sample timer is cleared and held to zero. When the level on the pin is returned to high, the internal sample timer instantly starts counting down from the programmed value.

Connecting all $\overline{\text{SYNC}}$ pins together in the system and pulsing the $\overline{\text{SYNC}}$ signal from the host processor will synchronize all controllers.

$\overline{\text{Limit}}$ Pin

This emergency-flag input is used to disable the control modes of the HCTL-1100. A low level on this input pin causes the internal Limit flag to be set. If this pin is NOT used, it must be pulled up to V_{DD}. If it is not connected, the pin could float low, and possibly trigger a false emergency condition.

The Limit flag, when set in any control mode, causes the HCTL-1100 to go into the Initialization/Idle mode, clearing the Motor Command and causing an immediate motor shutdown. When the Limit flag is set, none of the three control mode flags (F0, F3, or F5) are cleared as the HCTL-1100 enters the Initialization/Idle mode. The user should be aware that these flags are still set before commanding the HCTL-1100 to re-enter one of the four control modes from Initialization/Idle mode.

In general, the user should clear all control mode flags after the limit pin has been pulled low, then proceed.

$\overline{\text{Stop}}$ Pin

The Stop flag affects the HCTL-1100 only in the Integral Velocity Mode.

When a low level is present on this emergency-flag input, the internal stop flag is set. If this pin is NOT used, it must be pulled up to V_{DD}. If it is not connected, the pin could float low, and possibly trigger a false emergency condition.

When the STOP flag is set, the system will come to a decelerated stop and stay in this mode with a command velocity of zero until the Stop flag is cleared and a new command velocity is specified.

Notes on Limit and Stop Flags

Stop and Limit flags are set by a low level input at their respective pins. The flags can only be cleared when the input to the corresponding pin goes high, signifying that the emergency condition has been corrected, AND a write to the Status register (R07H) is executed. That is, after the emergency pin has been set and cleared, the flag also must be cleared by writing to R07H. Any word that is written to R07H after the emergency pin is set and cleared will clear the emergency flag. The lower four bits of that word will also reconfigure the Status register.

Encoder Input Pins (CHA, CHB, INDEX)
The HCTL-1100 accepts TTL compatible outputs from 2 and 3 channel incremental encoders such as the HEDS-5XXX, 6XXX, and 9XXX series encoders. Channels A and B are internally decoded into quadrature counts which increment or decrement the 24-bit position counter. For example, a 500-count encoder is decoded into 2000 quadrature counts per revolution. The position counter will be incremented when Channel B leads Channel A. The Index channel is used only for the Commutator and its function is to serve as a reference point for the internal Ring Counter.

The HCTL-1100 employs an internal 3-bit state delay filter to remove any noise spikes from the encoder inputs to the HCTL-1100. This 3-bit state delay filter requires the encoder inputs to remain stable for three consecutive clock rising edges for an encoder pulse to be considered valid by the HCTL-1100's actual position counter (i.e., an encoder pulse must remain at a logic level high or low for three consecutive clock rising edges for the HCTL-1100's actual position counter to be incremented or decremented.) The designer should therefore generally avoid creating the encoder pulses of less than 3 clock cycles.

The index signal of an encoder is used in conjunction with the Commutator. It resets the internal ring counter which keeps track of the rotor position so that no cumulative errors are generated.

The Index pin of the HCTL-1100 also has a 3-bit filter on its input. The Index pin is *active low and level transition sensitive*. It detects a valid high-to-low transition and qualifies the low input level through the 3-bit filter. At this point, the Index signal is internally detected by the commutator logic. This type of configuraiton allows an Index or Index signal to be used to generate the reference mark for commutator operation as long as the AC specifications for the Index signal are met.

Motor Command Port (MC0-MC7)
The 8-bit Motor Command port consists of register R08H whose data goes directly to external pins MC0-MC7. MC7 is the most significant bit. R08H can be read and written to, however, it should be written to only during the Initialization/Idle mode. During any of the four Control modes, the controller writes the motor command into R08H.

This topic is further discussed in the "Register Section" under "Motor Command Register R08H".

Pulse Width Modulation (PWM) Output Port (Pulse, Sign)
The PWM port consists of the Pulse and Sign pins. The PWM port outputs the motor command as a pulse width modulated signal with the correct polarity. This topic is further discussed in the "Register Section" under "PWM Motor Command Register R09H".

Trapezoid Profile Pin (Prof)
The Trapezoid Profile Pin is internally connected to software flag bit 4 in the Status Register. This flag is also represented by bit 0 in the Flag Register (R00H). See the "Register Section" for more information. Both the Pin and the Flag indicate the status of a trapezoid profile move. When the HCTL-1100 begins a trapezoid move, this flag is set by the controller (a high level appears on the pin), indicating the move is in progress. When the HCTL-1100 finishes the move, this flag is cleared by the controller.

Note that the instant the flag is cleared may not be the same instant the motor stops. The flag indicates the completion of the command profile, not the actual profile. If the motor is stalled during the move, or cannot physically keep up with the move, the flag will be cleared before the move is finished.

INIT/IDLE Pin (INIT)
This pin indicates that the HCTL-1100 is in the INIT/IDLE mode, waiting to begin control. This pin is internally connected to the software flag bit 5 in the Status Register R07H. This flag is also represented by bit 1 in the Flag Register (R00H) (See the "Register Section" for more information).

Commutator Pins (PHA-PHD)
These pins are connected only when using the commutator of the HCTL-1100 to drive a brushless motor or step motor. The four pins can be programmed to energize each winding on a multiphase motor.

Operation of the HCTL-1100

Registers

The HCTL-1100 operation is controlled by a bank of 64 8-bit registers, 35 of which are user accessible. These registers contain command and configuration information necessary to properly run the controller chip. The 35 user-accessible registers are listed in Tables 1 and 2. The register number is also the address. A functional block diagram of the HCTL-1100 which shows the role of the user-accessible registers is also included in Figure 3. The other 29 registers are used by the internal CPU as scratch registers and should not be accessed by the user.

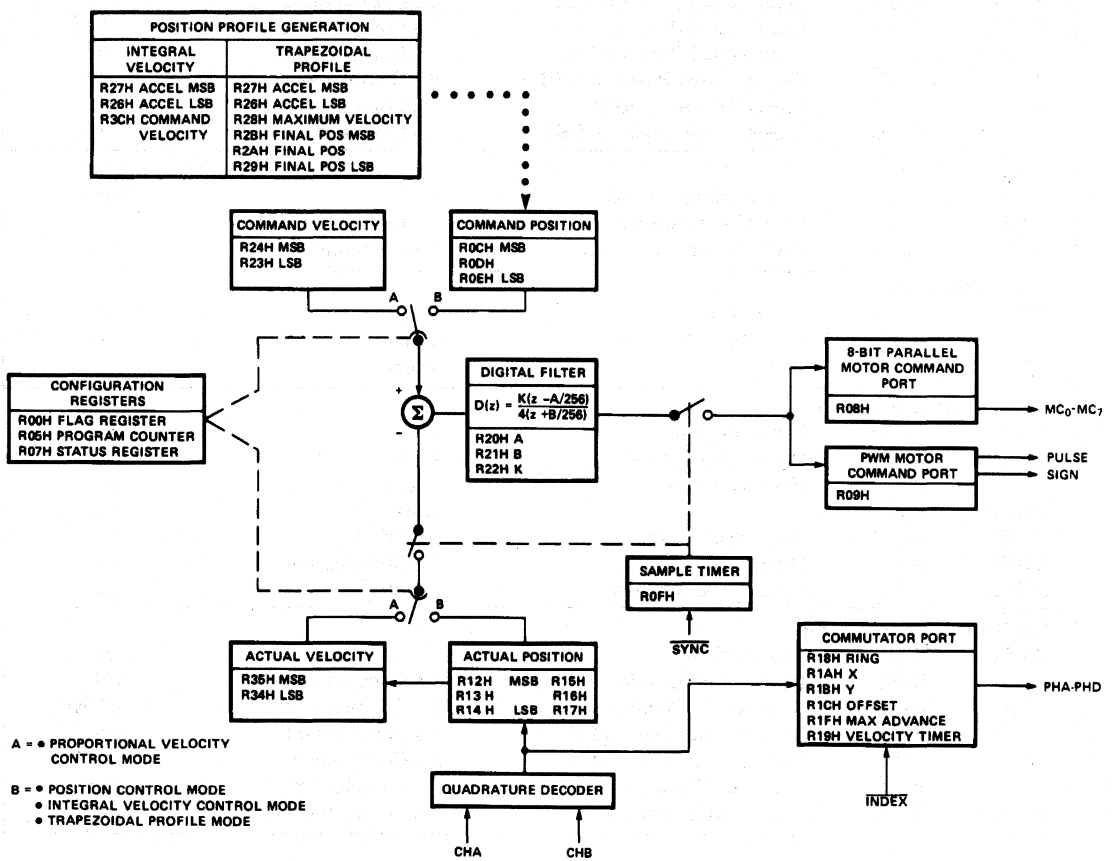


Figure 3. Register Block Diagram.

Table 1. Register Reference By Mode

Register		Function	Data Type[1]	User Access
Hex	Dec.			
General Control				
R00H	R00D	Flag Register		r/w
R05H	R05D	Program Counter	scalar	r/w
R07H	R07D	Status Register	-	r/w[2]
R0FH	R15D	Sample Timer	scalar	r/w
R12H	R18D	Read Actual Position MSB	2's Complement	r[4]
R13H	R19D	Read Actual Position	2's Complement	r[4]/w[5]
R14H	R20D	Read Actual Position LSB	2's Complement	r[4]
R15H	R21D	Preset Actual Position MSB	2's Complement	w[8]
R16H	R22D	Preset Actual Position	2's Complement	w[8]
R17H	R23D	Preset Actual Position LSB	2's Complement	w[8]
Output Registers				
R07H	R07D	Sign Reversal Inhibit	-	r/w[2]
R08H	R08D	8 bit Motor Command	2's Complement+80H	r/w
R09H	R09D	PWM Motor Command	2's Complement	r/w
Filter Registers				
R20H	R32D	Filter Zero, A	scalar	r/w
R21H	R33D	Filter Pole, B	scalar	r/w
R22H	R34D	Gain, K	scalar	r/w
Commutator Registers				
R07H	R07D	Status Register	-	r/w[2]
R18H	R24D	Commutator Ring	scalar[6,7]	r/w
R19H	R25D	Velocity Timer	scalar	w
R1AH	R26D	X	scalar[6,7]	r/w
R1BH	R27D	Y Phase Overlap	scalar[6,7]	r/w
R1CH	R28D	Offset	2's Complement[7]	r/w
R1FH	R31D	Max. Phase Advance	scalar[6,7]	r/w
Position Control Mode				
R00H	R00D	Flag Register	-	r/w
R12H	R18D	Read Actual Position MSB	2's Complement	r[4]
R13H	R19D	Read Actual Position	2's Complement	r[4]/w[5]
R14H	R20D	Read Actual Position LSB	2's Complement	r[4]
R0CH	R12D	Command Position MSB	2's Complement	r/w[3]
R0DH	R13D	Command Position	2's Complement	r/w[3]
R0EH	R14D	Command Position LSB	2's Complement	r/w[3]

Table 1. (continued).

Register		Function	Data Type	User Access
Hex	Dec.			
Trapezoid Profile Control Mode				
R00H	R00D	Flag Register	-	r/w
R07H	R07D	Status Register	-	r/w[2]
R12H	R18D	Read Actual Position MSB	2's Complement	r[4]
R13H	R19D	Read Actual Position	2's Complement	r[4]/w[5]
R14H	R20D	Read Actual Position LSB	2's Complement	r[4]
R29H	R41D	Final Position LSB	2's Complement	r/w
R2AH	R42D	Final Position	2's Complement	r/w
R2BH	R43D	Final Position MSB	2's Complement	r/w
R26H	R38D	Acceleration LSB	scalar	r/w
R27H	R39D	Acceleration MSB	scalar[6]	r/w
R28H	R40D	Maximum Velocity	scalar[6]	r/w
Integral Velocity Mode				
R00H	R00D	Flag Register	-	r/w
R12H	R18D	Read Actual Position MSB	2's Complement	r[4]
R13H	R19D	Read Actual Position	2's Complement	r[4]/w[5]
R14H	R20D	Read Actual Position LSB	2's Complement	r[4]
R26H	R38D	Acceleration LSB	scalar	r/w
R27H	R39D	Acceleration MSB	scalar[6]	r/w
R3CH	R60D	Command Velocity	2's Complement	r/w
Proportional Velocity Mode				
R00H	R00D	Flag Register	-	r/w
R12H	R18D	Read Actual Position MSB	2's Complement	r[4]
R13H	R19D	Read Actual Position	2's Complement	r[4]/w[5]
R14H	R20D	Read Actual Position LSB	2's Complement	r[4]
R23H	R35D	Command Velocity LSB	2's Complement	r/w
R24H	R36D	Command Velocity MSB	2's Complement	r/w
R34H	R52D	Actual Velocity LSB	2's Complement	r
R35H	R53D	Actual Velocity MSB	2's Complement	r

Notes:
1. Consult appropriate section for data format and use.
2. Upper 4 bits are read only.
3. Writing to R0EH (LSB) latches all 24 bits.
4. Reading R14H (LSB) latches data in R12H and R13H.
5. Writing to R13H clears Actual Position Counter to zero.
6. The scalar data is limited to positive numbers (00H to 7FH).
7. The commutator registers (R18H, R1CH, R1FH) have further limits which are discussed in the Commutator section of this data sheet.
8. Writing to R17H (R23D) latches all 24 bits (only in INIT/IDLE mode).

Table 2. Register Reference Table by Register Number

Register		Function	Mode Used	Data Type	User Access
Hex	Dec.				
R00H	R00D	Flag Register	All	–	r/w
R05H	R05D	Program Counter	All	scalar	w
R07H	R07D	Status Register	All	–	r/w[2]
R08H	R08D	8 bit Motor Command Port	All	2's complement + 80H	r/w
R09H	R09D	PWM Motor Command Port	All	2's complement	r/w
R0CH	R12D	Command Position (MSB)	All except Proportional Velocity	2's complement	r/w[3]
R0DH	R13D	Command Position	All except Proportional Velocity	2's complement	r/w[3]
R0EH	R14D	Command Position (LSB)	All except Proportional Velocity	2's complement	r/w[3]
R0FH	R15D	Sample Timer	All	scalar	r/w
R12H	R18D	Read Actual Position (MSB)	All	2's complement	r[4]
R13H	R19D	Read Actual Position	All	2's complement	r[4]/w[5]
R14H	R20D	Read Actual Position (LSB)	All	2's complement	r[4]
R15H	R21D	Preset Actual Position (MSB)	INIT/IDLE	2's complement	w[8]
R16H	R22D	Preset Actual Position	INIT/IDLE	2's complement	w[8]
R17H	R23D	Preset Actual Position (LSB)	INIT/IDLE	2's complement	w[8]
R18H	R24D	Commutator Ring	All	scalar[6,7]	r/w
R19H	R25D	Commutator Velocity Timer	All	scalar	w
R1AH	R26D	X	All	scalar[6]	r/w
R1BH	R27D	Y Phase Overlap	All	scalar[6]	r/w
R1CH	R28D	Offset	All	2's complement[7]	r/w
R1FH	R31D	Maximum Phase Advance	All	scalar[6,7]	r/w
R20H	R32D	Filter Zero, A	All except Proportional Velocity	scalar	r/w
R21H	R33D	Filter Pole, B	All except Proportional Velocity	scalar	r/w
R22H	R34D	Gain, K	All	scalar	r/w
R23H	R35D	Command Velocity (LSB)	Proportional Velocity	2's complement	r/w
R24H	R36D	Command Velocity (MSB)	Proportional Velocity	2's complement	r/w
R26H	R38D	Acceleration (LSB)	Integral Velocity and Trapezoidal Profile	scalar	r/w
R27H	R39D	Acceleration (MSB)	Integral Velocity and Trapezoidal Profile	scalar[6]	r/w
R28H	R40D	Maximum Velocity	Trapezoidal Profile	scalar[6]	r/w
R29H	R41D	Final Position (LSB)	Trapezoidal Profile	2's complement	r/w
R2AH	R42D	Final Position	Trapezoidal Profile	2's complement	r/w
R2BH	R43D	Final Position (MSB)	Trapezoidal Profile	2's complement	r/w
R34H	R52D	Actual Velocity (LSB)	Proportional Velocity	2's complement	r
R35H	R53D	Actual Velocity (MSB)	Proportional Velocity	2's complement	r
R3CH	R60D	Command Velocity	Integral Velocity	2's complement	r/w

Notes:
1. Consult appropriate section for data format and use.
2. Upper 4 bits are read only.
3. Writing to R0EH (LSB) latches all 24 bits.
4. Reading R14H (LSB) latches data in R12H and R13H.
5. Writing to R13H clears Actual Position Counter to zero.
6. The scalar data is limited to positive numbers (00H to 7FH).
7. The commutator registers (R18H, R1CH, R1FH) have further limits which are discussed in the Commutator section of this data sheet.
8. Writing to R17H (R23D) latches all 24 bits (only in INIT/IDLE mode).

Register Descriptions – General Control, Output, Filter, and Commutator

Flag Register (R00H)

The Flag register contains flags F0 through F5. This register is a read/write register. Each flag is set and cleared by writing an 8-bit data word to R00H. When writing to R00H, the upper four bits are ignored by the HCTL-1100, bits 0,1,2 specify the flag address, and bit 3 specifies whether to set (bit=1) or clear (bit=0) the addressed flag.

Flag Descriptions

F0–Trapezoidal Profile Flag – set by the user to execute Trapezoidal Profile Control. The flag is reset by the controller when the move is completed. The status of F0 can be monitored at the Profile pin and in Status register R07H bit 4.

F1–Initialization/Idle Flag – set/cleared by the HCTL-1100 to indicate execution of the Initialization/Idle mode. The status of F1 can be monitored at the Initialization/Idle pin and in bit 5 of the Status register (R07H). The user should not attempt to set or clear F1.

F2–Unipolar Flag – set/cleared by the user to specify Bipolar (clear) or Unipolar (set) mode for the Motor Command port.

F3–Proportional Velocity Control Flag – set by the user to specify Proportional Velocity control.

F4–Hold Commutator flag – set/cleared by the user or automatically by the Align mode. When set, this flag inhibits the internal commutator counters to allow open loop stepping of a motor by using the commutator. (See "Offset register" description in the "Commutator section.")

F5–Integral Velocity Control – set by the user to specify Integral Velocity Control. Also set and cleared by the HCTL-1100 during execution of the Trapezoidal Profile mode. This is transparent to the user except when the Limit flag is set (see "Emergency Flags" section).

Writing to the Flag Register

When writing to the flag register, only the lower four bits are used. Bit 3 indicates whether to set or clear a certain flag, and bits 0,1,and 2 indicate the desired flag. The following table shows the bit map of the Flag register:

Bit Number	Function
7-4	Don't Care
3	1 = set 0 = clear
2	AD2
1	AD1
0	AD0

The following table outlines the possible writes to the Flag Register:

Flag	SET	CLEAR
F0	08H	00H
F1	-	-
F2	0AH	02H
F3	0BH	03H
F4	0CH	04H
F5	0DH	05H

Reading the Flag Register

Reading register R00H returns the status of the flags in bits 0 to 5. For example, if bit 0 is set (logic 1), then flag F0 is set. If bit 4 is set, then flag F4 is set. If bits 0 and 5 are set, then both flags F0 and F5 are set.

The following table outlines the Flag Register Read:

Bit Number	Flag (1 = set) (0 = clear)
8-6	Don't Care
5	F5
4	F4
3	F3
2	F2
1	F1
0	F0

Notes:

1. A soft reset (writing 00H to R05H) will not reset the flags in the flag register. A hard reset ($\overline{\text{RESET}}$ pin low) is required to reset all the flags. The flags can also be reset by writing the proper word to the Flag register as explained above.
2. While in Trapezoid Profile Mode, Flag F0 will be set, and Flag F5 may be set. F5 is used for internal purposes. Both flags will be cleared at the end of the profile.

Program Counter Register (R05H)

The Program Counter, which is a write-only register, executes the preprogrammed functions of the controller. The program counter is used along with the control flags F0, F3, and F5 in the Flag register (R00H) to change control modes. The user can write any of the following four commands to the Program Counter.

Value written to R05H	Action
00H	Software Reset
01H	Enter Init/Idle Mode
02H	Enter Align Mode (only from INIT/IDLE Mode)
03H	Enter Control Mode (only from INIT/IDLE Mode)

These Commands are discussed in more detail in the "Operating Modes" section.

Status Register (R07H)
The Status register indicates the status of the HCTL-1100. Each bit decodes into one signal. All 8 bits are user readable and are decoded as shown below. Only the lower 4 bits can be written to by the user to configure the HCTL-1100. To set or clear any of the lower 4 bits, the user writes an 8-bit word to R07H. The upper 4 bits are ignored. Each of the lower 4 bits directly sets/clears the corresponding bit of the Status register as shown below. For example, writing XXXX0101 to R07H sets the PWM Sign Reversal Inhibit, sets the Commutator Phase Configuration to "3 Phase," and sets the Commutator Count Configuration to "full."

Motor Command Register (R08H)
The 8-bit Motor Command Port consists of register R08H. The register is connected to external pins MC0-MC7. MC7 is the most significant bit. R08H can be read and written to; however, it should be written to only in the Initialization/Idle mode. During any of the four control modes, the HCTL-1100 writes values to register R08H.

The Motor Command Port operates in two modes, bipolar and unipolar, when under control of internal software. Bipolar mode allows the full range of values in R08H (-128D to +127D). The data written to the Motor Command Port by the control algorithms is the internally computed 2's-complement motor command with an 80H offset added. This allows direct interfacing to a DAC. Connecting the Motor Command Port to a DAC, Bipolar mode allows the full voltage swing (positive and negative).

Unipolar mode functions such that with the same DAC circuit, the motor command output is restricted to positive values (80H to FFH) when in a control mode. Unipolar mode is used with multi-phase motors when the commutator controls the direction of movement. (If needed, the Sign pin could be used to indicate direction). In Unipolar mode, the user can still write a negative value to R08H in INIT/IDLE mode.

Unipolar mode or Bipolar mode is programmed by setting or clearing flag F2 in the Flag Register R00H.

Internally, the HCTL-1100 operates on data of 24, 16 and 8-bit lengths to produce the 8-bit motor command, available externally. Many times the computed motor command will be greater than 8 bits. At this point, the motor command is saturated by the controller. The saturated value output by the controller is not the full scale value 00H (00D), or FFH (255D). The saturated value is adjusted to 0FH (15D) (negative saturation) and F0H (240D) (positive saturation). Saturation levels for the Motor Command port are in Figure 4.

Table 3. Status Register

Status Bit	Function
0	PWM Sign Reversal Inhibit 0 = off 1 = on
1	Commutator Phase Configuration 0 = 3 phase 1 = 4 phase
2	Commutator Count Configuration 0 = quadrature 1 = full
3	Should always be set to 0
4	Trapezoidal Profile Flag F0 1 = in Profile Control
5	Initialization/Idle Flag F1 1 = in Initialization/Idle Mode
6	Stop Flag 0 = set (Stop triggered) 1 = cleared (no Stop)
7	Limit Flag 0 = set (Limit triggered) 1 = cleared (no Limit)

PWM Motor Command Register (R09H)

The PWM port outputs the motor command as a pulse width modulated signal with the correct sign of polarity. The PWM port consists of the Pulse and Sign pins and R09H.

The PWM signal at the Pulse pin has a frequency of External Clock/100 and the duty cycle is resolved into the 100 clocks. (For example, a 2 MHz clock gives a 20 KHz PWM frequency.)

The Sign pin gives the polarity of the command. Low output on Sign pin is positive polarity.

The 2's-complement contents of R09H determine the duty cycle and polarity of the PWM command. For example, D8H (–40D) gives a 40% duty cycle signal at the Pulse pin and forces the Sign pin high. Data outside the 64H (+100D) to 9CH (–100D) linear range gives 100% duty cycle. R09H can be read and written to. However, the user should only write to R09H when the controller is in the Initialization/Idle mode.

Figure 5 shows the PWM output versus the internal motor command.

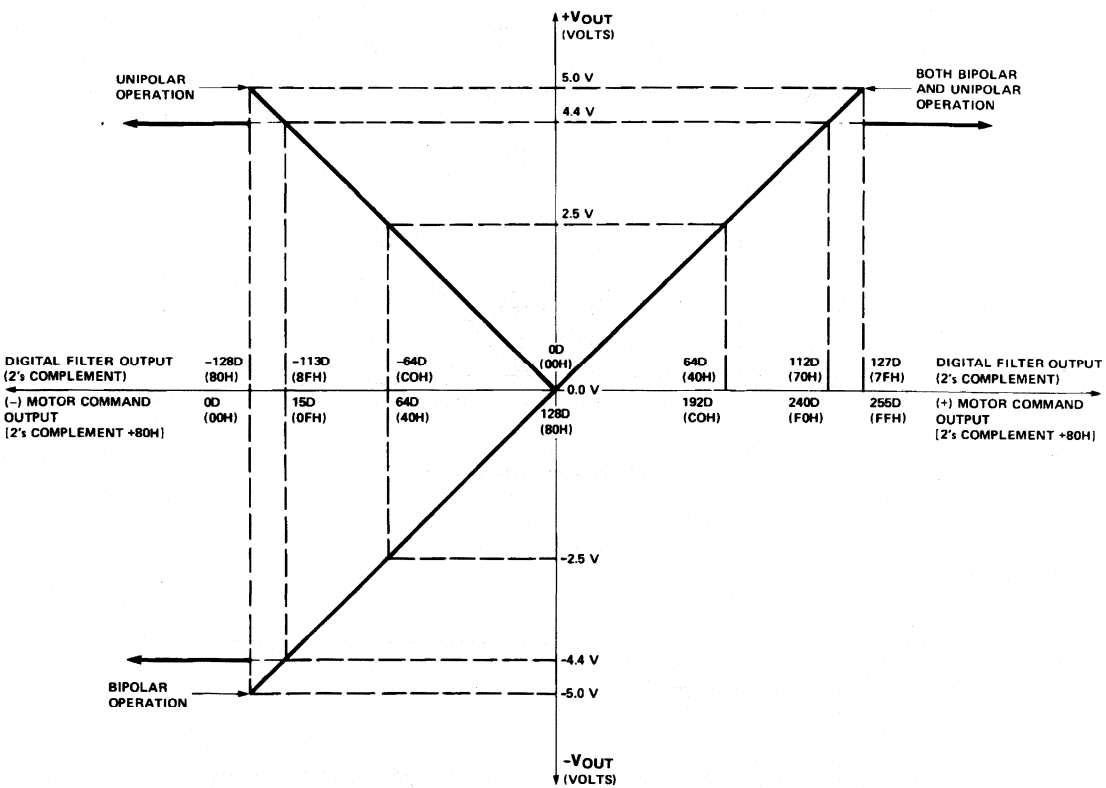


Figure 4. Motor Command Port Output.

When any Control mode is being executed, the unadjusted internal 2's-complement motor command is written to R09H. Because of the hardware limit on the linear range (64H to 9CH, ± 100D), the PWM port saturates sooner than the 8-bit Motor Command port (00H to FFH, +127D to –128D). When the internal motor command saturates above 8 bits, the PWM port is saturated to the full ± 100% duty cycle level. Figure 5 shows the actual values inside the PWM port. Note that the Unipolar flag, F2, does *not* affect the PWM port.

For commutation of brushless motors with the PWM port, only use the Pulse pin from the PWM port as the commutator already contains sign information. (See Figure 9.)

The PWM port has an option that can be used with H-bridge type amplifiers. The option is Sign Reversal Inhibit, which inhibits the Pulse output for one PWM period after a sign polarity reversal. This allows one pair of transistors to turn off before others are turned on and thereby avoids a short across the power supply. Bit 0 in the Status register (R07H) controls the Sign Reversal

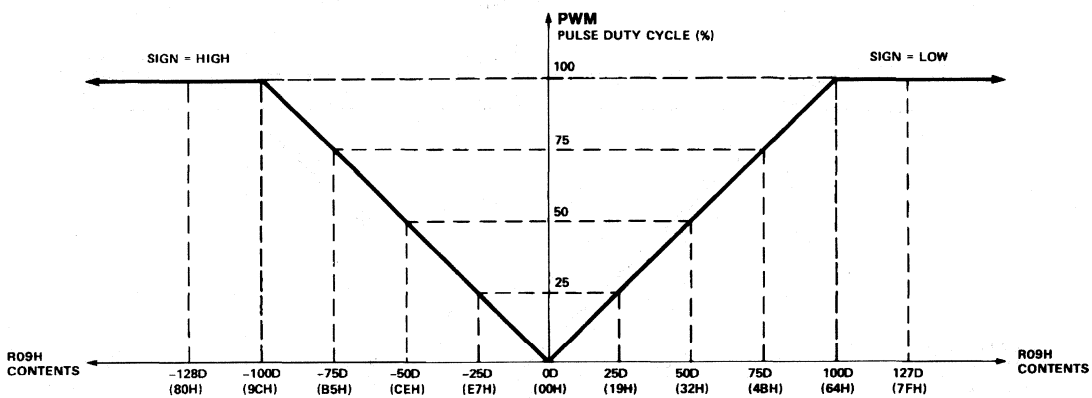


Figure 5. PWM Port Output.

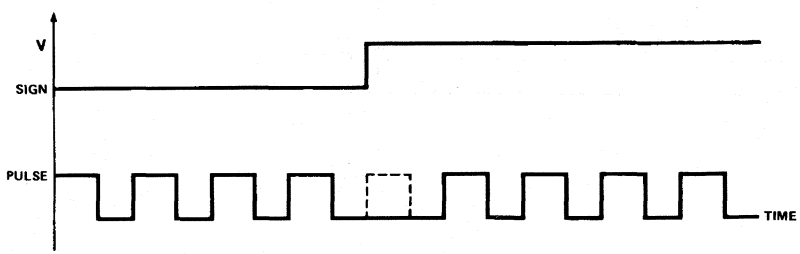


Figure 6. Sign Reversal Inhibit.

Inhibit option. Figure 6 shows the output of the PWM port when Bit 0 is set.

Actual Position Registers
Read, Clear: R12H,R13H,R14H
Preset : R15H,R16H,R17H

The Actual Position Register is accessed by two sets of registers in the HCTL-1100. When reading the Actual Position from the HCTL-1100, the host processor will read Registers R12H(MSB), R13H, and R14H(LSB). When presetting the Actual Position Register, the processor will write to Registers R15H(MSB), R16H, and R17H(LSB).

When reading the Actual Position registers, the order should be R14H, R13H, R12H. These registers are latched, such that, when reading Register R14H, all three bytes will be latched so that count data does not change while reading three separate bytes.

When presetting the Actual Position Register, write to R15H and R16H first. When R17H is written to, all three bytes are simultaneously loaded into the Actual Position Register.

Note that presetting the Actual Position Registers is only allowed while the HCTL-1100 is in INIT/IDLE mode.

The Actual Position Registers can be simultaneously cleared at any time by writing any value to R13H.

Digital Filter Registers

Zero (A)	R20H
Pole (B)	R21H
Gain (K)	R22H

All control modes use some part of the programmable digital filter D(z) to compensate for closed loop system stability. The compensation D(z) has the form:

$$D(z) = \frac{K\left(z - \frac{A}{256}\right)}{4\left(z + \frac{B}{256}\right)} \qquad [1]$$

where:
z = the digital domain operator
K = digital filter gain (R22H)
A = digital filter zero (R20H)
B = digital filter pole (R21H)

The compensation is a first-order lead filter which in combination with the Sample Timer T (R0FH) affects the dynamic step response and stability of the control system. The Sample Timer, T, determines the rate at which the control algorithm gets executed. All parameters, A, B, K, and T, are 8-bit scalars that can be changed by the user any time.

As shown in equations [2] and [3], the digital filter uses previously sampled data to calculate D(z). This old internally sampled data is cleared when the Initialization/Idle mode is executed.

In Position Control, Integral Velocity Control, and Trapezoidal Profile Control the digital filter is implemented in the time domain as shown below:

$$MC_n = (K/4)(X_n) - [(A/256)(K/4)(X_{n-1}) + (B/256)(MC_{n-1})] \qquad [2]$$

where:
n = current sample time
n-1 = previous sample time
MC_n = Motor Command Output at n
MC_{n-1} = Motor Command Output at n-1
X_n = (Command Position – Actual Position) at n
X_{n-1} = (Command Position – Actual Position) at n-1

In Proportional Velocity control the digital compensation filter is implemented in the time domain as:

$$MC_n = (K/4)(Y_n) \qquad [3]$$

where:

Y_n = (Command Velocity – Actual Velocity) at n

For more information on system sampling times, bandwidth, and stability, please consult Hewlett-Packard Application Note 1032, *Design of the HCTL-1000's Digital Filter Parameters by the Combination Method.*

Sample Timer Register (R0FH)
The contents of this register set the sampling period of the HCTL-1100. The sampling period is:

$$t = 16(T+1)(1/\text{frequency of the external clock}) \quad [4]$$

where:
T = contents of register R0FH

The Sample Timer has a limit on the minimum allowable sample time depending on the control mode being executed. The limits are given in Table 4 below.

The minimum value limits are to make sure the internal programs have enough time to complete proper execution.

The maximum value of T (R0FH) is FFH (255D). With a 2 MHz clock, the sample time can vary from 64 µsec to 2048 µsec. With a 1 MHz clock, the sample time can vary from 128 µsec to 4096 µsec.

Digital closed-loop systems with slow sampling times have lower stability and a lower bandwidth than similar systems with faster sampling times. To keep the system stability and bandwidth as high as possible the HCTL-1100 should typically be programmed with the fastest sampling time possible. This rule of thumb must be balanced by the needs of the velocity range to be controlled. Velocities are specified to the HCTL-1100 in terms of quadrature encoder counts per sample time. The faster the sampling time, the higher the slowest possible speed.

Hardware Description
The Sample Timer consists of a buffer and a decrement counter. Each time the counter reaches 00H, the Sampler Timer Value T (value written to R0FH) is loaded from the buffer into the counter, which immediately begins to decrement from T.

Writing to the Sample Timer Register
Data written to R0FH will be latched into the internal buffer and used by the counter after it completes the present sample time cycle by decrementing to 00H. The next sample time will use the newly written data.

Reading the Sample Timer Register
Reading R0FH gives the values directly from the decrementing counter. Therefore, the data read from R0FH will have a value anywhere between T and 00H, depending where in the sample time cycle the counter is.

Example –
1. On reset, the value of the timer is pre-set to 40H.
2. Reading R0FH shows
   3EH . . . 2BH . . . 08H . . .
   3CH . . .

Synchronizing Multiple Axes
Synchronizing multiple axes with HCTL-1100s can be achieved by using the $\overline{\text{SYNC}}$ pin as explained in the Pin Discussion section. Some users may not only want to synchronize several HCTL-1100s but also follow custom profiles for each axis. To do this, the user may need to write a new command position or command velocity during each sample time for the duration of the profile. In this case, data written to the HCTL-1100 has to be coordinated with the Sample Timer. This is so that only one command position or velocity is received during any one sample period, and that it is written at the proper time within a sample period.

At the beginning of each sample period, the HCTL-1100 is performing calculations and executions. New command positions and velocities should not be written to the HCTL-1100 during this time. If they are, the calculations may be thrown off and cause unpredictable control.

The user can read the Sample Timer Register to avoid writing too early during a sample period. Since the Sample Timer Register continuously counts down from its programmed value, the user can check if enough time has passed in the sample period to insure the completion of the internal calculations. The length of time needed by the HCTL-1100

Table 4.

Control Mode	R0FH Contents Minimum Limit
Position Control	07H(07D)
Proportional Velocity Control	07H(07D)
Trapezoidal Profile Control	0FH(15D)
Integral Velocity Control	0FH(15D)

to do its calculations is given by the Minimum Limits of R0FH (Sample Timer Register) as shown in Table 4. For Position Control Mode, the user should wait for the Sample Timer to count down 07H from its programmed value before writing the next command position or velocity. If the programmed sample timer value is 39H, wait until the Sample Timer Register reads 32H. Writing between 32H and 00H will make the command information available for the next sample period.

Commutator

Status Register	(R07H)
Commutator Ring	(R18H)
X Register	(R1AH)
Y Phase Overlap	(R1BH)
Offset	(R1CH)
Max. Phase Advance	(R1FH)
Velocity Timer	(R19H)

The commutator is a digital state machine that is configured by the user to properly select the phase sequence for electronic commutation of multiphase motors. The Commutator is designed to work with 2, 3, and 4-phase motors of various winding configurations and with various encoder counts. Along with providing the correct phase enable sequence, the Commutator provides programmable phase overlap, phase advance, and phase offset.

Phase overlap is used for better torque ripple control. It can also be used to generate unique state sequences which can be further decoded externally to drive more complex amplifiers and motors.

Phase advance allows the user to compensate for the frequency characteristics of the motor/amplifier combination. By advancing the phase enable command (in position), the delay in reaction of the motor/amplifier combination can be offset and higher performance can be achieved.

Phase offset is used to adjust the alignment of the commutator output with the motor torque curves. By correctly aligning the HCTL-1100's commutator output with the motor's torque curves, maximum motor output torque can be achieved.

The inputs to the Commutator are the three encoder signals, Channel A, Channel B, and Index, and the configuration data stored in registers.

The Commutator uses both channels and the index pulse of an incremental encoder. The index pulse of the encoder must be physically aligned to a known torque curve location because it is used as the reference point of the rotor position with respect to the Commutator phase enables.

The index pulse should be permanently aligned during motor encoder assembly to the last motor phase. This is done by energizing the last phase of the motor during assembly and permanently attaching the encoder codewheel to the motor shaft such that the index pulse is active as shown in Figures 7 and 8. Fine tuning of alignment for commutation purposes is done electronically by the Offset register (R1CH) once the complete control system is set up.

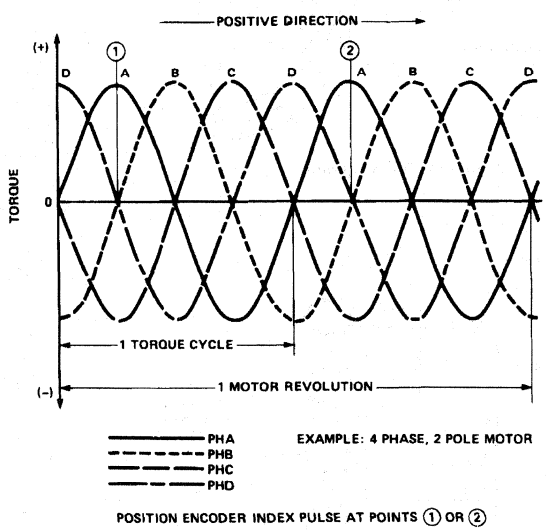


Figure 7. Index Pulse Alignment to Motor Torque Curves.

Each time an index pulse occurs, the internal commutator ring counter is reset to 0. The ring counter keeps track of the current position of the rotor based on the encoder feedback. When the ring counter is reset to 0, the Commutator is reset to its origin (last phase going low, Phase A going high) as shown in Figure 10.

The output of the Commutator is available as PHA, PHB, PHC, and PHD. The HCTL-1100's commutator acts as the electrical equivalent of the mechanical brushes in a motor. Therefore, the outputs of the commutator provide only proper phase sequencing for bidirectional operation. The magnitude information is provided to the motor via the Motor Command and PWM ports. The outputs of the commutator must be combined with the outputs of one of the motor ports to provide proper DC brushless and stepper motor control. Figure 9 shows an example of circuitry which uses the outputs of the commutator with the Pulse output of the PWM port to control a DC brushless or

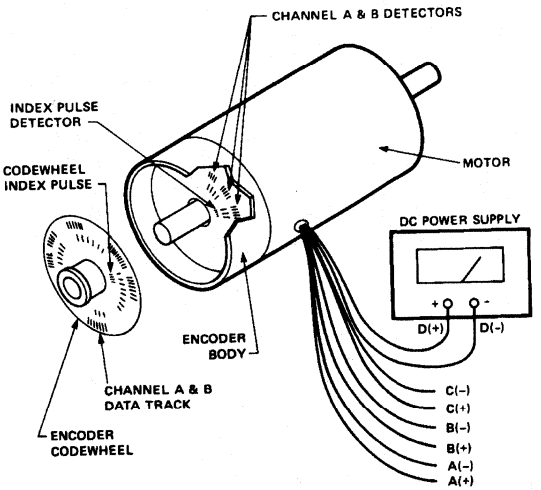


Figure 8. Codewheel Index Pulse Alignment.

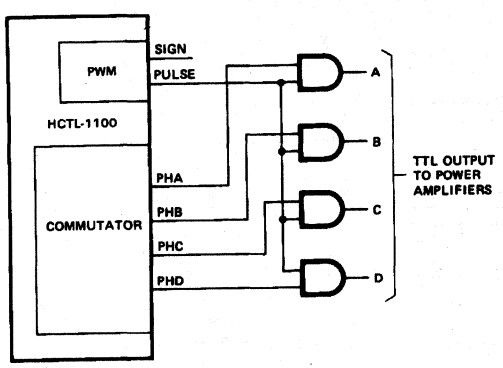


Figure 9. PWM Interface to Brushless DC Motors.

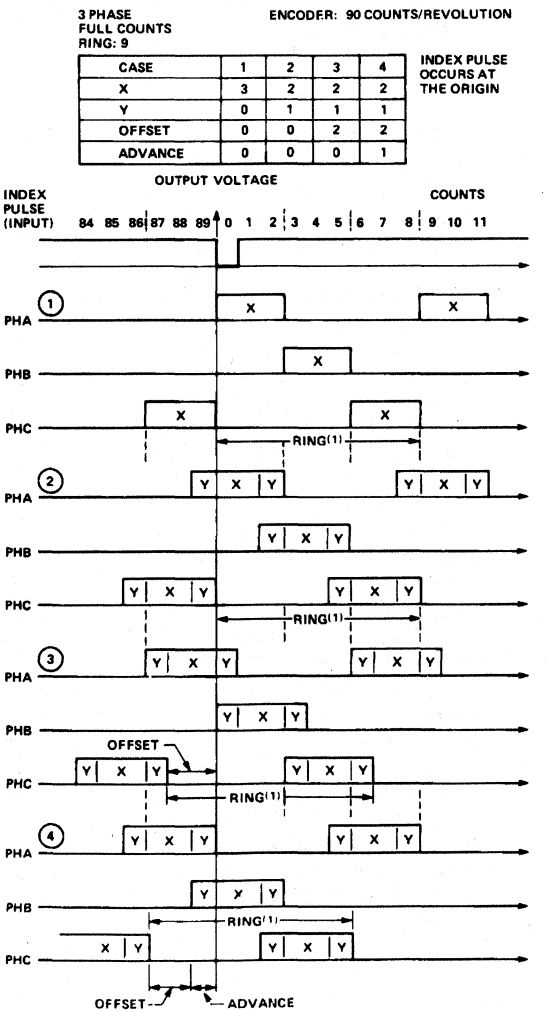


Figure 10. Commutator Configuration.

stepper motor. A similar procedure could be used to combine the commutator outputs PHA-PHD with a linear amplifier interface output (Figure 16) to create a linear amplifier system.

The Commutator is programmed by the data in the following registers. Figure 10 shows an example of the relationship between all the parameters.

Status Register (R07H)

Bit #1- 0 = 3-phase configuration, PHA, PHB, and PHC are active outputs.
1 = 4-phase configuration, PHA – PHD are active outputs.

Bit #2- 0 = Rotor position measured in quadrature counts (4x decoding).
1 = Rotor position measured in full counts (1 count = 1 codewheel bar and space.)

Bit #2 only affects the commutator's counting method. This includes the Ring register (R18H), the X and Y registers (R1AH & R1BH), the Offset register (R1CH), the Velocity Timer register (R19H), and the Maximum Advance register (R1FH).

Quadrature counts (4x decoding) are always used by the HCTL-1100 as a basis for position, velocity, and acceleration control.

Ring Register (R18H)

The Ring register is defined as 1 electrical cycle of the commutator which corresponds to 1 torque cycle of the motor. The Ring register is scalar and determines the length of the commutation cycle measured in full or quadrature counts as set by bit #2 in the Status register (R07H). The value of the ring must be limited to the range of 0 to 7FH.

X Register (R1AH)

This register contains scalar data which sets the interval during which only one phase is active.

Y Register (R1BH)

This register contains scalar data which set the interval during which two sequential phases are both active. Y is phase overlap. X and Y must be specified such that:

$$X + Y = \text{Ring}/(\#\text{ of phases}) \quad [5]$$

These three parameters define the basic electrical commutation cycle.

Offset Register (R1CH)

The Offset register contains two's-complement data which determines the relative start of the commutation cycle with respect to the index pulse. Since the index pulse must be physically referenced to the rotor, offset performs fine alignment between the electrical and mechanical torque cycles.

The Hold Commutator flag (F4) in the Status register (R07H) is used to decouple the internal commutator counters from the encoder input. Flag (F4) can be used in conjunction with the Offset register to allow the user to advance the commutator phases open loop. This technique may be used to create a custom commutator alignment procedure. For example, in Figure 10, case 1, for a three-phase motor where the ring = 9, X = 3, and Y = 0, the phases can be made to advance open loop by setting the Hold Commutator flag (F4) in the Flag register (R07H). When the values 0, 1, or 2 are written to the Offset register, phase A will be enabled. When the values 3, 4 or 5 are written to the Offset register, phase B will be enabled. And, when the values 6, 7, or 8 are written to the Offset register, phase C will be enabled. No values larger than the value programmed into the Ring register should be programmed into the Offset register.

Phase Advance Registers (R19H, R1FH)

The Velocity Timer register and Maximum Advance register linearly increment the phase advance according to the measured speed for rotation up to a set maximum.

The Velocity Timer register (R19H) contains scalar data which determines the amount of phase advance at a given velocity. The phase advance is interpreted in the units set for the Ring counter by bit #2 in R07H. The velocity is measured in revolutions per second.

$$\text{Advance} = N_f v \Delta t \quad [6]$$

$$\text{where: } \Delta t = \frac{16\,(\text{R19H} + 1)}{\text{f external clk}} \quad [7]$$

N_f = full encoder counts/revolution.
v = velocity (revolutions/second)

The Maximum Advance register (R1FH) contains scalar data which sets the upper limit for phase advance regardless of rotor speed.

Figure 11 shows the relationship between the Phase Advance registers. Note: If the phase advance feature is not used, set both R19H and R1FH to 0.

Commutator Constraints and Use

When choosing a three-channel encoder to use with a DC brushless or stepper motor, the user should keep in mind that the number of quadrature encoder counts (4x the number of slots in the encoder's codewheel) must be an integer multiple (1x, 2x, 3x, 4x, 5x, etc.) of the number of pole pairs in the DC brushless motor or steps in a stepper motor. To take full advantage of the commutator's overlap feature, the number of quadrature counts should be at least 3 times the number of pole pairs in the DC brushless motor or steps in the stepper motor. For example, a 1.8°, (200 step/revolution) stepper motor should employ at least a 150 slot codewheel = 600 quadrature counts/revolution = 3 x 200 steps/revolution).

There are several numerical constraints the user should be aware of to use the Commutator.

The parameters of Ring, X, Y, and Max Advance must be positive numbers (00H to 7FH). Additionally, the following equation must be satisfied:

$$(-128D)\ 80H \leq 3/2\ \text{Ring} + \text{Offset} \pm \text{Max Advance} \leq 7FH\ (127D) \quad [8]$$

In order to utilize the greatest flexibility of the Commutator, it must be realized that the Commutator works on a circular ring counter principle, whose range is defined by the Ring register (R18H). This means that for a ring of 96 counts and a needed offset of 10 counts, numerically the Offset register can be programmed as 0AH (10D) or AAH (-86D), the latter satisfying Equation 8.

If bit #2 in the Status register is set to allow the commutator to count in full counts, a higher resolution codewheel may be chosen for precise motor control without violating the commutator constraints equation (Equation 8).

Example: Suppose you want to commutate a 3-phase 15 deg/step Variable Reluctance Motor attached to a 192 count encoder.

1. Select 3-phase and quadrature mode for commutator by writing 0 to R07H.
2. With a 3-phase 15 degree/step Variable Reluctance motor the torque cycle repeats every 45 degrees or 8 times/revolution.
3. Ring register
   $$= \frac{(4)(192)\ \text{counts/revolution}}{8/\text{revolution}}$$
   = 96 quadrature counts
   = 1 commutation cycle
4. By measuring the motor torque curve in both directions, it is determined that an offset of 3 mechanical degrees, and a phase overlap of 2 mechanical degrees is needed.
   $$\text{Offset} = 3° \frac{(4)\ (192)}{360°}$$
   ≅ 6 quadrature counts

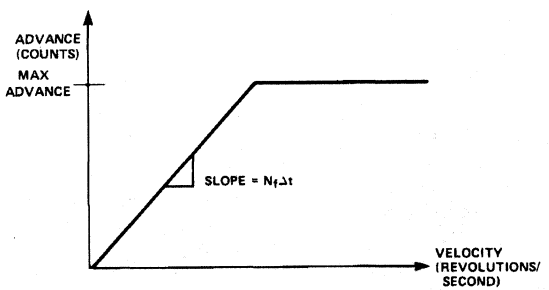


Figure 11. Phase Advance vs. Motor Velocity.

To create the 3 mechanical degree offset, the Offset register (R1CH) could be programmed with either A6H (-90D) or 06H (+06D). However, because 06H (+06D) would violate the commutator constraints Equation 8, A6H (-90D) is used.

$$Y = \text{overlap} = \frac{(2°)\,(4)\,(192)}{360°} \cong 4$$

$$X + Y = 96/3$$

Therefore, $X = 28$

$Y = 4$

For the purposes of this example, the Velocity Timer and Maximum Advance are set to 0.

Operation Flowchart

The HCTL-1100 executes any one of three setup routines or four control modes selected by the user. The three setup routines include:

- Reset
- Initialization/Idle
- Align.

The four control modes available to the user include:

- Position Control
- Proportional Velocity Control
- Trapezoidal Profile Control
- Integral Velocity Control

The HCTL-1100 switches from one mode to another as a result of one of the following three mechanisms:

1. The user writes to the Program Counter.
2. The user sets/clears flags F0, F3, or F5 by writing to the Flag register (R00H).
3. The controller switches automatically when certain initial conditions are provided by the user.

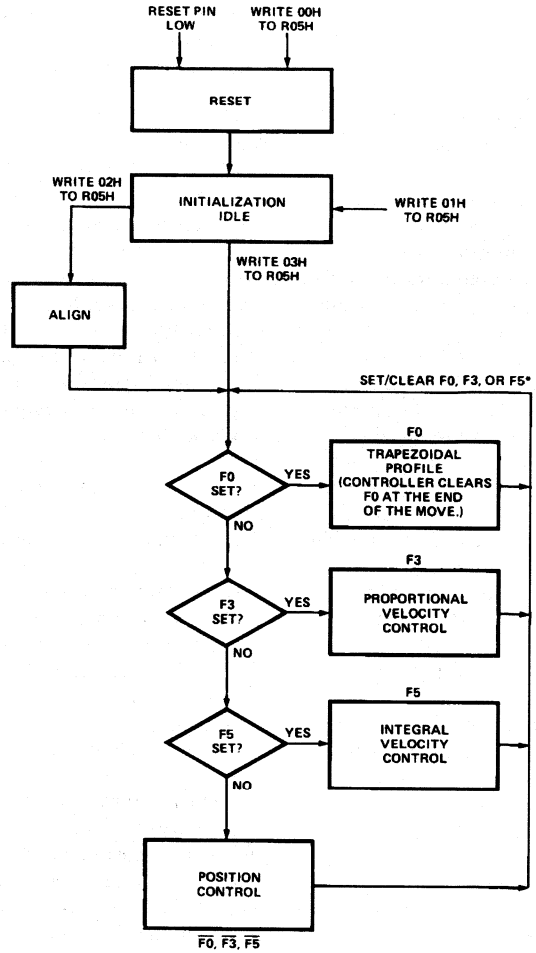


Figure 12. Operation Flowchart.

This section describes the function of each setup routine and control mode and the initial conditions which must be provided by the user to switch from one mode to another. Figure 12 shows a flowchart of the setup routines and control modes, and shows the commands required to switch from one mode to another.

Setup Modes

Hard Reset
Executed by:
-Pulling the RESET pin low (required at power up)

When a hard reset is executed (RESET pin goes low), the following conditions occur:
- All output signal pins are held low except Sign, Data bus, and Motor Command.
- All flags (F0 to F5) are cleared.
- The Pulse pin of the PWM port is set low while the Reset pin is held low. After the Reset pin is released (goes high) the Pulse pin goes high for one cycle of the external clock driving the HCTL-1100. The Pulse pin then returns to a low output.
- The Motor Command port (R08H) is preset to 80H (128D).
- The Commutator logic is cleared.
- The I/O control logic is cleared.
- A soft reset is automatically executed.

Soft Reset
Executed by:
- Writing 00H to R05H, or
- Automatically called after a hard reset

When a soft reset is executed, the following conditions occur:
- The digital filter parameters are preset to
  A (R20H) = E5H (229D)
  B (R21H) = K (R22H) = 40H (64D)
- The Sample Timer (R0FH) is preset to 40H (64D).
- The Status register (R07H) is cleared.
- The Actual Position Counters (R12H, R13H, R14H) are cleared to 0.

From Reset mode, the HCTL-1100 goes automatically to Initialization/Idle mode.

Initialization/Idle
Executed by:
- Writing 01H to R05H, or
- Automatically executed after a hard reset, soft reset, or
- Limit pin goes low.

The Initialization/Idle mode is entered either automatically from Reset, by writing 01H to the Program Counter (R05H) under any conditions, or pulling the Limit pin low.

In the Initialization/Idle mode, the following occur:
- The Initialization/Idle flag (F1) is set.
- The PWM port R09H is set to 00H (zero command).
- The Motor Command port (R08H) is set to 80H (128D) (zero command).
- Previously sampled data stored in the digital filter is cleared.

It is at this point that the user should pre-program all the necessary registers needed to execute the desired control mode. The HCTL-1100 stays in this mode (idling) until a new mode command is given.

Align
Executed by:
- Writing 02H to R05H

The Align mode is executed only when using the commutator feature of the HCTL-1100. This mode automatically aligns multiphase motors to the HCTL-1100's internal Commutator.

The Align mode can be entered only from the Initialization/Idle mode by writing 02H to the Program Counter register (R05H). Before attempting to enter the Align mode, the user should clear all control mode flags and set both the Command Position registers (R0CH, R0DH, and R0EH) and the Actual Position registers (R12H, R13H, and R14H) to zero. After the Align mode has been executed, the HCTL-1100 will automatically enter the Position Control mode and go to position zero. By following this procedure, the largest movement in the Align mode will be one torque cycle of the motor.

The Align mode assumes: the encoder index pulse has been physically aligned to the last motor phase during encoder/motor assembly, the Commutator parameters have been correctly preprogrammed (see the section called Commutator for details), and a hard reset has been executed while the motor is stationary.

The Align mode first disables the Commutator and with open loop control enables the first phase (PHA) and then the last phase (PHC or PHD) to orient the motor on the last phase torque detent. Each phase is energized for 2048 system sampling periods (t). For proper operation, the motor must come to a complete stop during the last phase enable. At this point the Commutator is enabled and commutation is closed loop.

The HCTL-1100 then automatically switches from the Align mode to Position Control mode.

Control Modes

Control flags F0, F3, and F5 in the Flag register (R00H) determine which control mode is executed. Only one control flag can be set at a time. After one of

these control flags is set, the control modes are entered either automatically from Align or from the Initialization/Idle mode by writing 03H to the Program Counter (R05H).

Position Control Mode

Flags: F0 Cleared
F3 Cleared
F5 Cleared

Registers Used:

Register		Function
R00H	R00D	Flag Register
R12H	R18D	Read Actual Position MSB
R13H	R19D	Read Actual Position
R14H	R20D	Read Actual Position LSB
R0CH	R12D	Command Position MSB
R0DH	R13D	Command Position
R0EH	R14D	Command Position LSB

Position Control performs point-to-point position moves with no velocity profiling. The user specifies a 24-bit position command, which the controller compares to the 24-bit actual position. The position error is calculated, the full digital lead compensation is applied and the motor command is output.

The controller will remain position-locked at a destination until a new position command is given.

The actual and command position data is 24-bit two's-complement data stored in six 8-bit registers. Position is measured in encoder quadrature counts.

The command position resides in R0CH (MSB), R0DH, R0EH (LSB). Writing to R0EH latches all 24 bits at once for the control algorithm. Therefore, the command position is written in the sequence R0CH, R0DH and R0EH. The command registers can be read in any desired order.

The actual position resides in R12H (MSB), R13H, and R14H (LSB). Reading R14H latches the upper two bytes into an internal buffer. Therefore, Actual Position registers are read in the order of R14H, R13H, and R12H for correct instantaneous position data.

The largest position move possible in Position Control mode is 7FFFFFH (8,388,607D) quadrature encoder counts.

Proportional Velocity Mode

Flags: F0 Cleared
F3 Set
F5 Cleared

Registers Used:

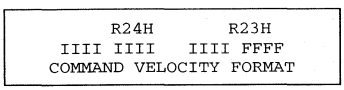
Register		Function
R00H	R00D	Flag Register
R23H	R35D	Command Velocity LSB
R24H	R36D	Command Velocity MSB
R34H	R52D	Actual Velocity LSB
R35H	R53D	Actual Velocity MSB

Proportional Velocity Control performs control of motor speed using only the gain factor, K, for compensation. The dynamic pole and zero lead compensation are not used. (See the "Digital Filter" section of this data sheet.)

```
Example Code to Program Position Moves

    { Begin }
         Hard Reset { HCTL-1100 goes into INIT/IDLE Mode }

         Initialize Filter, Timer, Command Position Registers

         Write 03H to Register R05H
              { HCTL-1100 is now in Position Mode }

         Write Desired Command Position to Command Position Registers
              { Controller Moves to new position }

         Continue writing in new Command Positions
    { end }
```

The command and actual velocity are 16-bit two's-complement words.

The command velocity resides in registers R24H (MSB) and R23H (LSB). These registers are unlatched which means that the command velocity will change to a new velocity as soon as the value in either R23H or R24H is changed. The registers can be read or written to in any order.



The units of velocity are quadrature counts/sample time. To convert from rpm to quadrature counts/sample time, use the formula shown below:

$$Vq = (Vr)(N)(t)(0.01667/rpm\text{-}sec) \quad [9]$$

Where:
Vq = velocity in quadrature counts/sample time
Vr = velocity in rpm
N = 4 times the number of slots in the codewheel (i.e., quadrature counts).
t = The HCTL-1100 sample time in seconds. (See the section on the HCTL-1100's Sample Timer register).

Because the Command Velocity registers (R24H and R23H) are internally interpreted by the HCTL-1100 as 12 bits of integer and 4 bits of fraction, the host processor must multiply the desired command velocity (in quadrature counts/sample time) by 16 before programming it into the HCTL-1100's Command Velocity registers.

The actual velocity is computed only in this algorithm and stored in scratch registers R35H (MSB) and R34H (LSB). There is no fractional component in the actual velocity registers and they can be read in any order.

The controller tracks the command velocity continuously until new mode command is given. The system behavior after a new velocity command is governed only by the system dynamics until a steady state velocity is reached.

Integral Velocity Mode

Flags: F0 Cleared
F3 Cleared
F5 Set to begin move

Registers Used:

Register	Function
R00H R00D	Flag Register
R26H R38D	Acceleration LSB
R27H R39D	Acceleration MSB
R3CH R60D	Command Velocity

Integral Velocity Control performs continuous velocity profiling which is specified by a command velocity and command acceleration. Figure 13 shows the capability of this control algorithm.

The user can change velocity and acceleration any time to continuously profile velocity in time. Once the specified velocity is reached, the HCTL-1100 will maintain that velocity until a new command is specified. Changes between actual velocities occur at the presently specified linear acceleration.

The command velocity is an 8-bit two's-complement word stored in R3CH. The units of velocity are

```
Example Code for Programming Proportional Velocity Mode

    { Begin }
        Hard Reset { HCTL-1100 goes into INIT/IDLE Mode }

        Initialize Filter, Timer, Command Position Registers

        Write 03H to Register R05H
            { HCTL-1100 is now in Position Mode }

        Write Desired Command Velocity (if needed)

        Set Flag F3 {Proportional Velocity Move Begins}

        { System ramps to Command Velocity }

        Continue writing new Command Velocities
    {end}
```

quadrature counts/sample time.

The conversion from rpm to quadrature counts/sample time is shown in equation 9. The Command Velocity register (R3CH) contains only integer data and has no fractional component.

While the overall range of the velocity command is 8 bits, two's-complement, the difference between any two sequential commands cannot be greater than 7 bits in magnitude (i.e., 127 decimal). For example, when the HCTL-1100 is executing a command velocity of 40H (+64D), the next velocity command must fall in the range of 7FH (+127D), the maximum command range, C1H (-63D), the largest allowed difference.

The command acceleration is a 16-bit scalar word stored in R27H and R26H. The upper byte (R27H) is the integer part and the lower byte (R26H) is the fractional part provided for resolution. The integer part has a range of 00H to 7FH. The contents of R26H are internally divided by 256 to produce the

R27H	R26H
0IIIIIII	FFFFFFFF/256

Command Acceleration Format

fractional resolution.

The units of acceleration are quadrature counts/sample time squared.

To convert from rpm/sec to quadrature counts/[sample time]^2, use the formula shown below:

$$Aq = (Ar)(N)(t^2)(0.01667/rpm\text{-}sec) \quad [10]$$

Where:

Aq = Acceleration in quadrature counts/[sample time]^2

Ar = Acceleration in rpm/sec

N = 4 times the number of slots in the codewheel (i.e., quadrature counts)

t = The HCTL-1100 sample time in seconds. (See the section on the HCTL-1100's Sample Timer register).

Because the Command Acceleration registers (R27H and R26H) are internally interpreted by the HCTL-1100 as 8 bits of integer and 8 bits of fraction, the host processor must multiply the desired command acceleration (in quadrature counts/[sample time]^2) by 256 before programming it into the HCTL-1100's Command Acceleration registers.

Internally, the controller performs velocity profiling through position control.

Each sample time, the internal profile generator uses the information which the user has programmed into the Command Velocity register (R3CH) and the Command Acceleration registers (R27H and R26H) to determine the value which will be automatically loaded into the Command Position registers (R0CH, R0DH, and R0EH). After the new command position has been generated, the difference between the value in the Actual Position registers (R12-R13H, and R14H) and the new value in the Command Position registers is calculated as the new position error. This new position error is used by the full digital compensation filter to compute a new motor command output by this sample time. The register block in Figure 3 further shows how the internal profile generator works in Integral Velocity mode. In control theory terms, integral compensation has been added and therefore, this system has zero steady-state error.

Although Integral Velocity Control mode has the advantage over Proportional Velocity mode of zero steady state velocity error, its disadvantage is that the closed

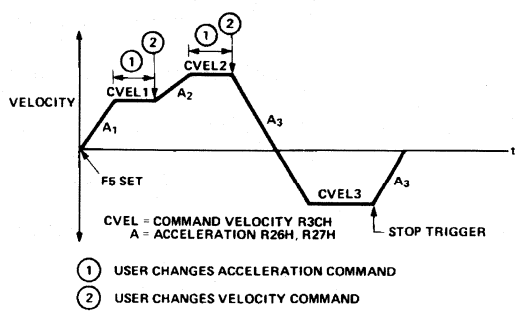


Figure 13. Integral Velocity Modes.

loop stability is more difficult to achieve. In Integral Velocity Control mode the system is actually a position control system and therefore the complete dynamic compensation D(z) is used.

If the external Stop flag F6 is set during this mode signalling an emergency situation, the controller automatically decelerates to zero velocity at the presently specified acceleration factor and stays in this condition until the flag is cleared. The user then can specify new velocity profiling data.

Trapezoid Profile Mode

Flags: F0 Set to begin move
F3 Cleared
F5 Cleared

Registers Used:

Register		Function
R00H	R00D	Flag Register
R07H	R07D	Status Register
R12H	R18D	Read Actual Position MSB
R13H	R19D	Read Actual Position
R14H	R20D	Read Actual Position LSB
R29H	R41D	Final Position LSB
R2AH	R42D	Final Position
R2BH	R43D	Final Position MSB
R26H	R38D	Acceleration LSB
R27H	R39D	Acceleration MSB
R28H	R40D	Maximum Velocity

Trapezoid Profile Control performs point-to-point position moves and profiles the velocity trajectory to a trapezoid or triangle. The user specifies only the desired final position, acceleration and maximum velocity. The controller computes the necessary profile to conform to the command data. If maximum velocity is reached before the distance halfway point, the profile will be trapezoidal, otherwise the profile will be triangular. Figure 14 shows the possible trajectories with Trapezoidal Profile Control.

The command data for Trapezoidal Profile Control mode consists of a final position, a command acceleration, and a maximum velocity. The 24-bit,

```
Example Code for Programming Integral Velocity Mode

     (Begin)
          Hard Reset {HCTL-1100 goes into INIT/IDLE Mode}

          Initialize Filter, Timer, Command Position Registers

          Write 03H to Register R05H
               {HCTL-1100 is now in Position Mode}

          Write Desired Acceleration (if needed)

          Write Desired Maximum Velocity (if needed)

          Set Flag F5 {Integral Velocity Move Begins}

          {System ramps to Maximum Velocity}

          Continue writing new Accelerations and Velocities
     { end }
```

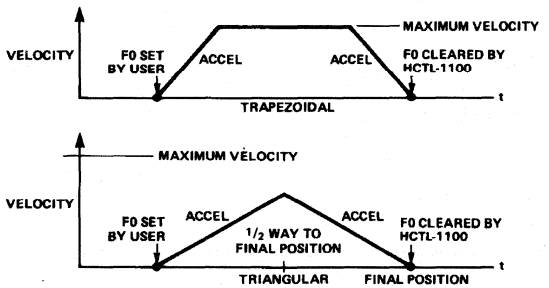


Figure 14. Trapezoidal Profile Mode.

two's-complement final position is written to registers R2BH, (MSB), R2AH, and R29H (LSB). The 16-bit command acceleration resides in registers R27H (MSB) and R26H (LSB). The command acceleration has the same integer and fraction format as discussed in the Integral Velocity Control mode section. The 7-bit maximum velocity is a scalar value with the range of 00H to 7FH (0D to 127D). The maximum velocity has the units of quadrature counts per sample time, and resides in register R28H. The command data registers may be read or written to in any order.

The internal profile generator produces a position profile using the present Command Position (R0CH-R0EH) as the starting point and the Final Position (R2BH-R29H) as the end point.

Once the desired data is entered, the user sets flag F0 in the Flag register (R00H) to commence motion (if the HCTL-1100 is already in Position Control mode).

When the profile generator sends the last position command to the Command Position registers to complete the trapezoidal move, the controller clears flag F0. The HCTL-1100 then automatically goes to Position Control mode with the final position of the trapezoidal move as the command position.

When the HCTL-1100 clears flag F0 it does NOT indicate that the motor and encoder are at the final position NOR that the motor and encoder have stopped. The flag indicates that the command profile has finished. The motor and encoder's true position can only be determined by reading the Actual Position registers. The only way to determine if the motor and encoder have stopped is to read the Actual Position registers at successive intervals.

The status of the Profile flag can be monitored both in the Status register (R07) and at the external Profile pin at any time. While the Profile flag is high NO new command data should be sent to the controller.

Each sample time, the internal profile generator uses the information which the user has programmed into the Maximum Velocity register (R28H), the Command Acceleration registers (R27H and R26H), and the Final Position registers (R2BH, R2AH, and R29H) to determine the value which will be automatically loaded into the Command Position registers (R0EH, R0DH, and R0CH). After the new command position has been generated, the difference between the value in the Actual Position registers (R12H, R13H, and R14H) and the new value in the Command Position registers is calculated as the new position error. This new position error is used by the full digital compensation filter to compute a new motor command output for the sample time. (The register block diagram in Figure 3 further shows how the internal profile generator works in Trapezoidal Profile mode.)

Example Code for Programming Trapezoid Moves

```
{ Begin }
     Hard Reset { HCTL-1100 goes into INIT/IDLE Mode }

     Inititalize Filter, Timer, Command Position Registers

     Write 03H to Register R05H
        { HCTL-1100 is now in Position Mode }

     { Profile #1}

     Write Desired Acceleration

     Write Desired Maximum Velocity

     Write Final Position

     Set Flag F0 {Trapezoid Move Begins, PROF pin goes high}

     Poll PROF pin until it goes low (Move is complete)

     { Profile #2}

     Write Desired Acceleration

     Write Desired Maximum Velocity

     Write Final Position

     Set Flag F0 {Trapezoid Move Begins, PROF pin goes high}

     Poll PROF pin until it goes low (Move is complete)

     { Repeat }
     .
     .
     .
     .
{ end }
```

Applications of the HCTL-1100

Interfacing the HCTL-1100 to Host Processors

The HCTL-1100 looks to the host microprocessor like a bank of 8-bit registers to which the host processor can read and write (i.e., the host processor treats the HCTL-1100 like RAM). The data in these registers controls the operation of the HCTL-1100. The host processor communicates to the HCTL-1100 over a bidirectional multiplexed 8-bit data bus. The four I/O control lines. $\overline{ALE}$, $\overline{CS}$, $\overline{OE}$, and R/$\overline{W}$ execute the data transfers (see Figure 15).

There are three different timing configurations which can be used to give the user greater flexibility to interface the HCTL-1100 to most microprocessors (see Timing diagrams). They are differentiated from one another by the arrangement of the ALE signal with respect to the CS signal. The three timing configurations are listed below.

1. $\overline{\text{ALE}}$, $\overline{\text{CS}}$ non-overlapped
2. $\overline{\text{ALE}}$, $\overline{\text{CS}}$ overlapped
3. $\overline{\text{ALE}}$ within $\overline{\text{CS}}$

Any I/O operation starts by asserting the $\overline{\text{ALE}}$ signal which starts sampling the external bus into an internal address latch. Rising $\overline{\text{ALE}}$ or falling $\overline{\text{CS}}$ during $\overline{\text{ALE}}$ stops the sampling into the address latch.

$\overline{\text{CS}}$ low after rising $\overline{\text{ALE}}$ samples the external bus into the data latch. Rising $\overline{\text{CS}}$ stops the sampling into the data latch, and starts the internal synchronous process.

In the case of a write, the data in the data latch is written into the addressed location. In the case of a read, the addressed location is written into an internal output latch. $\overline{\text{OE}}$ low enables the internal output latch onto the external bus. The $\overline{\text{OE}}$ signal and the internal output latch allow the I/O port to be flexible and avoid bus conflicts during read operations.

It is important that the host microprocessor does not attempt to perform too many I/O operations in a single sample time of the HCTL-1100. Each I/O operation interrupts the execution of the HCTL-1100's internal code for 1 clock cycle. Although extra clock cycles have been allotted in each sample time for I/O operations, the number of extra cycles is reduced as the value programmed into the Sample Timer register (R0FH) is reduced.

Table 5 shows the maximum number of I/O operations allowed under the given conditions.

The number of external clock cycles available for I/O operations in any of the four control modes can be increased by increasing the value in the Sample Timer register (R0FH).

For every unit increase in the Sample Timer register (R0FH) above the minimums shown in Table 5 the user may perform 16 additional I/O operations per sample time.

Interfacing the HCTL-1100 to Amplifiers and Motors

The Motor Command port is the ideal interface to an 8-bit DAC, configured for bipolar output. The data written to the 8-bit Motor Command port by the control algorithms is the internally computed 2's-complement motor command with an 80H offset added. This allows direct interfacing to a DAC. Figure 16 shows a typical DAC interface to the HCTL-1100. An inexpensive DAC, such as MC1408 or equivalent, has its digital inputs directly connected to the Motor Command port. The DAC produces an output current which is converted to a voltage by an operational amplifier. R_O and R_G control the analog offset and gain. The circuit is easily adjusted for +5 V to –5 V operation by first writing 80H to R08H and adjusting R_O for 0 V output. Then FFH is written to R08H and R_G is adjusted until the output is 5 V. Note that 00H in R08H corresponds to –5 V out.

Figure 17 shows an example of how to interface the HCTL-1100 to an H-bridge amplifier. An H-bridge amplifier allows bipolar motor operation with a unipolar power supply.

Table 5. Maximum Number of I/O Allowed

Sample Timer Register Value	Operating Mode	Maximum Number of I/O Operations Allowed per Sample
07H (07D)	Position Control or Prop. Vel. Control	5
OFH (15D)	Position Control or Prop. Vel. Control	133
	Trapezoidal Prof. or Integral Vel. Control	6

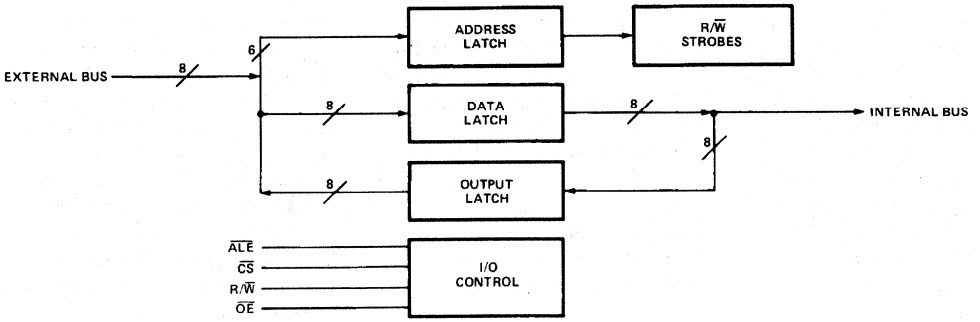


Figure 15. I/O Port Block Diagram.

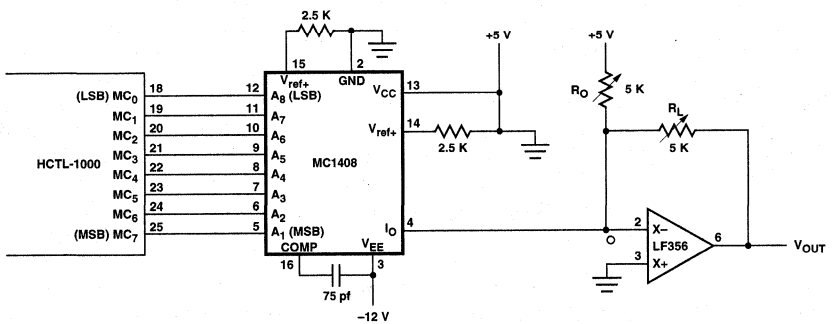


Figure 16. Linear Amplifier Interface.

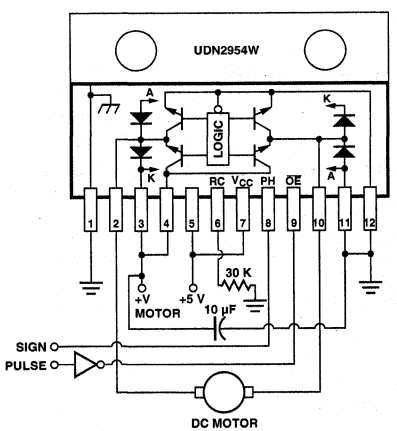


Figure 17. H-Bridge Amplifier Interface.

Additional Information From Hewlett-Packard

Application notes and Application briefs regarding the HCTL-1100 is are from the Hewlett-Packard Motion Control Factory. Please contact your local HP sales representative for more information.

- M003 - Z80 Interface to the HCTL-1100
- M005 - Sample Timer and Digital Filter
- M009 - List of Board Level Vendors Using HCTL-1100
- M010 - HCTL-1100 Trouble Shooting Guide
- M012 - Commutator Port in the HCTL-1100
- M015 - Interfacing the HCTL-1100 to the 8051
- M016 - 8051/HCTL-1100 Stand Alone Controller with RS232 Port
- M018 - The Effects of High-Frequency Noise on the HCTL-1100
- M021 - Interfacing the HCTL-1100 to 68HC11.
- M024 - Using the HCTL-1100 with DC Brush Motors.
- M025 - Using the HCTL-1100 with DC Brushless Motors.
- M026 - Using the HCTL-1100 with Stepper Motors.

Ordering Information

HCTL-1100: 40 Pin DIP Package
HCTL-1100#PLC: 44 Pin PLCC Package

HEWLETT® PACKARD

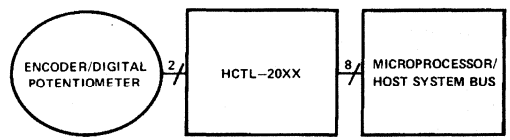
Quadrature Decoder/Counter Interface ICs

Technical Data

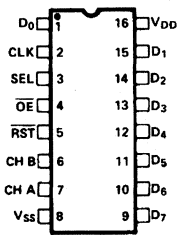
HCTL-2000
HCTL-2016
HCTL-2020

Features

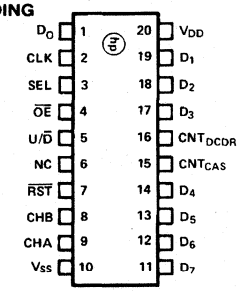
- **Interfaces Encoder to Microprocessor**
- **14 MHz Clock Operation**
- **Full 4X Decode**
- **High Noise Immunity:** Schmitt Trigger Inputs Digital Noise Filter
- **12 or 16-Bit Binary Up/ Down Counter**
- **Latched Outputs**
- **8-Bit Tristate Interface**
- **8, 12, or 16-Bit Operating Modes**
- **Quadrature Decoder Output Signals, Up/Down and Count**
- **Cascade Output Signals, Up/ Down and Count**
- **Substantially Reduced System Software**



DIGITAL MOTION ENCODING



PINOUT A



PINOUT B

Applications

- **Interface Quadrature Incremental Encoders to Microprocessors**
- **Interface Digital Potentiometers to Digital Data Input Buses**

Description

The HCTL-2000, 2016, 2020 are CMOS ICs that perform the quadrature decoder, counter, and bus interface function. The HCTL-20XX family is designed to improve system performance

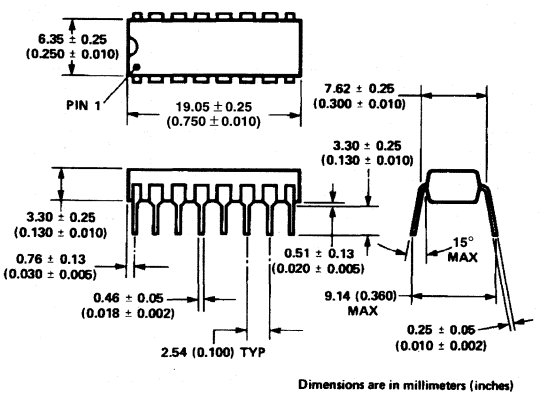
Devices

Part Number	Description	Package Drawing
HCTL-2000	12-bit counter. 14 MHz clock operation.	A
HCTL-2016	All features of the HCTL-2000. 16-bit counter.	A
HCTL-2020	All features of the HCTL-2016. Quadrature decoder output signals. Cascade output signals.	B

ESD WARNING: Standard CMOS handling precautions should be observed with the HCTL-20XX family ICs.

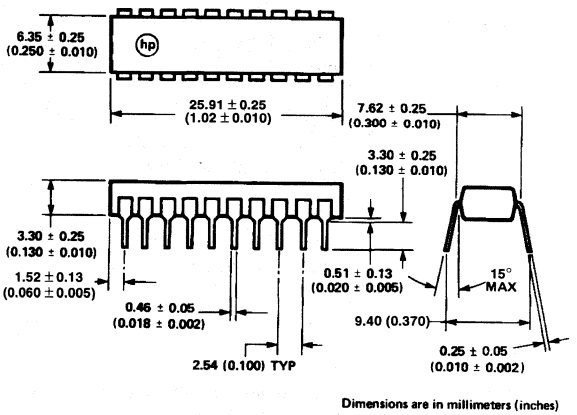
in digital closed loop motion control systems and digital data input systems. It does this by shifting time intensive quadrature decoder functions to a cost effective hardware solution. The entire HCTL-20XX family consists of a 4x quadrature decoder, a binary up/down state counter, and an 8-bit bus interface. The use of Schmitt-triggered CMOS inputs and input noise filters allows reliable operation in noisy environments. The HCTL-2000 contains a 12-bit counter. The HCTL-2016 and 2020 contain a 16-bit counter. The HCTL-2020 also contains quadrature decoder output signals and cascade signals for use with many standard counter ICs. The HCTL-20XX family provides LSTTL compatible tri-state output buffers. Operation is specified for a temperature range from -40 to +85°C at clock frequencies up to 14 MHz.

Package Dimensions



PACKAGE A LEAD FINISH: SOLDER DIPPED

PACKAGE A



PACKAGE B LEAD FINISH: SOLDER DIPPED

PACKAGE B

Operating Characteristics

Table 1. Absolute Maximum Ratings

(All voltages below are referenced to V_{SS})

Parameter	Symbol	Limits	Units
DC Supply Voltage	V_{DD}	-0.3 to +5.5	V
Input Voltage	V_{IN}	-0.3 to V_{DD} +0.3	V
Storage Temperature	T_S	-40 to +125	°C
Operating Temperature	T_A[1]	-40 to +85	°C

Table 2. Recommended Operating Conditions

Parameter	Symbol	Limits	Units
DC Supply Voltage	V_{DD}	+4.5 to +5.5	V
Ambient Temperature	T_A[1]	-40 to +85	°C

Table 3. DC Characteristics V_{DD} = 5 V ± 5%; T_A = -40 to 85°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IL}[2]	Low-Level Input Voltage				1.5	V
V_{IH}[2]	High-Level Input Voltage		3.5			V
V_{T+}	Schmitt-Trigger Positive-Going Threshold			3.5	4.0	V
V_{T-}	Schmitt-Trigger Negative-Going Threshold		1.0	1.5		V
V_H	Schmitt-Trigger Hysteresis		1.0	2.0		V
I_{IN}	Input Current	V_{IN} = V_{SS} or V_{DD}	-10	1	+10	µA
V_{OH}[2]	High-Level Output Voltage	I_{OH} -1.6 mA	2.4	4.5		V
V_{OL}[2]	Low-Level Output Voltage	I_{OL} = +4.8 mA		0.2	0.4	V
I_{OZ}	High-Z Output Leakage Current	V_O = V_{SS} or V_{DD}	-10	1	+10	µA
I_{DD}	Quiescent Supply Current	V_{IN} = V_{SS} or V_{DD}, V_O = HiZ		1	5	µA
C_{IN}	Input Capacitance	Any Input[3]		5		pF
C_{OUT}	Output Capacitance	Any Output[3]		6		pF

Notes:
1. Free air.
2. In general, for any V_{DD} between the allowable limits (+4.5 V to +5.5 V), V_{IL} = 0.3 V_{DD} and V_{IH} = 0.7 V_{DD}; typical values are V_{OH} = V_{DD} - 0.5 V @ I_{OH} = -40 µA and V_{OL} = V_{SS} + 0.2 V @ I_{OL} = 1.6 mA.
3. Including package capacitance.

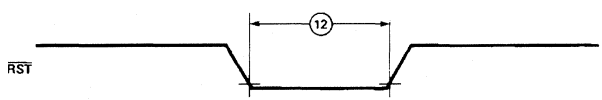


Figure 1. Reset Waveform.

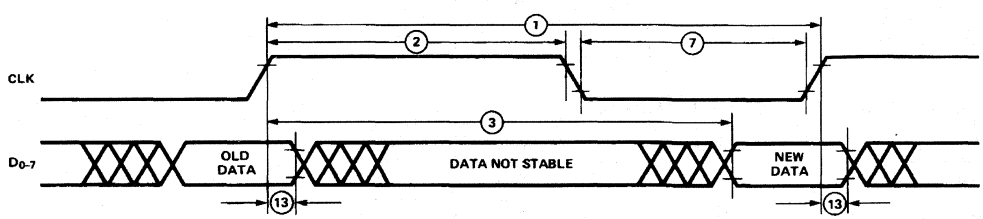


Figure 2. Waveform for Positive Clock Related Delays.

Functional Pin Description

Table 4. Functional Pin Descriptions

Symbol	Pin 2000/2016	Pin 2020	Description
V_{DD}	16	20	Power Supply
V_{SS}	8	10	Ground
CLK	2	2	CLK is a Schmitt-trigger input for the external clock signal.
CHA CHB	7 6	9 8	CHA and CHB are Schmitt-trigger inputs which accept the outputs from a quadrature encoded source, such as incremental optical shaft encoder. Two channels, A and B, nominally 90 degrees out of phase, are required.
$\overline{RST}$	5	7	This active low Schmitt-trigger input clears the internal position counter and the position latch. It also resets the inhibit logic. $\overline{RST}$ is asynchronous with respect to any other input signals.
$\overline{OE}$	4	4	This CMOS active low input enables the tri-state output buffers. The $\overline{OE}$ and SEL inputs are sampled by the internal inhibit logic on the falling edge of the clock to control the loading of the internal position data latch.
SEL	3	3	This CMOS input directly controls which data byte from the position latch is enabled into the 8-bit tri-state output buffer. As in $\overline{OE}$ above, SEL also controls the internal inhibit logic. **SEL** / **BYTE SELECTED** 0 / High 1 / Low
CNT_{DCDR}		16	A pulse is presented on this LSTTL-compatible output when the quadrature decoder has detected a state transition.
$U/\overline{D}$		5	This LSTTL-compatible output allows the user to determine whether the IC is counting up or down and is intended to be used with the CNT_{DCDR} and CNT_{CAS} outputs. The proper signal U (high level) or $\overline{D}$ (low level) will be present before the rising edge of the CNT_{DCDR} and CNT_{CAS} outputs.
CNT_{CAS}		15	A pulse is presented on this LSTTL-compatible output when the HCTL-2020 internal counter overflows or underflows. The rising edge on this waveform may be used to trigger an external counter.
D0	1	1	These LSTTL-compatible tri-state outputs form an 8-bit output port through which the contents of the 12/16-bit position latch may be read in 2 sequential bytes. The high byte, containing bits 8-15, is read first (on the HCTL-2000, the most significant 4 bits of this byte are set to 0 internally). The lower byte, bits 0-7, is read second.
D1	15	19	
D2	14	18	
D3	13	17	
D4	12	14	
D5	11	13	
D6	10	12	
D7	9	11	
NC		6	Not connected - this pin should be left floating.

Switching Characteristics

Table 5. Switching Characteristics Min/Max specifications at V_{DD} = 5.0 ± 5%, T_A = -40 to + 85°C.

Symbol Description			Min.	Max.	Units
1	t_{CLK}	Clock period	70		ns
2	t_{CHH}	Pulse width, clock high	28		ns
3	t_{CD}[1]	Delay time, rising edge of clock to valid, updated count information on D0-7		65	ns
4	t_{ODE}	Delay time, $\overline{OE}$ fall to valid data		65	ns
5	t_{ODZ}	Delay time, $\overline{OE}$ rise to Hi-Z state on D0-7		40	ns
6	t_{SDV}	Delay time, SEL valid to stable, selected data byte (delay to High Byte = delay to Low Byte)		65	ns
7	t_{CLH}	Pulse width, clock low	28		ns
8	t_{SS}[2]	Setup time, SEL before clock fall	20		ns
9	t_{OS}[2]	Setup time, $\overline{OE}$ before clock fall	20		ns
10	t_{SH}[2]	Hold time, SEL after clock fall	0		ns
11	t_{OH}[2]	Hold time, $\overline{OE}$ after clock fall	0		ns
12	t_{RST}	Pulse width, $\overline{RST}$ low	28		ns
13	t_{DCD}	Hold time, last position count stable on D0-7 after clock rise	10		ns
14	t_{DSD}	Hold time, last data byte stable after next SEL state change	5		ns
15	t_{DOD}	Hold time, data byte stable after $\overline{OE}$ rise	5		ns
16	t_{UDD}	Delay time, U/$\overline{D}$ valid after clock rise		45	ns
17	t_{CHD}	Delay time, CNT_{DCDR} or CNT_{CAS} high after clock rise		45	ns
18	t_{CLD}	Delay time, CNT_{DCDR} or CNT_{CAS} low after clock fall		45	ns
19	t_{UDH}	Hold time, U/$\overline{D}$ stable after clock rise	10		ns
20	t_{UDCS}	Setup time, U/$\overline{D}$ valid before CNT_{DCDR} or CNT_{CAS} rise	t_{CLK}-45		ns
21	t_{UDCH}	Hold time, U/$\overline{D}$ stable after CNT_{DCDR} or CNT_{CAS} rise	t_{CLK}-45		ns

Notes:
1. t_{CD} specification and waveform assume latch not inhibited.
2. t_{SS}, t_{OS}, t_{SH}, t_{OH} only pertain to proper operation of the inhibit logic. In other cases, such as 8 bit read operations, these setup and hold times do not need to be observed.

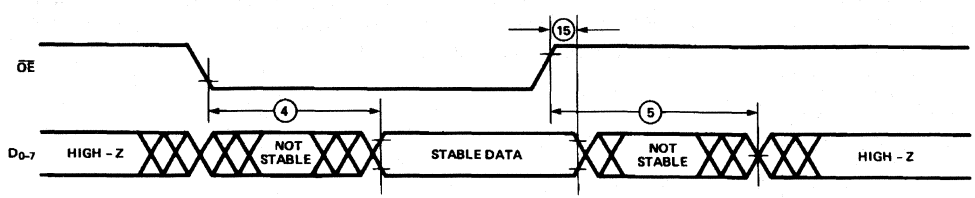


Figure 3. Tri-State Output Timing.

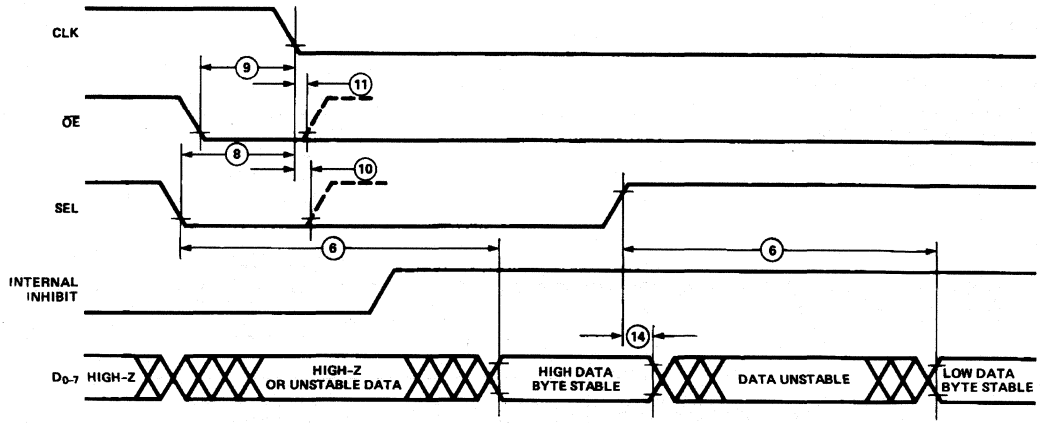


Figure 4. Bus Control Timing.

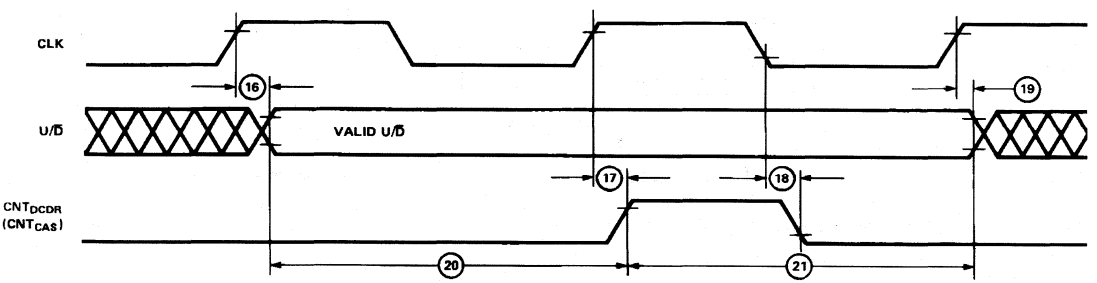


Figure 5. Decoder, Cascade Output Timing (HCTL-2020 only).

Operation

A block diagram of the HCTL-20XX family is shown in Figure 6. The operation of each major function is described in the following sections.

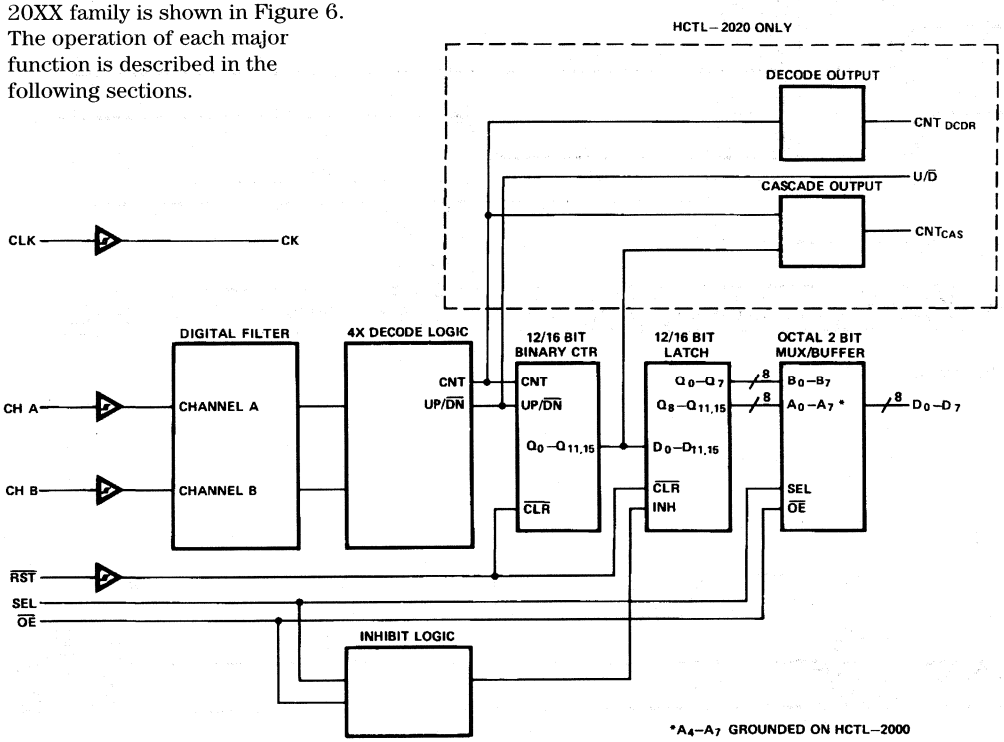


Figure 6. Simplified Logic Diagram.

Digital Noise Filter

The digital noise filter section is responsible for rejecting noise on the incoming quadrature signals. The input section uses two techniques to implement improved noise rejection. Schmitt-trigger inputs and a three-clock-cycle delay filter combine to reject low level noise and large, short duration noise spikes that typically occur in motor system applications. Both common mode and differential mode noise are rejected. The user benefits from these techniques by improved integrity of the data in the counter. False counts triggered by noise are avoided.

Figure 7 shows the simplified schematic of the input section. The signals are first passed through a Schmitt trigger buffer to address the problem of input signals with slow rise times and low level noise (approximately < 1 V). The cleaned up signals are then passed to a four-bit delay filter. The signals on each channel are sampled on rising clock edges. A time history of the signals is stored in the four-bit shift register. Any change on the input is tested for a stable level being present for three consecutive rising clock edges. Therefore, the filtered output waveforms can change only after an input level has the same value for three consecutive rising clock edges. Refer to Figure 8 which shows the timing diagram. The result of this circuitry is that short noise spikes between rising clock edges are ignored and pulses shorter than two clock periods are rejected.

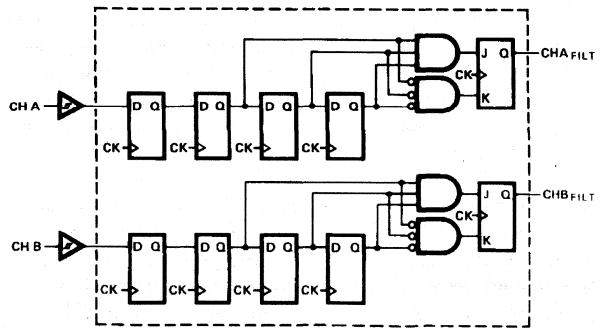


Figure 7. Simplified Digital Noise Filter Logic.

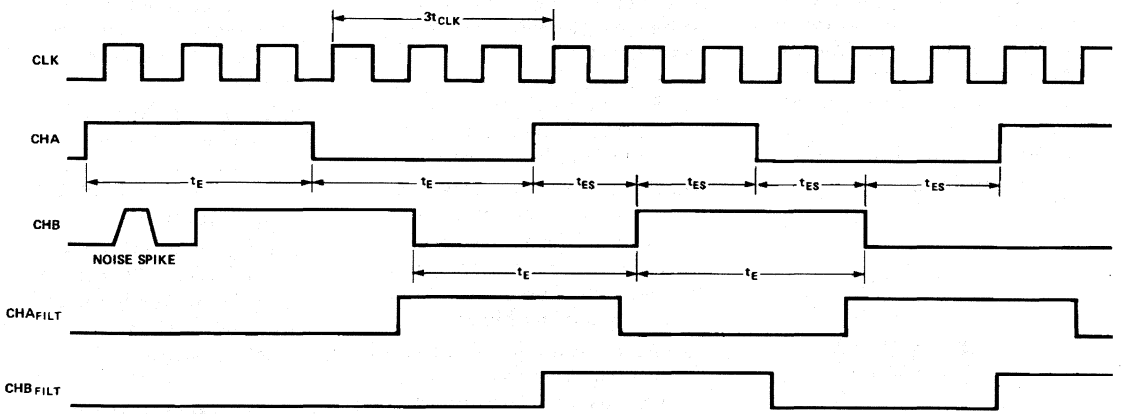


Figure 8. Signal Propagation through Digital Noise Filter.

Quadrature Decoder

The quadrature decoder decodes the incoming filtered signals into count information. This circuitry multiplies the resolution of the input signals by a factor of four (4X decoding). When using an encoder for motion sensing, the user benefits from the increased resolution by being able to provide better system control.

The quadrature decoder samples the outputs of the CHA and CHB filters. Based on the past binary state of the two signals and the present state, it outputs a count signal and a direction signal to the internal position counter. In the case of the HCTL-2020, the signals also go to external pins 5 and 16 respectively.

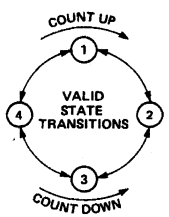
Figure 9 shows the quadrature states and the valid state transitions. Channel A leading channel B results in counting up. Channel B leading channel A results in counting down. Illegal state transitions, caused by faulty encoders or noise severe enough to pass through the filter, will produce an erroneous count.

Design Considerations

The designer should be aware that the operation of the digital filter places a timing constraint on the relationship between incoming quadrature signals and the external clock. Figure 8 shows the timing waveform with an incremental encoder input. Since an input has to be stable for three rising clock edges, the encoder pulse width (t_E - low or high) has to be greater than three clock periods ($3t_{CLK}$). This guarantees that the asynchronous input will be stable during three consecutive rising clock edges. A realistic design also has to take

into account finite rise times of the waveforms, asymmetry of the waveforms, and noise. In the presence of large amounts of noise, t_E should be much greater than $3t_{CLK}$ to allow for the interruption of the consecutive level sampling by the three-bit delay filter. It should be noted that a change on the inputs that is qualified by the filter will internally propagate in a maximum of seven clock periods.

The quadrature decoder circuitry imposes a second timing constraint between the external clock and the input signals. There must be at least one clock period between consecutive quadrature states. As shown in Figure 9, a quadrature state is defined by consecutive edges on both channels. Therefore, t_{ES} (encoder state period) > t_{CLK}. The designer must account for deviations from the nominal 90 degree phasing of input signals to guarantee that $t_{ES} > t_{CLK}$.



CHA	CHB	STATE
1	0	1
1	1	2
0	1	3
0	0	4

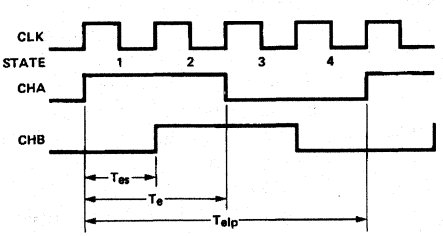


Figure 9. 4x Quadrature Decoding.

Position Counter

This section consists of a 12-bit (HCTL-2000) or 16-bit (HCTL-2016/2020) binary up/down counter which counts on rising clock edges as explained in the Quadrature Decoder Section. All 12 or 16 bits of data are passed to the position data latch. The system can use this count data in several ways:

A. System total range is ≤ 12 or 16 bits, so the count represents "absolute" position.

B. The system is cyclic with ≤ 12 or 16 bits of count per cycle. RST is used to reset the counter every cycle and the system uses the data to interpolate within the cycle.

C. System count is > 8, 12, or 16 bits, so the count data is used as a relative or incremental position input for a system software computation of absolute position. In this case counter rollover occurs. In order to prevent loss of position information, the processor must read the outputs of the IC before the count increments one-half of the maximum count capability (i.e. 127. 2047, or 32,767 quadrature counts). Two's-complement arithmetic is normally used to compute position from these periodic position updates. Three modes can be used:

1. The IC can be put in 8-bit mode by tying the SEL line high, thus simplifying IC interface. The outputs must then be read at least once every 127 quadrature counts.
2. The HCTL-2000 can be used in 12-bit mode and sampled at least once every 2047 quadrature counts.
3. The HCTL-2016 or 2020 can be used in 16-bit mode and sampled at least once every 32,767 quadrature counts.

D. The system count is > 16 bits so the HCTL-2020 can be cascaded with other standard counter ICs to give absolute position.

Position Data Latch

The position data latch is a 12/16-bit latch which captures the position counter output data on each rising clock edge, except when its inputs are disabled by the inhibit logic section during two-byte read operations. The output data is passed to the bus interface section. When active, a signal from the inhibit logic section prevents new data from being captured by the latch, keeping the data stable while successive reads are made through the bus section. The latch is automatically reenabled at the end of these reads. The latch is cleared to 0 asynchronously by the RST signal.

Inhibit Logic

The Inhibit Logic Section samples the OE and $\overline{SEL}$ signals on the falling edge of the clock and, in response to certain conditions (see Figure 10 below), inhibits the position data latch. The RST signal asynchronously clears the inhibit logic, enabling the latch. A simplified logic diagram of the inhibit circuitry is illustrated in Figure 11.

Bus Interface

The bus interface section consists of a 16 to 8 line multiplexer and an 8-bit, three-state output buffer. The multiplexer allows independent access to the low and high bytes of the position data latch. The SEL and $\overline{OE}$ signals determine which byte is output and whether or not the output bus is in the high-Z state. In the case of the HCTL-2000 the data latch is only 12 bits wide and the upper four bits of the high byte are internally set to zero.

Quadrature Decoder Output (HCTL-2020 Only)

The quadrature decoder output section consists of count and up/down outputs derived from the 4X decode logic of the HCTL-2020. When the decoder has detected a count, a pulse, one-half clock cycle long, will be output on the CNT_{DCDR} pin. This output will occur during the clock cycle in which the internal counter is updated. The U/D pin will be set to the proper voltage level one clock cycle before the rising edge of the CNT_{DCDR} pulse, and held one clock cycle after the rising edge of the CNT_{DCDR} pulse. These outputs are not affected by the inhibit logic. See Figures 5 and 12 for detailed timing.

Cascade Output (HCTL-2020 Only)

The cascade output also consists of count and up/down outputs. When the HCTL-2020 internal counter overflows or underflows, a pulse, one-half clock cycle long, will be output on the CNT_{CAS} pin. This output will occur during the clock cycle in which the internal counter is updated. The U/D pin will be set to the proper voltage level one clock cycle before the rising edge of the CNT_{CAS} pulse, and held one clock cycle after the rising edge of the CNT_{CAS} pulse. These outputs are not affected by the inhibit logic. See Figures 5 and 12 for detailed timing.

Step	SEL	$\overline{OE}$	CLK	Inhibit Signal	Action
1	L	L	⌐	1	Set inhibit; read high byte
2	H	L	⌐	1	Read low byte; starts reset
3	X	H	⌐	0	Completes inhibit logic reset

Figure 10. Two Byte Read Sequence.

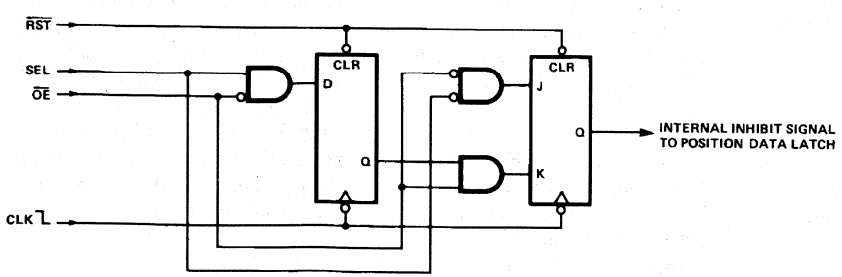
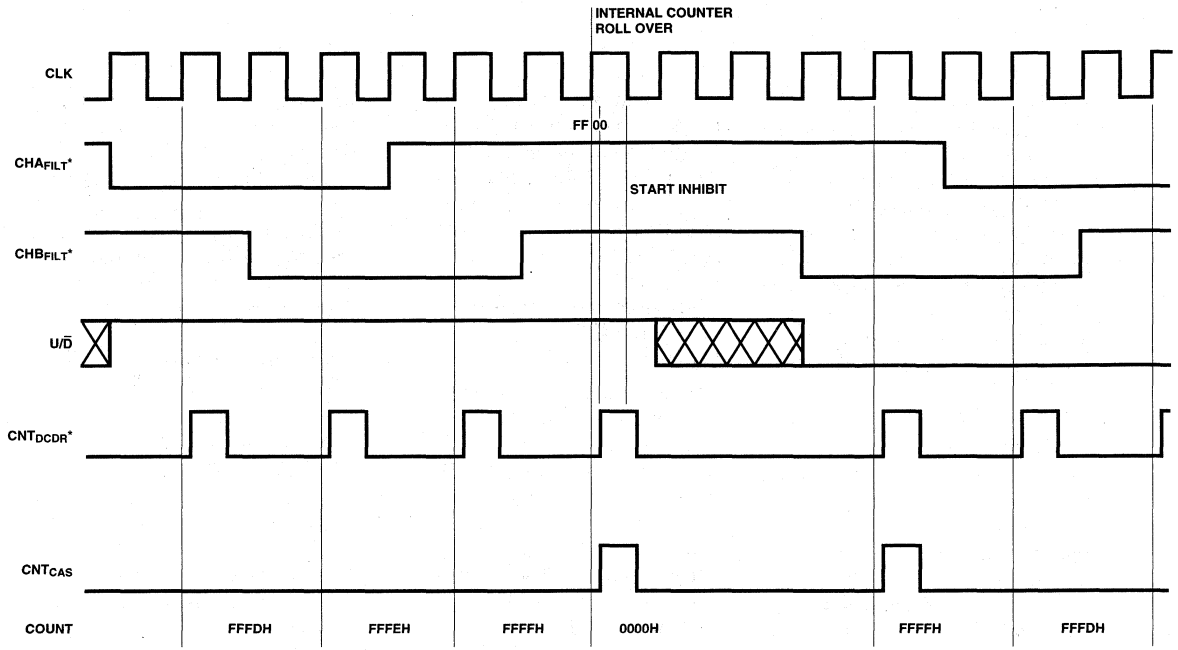


Figure 11. Simplified Inhibit Logic.



*CHA$_{FILT}$ AND CHB$_{FILT}$ ARE THE OUTPUTS OF THE DIGITAL NOISE FILTER (SEE FIGURES 7 AND 8).

Figure 12. Decode and Cascade Output Diagram.

Cascade Considerations (HCTL-2020 Only)

The HCTL-2020's cascading system allows for position reads of more than two bytes. These reads can be accomplished by latching all of the bytes and then reading the bytes sequentially over the 8-bit bus. It is assumed here that, externally, a counter followed by a latch is used to count any count that exceeds 16 bits. This configuration is compatible with the HCTL-2020 internal counter/latch combination.

Consider the sequence of events for a read cycle that starts as the HCTL-2020's internal counter rolls over. On the rising clock edge, count data is updated in the internal counter, rolling it over. A count-cascade pulse (CNT_{CAS}) will be generated with some delay after the rising clock edge (t_{CHD}). There will be additional propagation delays through the external counters and registers. Meanwhile, with SEL and OE low to start the read, the internal latches are inhibited at the falling edge and do not update again till the inhibit is reset. If the CNTCAS pulse now toggles the external counter and this count gets latched a major count error will occur. The count error is because the external latches get updated when the internal latch is inhibited.

Valid data can be ensured by latching the external counter data when the high byte read is started (SEL and OE low). This latched external byte corresponds to the count in the inhibited internal latch. The cascade pulse that occurs during the clock cycle when the read begins gets counted by the external counter and is not lost.

For example, suppose the HCTL-2020 count is at FFFFH and an external counter is at F0H, with the count going up. A count occurring in the HCTL-2020 will cause the counter to roll over and a cascade pulse will be generated. A read starting on this clock cycle will show FFFFH from the HCTL-2020. The external latch should read F0H, but if the host latches the count after the cascade signal propagates through, the external latch will read F1H.

General Interfacing

The 12-bit (HCTL-2000) or 16-bit (HCTL-2016/2020) latch and inhibit logic allows access to 12 or 16 bits of count with an 8-bit bus. When only 8-bits of count are required, a simple 8-bit (1-byte) mode is available by holding SEL high continuously. This disables the inhibit logic. $\overline{OE}$ provides control of the tri-state bus, and read timing is shown in Figures 2 and 3.

For proper operation of the inhibit logic during a two-byte read, $\overline{OE}$ and SEL must be synchronous with CLK due to the falling edge sampling of $\overline{OE}$ and SEL.

The internal inhibit logic on the HCTL-20XX family inhibits the transfer of data from the counter to the position data latch during the time that the latch outputs are being read. The inhibit logic allows the microprocessor to first read the high order 4 or 8 bits from the latch and then read the low order 8 bits from the latch. Meanwhile, the counter can continue to keep track of the quadrature states from the CHA and CHB input signals.

Figure 11 shows the simplified inhibit logic circuit. The operation of the circuitry is illustrated in the read timing shown in Figure 13.

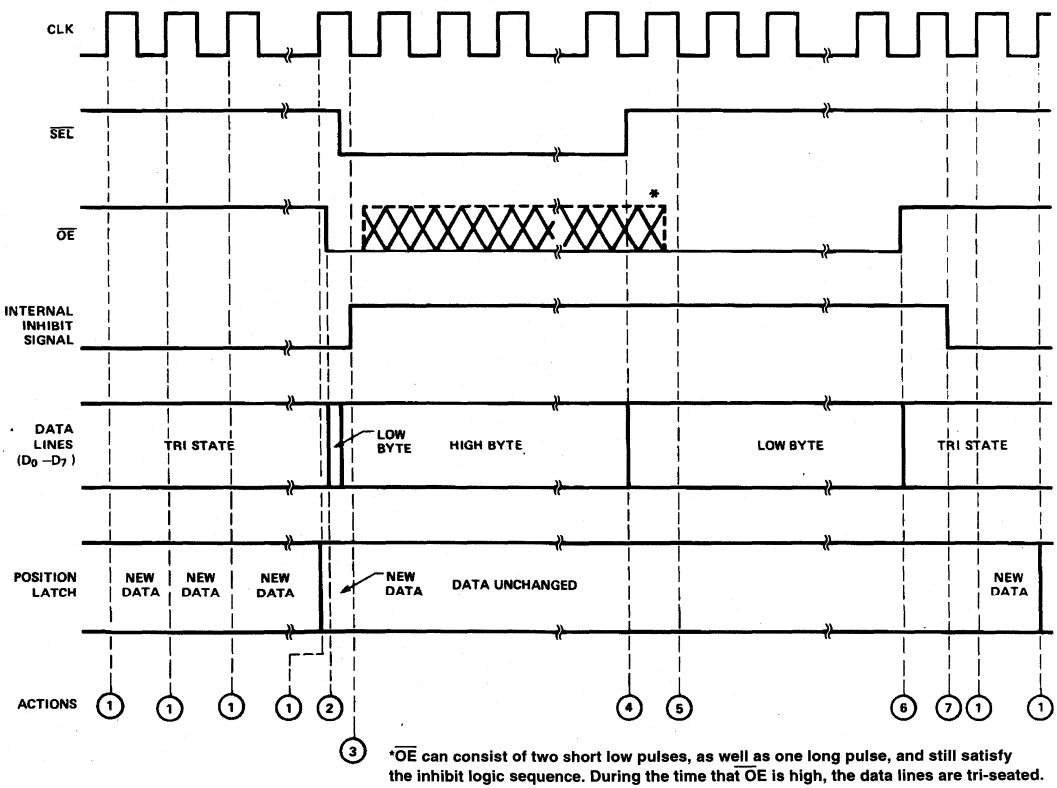


Figure 13. Typical Interface Timing.

Actions

1. On the rising edge of the clock, counter data is transferred to the position data latch, provided the inhibit signal is low.
2. When $\overline{OE}$ goes low, the outputs of the multiplexer are enabled onto the data lines. If SEL is low, then the high order data bytes are enabled onto the data lines. If SEL is high, then the low order data bytes are enabled onto the data lines.
3. When the IC detects a low on OE and SEL during a falling clock edge, the internal inhibit signal is activated. This blocks new data from being transferred from the counter to the position data latch.
4. When SEL goes high, the data outputs change from the high byte to the low byte.
5. The first of two reset conditions for the inhibit logic is met when the IC detects a logic high on SEL and a logic low on OE during a falling clock edge.
6. When OE goes high, the data lines change to a high impedance state.
7. The IC detects a logic high on OE during a falling clock edge. This satisfies the second reset condition for the inhibit logic.

Interfacing the HCTL-2020 to a Motorola 6802/8 and Cascading the Counter for 24 Bits

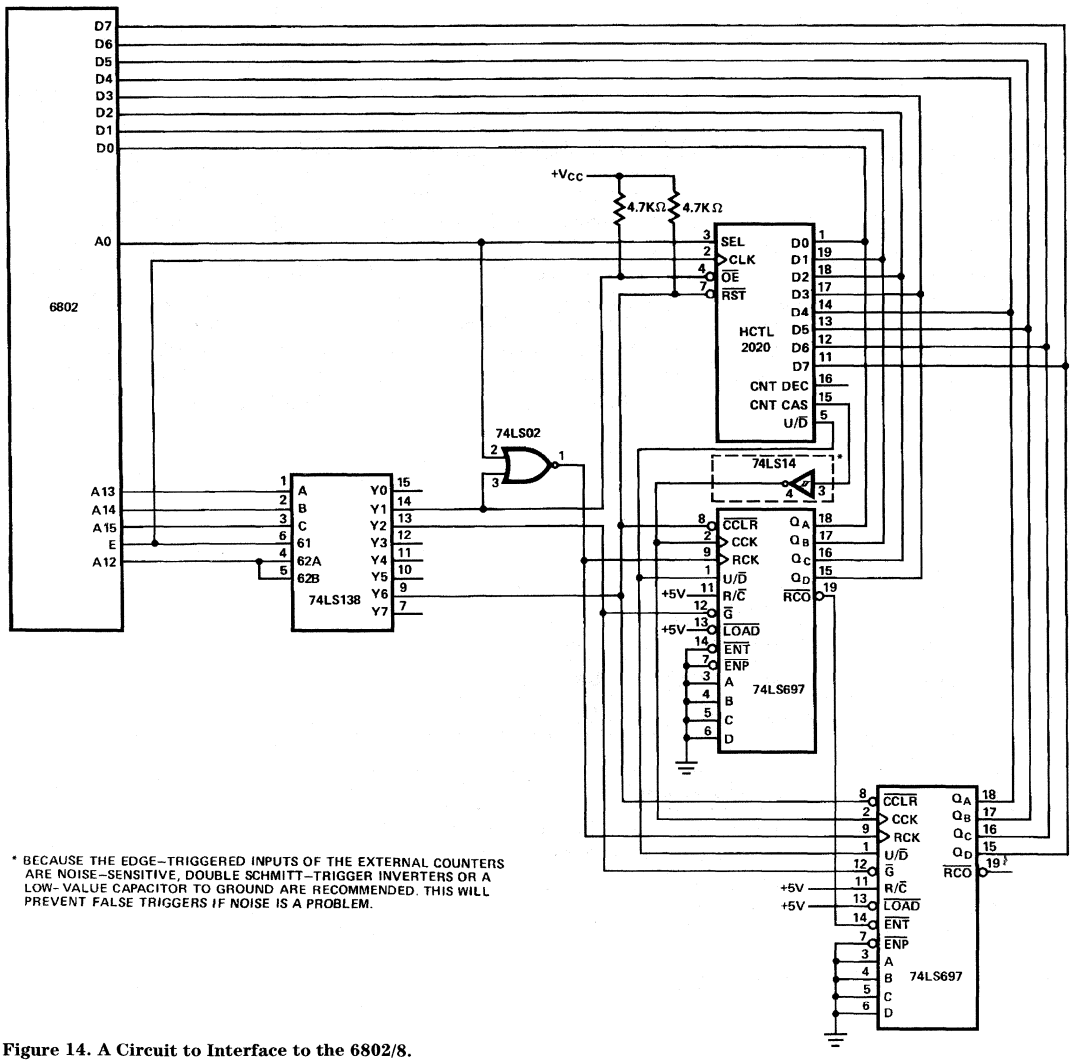


Figure 14. A Circuit to Interface to the 6802/8.

In this circuit an interface to a Motorola 6802/8 and a cascading scheme for a 24-bit counter are shown. This circuit provides a minimum part count by: 1) using two 74LS697 Up/Down counters with output registers and tri-state outputs and 2) using a Motorola 6802/8 LDX instruction which stores 16 bits of data into the index registers in two consecutive clock cycles.

The HCTL-2020 $\overline{OE}$ and the 74LS697 $\overline{G}$ lines are decoded from Address lines A15-A13. This results in counter data being enabled onto the bus whenever an external memory access is made to locations 4XXX or 2XXX. Address line A12 and processor clock E enables the 74LS138. The processor clock E is also used to clock the HCTL-2020. Address AO is connected directly to the SEL pin on the HCTL-2020. This line selects the low or high byte of data from the HCTL-2020.

Cascading is accomplished by connecting the CNT_{CAS} output on the HCTL-2020 with the counter clock (CCK) input on both 74LS697s. The U/D pin on the HCTL-2020 and the U/D pin on both 74LS697s are also directly connected for easy expansion. The RCO of the first 4-bit 74LS697 is connected to the ENT pin of the second 74LS697. This enables the second counter only when there is a RCO signal on the first counter.

This configuration allows the 6802 to read both data bytes with a single double-byte fetch instruction (LDX 2XX0). This instruction is a five cycle instruction which reads external memory location 2XX0 and stores the high order byte into the high byte of the index register. Memory location 2XX1 is next read and stored in the low order byte of the index register. The high byte of counter data is clocked into the 74LS697 registers when SEL is low and OE goes low. This upper byte can be read at any time by pulling the 74LS697 G low when reading address 4XXX. Figure 15 shows memory addresses and gives an example of reading the HCTL-2020. Figure 16 shows the interface timing for the circuit.

Address	Function
CXXX	Reset Counters
4XXX	Enable High Byte on Data Lines
2XX0	Enable Mid Byte on Data Lines
2XX1	Enable Low Byte on Data Lines

Read Example	
LDX 2000 STX 0100	Loads mid byte and then low byte into memory locations 0100 and 0101
LDAA 4000 STAA 0102	Loads the high byte into memory location 0102

Figure 15. Memory Addresses and Read Example.

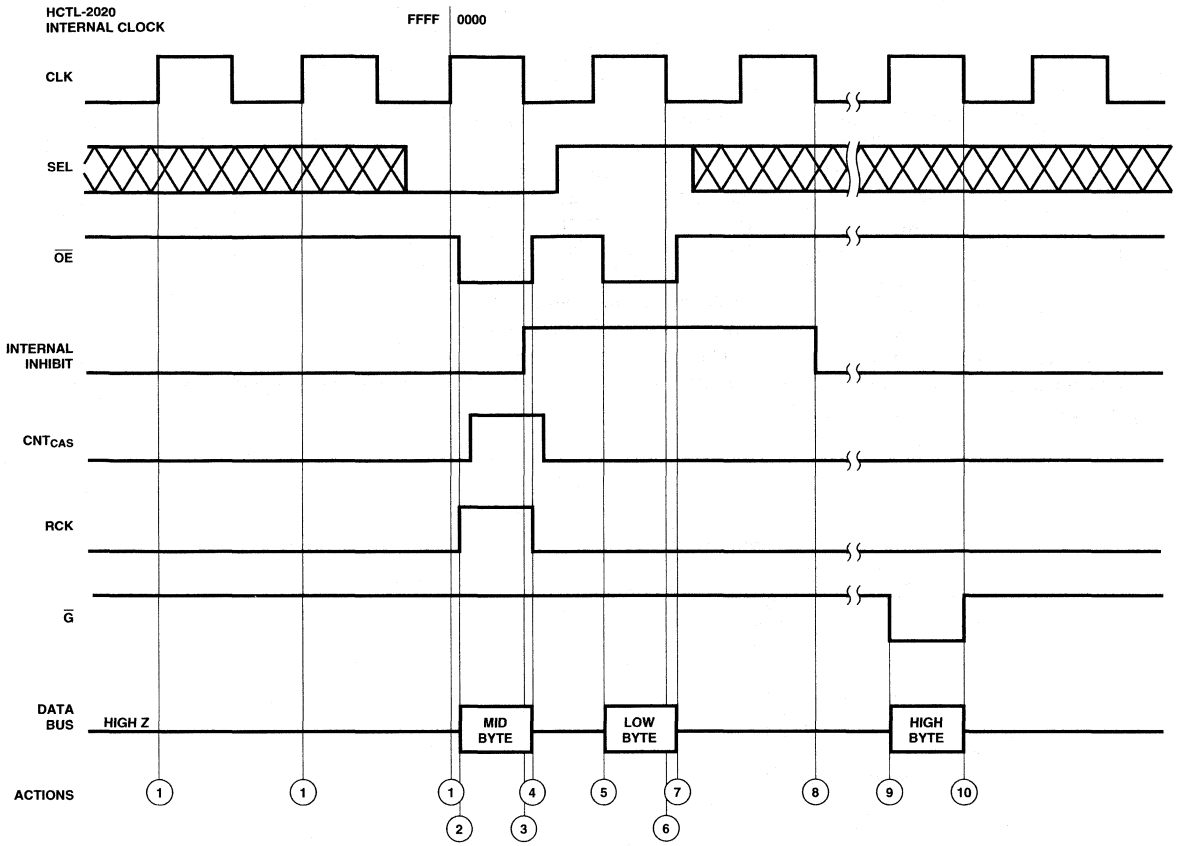


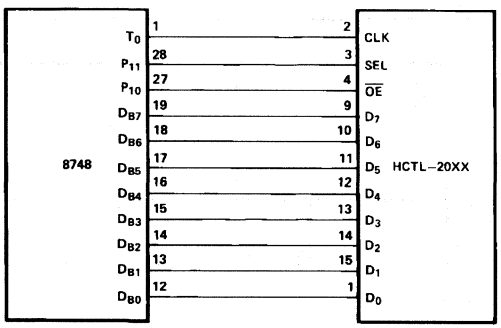
Figure 16. Interface Timing for the 6802/8.

Actions

1. The microprocessor clock output is E. If the internal HCTL-2020 inhibit is not active, new data is transferred from the internal counter to the position data latch.
2. An even address output from the 6802 causes SEL to go low. When E goes high, the address decoder output for the HCTL-2020 $\overline{OE}$ signal goes low. This causes the HCTL-2020 to output the middle byte of the system counter (high byte of the HCTL-2020 counter). This middle byte, FFFFH is available at (2) through (4), the first time OE is low. In this example an overflow has occurred and $\overline{OE}$ has been pulled low to start a read cycle. SEL and OE are gated to give RCK which latches the external high byte, equal to 00H. The falling edge, of the CNT_{CAS} signal counts up the external counter to 0001H.
3. With the first negative edge of the clock after SEL and OE are low the internal latches are inhibited from counting and the 6802 reads the high byte in.
4. $\overline{OE}$ goes high and the data bus goes into a high impedance state.
5. $\overline{OE}$ is low and SEL is high and the low byte is enabled onto the data bus. The low byte is valid through (7).
6. With the first negative edge after $\overline{OE}$ and SEL go high, the first of the two HCTL-2020 inhibit reset conditions is met and the 6802 reads the low byte in.
7. The data bus returns to the high impedance state, when OE goes high.
8. With the first negative edge of the clock after OE goes high, inhibit reset is complete.
9. With the positive going edge of the clock, G is asserted and the external high byte, 00H is available on the data bus from 9 through 10 and the 6802 reads the high byte in at (10).

Interfacing the HCTL-20XX to an Intel 8748

The circuit shown in Figure 17 shows the connections between an HCTL-20XX and an 8748. Data lines D0-D7 are connected to the 8748 bus port. Bits 0 and 1 of port 1 are used to control the OE and SEL inputs of the HCTL-20XX respectively. T0 is used to provide a clock signal to the HCTL-20XX. The frequency of T0 is the crystal frequency divided by 3. T0 must be enabled by executing the ENT0 CLK instruction after each system reset, but prior to the first encoder position change. An 8748 program which interfaces to the circuit in Figure 17 is given in Figure 18. The resulting interface timing is shown in Figure 19.



* NOTE: PIN NUMBERS ARE DIFFERENT FOR THE HCTL-2020.

Figure 17. An HCTL-20XX-to-Intel 8748 Interface.

LOC	Object Code	Source Statements	Comments
000	99 00	ANL P1, 00H	Enable output and higher order bits
002	08	INS A, BUS	Load higher order bits into ACC
003	A8	MOVE R0, A	Move data to register 0
004	89 02	ORL P1, 02H	Enable output and lower order bits
006	08	INS A, BUS	Load order bits into AC
008	A9	MOV R1, A	Move data to register 1
009	89 03	ORL P1, 03H	Disable outputs
00B	93	RETR	Return

Figure 18. A Typical Program for Reading HCTL-20XX with an 8748.

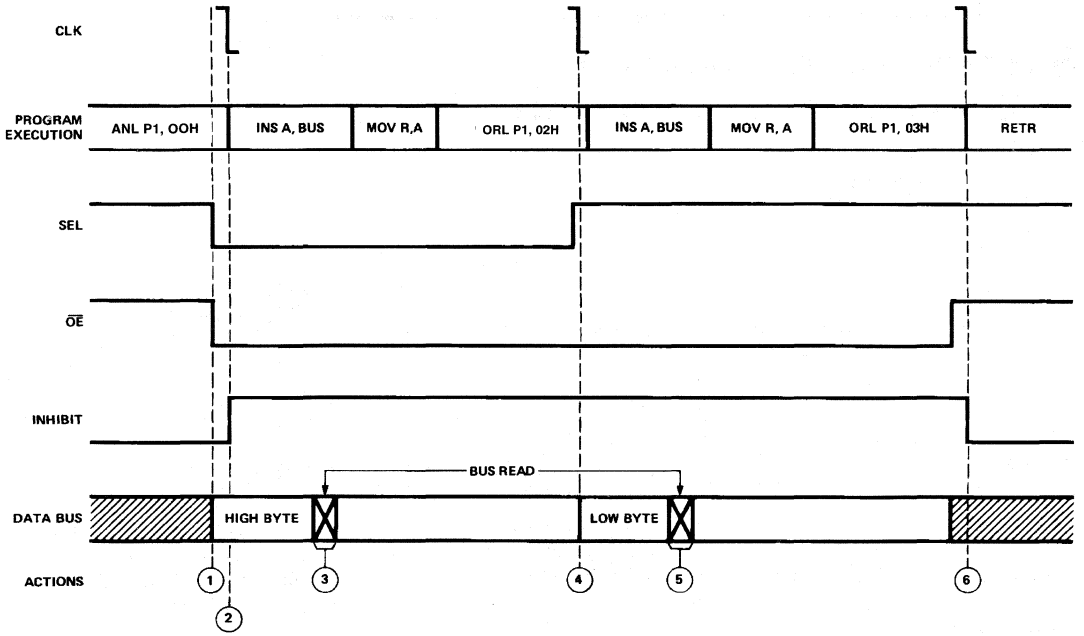


Figure 19. 8748 READ Cycle from Figure 18.

Actions

1. ANL P1, 00H has just been executed. The output of bits 0 and 1 of Port 1 cause SEL and $\overline{OE}$ to be logic low. The data lines output the higher order byte.
2. The HCTL-20XX detects that $\overline{OE}$ and SEL are low on the next falling edge of the CLK and asserts the internal inhibit signal. Data can be read without regard for the phase of the CLK.
3. INS A, BUS has just been executed. Data is read into the 8748.
4. ORL PORT 1, 02H has just been executed. The program sets SEL high and leaves $\overline{OE}$ low by writing the correct values to port 1. The HCTL-20XX detects $\overline{OE}$ is low and SEL is high on the next falling edge of the CLK, and thus the first inhibit reset condition is met.
5. INS A, BUS has just been executed. Lower order data bits are read into the 8748.
6. ORL P1, 03H has just been executed. The HCTL-20XX detects $\overline{OE}$ high on the next falling edge of CLK. The program sets $\overline{OE}$ and SEL high by writing the correct values to port 1. This causes the data lines to be tristated. This satisfies the second inhibit and reset condition. On the next rising CLK edge new data is transferred from the counter to the position data latch.

Additional Information from Hewlett-Packard

Application briefs are available from the factory. Please contact your local HP sales representative for the following.

M027 Interfacing the HCTL-20XX to the 8051

M019 Commonly Asked Questions about the HCTL-2020 and Answers

M020 A Simple Interface for the HCTL-2020 with a 16-bit DAC without Using a Processor

M023 Interfacing the MC68HCII to the HCTL-2020

HEWLETT® PACKARD

Surface Mount Quadrature Decoder/Counter Interface ICs

Technical Data

HCTL-2016 #PLC
HCTL-2020 #PLC

Features

- **20 Pin PLCC Surface Mount Package**
- **All Features of the HCTL-2016 and HCTL-2020 PDIP**

Description

The HCTL-2016 #PLC and HCTL-2020 #PLC are quadrature decoder/counter interface ICs in a 20 pin PLCC (plastic leaded chip carrier) surface mount package. These CMOS ICs interface incremental encoders to microprocessors by performing the quadrature decoder, counter, and bus transfer functions.

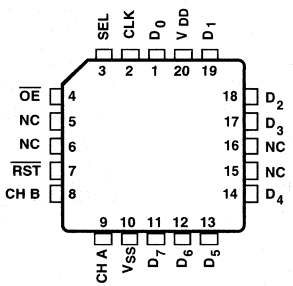
The HCTL-2016 #PLC and HCTL-2020 #PLC have all of the same features, functions, and operating characteristics as the HCTL-2016 and HCTL-2020 PDIP (plastic dual-in-line package).

For further information on the operation and function of the HCTL-2016 #PLC and 2020 #PLC, please refer to the HCTL-2000/HCTL-2016/HCTL-2020 data sheet.

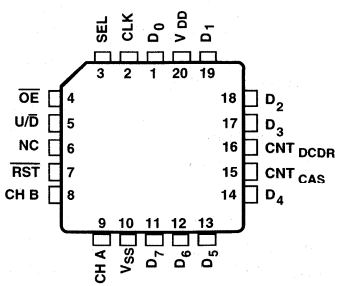
Applications

Typical applications include interfacing incremental encoders to microprocessors and interfacing digital potentiometers to digital data input buses.

Pinouts



HCTL-2016 #PLC

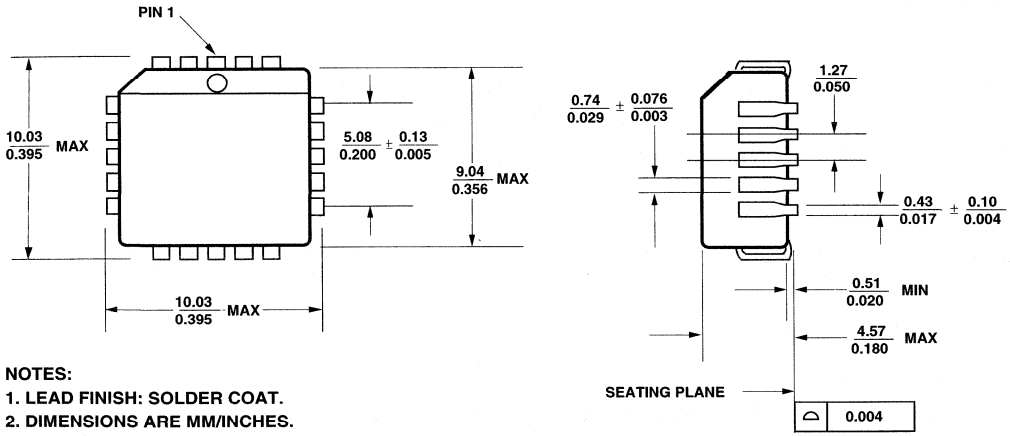


HCTL-2020 #PLC

ESD WARNING: NORMAL HANDLING PRECAUTIONS SHOULD BE TAKEN TO AVOID STATIC DISCHARGE.

5965-5895E

Package Dimensions



NOTES:
1. LEAD FINISH: SOLDER COAT.
2. DIMENSIONS ARE MM/INCHES.

20 PIN PLASTIC LEADED CHIP CARRIER PACKAGE

Devices

Part No.	Description
HCTL-2016 #PLC	16-bit counter; 14 MHz clock operation; 20 pin PLCC surface mount package.
HCTL-2020 #PLC	All features of HCTL-2016 #PLC plus quadrature decoder output signals and cascade output signals.

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Applications

The following application information is either published in this catalog or available from your local Hewlett-Packard sales office, authorized distributor, or representative.

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Design of the HCTL-1000's/1100's Digital Filter Parameters by the Combination Method

Application Note 1032

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Introduction

The objective of this application note is to explain the combination method and to show how it can be used for calculation of the HCTL-1000's digital compensation filter parameters to provide a stable, closed loop position control system.

One of the primary advantages of digital closed loop control is that digital compensation can be added to the system to provide the desired closed loop response. Although the HCTL-1000 is a digital controller that employs a discrete sampling rate, the combination method allows the user to model all the system components as continuous (or analog) in the s-plane. This allows the designer to use the experience gained in s-plane, analog control theory to design with the HCTL-1000's digital compensation filter. This application note shows the designer how the combination method can be used for digital compensation design with position control systems that employ a DC motor, an amplifier, an incremental encoder, and the HCTL-1000. The amplifier can be a current or voltage source amplifier. The HCTL-1000 provides an

8 bit motor command port for a linear amplifier and a sign and pulse signal for a pulse width modulated amplifier. Digital compensation filter parameters for two example closed loop systems employing the HCTL-1000 will be designed in appendices A and B of this application note to illustrate the use of the combination method.

The Hewlett-Packard HCTL-1000 is a high performance, general purpose, digital motion control IC which can be used in microprocessor based, digital closed loop systems. The HCTL-1000 is designed to communicate with a host microprocessor through an 8 bit parallel I/O port as shown in Figure 1. Commands from the host processor are used by the HCTL-1000 to control an amplifier/motor combination. A motor with an incremental shaft encoder such as a Hewlett-Packard HEDS-5500 encoder is connected to the amplifier. The encoder's quadrature output is then fed back into the HCTL-1000 to "close the loop".

Open Loop vs. Closed Loop (Feedback) Control Systems:

A block diagram of an open loop control system is shown in Figure 2. The input to an open loop control system is independent of the output of the system. Therefore, if the open loop system does not provide the desired response to an input, the error between the actual response and the desired response of the system will not be detected. Figure 1 shows the block diagram of a closed loop control system. Closed loop control systems compare their actual output with a desired command input and use the difference

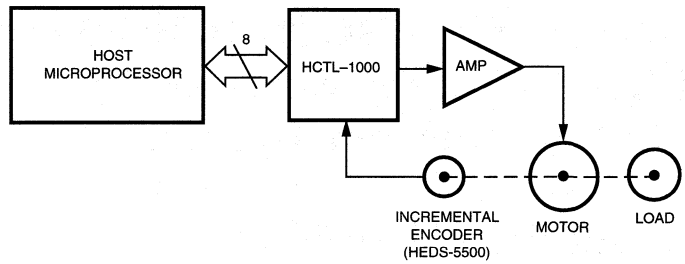

Figure 1. Block Diagram of a Closed Loop Motion Control System with the HCTL-1000.

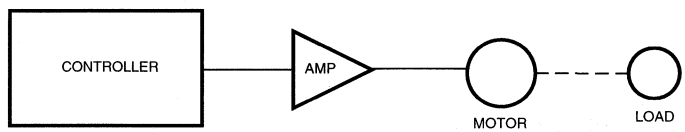

Figure 2. Block Diagram of an Open Loop System.

between them to regulate the system's output. Some of the advantages of closed loop control systems over open loop systems are:

A. Increased accuracy of the system's response to an input.

B. Increased system bandwidth (speed). The bandwidth of a system is the range frequencies over which a system will respond "satisfactorily" to an input. The system's bandwidth is a measure of the speed of the system's response. The terms "bandwidth" and "satisfactory response" are explained in more detail in the section of this application note "Bode Plots: Gain Crossover Frequency, Phase Crossover Frequency, Gain Margin, Phase Margin, and System Bandwidth".

The disadvantage of closed loop control systems is that they can become unstable and oscillate. The HCTL-1000 has a built in, programmable digital filter for compensation to increase the stability of the system. In this application note, the combination method will be used to determine values for the HCTL-1000's digital filter that will make the closed system stable.

Theory

Component Transfer Functions and the Open Loop System Model:

Each of the components in an open or closed loop system can be modeled mathematically by using the "transfer function" of the component. The transfer function models the dynamics of a component by relating the component's output to its input. The transfer functions of commonly used components can be found in most books on control systems.

A block diagram represents the physical system mathematically by showing the transfer functions of each component in its block of the diagram. A typical block diagram with its transfer function is shown in Figure 3. The parameters in each transfer function must be determined to accurately model the system. The response of open loop system is then modeled with a Bode plot to determine the stability and performance of the system when the loop is closed. Based on the characteristics of

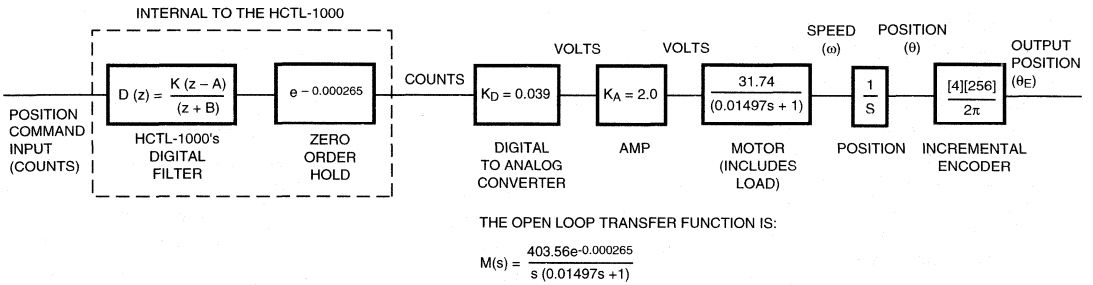

Figure 3. Open Loop Block Diagram of the Example System with a Voltage Source Amplifier.

the open loop system, the HCTL-1000's programmable digital filter parameters A, B, and K can be calculated using the combination method. When the properly calculated values of A, B, and K are programmed into the HCTL-1000, the closed loop system will respond in a stable fashion with the desired performance when the system is run in its linear region of operation. (i.e.. No component in the system is saturated during the step response.)

This application note assumes that the reader has a general working knowledge of analog control design methods. Specifically, the reader should be familiar with Laplace transforms, the s domain, pole/zero concepts, and Bode plots. Working knowledge of Bode plots is especially important for understanding the combination method for digital compensation filter design. It is for this reason that Bode plot design techniques are reviewed in the next section.

Bode Plots: Gain Crossover Frequency, Phase Crossover Frequency. Gain Margin, Phase Margin, and System Bandwidth:

Bode plots are used to model the frequency characteristics and the relative stability of a system. A Bode plot consists of two graphs: the magnitude and the phase of a transfer function of a system plotted as a function of frequency. The substitution $s = j\omega$ transforms the s domain transfer function into a complex number whose magnitude and phase can be directly computed at any frequency (ω). The Bode plot provides two values which are used to determine the stability and performance of a closed loop system from plots of the open loop system. These two values are known as the phase margin and the gain margin.

Figure 4 shows a Bode plot of the transfer function representing the block diagram and transfer function shown in Figure 3. The frequency at which the open loop gain is 1 (0 db) is called the gain crossover frequency (ω_C). The frequency where the phase angle is -180 degrees is called the phase crossover frequency ((ω_P). The gain margin (G_M) is defined as the magnitude of the open loop transfer function evaluated at the phase crossover frequency and referenced to the 0 db axis.

The phase margin (P_{MU}) is defined as the sum of the phase angle of the open loop transfer function evaluated at the gain crossover frequency plus 180 degrees. In cases where both the phase and gain margins of the open loop transfer function are positive and there are no poles or zeros in the right half of the s-plane, the closed loop system will be stable.

In this application note the phase of the system components and transfer functions will be calculated in radians. When a Bode plot is generated the phase and phase margin will be plotted in degrees. The conversion factor from radians to degrees is:

1 radian = 57.296 degrees. (1)

Similarly, the magnitude of the system components and transfer functions will be calculated as decimal quantities (i.e. X.XXX) while the magnitude and gain margin will be plotted on a Bode plot in decibels (db). The conversion factor from decimal to db is:

db = 20 log (decimal) (2)

Use of these conversions is standard practice in motion control design.

The phase margin of a system is a measure of the system's stabil-

ity. The higher the phase margin of the open loop system, the more stable the closed loop system becomes. The designer selects a compensated phase margin (P_{HC}) to provide the desired closed loop system response to a step input and then designs a compensator (digital filter) to provide the desired phase margin. A compensated phase margin of 30 to 60 degrees is generally recommended for stable designs. Figure 5 shows the effect of different compensated phase margins on the step response of an actual closed loop system employing a small DC motor, and a voltage source amplifier.

Increasing the gain margin of the open loop system also increases the stability of the closed loop system. The combination method does not directly assist the designer in easily computing a new gain margin for the compensated system.

The system bandwidth is the range of frequencies over which a system will respond "satisfactorily" to an input. "Satisfactory response" of the system is defined as the range of frequencies over which the magnitude of the Bode plot does not differ from its DC value by more than -3db.

In this application note, the closed loop bandwidth (BW) will be approximated as equal to the open loop gain crossover frequency (ω_C) for systems with a high phase margin:*

$$\omega_C \cong BW \qquad (3)$$

For systems with a low phase margin, the bandwidth (BW) is greater than or equal to the gain crossover frequency (ω_C) of the system and a corresponding increase in overshoot occurs;*

$$BW \geq \omega_C \qquad (4)$$

*Note: These approximations are based on a two pole dominant closed loop system model.

For more information on approximating the closed loop bandwidth by the desired open loop gain crossover frequency and other relationships in these systems involving bandwidth, gain crossover frequency, risetime, falltime, percent overshoot, etc. several references on motion control are listed in the bibliography at the end of this application note.

Summary of the Design Procedure

The HCTL-1000's Digital Filter Design Procedure Using the Combination Method:

The procedure recommended in this application note for designing closed loop systems that employ the HCTL-1000's digital filter is as follows:

A. Choose a motor to drive the required load. One com-

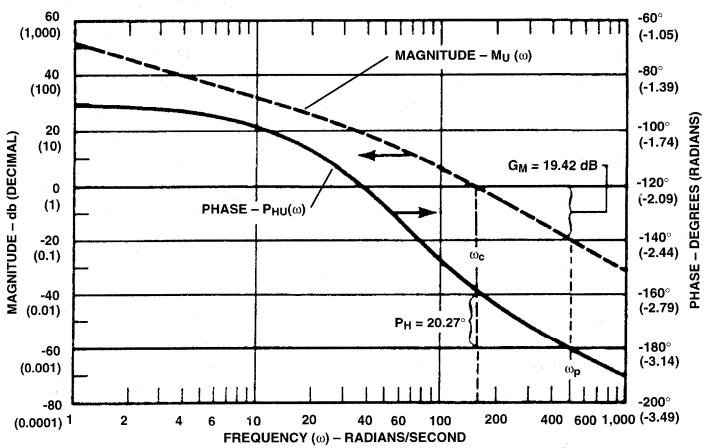

Figure 4. Bode Plot for the Open Loop System and Transfer Function Shown in Figure 3.

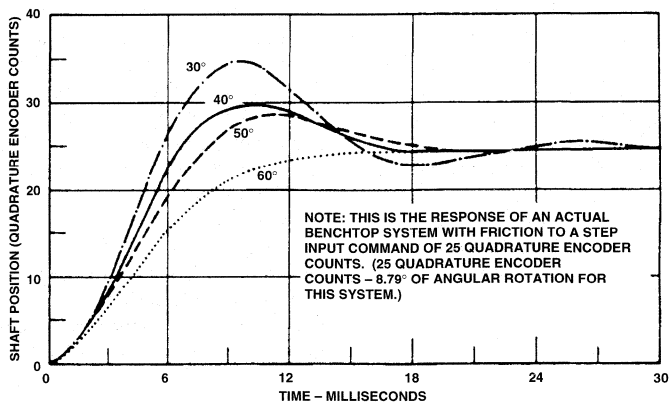

Figure 5. Shaft Position vs. Time for a Selection of Phase Margins.

mon criteria for choosing a motor is based on the ratio of the torque developed by the motor to the moment of inertia of the motor's armature and the load. It is desirable to choose a motor with a low armature inertia that can develop a high torque to quickly accelerate and decelerate the load (i.e. the motor has a high torque constant [K_T])

B. Choose a digital incremental encoder with quadrature output to monitor the position of the motor's shaft based on the encoder resolution and accuracy required for the application.

C. Choose an amplifier to drive the motor. The amplifier must be capable of supplying the current and voltage required by the motor for the load conditions.

D. Model the open loop transfer function of the system using s-plane transfer functions. A Bode plot showing the phase margin and gain margin of the open loop system can then be drawn from the open loop transfer function.

E. Choose the desired closed loop response (step response and bandwidth). The desired phase margin and gain crossover frequency for the compensated system can then be determined from the desired closed loop response.

F. Design the HCTL-1000's digital compensation filter based on the desired phase margin and gain crossover frequency for the compensated system.

System Modeling

Modeling the System Components in the S-Plane: The Open Loop Transfer Function

Introduction to the open loop transfer function:
Figures 6A and 6B show open loop block diagrams for systems which include a controller (the HCTL-1000's digital filter and the zero-order-hold representing the HCTL-1000's digital sampling delay), an amplifier, a motor, a load, and an incremental encoder. The block diagram in Figure 6A shows an open loop motion control system that employs a voltage source amplifier. The block diagram includes both the mechanical time constant of the motor and the electrical time constant of the motor. The block diagram shown in Figure 6B is used for systems that employ a current source

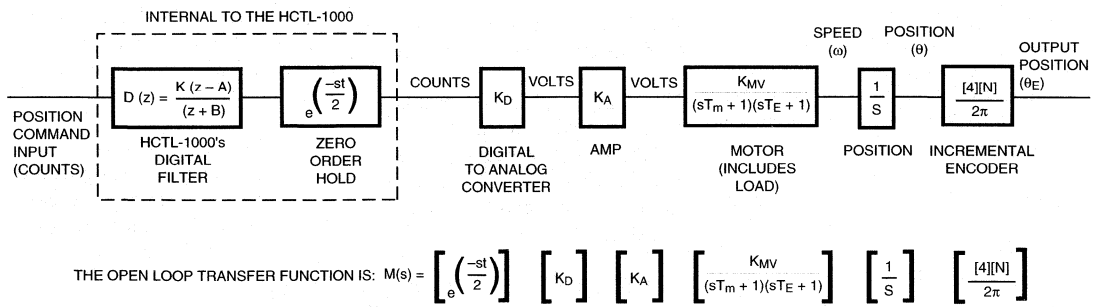

Figure 6a. The Open Loop Transfer Function of a System with a Voltage Source Amplifier. Note that the motor model includes the mechanical time constant (T_m) and the electrical time constant (T_E) of the motor.

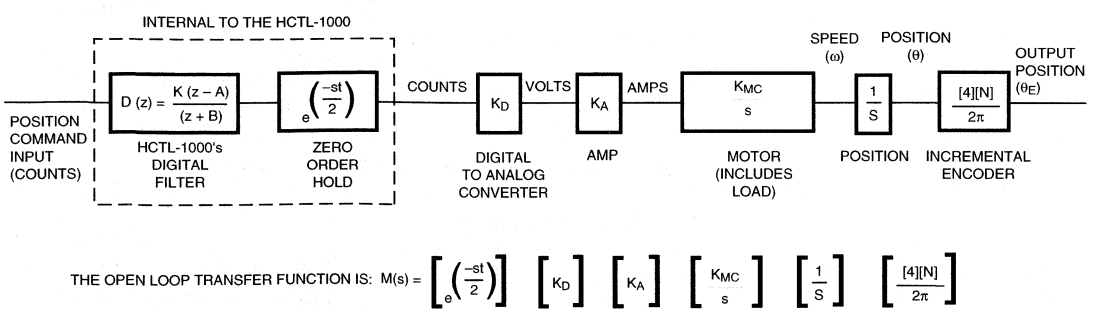

Figure 6b. The Open Loop Transfer Function of a System with a Current Source Amplifier.

amplifier. This model does not use the electromechanical time constants of the motor.

The open loop transfer function M(s) for these systems is determined by multiplying all of the individual component transfer functions together.

M(s) = [DAC gain (if used)] [Zero order hold] [Amp gain] [Motor transfer function] [encoder quadrature counts/(2 π)] (5)

The following sections describe the method for determining the transfer function of each component, determining the magnitude and phase contribution of each component, computing the open loop transfer function of the system, and then drawing a Bode plot of the open loop system.

The Zero Order Hold (ZOH) transfer function:
The zero order hold (ZOH) models the delay of the discrete sampling time of the HCTL-1000. The transfer function (Z(s)) of the zero order hold (ZOH) is:

$$Z(s) = e^{-st/2} \quad (6)$$

Where:
t = the sampling time (ie. time between successive samples) of the HCTL-1000 (in seconds).

This transfer function of the ZOH allows the designer to model the time delay of the HCTL-1000 as a continuous element in the system. Analog, s-plane design techniques can therefore be used to analyze the system.

The ZOH's contribution to the phase ($P_{ZOH}(\omega)$) of the open loop transfer function is:

$$P_{ZOH}(\omega) = -\frac{[\omega]\,[t]}{2} \text{ (radians)} \quad (7)$$

Where:

ω = the frequency of interest (in radians/sec)
t = the sampling time of the HCTL-1000 (in seconds)

Phase lag is added to the system by increasing the time delay between successive samples of the ZOH. It is usually desirable therefore to choose the fastest sampling time possible so as to induce the least amount of phase lag. Generally, the sampling frequency (1 /t) should exceed the system bandwidth (in hertz) at least tenfold:

Sampling time (t) < [1/10 System bandwidth)] (8)

The ZOH provides unity gain at all frequencies of the system.

The sampling time (t), can be programmed into the HCTL-1000 through register ROFH. The sampling time (t) can be determined from the equation:

$$t = [16]\,[ROFH + 1]\,[1/f_{CLK}] \text{ (seconds)} \quad (9)$$

where:

t = sample time (in seconds)

f_{CLK} = freq- of the HCTL-1000's external clock (1 or 2 MHz)
ROFH = sample timer register

The limits of minimum values (ie. fastest sampling times) that can be programmed into register ROFH are:

ROFH Contents

Mode:	Minimum Limit:
Position Control	7 (decimal)
Proportional Velocity Control	7 (decimal)
Trapezoidal Profile Control	15 (decimal)
Integral Velocity Control	15 (decimal)

The Digital to Analog Converter (DAC) transfer function:
Linear voltage source and current source amplifiers require a digital to analog converter to interface with the HCTL-1000.

The DAC's transfer function is simply its gain (K_D). The digital to analog converter (DAC) transfer function can include an electrical time constant, but it is usually neglected because the bandwidth of the DAC is generally much higher than the desired bandwidth of the closed loop system.

The gain (K_D) is the DAC's contribution to the magnitude of the open loop transfer function. The formula for computing the gain (K_D) of the DAC is:

$$\text{Gain } (K_D) = \frac{\text{Voltage range (volts)}}{2^N \text{ (bits or counts)}} \quad (10)$$

Example:
For an eight bit DAC with an output range of -5 to +5 volts the equation would be:

$$K_D = \frac{5 - (-5) \text{ volts}}{2^8 \text{ counts}} = \frac{10}{256} =$$

.039 volts/count

Note that the units of the DAC gain is volts/count. This gives the combination of the linear voltage

source amplifier and the DAC the units of volts/count, and the linear current source amplifier/ DAC the units of amps/count.

The DAC does not contribute a phase shift to the open loop transfer function.

The amplifier transfer function:
The amplifier transfer function is its gain (K_A). The choice between using either a current or voltage amplifier affects the motor transfer function. The amplifier's transfer function can include an electrical time constant, but this is usually neglected as the amplifier's bandwidth is generally much higher than the desired bandwidth of the closed loop system. In general, if the desired bandwidth of the system is 10 times smaller than the amplifier's bandwidth, then the amplifier's electrical time constant can be neglected. Note that the units of the gain (K_A) vary with the type of amplifier chosen.

There are four types of amplifiers that can be used with the HCTL-1000:

- Voltage source – pulse width modulated
- Current source – pulse width modulated
- Voltage source – linear
- Current source – linear

The HCTL-1000 provides an 8 bit binary word on its motor command port to drive a linear amplifier, and a pulse and sign signal to drive a pulse width modulated amplifier.

The amplifier does not contribute a phase shift to the open loop transfer function when its electrical time constant is neglected. The gain (K_A) is the amplifier's contribution to the magnitude of the open loop transfer function.

The gain and bandwidth of most linear amplifiers can be obtained from the manufacturer's data sheet. If the user desires to measure the amplifier's gain, the DC-output for a given DC-input can be measured directly. The units for the gain (K_A) of a linear voltage source amplifier are volts/volt. The units for the gain (K_A) of a linear current source amplifier are amps/volt.

A simplified formula that will be used in this application note for computing the gain of a pulse width modulated (PWM) amplifier is:

$$K_A = \frac{\left[\begin{array}{l}\text{Maximum}\\ \text{signal}\\ \text{output}\end{array}\right] - \left[\begin{array}{l}\text{Minimum}\\ \text{signal}\\ \text{output}\end{array}\right] \text{(current or voltage)}}{\left[\begin{array}{l}\text{duty cycle}\\ \text{input to}\\ \text{get maximum}\\ \text{output}\end{array}\right] - \left[\begin{array}{l}\text{duty cycle}\\ \text{input to}\\ \text{get minimum}\\ \text{output}\end{array}\right]} \quad (11)$$

The gain of a PWM amplifier is measured by inputting a waveform with a known duty cycle. If a voltage source PWM amplifier is being measured, the output voltage can be read with a DC voltmeter to average the output of the amplifier. If a current source PWM amplifier is being measured, the current can be dropped across a load of known value to produce a voltage and then that voltage can be read with a DC voltmeter to average the output of the amplifier.

For the HCTL-1000, the duty cycle of the input to the PWM amplifier is regulated by register R09H. Register R09H has a range of 64H to 9CH (-100 to +100 decimal). The units of the gain (K_A) are for the HCTL-1000 and PWM amplifier combination are therefore volts or current per count.

The DC motor transfer function:
The DC motor transfer function is calculated based on the total inertia of the system, the parameters used to describe the motor's dynamic response, and the type of amplifier used to drive the motor. Different transfer functions are used for a motor driven by a voltage source amplifier than for a motor driven by a current source amplifier. The total inertia of the system and the parameters used to describe the system's dynamic response are the same for both motor transfer functions. They are described in the next two sections. Following these two sections are two sections which describe the transfer functions for motors driven by current source amplifiers and motors driven by voltage source amplifiers.

1. DC motor manufacturer's motor parameters:
The DC motor parameters of interest that describe the electromechanical characteristics of motor mathematically are: the torque constant (K_T) [in N-m/amp], the moment of inertia of the armature (J_M [in kg-m^2], the terminal resistance (R) [in ohms], the voltage constant (K_E) [in volt-sec/rad], and the armature inductance (L) [in henries]. These motor parameters can all be obtained directly from the motor manufacturer's data sheet.

2. Total system moment of inertia:
The first step in determining the moment of inertia of the system is to determine the moment of inertia of the load (J_L). For many loads the moment of inertia of

the load (J_L) can be read directly from the manufacturer's data sheet. The moment of inertia of the incremental encoder's codewheel (J_C) can also be read directly from the encoder manufacturer's data sheet. It is recommended that a book on mechanical design be consulted to find the moment of inertia of other loads.

The total moment of inertia for the system (J) includes the motor's armature inertia (Jm), the load inertia (J_L), and the encoder codewheel inertia (J_C) Therefore:

$$J = J_M + J_L + J_C \qquad (12)$$

3. DC motors driven by voltage source amplifiers:
The DC motor transfer function for a motor driven by a voltage source amplifier is:

$$G(s) = \frac{\text{position output}}{\text{voltage input}} = \frac{\theta(s)}{v(s)} = \frac{K_{MV}}{s(sT_m + 1)(sT_E + 1)} \qquad (13)$$

The term s in the denominator indicates integration due to the fact that position is the output. Note that the transfer function for a motor driven by a voltage source amplifier has three main components; a gain constant (K_{MV}), a mechanical time constant (T_M) [in seconds] and an electrical time constant (T_E) [in seconds]. The gain constant (K_{MV}) of the motor driven by a voltage source amplifier is defined as the velocity at which the motor's shaft will turn when 1 volt is applied to the input terminals. The mechanical and electrical time constants of the motor describe the response time of the motor to an input. The mechanical time constant (T_M) of a motor is defined as the time required for the unloaded motor to reach 63.2% of its final velocity after the application of a DC step voltage to the motor's armature. The electrical time constant (T_E) of a motor is defined as the ratio of the armature inductance to the armature resistance.

The constants in the motor transfer functions T_E, T_M, and K_{MV} are determined by the manufacturer's motor parameters and the total system inertial load that the motor is driving.

The equations for the mechanical (T_M) and electrical (T_E) time constants are:

$$T_M = \frac{[R]\,[J]}{[K_E]\,[K_T]} \text{ (seconds)} \qquad (14)$$

$$T_E = \frac{L}{R} \text{ (seconds)} \qquad (15)$$

The equation to calculate the gain constant (K_{MV}) is:

$$K_{MV} = \frac{1}{K_E} \text{ (rad/volt-sec)} \qquad (16)$$

Where:

- R = the terminal resistance of the motor (in ohms)
- J = the total system moment of inertia (in kg-m^2)
- K_E = the voltage constant of the motor (volt-sec/rad)
- K_T = the torque constant of the motor (in N-m/amp)

The electrical time constant can be neglected if the mechanical time constant is greater than 10 times the value of the electrical time constant. This reduces the motor transfer function to:

$$G(s) = \frac{\text{position output}}{\text{voltage input}} = \frac{\theta(s)}{v(s)} = \frac{K_{MV}}{s(sT_M + 1)} \qquad (17)$$

The phase contribution of a motor [$P_M(\omega)$], driven at frequency (ω) by a voltage source amplifier is:

$$P_M(\omega) = -\arctan([\omega][T_M]) - \arctan([\omega][T_E]) - \left[\frac{\pi}{2}\right] \text{(radians)}^* \qquad (18)$$

The magnitude contribution of a motor [$M_M(\omega)$], driven at frequency (ω) by a voltage source amplifier is:

$$M_M(\omega) = \frac{K_{MV}}{\omega\sqrt{1 + ([\omega]\,[T_M])^2}\sqrt{1 + ([\omega]\,[T_e])^2}}^* \qquad (19)$$

Where:

- (ω) = the frequency of interest (in radians)
- T_M = the mechanical time constant of the motor (in seconds)
- T_E = the electrical time constant of the motor (in seconds)
- K_{MV} = the gain constant of the motor (in rad/volt-sec)

Note: For cases where the electrical time constant has been neglected let $T_E = 0$.

4. DC motors driven by current source amplifiers:
The DC motor transfer function for a motor driven by a current source is:

$$G(s) = \frac{\text{position output}}{\text{current input}} = \frac{\theta(s)}{1(s)} = \frac{K_{MC}}{s^2} \qquad (20)$$

The gain constant (K_{MC}) for systems employing a current source amplifier is computed as:

$$K_{MC} = \frac{K_T}{J} \text{ (rad/amp sec}^2\text{)} \quad (21)$$

Where:

J = the total system moment of inertia (in kg-m2)

K_T = the torque constant of the motor (in N-m/amp)

The phase contribution of a motor [$P_M(\omega)$] driven at frequency (ω) by a current source amplifier is:

$$P_M(\omega) = -\pi \text{ (radians)} \quad (22)$$

The magnitude contribution of a motor [$M_M(\omega)$], driven at frequency (ω) by a current source amplifier is:

$$M_M(\omega) = \frac{K_{MC}}{(\omega)^2} \quad (23)$$

Where:

ω = the frequency of interest (in radians)

K_{MC} = the gain constant of the motor (in rad/amp-sec^2)

The encoder transfer function:

The incremental encoder's transfer function (E) is:

$$E = \frac{C}{2\pi} = \frac{[4]\,[N]}{2\pi} \text{ (count/rad)} \quad (24)$$

Where:

C = quadrature counts per revolution of the encoder's codewheel

N = the number of slits in the encoder's codewheel

The 2π indicates the number of radians in one revolution of the codewheel. Because the HCTL-1000 utilizes a four times quadrature decoder, the closed loop system has four times the resolution (C) as the number of slits in the codewheel (N). The number of slits in the codewheel (N) can be found from the encoder manufacturer's data sheet.

The encoder's codewheel count does not contribute to the phase of the open loop transfer function. The magnitude contribution of the encoder's codewheel count (E) to the open loop transfer function is independent of frequency:

$$E = \frac{C}{2\pi} \text{ (count/rad)} \quad (25)$$

Where:

C = quadrature counts per revolution of the encoder's codewheel

The phase and magnitude contribution of the codewheel's inertia (J_C), has already been considered in the total system load on the motor.

Determination of the Open Loop transfer function:

Now that all of the individual transfer functions have been determined for each component of the open loop system, the open loop transfer function M(s) can be determined by multiplying the individual transfer functions together.

For example, the open loop transfer function for the system with the current source amplifier shown in Figure 6B is:

$$M(s) = [e^{-st/2}][Kd][Ka]\left[\frac{K_M}{s}\right]\left[\frac{1}{s}\right]\left[\frac{C}{(2\pi)}\right] \quad (26)$$

Determination of the gain crossover frequency, phase crossover frequency, gain margin, and phase margin of the open loop transfer function using a Bode plot:

A Bode plot can be created using the open loop transfer function generated in the last section.

The purpose of creating the Bode plot is to show the characteristics of the uncompensated system over frequency. The Bode plot also shows the designer how much compensation should be added to the system to achieve the desired system bandwidth and stability.

The method for creating a Bode plot from the open loop transfer function is to plot the phase and magnitude of the open loop transfer function over frequency. In the following equations for the phase and magnitude the constants are:

E = the gain of the incremental encoder (counts/ radian)

K_A = the gain of the amplifier (volts/volt for linear voltage source amplifiers, amps/volt for linear current source amplifiers, volts/count for PWM voltage source amplifiers, amps/count for PWM current source amplifiers.)

K_D = the gain of the DAC (volts/count)

K_{MC} = the gain constant of a motor driven by a current source amplifier (rad/amp-sec^2)

K_{MV} = the gain constant of a motor driven by a voltage source amplifier (rad/volt-sec)

$M_M(\omega)$ = the magnitude of the motor transfer function

$P_M(\omega)$ = the phase of the motor transfer function (radians)

$P_{ZOH}(\omega)$ = the phase of the zero order hold transfer function (radians)

t = the sampling time of the HCTL-1000 (seconds)

T_E = the electrical time con-

stant of the motor (seconds)

T_M = the mechanical time constant of the motor (seconds)

ω = the frequency of interest (radians)

The phase $[P_{HU}(\omega)]$ of the uncompensated open loop transfer function over frequency (ω) is determined by the equation:

$$P_{HU}(\omega) = P_M(\omega) + P_{ZOH}(\omega) \text{ (radians)} \quad (27)$$

For a system employing a voltage source amplifier, the following equation is used for calculation of the phase $[P_{HU}(\omega)]$ of the open

$$P_{HU}(\omega) = -\arctan([\omega][T_M]) - \arctan([\omega][T_e]) - \left[\frac{\pi}{2}\right] - \left[\frac{[\omega]\,[t]}{2}\right] \text{(rad)}^* \quad (28)$$

For systems with a voltage source amplifier where the electrical time constant (T_E) has been neglected, the equation becomes:

$$P_{HU}(\omega) = -\arctan([\omega][T_M]) - \left[\frac{\pi}{2}\right] - \left[\frac{[\omega]\,[t]}{2}\right] \text{(rad)}^* \quad (29)$$

For systems with a current source amplifier the eqation becomes:

$$P_{HU}(\omega) = -\pi - \left[\frac{[\omega]\,[t]}{2}\right] \text{(rad)}^* \quad (30)$$

*Note: Multiply $P_{HU}(\omega)$ by 57.296 (deg/rad) to obtain the phase in degrees. (31)

The magnitude $[M_U(\omega)]$ of the uncompensated open loop transfer function over frequency (ω) is:

$$M_U(\omega) = [M_M(\omega)][K_D][K_A][E] \quad (32)$$

The magnitude $[M_U(\omega)]$ of the uncompensated open loop transfer function of a system with a voltage amplifier is:

$$M_U(\omega) = \frac{[K_{MV}][K_D][K_A][(C/2\pi)]}{\omega\sqrt{[1+([\omega]\,[T_M])^2]}\sqrt{[1+([\omega]\,[T_e])^2]}} \quad ** \quad (33)$$

For systems with a voltage source amplifier where the electrical time constant (T_E) has been neglected, the uncompensated magnitude $[M_U(\omega)]$ is:

$$M_U(\omega) = \frac{[K_{MV}][K_D][K_A][C/(2\pi)]}{\omega\sqrt{[1+([\omega]\,[T_M])^2]}} \quad ** \quad (34)$$

The uncompensated magnitude $[M_U(\omega)]$ for the loop transfer function of systems with a current source amplifier is:

$$M_U(\omega) = \frac{[K_{MC}][K_D][K_A][C/(2\pi)]}{(\omega)^2} \quad ** \quad (35)$$

**Note: To express the magnitude in db, use:

$$\text{db} = 20 \log [M_U(\omega)] \quad (36)$$

loop transfer function:
When the equations for the phase $[P_{HU}(\omega)]$ and gain $[M_U(\omega)]$ of the open loop transfer function have been determined in terms of component parameters and frequency (ω), then different values of frequency (ω) may be substituted into these equations to create a Bode plot of the phase and gain of the open loop system.

The next step is to evaluate the phase and gain crossover frequencies and the phase and gain margins from the Bode plot. To find the phase crossover frequency (ω_P) let the phase $[P_{HU}(\omega)]$ equal - π radians (i.e. -180 degrees) in the appropriate phase equation and solve for the frequency (ω). This value of the frequency (ω) is the phase crossover frequency (ω_P). (37)

To find the gain crossover frequency (ω_C) let the magnitude $[M_U(\omega)]$ equal 1 (0 db) in the appropriate magnitude equation and solve for the frequency (ω). This value of the frequency (ω) is the gain crossover frequency (ω_C). (38)

$$G_M = \frac{1}{M_U(\omega_P)} \text{ (decimal)} = 20 \log \left[\frac{1}{M_U(\omega_P)}\right] \text{(db)} \quad (39)$$

$$G_M = -20 \log M_U(\omega_P) \quad (40)$$

Where:
$M_U(\omega_P)$ = the magnitude of the open loop system evaluated at the phase crossover frequency (ω_P).

The phase margin (P_H) is

$$(P_H) = [180 \text{ deg} + (57.296 \text{ (deg/rad)} \times P_{HU}(\omega_C))] \text{ (degrees)} \quad (41)$$

Where:

$P_{HU}(\omega_C)$ = the phase of the open loop system evaluated at the gain crossover frequency (ω_C).

The gain margin (G_M) [in db] is:
Figure 4 shows an example of a Bode plot drawn from the open loop transfer function of the block diagram shown in Figure 3. The Bode plot includes the phase crossover frequency, gain cross-

over frequency, phase margin, and gain margin of the uncompensated, open loop system.

Once the Bode plot of the uncompensated, open loop transfer function has been completed, the designer can determine how much compensation should be added to the system to achieve the desired system bandwidth and stability. A method for determining how much compensation to add to the system is described in the next section.

Modification of the Open Loop System Transfer Function Using Compensation to Achieve the Desired Closed Loop Characteristics

Once the phase and gain margins of the open loop transfer function are known at the original gain and phase crossover frequencies, a new phase margin and gain crossover frequency can be chosen to achieve a stable closed loop system at a bandwidth equal to or higher than the uncompensated bandwidth.

The open loop transfer function can be modified with the HCTL-1000's digital compensation filter to improve the bandwidth (speed) and stability of the system when the loop is closed with the HCTL-1000. The stability of the closed loop system can be increased by increasing the phase margin of the system. The bandwidth and the gain crossover frequency of the system can be increased by increasing the gain of the system.

Generation of new desired open loop characteristics using the desired closed loop bandwidth:

In this application note, the desired closed loop bandwidth (BW) will be approximated as equal to the desired open loop gain crossover frequency (ω_C') for high phase margin systems.

$$\omega_C' \cong BW \text{ [closed loop]} \quad (42)$$

Based on the required step response of the system, the user should choose a realistic closed loop bandwidth (BW), and compensated phase margin (P_{HC}). The digital compensation filter can contribute a maximum phase lead of approximately 80 degrees to the uncompensated phase margin. The amount of bandwidth that can be added by the digital filter depends on the type of system being compensated. Both the gain of the amplifier (K_A) and the gain of the digital filter (K) can be used to change the gain margin of the system.

The desired gain crossover frequency (ω_C') is now the frequency of interest that will be substituted into both the phase and gain equations described in the next section.

Determination of the phase margin and gain of the open loop transfer function at the desired, open loop gain crossover frequency:

The next step is to calculate the phase margin (P_{MU}) of the uncompensated system at the desired frequency (ω_C') and the gain (K_F) required to achieve the desired frequency (ω_C').

The uncompensated phase margin (P_{MU}) at the desired open loop gain crossover frequency (ω_C') can be calculated by substituting ω_C' as the frequency of interest (ω) in the appropriate equation for the phase [$P_{HU}(\omega)$]:

$$P_{MU} = [180 \text{ deg} + [P_{HU}(\omega_C')] \times 57.296(\text{deg/rad})] \text{ degrees} \quad (43)$$

Where:

$P_{HU}(\omega_C')$ = the phase angle of the open loop system evaluated at the desired gain crossover frequency (ω_C').

The phase lead (P_L) that the HCTL-1000's digital filter must provide to the closed loop system to make it stable can be found from the following equation:

$$P_L = P_{HC} - P_{MU} \text{ (degrees)} \quad (44)$$

Where:

P_{HC} = the desired compensated margin at ω_C' (degrees)

P_{MU} = the uncompensated phase margin at ω_C' (degrees)

The gain (K_F) required from the digital compensation filter to make the overall gain equal to one at the desired gain crossover frequency (ω_C') is:

$$K_F = \frac{1}{M_U(\omega_C')} \quad (45)$$

Where:

$M_U(\omega_C')$ = the magnitude of the open loop system evaluated at the desired gain crossover frequency (ω_C').

The HCTL-1000's digital compensation filter, and a method for computing the values for the gain factor (K), the pole (B) and the zero (A) are discussed in the next section of this application

note.

Use of the Combination Method to Design the HCTL-1000's Digital Compensation Filter:

Characteristics of the HCTL-1000's digital filter:

The digital compensation filter of the HCTL-1000 is of the form:

$$D(z) = \frac{[K][z - A]}{[4][z + B]} =$$

$$\left[\frac{K}{4}\right]\left[\frac{Z - A}{Z}\right]\left[\frac{Z}{Z - B}\right] \quad (46)$$

Both the pole term (B) and the zero term (A) contribute phase lead to the system. The K term is an independent gain factor that can be used to raise the system gain for higher bandwidth, and to compensate for the gain reduction associated with the digital filter's pole and zero term.

The combination method and the phase and magnitude graphs:

The combination method is a graphical analysis technique that can be used to design HCTL-1000's digital compensator filter. The four graphs shown in Figures 7, 8, 9, and 10 are employed by the combination method to show the phase of digital filter's pole [$P_P(\omega_N)$], the phase of digital filter's zero [$P_Z(\omega_N)$], the magnitude of the digital filter's pole [$M_P(\omega_N)$]. and the magnitude of the digital filter's zero [$M_Z(\omega_N)$] Note that the magnitude and phase for both the pole and zero terms are plotted on individual graphs. The combination method employs these plots to determine values for the pole (B), zero (A), and gain (K) that will provide the required phase lead and gain for the desired closed loop system response to a step input over a specified bandwidth.

Normalized frequencies are used in these graphs to allow digital compensation to be designed for systems with a wide range of bandwidths and sample times. The normalized frequency [$\omega_N(\omega)$] is calculated as the frequency (ω) multiplied by the sampling time (t) of the system:

$$\omega_N(\omega) = [\omega]\ [t] \text{ (radians)} \quad (47)$$

ω_{NC}' is the desired gain crossover frequency (ω_C'), normalized to the sampling time (t) of the HCTL-1000 by equation (47):

$$\omega_{NC}' = [\omega_C]\ [t] \text{ (radians)} \quad (48)$$

Where:

ω_C' = the desired gain crossover frequency (radians/sec)
t = the sampling time of the HCTL-1000 (seconds)

The normalized desired gain crossover frequency (ω_{NC}') is used as the frequency at which the phase and magnitude contributions of the digital filter's pole and zero term are evaluated.

Figures 11, 12, 13, and 14 show expanded versions of the phase and magnitude graphs for the pole (B) and zero (A) term. These graphs have been expanded for values of the normalized frequency [$\omega_N(\omega)$] between 0.0 and 0.65. This range of values is most often used due to the requirement that the sampling frequency (1/t) must be at least 10 times the system bandwidth (in Hertz).

$$t \le 1/(10 \times BW) \quad (8)$$
$$t \le (2 \times \pi)/(10 \times \omega_C')$$

Now:

$$\omega_{NC}' \le \omega_C' \times t \quad (48)$$
$$\omega_{NC}' \le \omega_C' \times (2 \times \pi)/(10 \times \omega_C')$$
$$\omega_{NC}' \le (2 \times \pi)/10$$

Therefore:

$$\omega_{NC}' \le .628$$

Note that for all four graphs the value of the pole term (B) and the zero term (A) is always less than or equal to 1.0 for proper system design. Also note that when the phase lead from the HCTL-1000's compensator is increased the gain of the system is decreased by the pole and zero terms.

The normalized frequency plots for the phase and magnitude of the pole and zero terms allow the designer to use analog design techniques to determine values for the HCTL-1000's digital compensation filter. This is accomplished by mapping from the digital z-plane to the analog s-plane through the equation $z = e^{st} = e^{j\omega t}$ where t is the sampling time of the system, and $\omega_N(\omega)$ is the normalized frequency of the system.

Generation of the phase and magnitude graphs:

The following text describes the method and equations for generating the phase and magnitude graphs. This information is useful for designers who would like to implement the combination method in software, but it is not necessary to read this text for the designer to use the graphs for filter design.

The graphs for the pole term are generated from the z/(z + B) portion of equation (46). The plot for the phase of the pole term is derived by substituting $z = e^{j\omega t}$ into z/(z + B) and then taking the

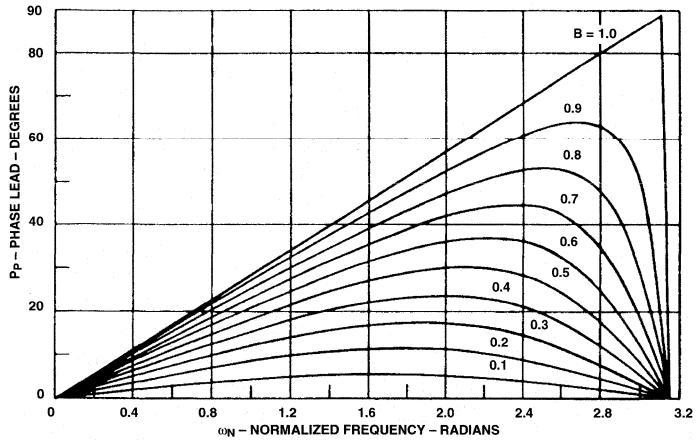

Figure 7. Phase Lead Contribution of the Pole Term.

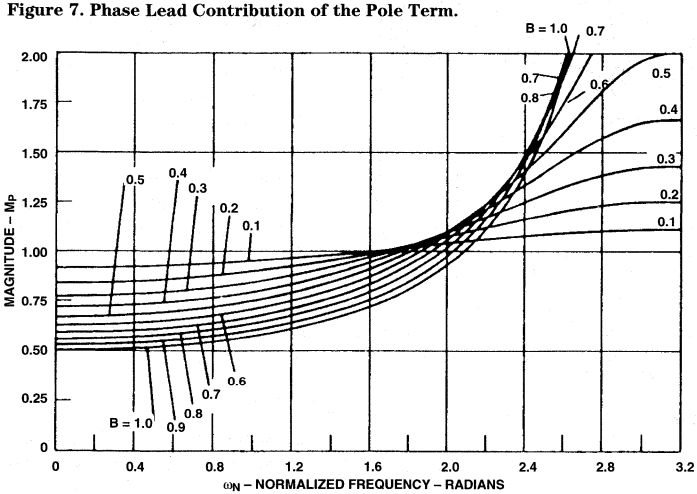

Figure 8. Magnitude Contribution of the Pole Term.

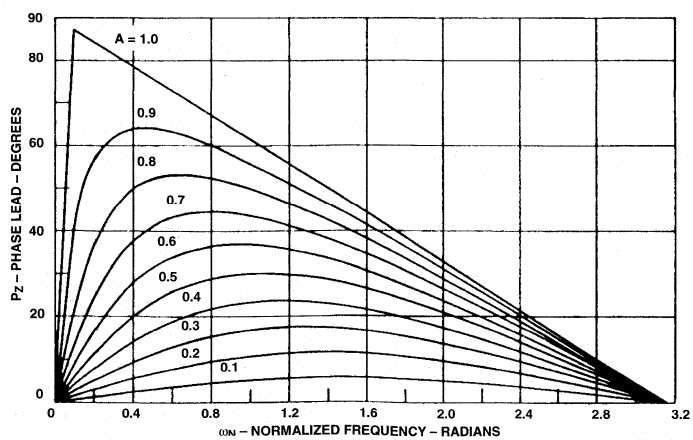

Figure 9. Phase Lead Contribution of the Zero Term.

argument of this term to get:

$$P_P(\omega_N) = \arg\left[\frac{e^{j\omega t}}{e^{j\omega t} + B}\right] = \arctan\left[\frac{B \sin \omega t}{(B \cos \omega t) + 1}\right] \quad (49)$$

The magnitude of the pole term is derived from:

$$M_P(\omega_N) = \left[\frac{e^{j\omega t}}{e^{j\omega t} + B}\right] = \frac{1}{\sqrt{[(B \cos \omega_T) + 1]^2 + [B \sin \omega_T]^2}} \quad (50)$$

The graphs of the zero term are derived from the (z-A)/z portion of equation (46). The plot of the phase of the zero term is found by substituting $z = e^{j\omega t}$ into (z-A)/z and then taking the argument

$$P_Z(\omega_N) = \arg\left[\frac{e^{j\omega t} - A}{e^{j\omega t}}\right] = \arctan\left[\frac{A \sin \omega t}{(-A \cos \omega t) + 1}\right] \quad (51)$$

The plot of the magnitude of the zero term is derived from:

$$M_Z(\omega_N) = \left[\frac{e^{j\omega t} - A}{e^{j\omega t}}\right] = \sqrt{[(-A \cos \omega t) + 1]^2 + [A \sin \omega t]^2} \quad (52)$$

of this term to get:

Determination of the HCTL-1000's Digital Filter Parameters: A, B, and K by the Combination Method:

Three programmable components, the zero (A), the pole (B), and the gain (K) are accessible to the user through registers 20H, 21H, and 22H of the HCTL-1000 respectively. By changing these three numbers, the user can change the response of

Table 1: Effect of changing digital filter parameters A, B, or K on the response of the system to a step input.

Increase in Parameter	Stability	Effect on Response	Stiffness
A	Better	Faster	Decreases
B	Slightly Better	Faster	Decreases
K	Worse	Faster	Increases

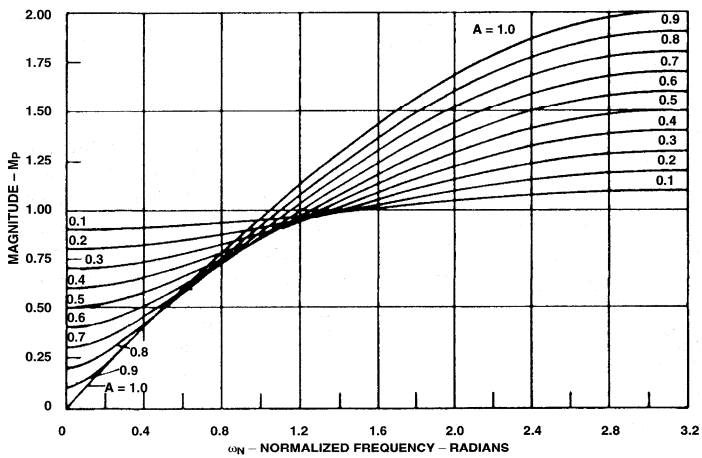

Figure 10. Magnitude Contribution of the Zero Term.

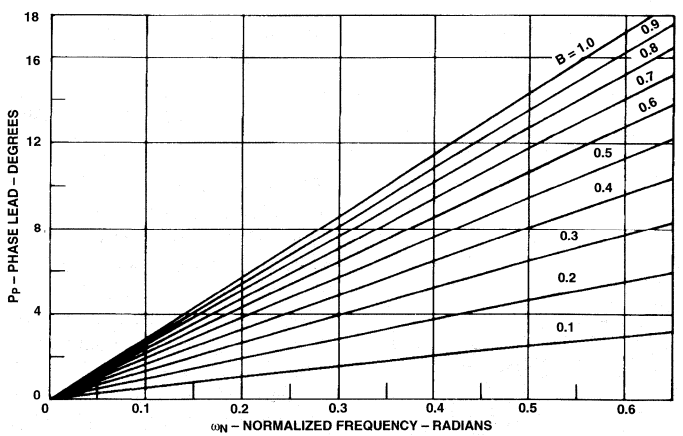

Figure 11. Phase Lead Contribution of the Pole Term.

the system to an input. Table 1 shows the effect of changing each of these parameters on the response of the system to a position step input. The combination method to find values for the pole (B), zero (A), and gain (K) is as follows:

1. On Figure 11, choose a large value for the pole term (B) to contribute significant phase lead [$P_P(\omega_{NC}')$] at the normalized desired gain crossover frequency of the system (ω_{NC}').
2. From Figure 12, read the value of the magnitude [$M_P(\omega_{NC}')$] for the chosen value of B at the normalized desire gain crossover frequency (ω_{NC}').
3. Determine the remaining phase lead [$P_Z(\omega_{NC}')$] which must be provided by the zero term (A) of the digital filter. This can be done by use of the equation:

$$P_Z(\omega_{NC}') = P_L - P_P(\omega_{NC}') \text{ (degrees)} \quad (53)$$

Where:

P_L = the required phase lead from the HCTL-1000's digital compensation filter (degrees)

$P_P(\omega_{NC}')$ = the phase lead contributed by the pole term (degrees)

4. On Figure 13, find the point where the normalized, desired gain crossover frequency (ω_{NC}') and the remaining phase lead [$P_Z(\omega_{NC}')$] intersect. Estimate the value of the term (A) at this point.
5. From Figure 14, find the value of the zero term's magnitude [$M_Z(\omega_{NC}')$] by plotting the estimated value of the zero (A) from step 4 at the normalized desired gain

crossover frequency (ω_{NC}') and reading from the zero magnitude (M_Z) axis.

6. Use the following equation to find the value of the gain (K):

$$K = \frac{K_F}{[M_Z(\omega_{NC}')][M_P(\omega_{NC}')]} \quad (54)$$

Where:

K_F = the gain required by the digital filter to provide the desired frequency (ω_{NC}')

$M_Z(\omega_{NC}')$ = the magnitude of the zero term

$M_P(\omega_{NC}')$ = the magnitude of the pole term

7. Program the HCTL-1000 with:
   Register R20H = 256 × A (55)
   Register R21H = 256 × B (56)
   Register R22H = 4 × K (57)

Note: The range of allowable values for registers 20H, 21 H, and 22H is integers between 0 and 255 decimal (0 to 0FF Hex). If the required number for the gain that must be programmed into register R22H is greater that 255 decimal, then the gain of some other component in the system must be increased, or the desired gain crossover frequency (ω_C') must be decreased.

Appendices

Appendix A: Design Example of a System with a Voltage Source Amplifier:

In this section the HCTL-1000's digital filter parameters A, B, and K will be computed for an actual benchtop system with a voltage source amplifier.

Open Loop System Model:

The open loop system model for a system with a voltage source amplifier is shown in Figure 6A.

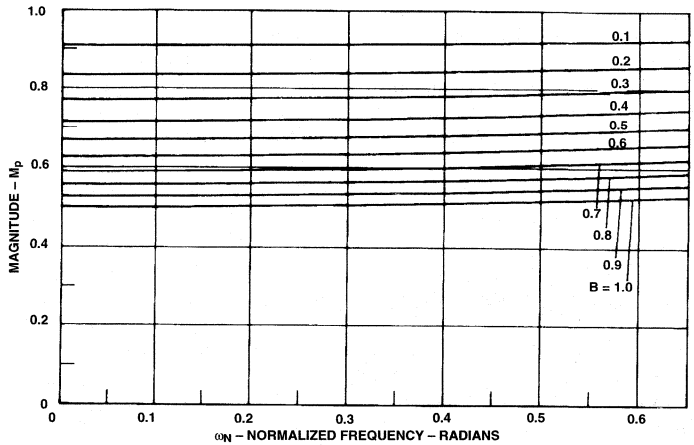

Figure 12. Magnitude Contribution of the Pole Term.

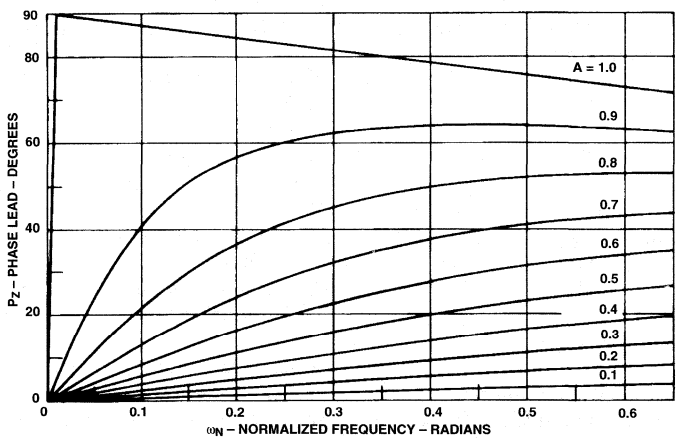

Figure 13. Phase Lead Contribution of the Zero Term.

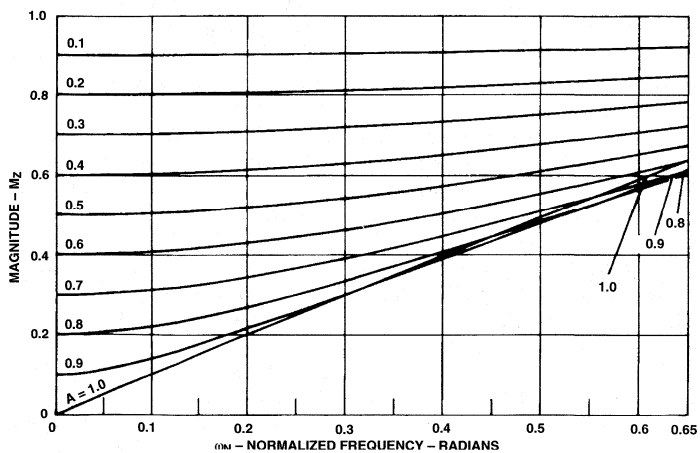

Figure 14. Magnitude Contribution of the Zero Term.

Choosing a bandwidth and sampling time:
The first step is to determine the desired bandwidth and sampling time of the system. For this example, a bandwidth of 60 Hz will be chosen. The sampling frequency of the HCTL-1000 should be at least 10 times the bandwidth of the system. The HCTL-1000's default sample time (t) of .00052 sec will be chosen. This makes the sampling frequency = 1/t = 1923 Hz which is approximately 32 times the bandwidth of the system. See Equation 8.

The Zero Order Hold (ZOH) transfer function:
The transfer function of the zero order hold is:

$$Z(s) = e^{-st/2} = e^{-.00026s} \quad (6)$$

Where the time between samples (sampling time) (t) of the HCTL-1000 has been chosen as .52 milliseconds.

t = 0.00052 seconds

The phase contribution of the zero order hold [$P_{ZOH}(\omega)$] to the system is:

$$P_{ZOH}(\omega) = \frac{-[\omega][t]}{2} \quad (7)$$

Digital to Analog Converter (DAC) Parameters:
A linear, voltage source amplifier has been chosen to drive the motor. This amplifier requires a digital to analog converter (DAC) to convert the 8 bit motor command word from the HCTL-1000 into an analog voltage. The gain (K_D) of the example -5 to +5 volt DAC is as follows:

$$K_D = \frac{5 - (-5) \text{ volts}}{256 - 0 \text{ counts}} \quad (10)$$

K_D = .039 volts/count

Amplifier Parameters:
Next, the gain of the voltage source amplifier must be determined. The gain of a linear, voltage source amplifier is determined by measuring the output voltage of the amplifier for a known input voltage. For the example system, the linear, voltage source amplifier's gain (K_A) is:

$$K_A = \frac{2.00 - 0 \text{ volts-out}}{1.00 - 0 \text{ volts-in}} \quad (11)$$

K_A = 2.00 volts-out/volt-in.

Motor Parameters:
The motor parameters from the manufacturer's data sheet are:

Motor torque constant (K_T) = 3.15×10^{-2} N-m/amp
Motor moment of inertia (J_M) = 2.69×10^{-6} kg-m^2
Terminal resistance (R) = 5.44 ohms
Voltage constant (K_E) = 3.15×10^{-2} volt-sec/rad
Armature inductance (L) = 9.80×10^{-4} henries

System Moment of Inertia:
The total moment of inertia of the system (J) is determined by adding the moment of inertia of the motor's rotor (J_M), the moment of inertia of the load (J_L), and the moment of inertia of the encoder codewheel (J_C). For the example system there is no load external to the motor other than the encoder codewheel. Therefore, the total system moment of inertia (J) is:

$$J = J_M + J_L + J_C = (2\text{-}69 \times 10^{-6}) + 0 + (4 \times 10^{-8}) \text{ kg-m}^2$$
$$= 2.73 \times 10^{-6} \text{ kg-m}^2 \quad (12)$$

The DC Motor Transfer Function:
The motor transfer function of a DC motor driven by a voltage source amplifier is:

$$G(s) = \frac{\theta(s)}{v(s)} = \frac{\text{position output}}{\text{voltage input}} = \frac{K_{MV}}{s[sT_M + 1][sT_E + 1]} \quad (13)$$

Calculation of the Transfer Function of the DC Motor:
The motor parameters and the total moment of inertia of the system are used to calculate the mechanical and electrical time constants and the gain constant of the motor. The equations for the mechanical time constant (T_M) and the electrical time constant (T_E) of the motor are:

$$T_M = \frac{[R][J]}{[K_E][K_T]} \text{ (seconds)} \quad (14)$$

$$T_E = \frac{L}{R} \text{ (seconds)} \quad (15)$$

The gain constant (K_{MV}) of the motor is computed as:

$$K_{MV} = \frac{1}{K_E} \text{ (rad/amp/-sec}^2\text{)} \quad (16)$$

For the example system:

$$T_M = \frac{[5.44][2.73 \times 10^{-6}]}{[.0315][.0315]} \text{ (seconds)}$$

T_M = .015 seconds

$$T_E = \frac{9.8 \times 10^{-4}}{5.44} \text{ (seconds)}$$

T_E = 0.18 milliseconds

$$K_{MV} = \frac{1}{.0315} \text{ rad/sec/volt}$$

K_{MV} = 31.75 rad/sec/volt

Because the mechanical time constant (T_M) is more than 10 times larger than the electrical time constant (T_E) of the example, the DC motor transfer reduces to:

$$G(s) = \frac{K_{MV}}{s(sT_M + 1)} = \frac{31.75}{s(0.15s + 1)} \quad (17)$$

The phase contribution $[P_M(\omega)]$ of the motor driven at frequency (ω) by a voltage source amplifier to the system is:

$$P_M(\omega) = -\arctan(\omega T_M) - \frac{\pi}{2} \text{ (radians)}$$

$$P_M(\omega) = -\arctan(\omega[.015]) - \frac{\pi}{2} \text{ (radians)} \quad (18)$$

Magnitude contribution $[M_M(\omega)]$ of the motor driven at frequency (ω) by a voltage source amplifier is:

$$M_M(\omega) = \frac{K_{MV}}{\omega\sqrt{1 + ([\omega][T_M])^2}} \quad (19)$$

$$M_M(\omega) = \frac{31.75}{\omega\sqrt{1 + ([\omega][.015])^2}}$$

Encoder Parameters:
The parameters of the encoder must be determined. The parameters of the Hewlett-Packard HEDS-5000 encoder chosen for this example are:

N = 256 slits in the codewheel
C = 4N = 1024 quadrature encoder counts/ codewheel revolution

$J_C = 4 \times 10^{-8}$ kg-m^2

Therefore, the transfer function and magnitude contribution (E) of the encoder to the system is:

$$E = \frac{C}{2\pi} = \frac{1024}{2\pi} \text{ (count/radians)} \quad (24)$$

Calculation of the Open Loop Transfer Function:
The open loop transfer function is calculated as:

$$M(s) = [K_D][ZOH][K_A][G(s)][C/(2 \times \pi)] \quad (5)$$

$$M(s) = [.039][e^{-.00026s}][2.0]\left[\frac{31.75}{s(.015s + 1)}\right]\left[\frac{1024}{2\pi}\right]$$

$$M(s) = \frac{403.56\, e^{-.00026s}}{s(.015s + 1)}$$

Determination of the Gain Crossover Frequency, Phase Crossover Frequency, Gain Margin, and Phase Margin of the Open Loop Transfer Function Using a Bode Plot:
The equation which is used to find the phase $[P_{HU}(\omega)]$ of the uncompensated, open loop transfer function is:

$$P_{HU}(\omega) = P_M(\omega) + P_{ZOH}(\omega) \text{ (radians)} \quad (27)$$

$$P_{HU}(\omega) = -\arctan(\omega \times T_M) - \frac{\pi}{2} - \frac{\omega t}{2} \text{ (radians)} \quad (29)$$

$$P_{HU}(\omega) = -\arctan(\omega \times .015) - \frac{\pi}{2} - \frac{\omega[.00052]}{2} \text{ (rad)}$$

The phase $[P_{HU}(\omega)]$ can now be calculated for various values of frequency (ω). To be graphed onto a Bode plot, the values for the phase $[P_{HU}(\omega)]$ must be converted from radians to degrees using the equation:

1 radian = 57.296 degrees (31)

Some values for the phase $[P_{HU}(\omega)]$ are shown in degrees for various values of frequency (ω) in Table 2.

The equation which is used to find the magnitude $[M_U(\omega)]$ of the uncompensated, open loop transfer function is:

(32)

$$M_U(\omega) = [M_U(\omega)][K_D][K_A][E]$$

$$M_U(\omega) = \frac{[K_{MV}][K_D][K_A][C/(2\pi)]}{\omega\sqrt{1 + ([T_M][\omega])^2}}$$

$$M_U(\omega) = \frac{[[31.75][.039][2.0][(1024/(2\pi)]}{\omega\sqrt{1 + ([.015][\omega])^2}}$$

The magnitude $[M_U(\omega)]$ can now be calculated for various values of frequency (ω). To be graphed onto a Bode plot, the values for the magnitude $[M_U(\omega)]$ must be converted from decimal to decibels using the equation:

$$db = 20 \log [M_U(\omega)] \quad (36)$$

Some values for the magnitude $[(M_U(\omega)]$ are shown in decibel for various values of frequency (ω) in Table 2.

Figure 15 shows a Bode plot of the phase $[P_{HU}(\omega)]$ and gain $[M_U(\omega)]$.

The next step is to find the gain and phase crossover frequencies of the uncompensated, open loop system. The gain crossover frequency (ω_C) of the uncompensated open loop system can be computed by setting the magnitude $[M_U(\omega)]$ in db equal to 0 db and solving the equation for (ω_C).

$$20 \log [M_U(\omega_C)] = 0 \text{ db} \quad (38)$$

$$20 \log \left[\frac{[K_{MV}][K_D][K_A][C/(2\pi)]}{\omega_C\sqrt{1 + ([\omega_C][T_M])^2}}\right] = 0 \text{ db}$$

The difficulty in choosing this method is that the solution can involve a fourth order (quartic) equation. A simpler method is to read the gain crossover frequency from the Bode plot

Table 2. The magnitude (M_U) and phase (P_{HU}) of the open loop transfer function over frequency (ω), for the system with a voltage source amplifier.

Frequency (ω) (radians/sec)	Magnitude (M_U) (decibels)	Phase (P_{HU}) (degrees)
1	52.12	-90.87
2	46.09	-91.75
3	42.57	-92.62
4	40.06	-93.49
5	38.11	-94.36
6	36.52	-95.22
7	35.17	-96.09
8	33.99	-96.95
9	32.95	-97.81
10	32.02	-98.66
20	25.72	-106.97
30	21.78	-114.63
40	18.74	-121.51
50	16.21	-127.56
60	13.98	-132.82
70	12.00	-137.38
80	10.19	-141.33
90	8.54	-144.76
100	7.01	-147.75
200	-3.89	-164.51
300	-10.68	-171.92
400	-15.59	-176.48
500	-19.42	-179.84
600	-22.57	-182.59
700	-25.23	-184.98
800	-27.54	-187.15
900	-29.58	-189.16
1000	-31.41	-191.08

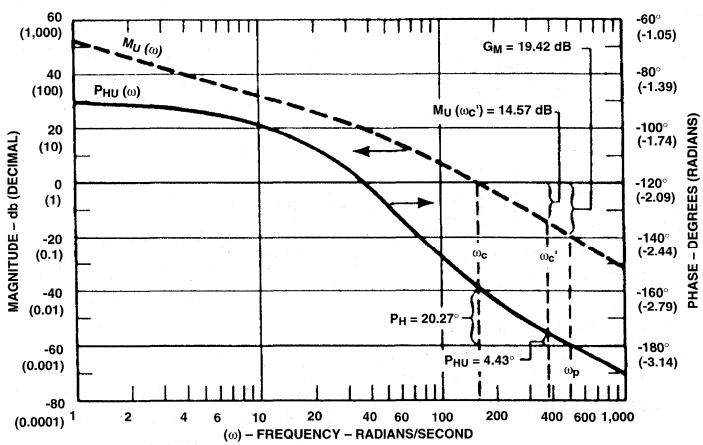

Figure 15. Bode Plot of the Open Loop System with the Voltage Source Before Compensation.

shown in Figure 15. From the Bode plot it can be seen that the magnitude $[M_U(\omega)]$ crosses the 0 db axis at approximately 160 radians/sec. Therefore the gain crossover frequency (ω_C) of the uncompensated, open loop system is:

$$\omega_C = 160 \text{ radians/sec} = 25.5 \text{ Hz}$$

The phase crossover frequency (ω_P) of the uncompensated, open loop system can be found by setting the phase $[P_{HU}(\omega)]$ equal to $-\pi$ radians (i.e. -180 degrees) and solving for (ω_P):

$$P_{HU}(\omega_p) = -\pi \text{ radians} - \arctan([\omega_p][T_M])$$

$$-\frac{\pi}{2} - \frac{[\omega_p][t]}{2} = -\pi \text{ radians} \quad (37)$$

As with the phase crossover frequency calculation, the simplest method to find the phase crossover frequency (ω_P) is to read it directly from the Bode plot. The phase crossover frequency (ω_P) is the point where the phase $[P_{HU}(\omega)]$ crosses the -180 degree axis. From the Bode plot shown in Figure 15 it can be seen that the phase crossover frequency (ω_P) is approximately:

$$\omega_P = 500 \text{ radians/sec} = 79.6 \text{ Hz}$$

The gain margin (G_M) is computed at the phase crossover frequency (ω_P) as:

$$G_M = -20 \log [M_U(\omega_p)] \text{ db} \quad (40)$$

$$G_M = -20 \log \left[\frac{[K_{MV}][K_D][K_A][C/(2\pi)]}{\omega_p \sqrt{1 + ([\omega_p][T_M])^2}} \right] \text{db}$$

$$= -20 \log \left[\frac{[[31.75][.039][2.0][(1024/(2\pi)]}{500 \times \sqrt{1 + ([500][.015])^2}} \right] \text{db}$$

$G_M = 19.42$ db

The gain margin (G_M) can also be read directly from the Bode plot as the difference between the 0 db axis and the magnitude $[M_U(\omega_P)]$ at the phase crossover frequency (ω_P).

The phase margin (P_H) is computed as 180 degrees plus the phase $[P_{HU}(\omega_C)]$ in degrees at the gain crossover frequency (ω_C).

$$P_H = [180 \text{ deg.} + [57.296(\text{deg/rad}) [P_{HU}(\omega_C)]] \text{ degrees} \quad (41)$$

$$= 180 + 57.296\left(-\arctan([\omega_C][T_M]) - \frac{\pi}{2} - \frac{[\omega_C][t]}{2}\right) \text{deg}$$

$$= 180 + 57.296\left(-\arctan([160][.015]) - \frac{\pi}{2} - \frac{[160][.00052]}{2}\right)$$

$= 20.27$ degrees

The phase margin (P_H) can also be read directly from the Bode plot as the difference between the phase $[P_{HU}(\omega)]$ at the gain crossover frequency (ω_C) and the -180 degree axis.

Modification of the Open Loop System Transfer Function Using Compensation to Achieve the Desired Closed Loop Characteristics:

Now that the uncompensated, open loop characteristics of the system are known and plotted on a Bode plot, the HCTL-1000's digital compensation filter can be designed to provide the desired closed loop characteristics.

For this system closed loop bandwidth (BW) of 60 Hertz [377 radians/sec] is desired, and a compensated, desired phase margin (P_{HC}) of 40 degrees has been chosen.

The desired open loop gain crossover frequency (ω_C') can be approximated as the desired closed loop bandwidth (BW):

$$(\omega_C') = \text{BW radians/sec} \quad (42)$$

$(\omega_C') = 377$ radians/sec

The normalized, desired gain crossover frequency (ω_{NC}') is:

$$\omega_{NC}' = [\omega_C'][t] \text{ radians} \quad (48)$$

$\omega_{NC}' = [377 \text{ rad/sec}][.00052 \text{ sec}]$
$= .1960$ radians

Determination of the phase margin and gain of the open loop transfer function at the desired, open loop gain crossover frequency:

For the example system with the voltage source amplifier, where the electrical time constant has been neglected, the phase margin (P_{MU}) of the uncompensated system at the desired gain crossover frequency (ω_C') is computed as:

$$P_{MU} = [180 \text{ deg.} + ([57.296 (\text{deg/rad})][P_{HU}(\omega_C')]] \text{ degrees} \quad (43)$$

$$P_{MU} = 180 + [57.296][-\arctan([\omega_C'][T_M]) - \left[\frac{\pi}{2} - \frac{[\omega_C][t]}{2}\right]$$

$$P_{MU} = 180 + [57.296][-\arctan([377][.015]) - \left[\frac{3.142}{2} - \frac{[377][.00052]}{2}\right]$$

$P_{MU} = 4.43$ degrees

The phase lead (P_L) that the HCTL-1000's digital filter must provide to achieve the desired closed loop performance is the difference between the desired, compensated phase margin (P_{HC}) at the gain crossover frequency (ω_C') and the uncompensated phase margin (P_{MU}) at frequency (ω_C'):

$$P_L = P_{HC} - P_{MU} \text{ degrees} \quad (44)$$

$P_L = 40 - 4.43 = 35.57$ degrees

The magnitude $[M_U(\omega_C')]$ of the uncompensated system at frequency (ω_C') with a voltage source amplifier where the electrical time constant has been neglected is:

$$M_U(\omega_C') = \frac{[K_{MV}][K_D][K_A][(C/(2 \times \pi)]}{\omega_C' \sqrt{1 + ([T_M][\omega_C'])^2}} \quad (34)$$

$$M_U(\omega_C') = \frac{[[31.74][.039][2.0][1024/([2][3.142])]}{377 \sqrt{1 + ([.015][377])^2}}$$

$M_U(\omega_C') = .186$
$(-20 \log .186 = 14.6$ db)

The gain (K_F) required from the digital filter to make the overall gain of the system equal to 1 at the desired gain crossover frequency (ω_C') is defined as:

$$K_F = \frac{1}{M_U(\omega_C')} \quad (45)$$

$$K_F = \frac{1}{.186}$$

$K_F = 5.38$

Use of the Combination Method to Design the HCTL-1000's Digital Compensation Filter:

On Figure 16 the plot of B = 0.9 is chosen to contribute 5.3 degrees of phase lead ($P_P((\omega_{NC}'))$ at ω_{NC}' = 0.196.

The plot of B = 0.9 in Figure 17 at ω_{NC}' = 0.196 gives a gain $[M_P(\omega_{NC}')]$ of 0.53.

The remaining phase lead at frequency (ω_C') which must be contributed by the zero term $[P_Z(\omega_{NC}')]$ is:

$$P_Z(\omega_{NC}') = P_L - P_P(\omega_{NC}') \quad (53)$$
$$= 35.57 - 5.3 = 30.27 \text{ degrees}$$

On Figure 18, the point where ω_{NC}' = .196 and $P_Z(\omega_{NC}')$ = 30.27 intersect is A = 0.76.

The magnitude of the zero term where A = .76 at ω_{NC}' = 0.196 on Figure 19 is $M_Z(\omega_{NC}')$ = 0.29. The gain (K) which must be contributed by the digital filter is:

$$K = \frac{K_F}{[M_P(\omega_{NC}')][M_Z(\omega_{NC}')]} = \frac{5.38}{[0.53][.295]} = 34.4 \quad (54)$$

The values which should be programmed into the HCTL-1000 are therefore:

A = [256][0.76] = 194.56 ≅ 195 (55)

B = [256][0.9] = 230.4 ≅ 230 (56)

K = [4][34.4] = 137.6 ≅ 138 (57)

Figure 20 shows the actual response of the closed loop system to a step input of 25 quadrature counts. (25 quadrature counts on a 256 count codewheel that is

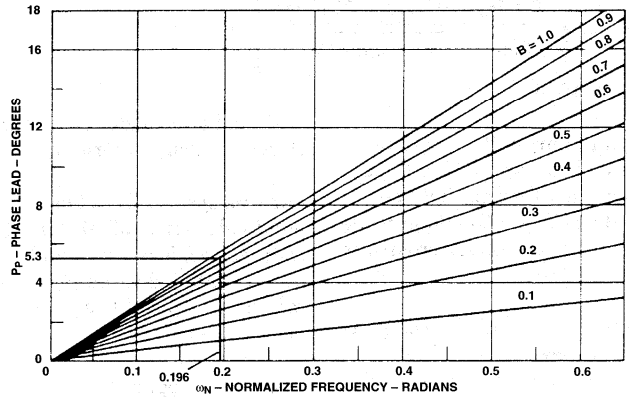

Figure 16. Phase Lead Contribution of the Pole Term to the Closed Loop System Compensator.

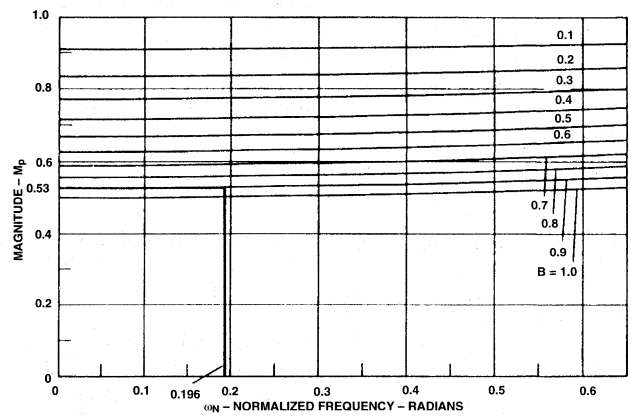

Figure 17. Magnitude Contribution of the Pole Term to the Closed Loop System Compensator.

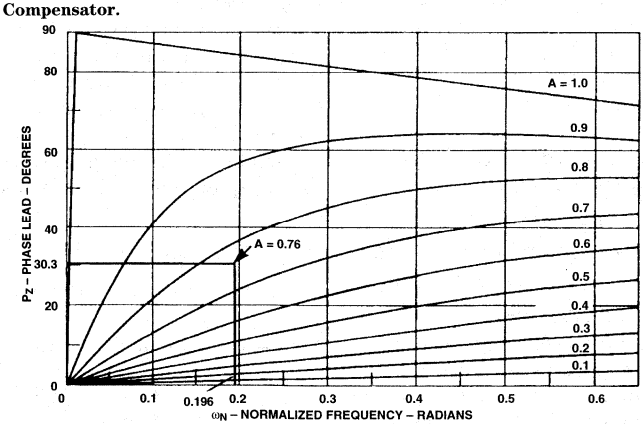

Figure 18. Phase Lead Contribution of the Zero Term to the Closed Loop System Compensator.

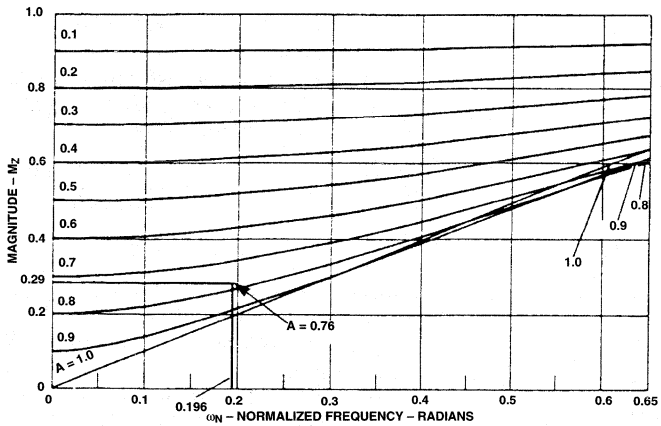

Figure 19. Magnitude Contribution of the Zero Term to the Closed Loop System Compensator.

multiplied by 4 equals 8.79 degrees of angular rotation). The amount of overshoot of the system's response is roughly consistent with a system with 40 degrees of phase margin.

For high phase margin systems the relationship between the risetime (t_C) and the bandwidth (BW) of a closed loop system can be approximated as:

$$t_R = \frac{2.2}{\text{BW (in radians/sec)}} \qquad (58)$$

For low phase margin systems which have some overshoot in the closed loop step response, the relationship between the risetime (t_R) and the bandwidth (BW) of a closed loop system can be approximated as:

$$\frac{0.6}{BW} < t_R < \frac{2.2}{BW} \qquad (59)$$

Figure 21 shows the actual rise time of the closed loop system to a step input of 25 quadrature counts. Note that the risetime is defined as the time required for the output to go from 10% to 90% of its final value. Since this system has some overshoot, equation (59) applies. The risetime (t_R) should therefore be:

$$\frac{0.6}{[60][6.28]} < t_R < \frac{2.2}{[60][6.28]} \text{ seconds}$$

$$.00159 < t_R < .0058 \text{ seconds}$$

The risetime measured from figure 21 is:

$$t_R = 0.0042 \text{ seconds}$$

Therefore the measured risetime falls within the expected range of values for a bandwidth of 60 Hertz.

Appendix B: Design Example of a System with a Current Source Amplifier:

In this section the HCTL-1000's digital filter parameters A, B, and K will be computed for an actual benchtop system with a current source amplifier.

Open Loop System Model:
The open loop system model for a system with a current source amplifier is shown in Figure 6B.

Choosing a bandwidth and sampling time:
The first step is to determine the desired bandwidth and sampling time of the system. For this example, a bandwidth of 60 Hz will be chosen. The sampling frequency of the HCTL-1000 should be at least 10 times the bandwidth of the system. The HCTL-1000's default sample time of .00052 sec will be chosen. This makes the sampling frequency = 1/t = 1923 Hz which is approximately 32 times the bandwidth of the system. See Equation 8.

The zero order hold (ZOH) transfer function:
The transfer function of the zero order hold is:

$$Z(s) = e^{-st/2} = e^{-.00026s} \qquad (6)$$

Where the time between samples (sampling time) (t) of the HCTL-1000 has been chosen as .52 milliseconds.

$$t = 0.00052 \text{ seconds}$$

The phase contribution of the zero order hold ($P_{ZOH}(\omega)$) to the system is:

$$P_{ZOH}(\omega) = -\frac{[\omega][t]}{2} \qquad (7)$$

Amplifier parameters:
Next, the gain of the current source amplifier must be determined. For the example system, a pulse width modulated, current source amplifier with a gain (K_A) = 0.02 amps-out/count has been chosen. No digital to analog converter (DAC) is used with a pulse width modulated amplifier.

$$K_A = 0.02 \text{amps-out/count} \qquad (11)$$

Motor parameters:
The motor parameters from the manufacturer's data sheet are:

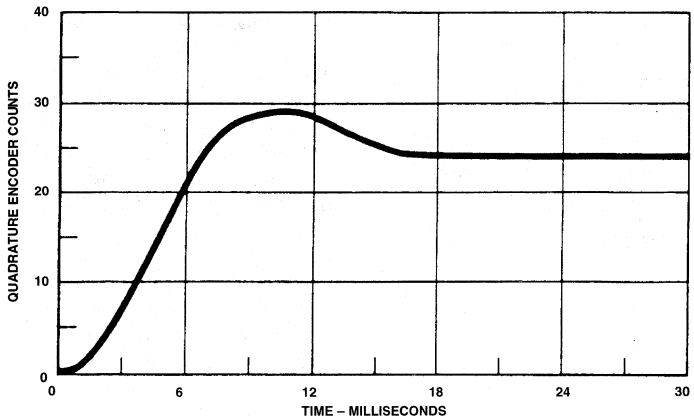

Figure 20. Response of the Closed Loop System to a Step Input of 25 Quadrature Encoder Counts.

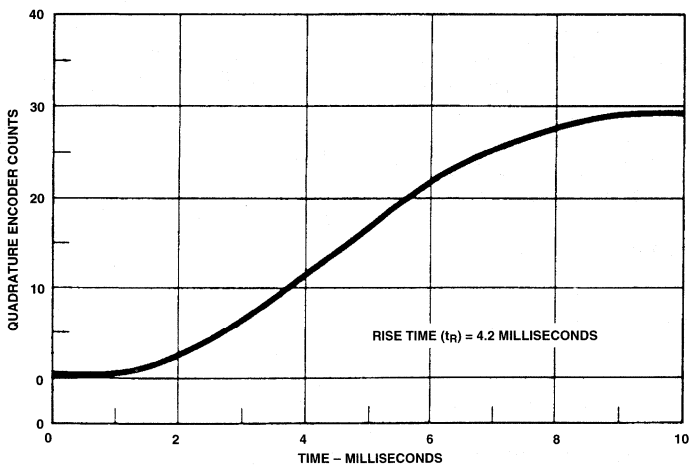

Figure 21. Rise Time of the Closed Loop System to a Step Input of 25 Quadrature Encoder Counts.

Motor torque constant (K_T) = 3.15×10^{-2} N-m/amp

Motor moment of inertia (J_M) = 2.69×10^{-6}kg-m^2

Terminal resistance (R) = 5.44 ohms

Voltage constant (K_E) = 3.15×10^{-2} volt-sec/rad

Armature inductance (L) = 9.8×10^{-4} henries

System moment of inertia:
The total moment of inertia of the system (J) is determined by adding the moment of inertia of the motor's rotor (J_M), the moment of inertia of the load (J_L), and the moment of inertia of the encoder codewheel (J_C). For the example system there is no load external to the motor other than the encoder codewheel. Therefore, the total system moment of inertia (J) is:

$$J = J_M + J_L + J_C = (2.69 \times 10\text{-}6) + 0 + (4 \times 10^{-8})\ \text{kg-m}^2 = 2.73 \times 10^{-6}\ \text{kg-m}^2 \quad (12)$$

The DC motor transfer function:
The motor transfer function of a DC motor driven by a current source amplifier is:

$$G(s) = \frac{\theta(s)}{v(s)} = \frac{\text{position output}}{\text{voltage input}} = \frac{K_{MC}}{s^2} \quad (20)$$

Calculation of the gain constant and transfer function of the DC motor:
The motor parameters and the total moment of inertia of the system including the motor are used to calculate the gain constant of the motor. The gain constant (K_{MC}) of the motor is computed as:

$$K_{MC} = \frac{K_T}{J}\ \text{(rad/amp/-sec}^2\text{)} \quad (21)$$

For the example system:

$$K_{MC} = \frac{.0315\ \text{N-m/amp}}{2.73 \times 10^{-6}\text{kg-m}^2} = 11{,}538.46\ \text{rad/amp-sec}^2$$

Therefore the motor transfer function is:

$$G(s) = \frac{K_{MC}}{s^2} = \frac{11{,}538.46}{s^2}$$

The phase contribution ($P_M(\omega)$) of the motor driven at frequency (ω) by a current source amplifier to the system is:

$$P_M(\omega) = -\pi\ \text{(radians)} \quad (22)$$

The magnitude contribution ($M_M(\omega)$) of the motor driven at frequency (ω) by a current source amplifier is:

$$M_U(\omega) = \frac{K_{MC}}{(\omega)^2} \quad (23)$$

$$M_U(\omega) = \frac{11{,}538.46}{(\omega)^2}$$

Encoder parameters:
The parameters of the encoder must be determined. The parameters of the Hewlett-Packard HEDS-5000 encoder chosen for this example are:

N = 256 slits in the codewheel
C = 4N = 1024 quadrature encoder counts/codewheel revolution
$J_C = 4 \times 10^{-8}$ kg-m^2

Therefore, the transfer function and magnitude contribution (E) of the encoder to the system is:

$$E = \frac{C}{2\pi} = \frac{1024}{2\pi} \text{ (counts/radian)} \quad (24)$$

Calculation of the open loop transfer function:
The open loop transfer function is calculated as:

$$M(s) = [ZOH] [K_A] [G(s)] [C/(2\pi)]$$

$$M(s) = [e^{-.00026s}][0.02] \left[\frac{11{,}538.46}{s^2}\right]\left[\frac{1024}{2\pi}\right] \quad (5)$$

$$M(s) = \frac{37{,}610[e^{-.00026s}]}{s^2}$$

Determination of the gain crossover frequency, phase crossover frequency, gain margin, and phase margin of the open loop transfer function using a Bode plot:
The equation which is to be used to find the phase $[P_{HU}(\omega)]$ of the uncompensated, open loop transfer function is:

$$P_{HU}(\omega) = P_M(\omega) + P_{ZOH}(\omega) \text{ (radians)} \quad (27)$$

$$P_{HU}(\omega) = -\pi - \frac{[\omega][t]}{2} \text{ (radians)} \quad (30)$$

$$P_{HU}(\omega) = -\pi - \frac{[\omega][.00052]}{2} \text{ (radians)}$$

The phase $[P_{HU}(\omega)]$ can now be calculated for various values of frequency (ω). To be graphed into a Bode plot, the values for the phase $[P_{HU}(\omega)]$ must be converted from radians to degrees using the equation:

1 radian = 57.296 degrees (31)

Some values for the phase $[P_{HU}(\omega)]$ are shown in degrees for various values of frequency (ω) in Table 3. The equation which is used to find the magnitude $[M_U(\omega)]$ of the uncompensated, open loop transfer function is:

$$M_U(\omega) = [M_M(\omega)][K_A][E] \quad (32)$$

$$M_U(\omega) = \frac{[K_{MC}][K_A][C/2\pi]}{\omega^2}$$

$$M_U(\omega) = \frac{11{,}538.46 \times 0.02 \times (1024/(2\pi))}{\omega^2}$$

The magnitude $[M_U(\omega)]$ can now be calculated for various values of frequency (ω). To be graphed onto a Bode plot, the values for the magnitude $[M_U(\omega)]$ must be converted from decimal to decibels using the equation:

$$db = 20 \log [M_U(\omega)] \quad (36)$$

Some values for the magnitude $[M_U(\omega)]$ are shown in decibel for various values of frequency (ω) in Table 3.

Figure 22 shows a Bode plot of the phase $[P_{HU}(\omega)]$ and gain $[M_U(\omega)]$.

The next step is to find the gain and phase crossover frequencies of the uncompensated, open loop system. The gain crossover frequency (ω_C) of the uncompensated open loop system can be computed by setting the magnitude $[M_U(\omega)]$ in db equal to 0 db and solving the equation for (ω_C):

$$20 \log [M_U(\omega_C)] = 0 \text{ db} \quad (38)$$

$$20 \log \left[\frac{[K_{MC}][K_A][(C/2\pi)]}{(\omega_C)^2}\right] = 0 \text{ db}$$

$$\omega_C = \sqrt{[K_{MC}][K_A][(C/(2\pi)]}$$

Another method is to read the gain crossover frequency from the Bode plot shown in Figure 22. From the Bode plot it can be seen that the magnitude $[M_U(\omega)]$ crosses the 0 db axis at approximately 195 radians/sec. Therefore gain crossover frequency (ω_C) of the uncompensated, open loop system is:

ω_C = 195 radians/sec
= 31.04 Hz

The phase crossover frequency (ω_P) of the uncompensated, open loop system can be found by setting the phase $[P_{HU}(\omega)]$ equal to $-\pi$ radians (-180 degrees) and solving for (ω_P):

$$P_{HU}(\omega_p) = -\pi \text{ radians} \quad (37)$$

$$-\pi - \frac{[\omega][t]}{2} = -\pi \text{ radians}$$

Another method to find the phase crossover frequency (ω_P) is to read it directly from the Bode plot. The phase crossover frequency (ω_P) is the point where the phase crosses the -180 degree axis. From the Bode plot shown in Figure 22 it can be seen that the phase crossover frequency (ω_P) is:

(ω_P) = 0.0 radians/sec
= 0.0 Hz

Table 3. The magnitude (M_U) and phase (P_{HU}) of the open loop transfer function over frequency (ω), for the system with a voltage source amplifier.

Frequency (ω) (radians/sec)	Magnitude (M_U) (decibels)	Phase (P_{HU}) (degrees)
1	91.61	-180.02
2	79.57	-180.03
3	72.52	-180.05
4	67.53	-180.06
5	63.65	-180.08
6	60.48	-180.09
7	57.81	-180.10
8	55.49	-180.12
9	53.44	-180.13
10	51.61	-180.15
20	39.57	-180.30
30	32.52	-180.45
40	27.53	-180.60
50	23.65	-180.75
60	20.48	-180.89
70	17.81	-181.04
80	15.49	-181.19
90	13.44	-181.34
100	11.61	-181.49
200	-.43	-182.98
300	-7.48	-184.47
400	-12.47	-185.96
500	-16.35	-187.45
600	-19.52	-188.94
700	-22.19	-190.43
800	-24.51	-191.92
900	-26.56	-193.41
1000	-28.39	-194.90

The gain margin (G_M) is computed at the phase crossover frequency (ω_P) as:

$$G_M = -20 \log [M_U(\omega_P)] \text{ db} \quad (40)$$

However, since the phase crossover frequency is zero, the system is unstable, and the gain margin is minus infinity.

The phase margin (P_H) can be computed as 180 degrees plus the phase $[P_{HU}(\omega)]$ in degrees at the gain crossover frequency (ω_C).

$$P_H = [180 \text{ deg.} + [57.296 \text{ (deg/rad)}][P_{HU}(\omega_C)]] \text{ degrees} \quad (41)$$

$$= 180 + [57.296]\left[-\pi - \frac{[\omega_C]\,[t]}{2}\right] \text{ degrees}$$

$$= [180 + 57.296]\left[-\pi - \frac{[195][.00052]}{2}\right]$$

= -2.9 degrees (ie. unstable!)

The phase margin (P_H) can also be read directly from the Bode plot as the difference between the phase $[P_{HU}(\omega)]$ at the gain crossover frequency (ω_C) and the -180 degree axis.

Modification of the Open Loop System Transfer Function Using Compensation to Achieve the Desired Closed Loop Characteristics

Now that the uncompensated, open loop characteristics of the system are known and plotted on a Bode plot, the HCTL-1000's digital compensation filter can be designed to provide the desired closed loop characteristics.

For this system closed loop bandwidth (BW) of 60 Hertz [377 radians/sec] is desired, and a compensated, phase margin (P_{HC}) of 40 degrees has been chosen.

The desired open loop gain crossover frequency (ω_C') can be approximated as the desired closed loop bandwidth (BW):

$$\omega_C' = \text{BW radians/sec} \quad (42)$$

$$\omega_C' = 377 \text{ radians/sec}$$

The normalized, desired gain crossover frequency (ω_{NC}') is:

$$\omega_{NC}' = [\omega_C'][t] \text{ radians} \quad (48)$$

$$\omega_{NC}' = [377 \text{ (rad/sec)}]\,[.00052 \text{ (sec)}] = .1960 \text{ radians}$$

Determination of the phase margin and gain of the open loop transfer function at the desired gain crossover frequency:

For the example system with the current source amplifier the phase margin (P_{MU}) of the uncompensated system at the desired gain crossover frequency (ω_C') is computed as:

$$P_{MU} = [180 \text{ deg.} + [57.296 \text{ (deg/rad)}][P_{HU}(\omega_C')]] \text{ degrees} \quad (43)$$

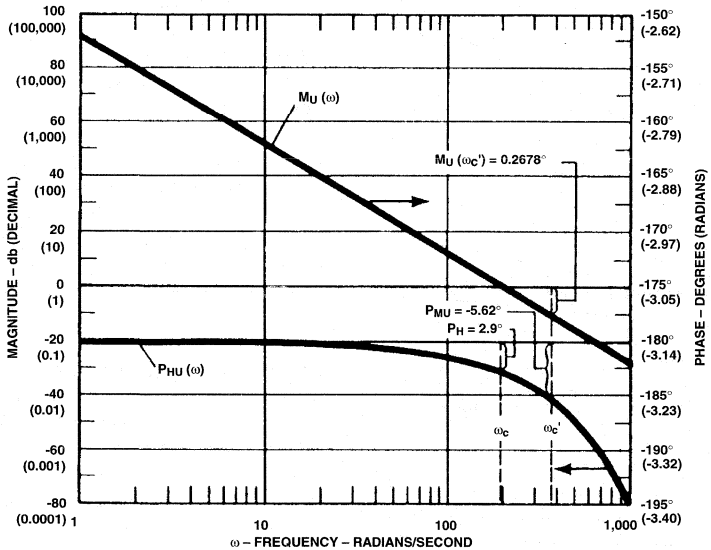

Figure 22. Bode Plot of the Open Loop System with the Current Source Before Compensation.

$$P_{MU} = 180 + 57.296\left[-\pi - \frac{[\omega_C'][t]}{2}\right]$$

$$P_{MU} = 180 + 57.296\left[-\pi - \frac{[377][.00052]}{2}\right]$$

$$P_{MU} = -5.62 \text{ degrees}$$

The phase lead (P_L) that the HCTL-1000's digital filter must provide to achieve the desired closed loop performance is the difference between the desired, compensated phase margin (P_{HC}) at the gain crossover frequency (ω_C') and the uncompensated phase margin (P_{MU}) at frequency (ω_C'):

$$P_L = P_{HC} - P_{MU} \text{ degrees} \quad (44)$$

$$P_L = 40 - (-5.62) = 45.62 \text{ degrees}$$

The magnitude [$M_U(\omega_C')$] of the uncompensated system at frequency (ω_C') with a current source amplifier is:

$$M_U(\omega) = \frac{[K_M][K_A][C/(2\pi)]}{(\omega_C')^2} \quad (35)$$

$$M_U(\omega) = \frac{[11{,}538.46] \times [0.02] \times [1024/(2 \times 3.1416)]}{(377)^2}$$

$$M_U(\omega) = .265$$

The gain (K_F) required from the digital filter to make the overall gain of the system equal to 1 at the desired gain crossover frequency (ω_C') is defined as:

$$K_F = \frac{1}{M_U(\omega_C')} \quad (45)$$

$$K_F = \frac{1}{.265}$$

$$K_F = 3.77$$

Use of the Combination Method to Design the HCTL-1000's Digital Compensation Filter:

On Figure 23 the plot of B = 0.9 is chosen to contribute 5.3 degrees of phase lead [$P_P(\omega_{NC}')$] at $\omega_{NC}' = 0.196$.

The plot of B = 0.9 in Figure 24 at $\omega_{NC}' = 0.196$ gives a gain [$M_P(\omega_{NC}')$] of 0.53.

The remaining phase lead at frequency (ω_C') which must be contributed by the zero term [$P_Z((\omega_{NC}')$] is:

$$P_Z(\omega_{NC}') = P_L - P_P(\omega_{NC}') \quad (53)$$
$$= 45.62 - 5.3 = 40.32 \text{ degrees}$$

On Figure 25, the point where $\omega_{NC}' = .196$ and $P_Z(\omega_{NC}') = 40.32$ intersect is A = 0.826.

The magnitude of the zero term where A = .826 at $\omega_{NC}' = 0.196$ on figure 26 is $M_Z(\omega_{NC}') = 0.249$.

The gain (K) which must be contributed by the digital filter is:

$$K = \frac{K_F}{[M_P(\omega_{NC}')][M_{Z(\omega_{NC}')}]}$$

$$= \frac{3.77}{[.53][.249]} = 28.57 \quad (54)$$

The values which should be programmed into the HCTL-1000 are therefore:

A = [256] [0.826] = 211.45 ≅ 211(55)
B = [256] [0.9] = 230.4 ≅ 230 (56)
K = [4] [28.57] = 114.3 ≅ 114 (57)

Figure 27 shows the actual response of the closed loop system to a step input of 25 quadrature counts. (25 quadrature counts on a 256 count codewheel that is multiplied by 4 equals 8.79 de-

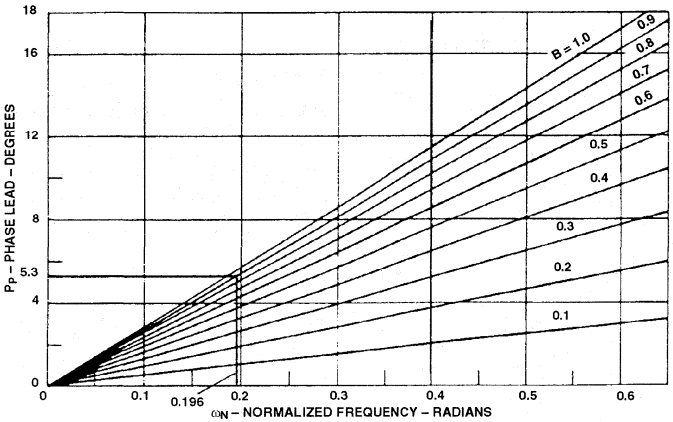

Figure 23. Phase Lead Contribution of the Pole Term to the Closed Loop System Compensator.

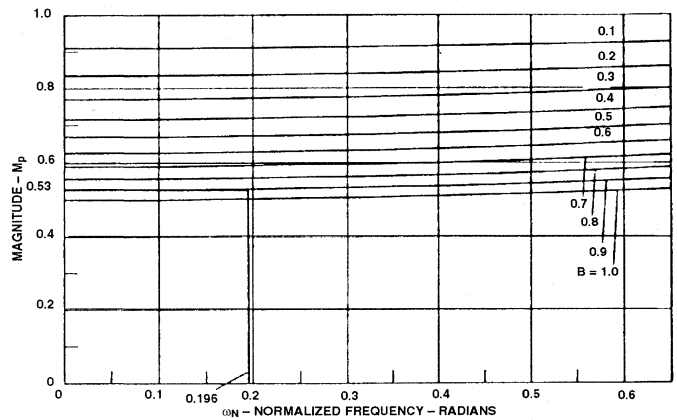

Figure 24. Magnitude Contribution of the Pole Term to the Closed Loop System Compensator.

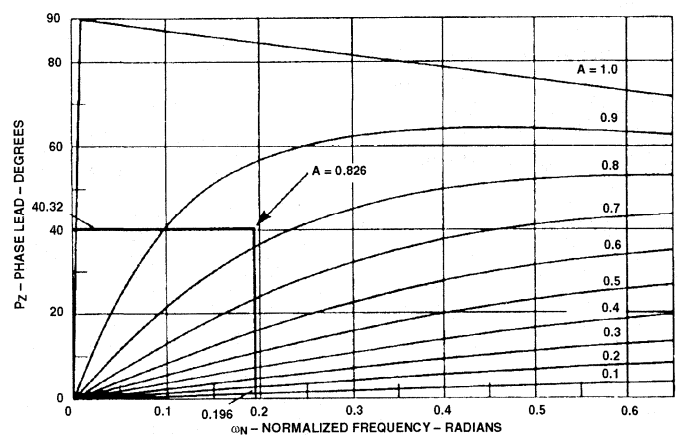

Figure 25. Phase Lead Contribution of the Zero Term to the Closed Loop System Compensator.

grees of angular rotation). The amount of overshoot of the system's response is roughly consistent with a system with 40 degrees of phase margin.

For high phase margin systems the relationship between the risetime (t_R) and the bandwidth (BW) of a closed loop system can be approximated as:

$$t_R = \frac{2.2}{\text{BW (in radians/sec)}} \qquad (58)$$

For low phase margin systems which have some overshoot in the closed loop step response, the relationship between the risetime (t_R) and the bandwidth (BW) of a closed loop system can be approximated as:

$$\frac{0.6}{\text{BW}} < t_R < \frac{2.2}{\text{BW}} \qquad (59)$$

Figure 28 shows the actual risetime of the closed loop system to a step input of 25 quadrature counts. Note that the rise time is defined as the time required for the output to go from 10% to 90% of its final value. Since this system has some overshoot, equation (59) applies. The risetime (t_R) should therefore be:

$$\frac{0.6}{[60][6.28]} < t_R < \frac{2.2}{[60][6.28]} \text{ seconds}$$

$$.00159 < t_R < .0058 \text{ seconds}$$

The risetime measured from figure 28 is:

$$t_R = 0.0050 \text{ seconds}$$

Therefore the measured risetime falls within the expected range of values for a bandwidth of 60 Hertz.

Appendix C: Symbols for Quantities and Their Units

Quantity	Definition	SI Units
A	the HCTL-1000 digital compensation filter's programmable zero term	_____
B	the HCTL-1000 digital compensation filter's programmable pole term	_____
BW	bandwidth	Hertz radians/sec
C	quadrature counts per revolution of the encoder's codewheel	counts
D(z)	the transfer function of the HCTL-1000's digital filter	
E	magnitude contribution of the encoder	counts/radian
f_{CLK}	frequency of the HCTL-1000's external clock	hertz
G(s)	motor transfer function	varies
G_M	the gain margin of the uncompensated open loop transfer function	decibels (db)
J	total system moment of inertia	kg-m^2
J_C	Moment of inertia of the encoder's codewheel	kg-m^2
J_L	Moment of inertia of the load	kg-m^2
J_M	Moment of inertia of the motor's armature	kg-m^2
K	the programmable gain of the HCTL-1000's digital compensation filter	_____
K_A	gain of the amplifier	volts/volt amps/volt volts/count amps/count
K_D	gain of the DAC	volts/ count
K_E	motor voltage constant	volt-sec/rad
K_F	the gain required from the HCTL-1000's digital filter to provide an overall gain equal to one at the desired gain crossover frequency (ω_C')	_____
K_{MC}	motor gain constant with a current source amp.	rad/amp-sec^2
K_{MV}	motor gain constant with a voltage source amp.	rad/volt-sec
K_T	motor torque constant	N-m/amp
L	motor armature inductance	henries
$M_M(\omega)$	magnitude contribution of the motor	_____
$M_P(\omega_N)$	the magnitude of the pole term at ω_{NC}'	_____
$M_Z(\omega_N)$	the magnitude of the zero term at ω_{NC}'	_____

Quantity	Definition	SI Units
M(s)	the open loop transfer function	varies
$M_U(\omega)$	the magnitude of the uncompensated open loop transfer function	_____
N	number of slits in the encoder's codewheel	_____
P_H	the phase margin of the uncompensated, open loop transfer function	degrees
P_{HC}	desired, compensated open loop phase margin	degrees
$P_{HU}(\omega)$	the phase of the uncompensated, open loop transfer function	radians
P_L	the phase lead required from the digital filter	degrees
$P_M(\omega)$	phase contribution of the motor	radians
P_{MU}	the phase margin of the uncompensated, open loop system at the desired gain crossover frequency (ω_C')	degrees
$P_P(\omega_N)$	the phase of the pole term at ω_{NC}'	degrees
$P_Z(\omega_N)$	the phase of the zero term at ω_{NC}	degrees
$P_{ZOH}(\omega)$	phase of the zero order hold	radians
R	terminal resistance of the motor	ohms
t	the sampling time of the HCTL-1000	seconds
T_E	electrical time constant of the motor	seconds
T_M	mechanical time constant of the motor	seconds
t_R	closed loop system rise time to a step response	seconds
ω	frequency	radians/sec
ω_C	the open loop gain crossover frequency	radians/sec
ω_C'	the desired open loop gain crossover frequency	radians/sec
$\omega_N(\omega)$	normalized frequency	radians
ω_{NC}'	the normalized desired gain crossover frequency (ω_C')	radians
ω_P	the open loop phase crossover frequency	radians/sec
Z(s)	zero order hold transfer function	_____

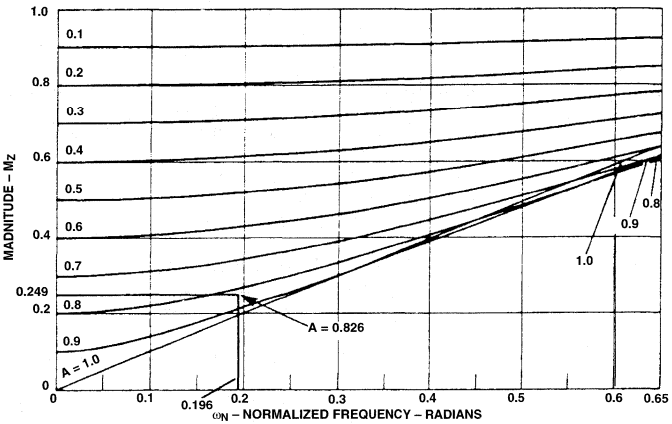

Figure 26. Magnitude Contribution of the Zero Term to the Closed Loop System Compensator.

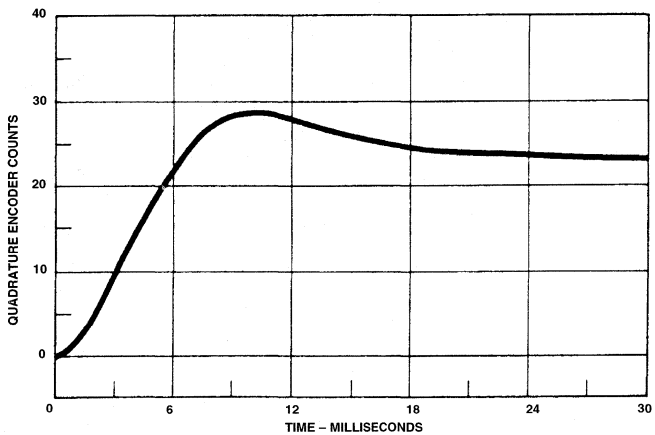

Figure 27. Response of the Closed Loop System to a Step Input of 25 Quadrature Encoder Counts.

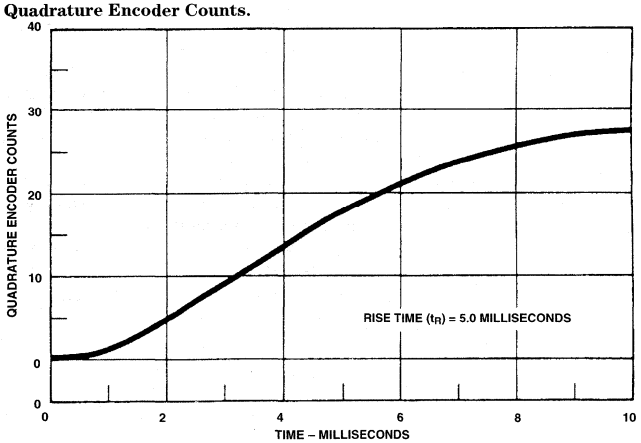

Figure 28. Rise Time of the Closed Loop System to a Step Input of 25 Quadrature Encoder Counts.

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Design and Performance Considerations with the HEDR-8000

Application Note 1079

Introduction

The HEDR-8000 is Hewlett-Packard's reflective optical encoder in a surface mount package. The HEDR-8000's two channel medium resolution encoding performance has been miniaturized into a super small SO-8 (small outline 8 pin) clear plastic package.

Because of the reflective technology, the HEDR-8000 is inherently different from other HP encoder modules. HP's other standard encoder modules use transmissive technology where light passes through a codewheel or codestrip. With the HEDR-8000, light reflects off the codewheel or codestrip. The properties of the reflective technology are significantly different and must be considered when designing an encoder system with the HEDR-8000.

The objective of this application note is to give designers information about the following:

1. Intended performance of the HEDR-8000
2. Performance characteristics as a function of operating parameters
3. Codewheels and codestrips to be used with the HEDR-8000
4. Notes about handling and usage of the HEDR-8000

(For the sake of simplicity, references to "codewheels" should be taken to mean both codewheels and codestrips.)

Basic Operating Principles

The HEDR-8000 combines an emitter and a detector in a single surface mount SO-8 package. As seen in the block diagram below, the HEDR-8000 has three key parts: a single LED light source, a photo-detector IC, and a pair of lenses molded into the package.

The lens over the LED focuses light onto the codewheel, and the image of the codewheel is reflected back through the lens to the photodetector IC.

As the codewheel rotates, an alternating pattern of light and dark corresponding to the pattern of the codewheel falls upon the photodiodes. This light pattern is used to produce internal signals A and its complement A', and B and B'. As part of the "push-pull" detector system, these signals are fed through comparators to produce the final digital outputs for Channels A and B.

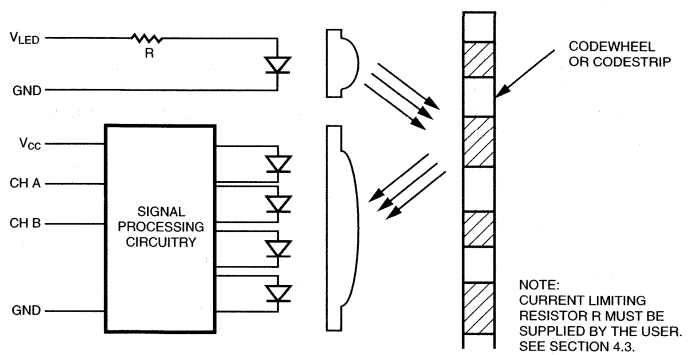


Figure 1. HEDR-8000 Block Diagram.

1.0. Intended Performance of the HEDR-8000

The HEDR-8000's encoding performance is characterized by the quality and consistency of the two encoding signals, Channel A and Channel B. These signals have a quadrature relationship such that as the codewheel passes in one direction Channel A leads Channel B, and as the codewheel passes in the other direction Channel B leads Channel A. Figure 2 shows the Output Waveforms.

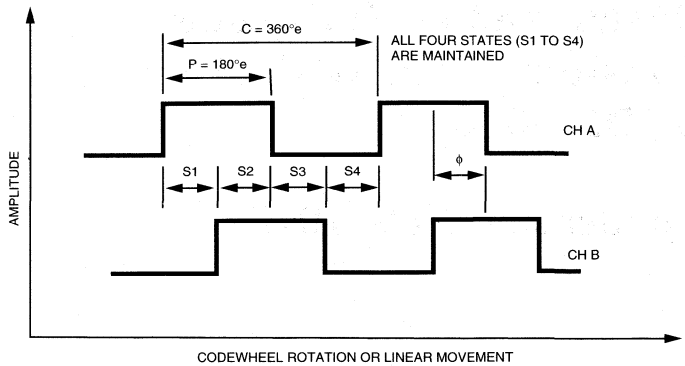


Figure 2. Output waveforms of the HEDR-8000.

The reflective HEDR-8000 has lower encoding performance than other HP transmissive-type encoders. Although the HEDR-8000 does have 2 channels in quadrature, this device is intended to be used such that Channel A gives information about counts, and Channel B gives information about direction.

This means that counting can be accomplished by:

- Counting every rising edge on Channel A (called "1X decoding" — number of rising edges per revolution on Ch. A equals the counts per revolution [CPR] of the codewheel).
- Counting every rising and falling edge on Channel A (called "2X decoding" — number of rising and falling edges per revolution on Ch. A is twice the CPR of the codewheel).

The state of Channel B (logic high or low) when a rising or falling edge occurs on Channel A can be used to determine the direction of rotation.

It is not recommended that full 4X quadrature decoding be used (every edge on both Channel A and B, or every logic state width). The relationship between Channels A and B is guaranteed to be in quadrature, but this relationship is not tightly controlled enough to enable accurate 4X decoding.

2.0. Performance and Operating Parameters

The Recommended Operating Conditions table in the HEDR-8000 data sheet gives conditions for the following parameters shown in Table 1. When the HEDR-8000 is used outside of these specified conditions, the performance of the device degrades. The derating curves that follow can be used to determine how much performance degrades.

2.1. Radial and Tangential Misalignment

The radial direction is defined by the line connecting the shaft center and the nominal device center. The tangential direction is the direction perpendicular to the radial direction at the nominal device location. Mechanical misalignment of the HEDR-8000 can be defined along these two axes. The radial and tangential directions are shown below in Figure 3 and apply only to rotary motion.

Table 1. Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Radial Misalignment	E_R			±0.38 (±0.015)	mm (in.)
Tangential Misalignment	E_T			±0.38 (±0.015)	mm (in.)
Codewheel or Codestrip Gap	G	1.52 (0.060)	2.03 (0.080)	2.54 (0.100)	mm (in.)
LED Current	I_{LED}	13	15	18	mA

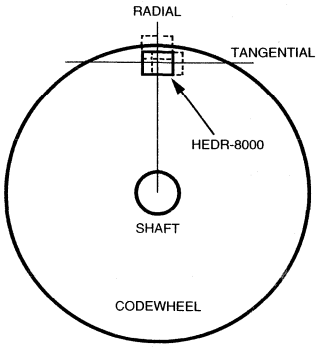


Figure 3. Radial and tangential directions for misalignment.

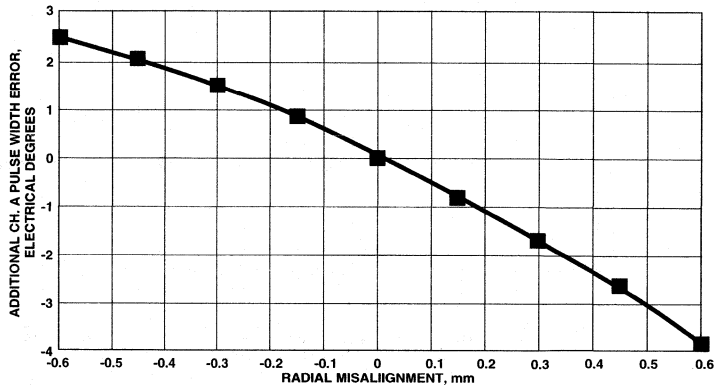


Figure 4. Typical Additional Channel A Pulse Width Error vs. Radial Misalignment.

Figure 4 shows the derating curve for Radial Misalignment. It shows how much additional Ch. A pulse width error will on average be incurred if the radial position of the HEDR-8000 is changed.

Here is an example how this graph can be used:

Question: An HEDR-8000 is being used as a rotary encoder with an 11.00 mm optical radius codewheel. However, instead of being placed at 11.00 mm from the shaft center, it is located at 11.50 mm from the shaft center. What will be the performance shift of the device?

Answer: The radial misalignment is +0.50 mm, so Figure 4 shows that there will be on average -3.1 °e of additional Ch. A pulse width error. So if the part at 0.00 mm radial misalignment has an average pulse width error of -10°e, at +0.50 mm misalignment the error will (for an average part) most likely be -13.1°e.

Note that if the user stays within the ±0.38 mm recommended operating condition, the maximum error as stated on the data sheet is ±55°e. By going outside the recommended condition to +0.50 mm, the maximum error will shift as well (in this case, the shift is very small). The calculation is shown in the table below. Figure 5 above shows the additional Ch. A pulse width error as a function of tangential misalignment. It shows that the HEDR-8000 Pulse Width error is insensitive to tangential misalignment. However, while Pulse Width error is not affected significantly,

Ch. A Pulse Width Error @+0.38 mm radial misalignment (from Figure 4)	-2.3 °e
Ch. A PW Error @ +0.50 mm rad. misalignment	-3.1°e
Error to add to Max Data sheet Value	-3.1°e - (-2.3°e) = -0.8°e
Modified Max Ch. A PW Error (@ +0.50 mm)	-55.8°e to +54.2°e

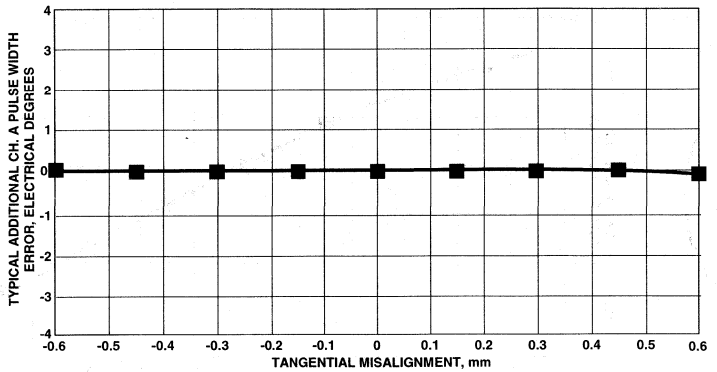


Figure 5. Typical Additional Channel A Pulse Width Error vs. Tangential Misalignment.

it is possible that other encoding parameters may get affected (such as the quadrature relationship between Channels A and B).

2.2 Gap and LED Current

Gap refers to the distance between the top surface of the HEDR-8000 and the codewheel or codestrip. The gap and the LED current have a combined effect on the encoding signal performance.

Figure 6 shows the typical additional Ch. A Pulse Width error as a function of gap and LED current. It shows that at 15 mA of LED current, the Ch. A pulse width is not affected significantly across a gap range of 1 to 3 mm. However, at other LED currents there will be some effect across the gap range.
Here is an example of how this graph can be used:

Question: An average HEDR-8000 is being driven at 10 mA of LED current at a gap of 2.5 mm. At these conditions, the device shows an average Ch. A pulse width error of 12°e. If the LED current is increased to 20 mA, what kind of performance shift can be expected in Ch. A pulse width?

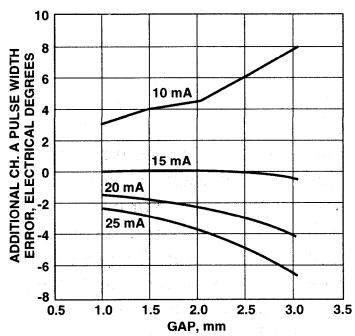


Figure 6. Typical Additional Ch. A Pulse Width Error vs. Gap at specified LED currents.

Answer: From the Figure 6, we see the following:

Gap	LED Current	Add'l Ch. A PW Error
2.5 mm	10 mA	+6°e
2.5 mm	20 mA	-3°e

By increasing the LED current, an average shift of (-3°e - 6°e) = -9°e. So the typical HEDR-8000, previously having an average Ch. A pulse width error of 12°e, will now have an average pulse width error of (12°e - 9°e) = 3°e.

3.0. Codewheels and Codestrips

The codewheel or codestrip surface must be both reflective and specular (mirror-like) so that the image of the pattern is reflected back onto the photodiodes of the HEDR-8000. In testing at HP, a handheld measuring instrument was used to determine if a codewheel or codestrip will work with the reflective optical sensor. This device is called a scatterometer and is made by a company called TMA Technologies:

Product: TMA μScan System
Company: TMA Technologies, Inc.
P. O. Box 3118
Bozeman, Montana
59715
U. S. A.
(406) 586-7684
Fax (406) 587-1428

Reflective surfaces with a specular reflectance of 60% or higher as measured by the μScan were compatible with the reflective encoder. The non-reflective areas should have a reflectance of less than 10%.

When testing for specular reflectance, testing should be done such that reflective surfaces are tested separately from non-reflective surfaces. Test the reflective surface by itself, then test the non-reflective surface. Do not perform tests on the patterned surface as this will only give an average reflectance across the pattern.

HP has not characterized any materials and, in general, does not plan to sell codewheels or codestrips to use with the reflective optical sensor. Potential reflective materials include metal and reflective film. One identified potential supplier of reflective codewheels is given below (HP does not endorse any suppliers of codewheels and codestrips, but rather provides this only as information to customers):

PWB Industrial Products GmbH
Siegburger Strasse 30
D-53757 Sankt Augustin
Germany

Phone: (49) 2241/91 47-0
Fax: (49) 2241/91 47-19

This document will be updated as HP identifies other potential vendors.

4.0. Notes About Handling and Usage

Because of its reflective technology and its surface mount package, the HEDR-8000 is inherently different than other HP transmissive-type encoders in terms of its handling and usage. These differences include:

- Pre-bake requirement
- IR reflow soldering
- User-provided current limiting resistor
- Exposure to high intensity light sources

These subjects are all included in the HEDR-8000 data sheet. Notes about these subjects are included below.

4.1. Pre-Bake Requirement

The optical grade materials used in the HEDR-8000 can absorb moisture directly out of the air. Absorbed moisture in components that have already been reflow soldered to a pc board is generally not a concern. However, moisture absorption prior to reflow soldering is of serious concern. If moisture is absorbed by the device prior to reflow soldering, the entrapped moisture turns to super-heated steam during the reflow solder process. The pressure of this steam can lead to catastrophic failure.

Therefore, a pre-bake prior to IR reflow soldering is required for the HEDR-8000. Remove the tube(s) of devices from the moisture barrier bag and remove the devices from the tubes. Place the individual devices on a tray and bake in an oven for 24 hours at 100°C. Solder to printed circuit board(s) within 24 hours of baking. Storage of the devices should be in a container with a relative humidity of less than 30%.

4.2. IR Reflow Soldering

The HEDR-8000 is the first HP encoder that is IR reflow solderable. The HEDR-8000 data sheet shows the recommended IR soldering profile. This profile meets the specifications of the Electronic Industries Association of Japan (EIAJ).

Figure 7 shows an example pc board layout for an HEDR-8000 and a resistor. This layout is for mounting an HEDR-8000 and codewheel on a motor at an optical radius of 11.00 mm (0.433 in.). Pinout access is through a 5 pin connector in a through-hole configuration. The pc board has a semi-circle feature for aligning to a motor boss. Pins 2 and 5 are electrically connected (GND), and Resistor R1 is connected in between Pin 8 and +5 V.

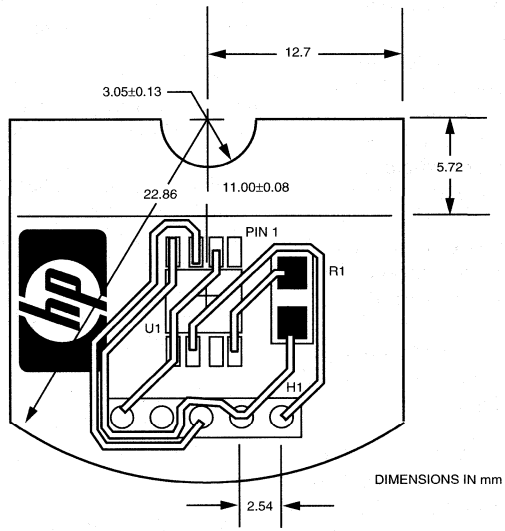


Figure 7. Example of a pc board layout for an HEDR-8000 and a resistor.

4.3 Current Limiting Resistor

Unlike other HP encoders, the HEDR-8000 does not have an integrated resistor to limit the current to the LED light source. This resistor must be provided by the user. The recommended value is 220 Ω (±10%) and should be placed in series between the 5 V supply and pin 8 of the device (V_{LED}). This will result in an LED current of approximately 15 mA.

4.4 Exposure to High Intensity Light Sources

Exposure of the HEDR-8000 to a high intensity light source can damage the photodiodes on the detector IC. Such light sources include photographic flashes and spot lights. Normal fluorescent and incandescent lighting will not cause any damage to the device.

Sample Timer and Digital Filter

Application Brief M-005

Introduction

This application brief describes the sample timer register and the digital filter as implemented in the HCTL-1100. The application brief should be used in conjunction with the data sheets for the HCTL-1100.

Sample Timer Register

The sample timer register R0FH is a read/write register that sets the sample time of the HCTL-1100. The HCTL-1100 calculates the position or velocity error, depending on the mode of operation, at the beginning of every sample time and outputs a control output to the amplifier.

The sample timer sets the sample time based on the input clock frequency according to the equation shown in Figure 1.

The minimum values listed in the table correspond to the time taken by the HCTL-1100 to compute the error and calculate the value of the control output to the amplifier every sample period. The sample timer should not be set to values smaller than those specified in the table for the different modes of operation.

The sample timer of more than one HCTL-1100 can be synchronized – be made to start the sample period at the same time, in the INIT/IDLE mode by holding the SYNC pin low on all the HCTL-1100 ICs that need to be synchronized, writing the commands into each of the HCTL-1100s and then pulling the SYNC pin high.

Digital Filter

The HCTL-1100 uses a digital lead filter to provide compensation in the closed loop mode of operation. The filter is implemented as shown in Figures 2 and 3.

The digital filter as shown in

$$t = \frac{16\,(ROFH + 1)}{f_{EXTERNAL\ CLK}}$$

Control Mode	ROFH Contents Minimum Limits	Min. Sample Rate 2 MHz	Min. Sample Rate 1 MHz	Max Sample Rate 2 MHz	Max Sample Rate 1 MHz
• Position Control	7	64 µs	128 µs	2048 µs	4096 µs
• Proportional Velocity Control	7	64 µs	128 µs	2048 µs	4096 µs
• Trapezoidal Profile Control	15	128 µs	256 µs	2048 µs	4096 µs
• Integral Velocity Control	15	128 µs	256 µs	2048 µs	4096 µs

Figure 1. HCTL-1000 Sample Timer.

$$D(Z) = \frac{K}{4} \frac{Z-(A/256)}{Z+(B/256)}$$

A = Zero (R20H)
B = Pole (R21H)
K = Gain (R22H)

Figure 2. Digital Compensation Filter Equation.

$$MCn = \frac{K}{4}(Xn) - \left[\frac{B}{256}(MCn - 1) + \frac{A}{256}\left(\frac{K}{4}\right)(Xn - 1)\right]$$

MCn = Present motor command output
Xn = Present (command position - actual position)
MCn - 1 = Previous motor command output [last sample time]
Xn - 1 = Previous (command position - actual position) [last sample time]

Used in position control, trapezoidal profile control, and integral velocity control modes

Figure 3. Digital Compensation Filter Implementation.

Figure 2 is utilized only in Position Control mode, Trapezoid Profile mode and Integral Velocity mode. In the Proportional Velocity mode only the gain term K in the digital filter is utilized to compute the control value output by the HCTL-1100 based on the velocity error, as shown in Figure 4.

Please refer to application note AN 1032 for an in-depth description of the effects of the various digital filter parameters on closed loop control performance. This application note also explains how to design a closed loop control system based on the HCTL-1100.

$$MCn = \frac{K}{4}(Yn)$$

MCn = Present motor command output
Yn = Present (command velocity - actual position)

Figure 4. HCTL-1000 Digital Filter Implementation.

Commutator Port in the HCTL-1100/1000

Application Brief M-012

Introduction

This application brief describes the functioning of the commutator port in the HCTL-1100/1000 with examples. This application brief should be used in conjunction with the data sheet for the HCTL-1100/1000 for a description of actual register addresses, reading and writing to the HCTL-1100/1000, and "Align" mode operation.

The commutator port in the HCTL-1100 is used for closed loop control of stepper and brushless motors that have a 2 or 3 channel encoder attached to them. For programming purposes the commutator is a set of 6 registers that can be read or written to. The physical output interface provided by the commutator consists of 4 signals – PH A, PH B, PH C and PH D. These signals can be used to control motors with four phases or less.

The 6 registers are:

- Commutator Ring
- X Register
- Y Register
- Offset Register
- Maximum Phase Advance Register
- Velocity Timer Register

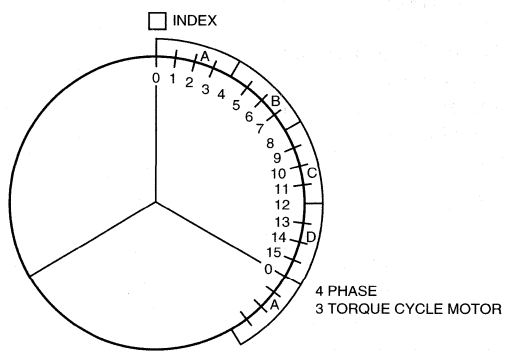
A Status Register is used to control whether the commutator works on the basis of quadrature counts or full cycles.

PHase A through PHase D signals are TTL logic compatible signals and they can be decoded to drive the power switches used to drive the phases of a brushless or stepper motor.

Programming the Commutator Registers

Example 1: For a 4 phase, 3 torque cycle motor with a 12 cycles per revolution (48 quadrature counts per revolution), 3 channel encoder, the diagram shown below illustrates how the 4 signals PH A, PH B, PH C and PH D are generated. The values programmed into the registers are:

Commutator Ring = 16
X Register = 4
Y Register = 0
Offset Register = 0
Maximum Phase Advance Register = 0
Velocity Timer Register = 0



- RING REGISTER DETERMINES THE NUMBER OF ENCODER COUNTS IN A TORQUE CYCLE
- RING REGISTER VALUE MAY BE IN FULL OR QUADRATURE COUNTS
- RING COUNTER CLEARED BY INDEX PULSE
- RING = 16

Figure 1. HCTL-1000 Ring Counter/Register.

The Status Register is programmed to enable the commutator to work in quadrature.

In example 1, the basic configuration of the commutator is used and the advanced features that could reduce the torque ripple in the motor are not used. Example 2, given below, illustrates how the torque ripple in the motor can be reduced.

Example 2: For the same motor used in example 1, if the register values are programmed as:

Commutator Ring = 16
X Register = 2
Y Register = 2
Offset Register = 0
Maximum Phase Advance Register = 0
Velocity Timer Register = 0

Status Register programmed to enable the commutator to work in quadrature, the PH A, PH B, PH C and PH D signals are as shown in Figure 4, 5, and 6.

Example 2 shows how the torque ripple can be improved.

The two additional features that can be used are the phase offset and phase advance. Phase offset is used to control the beginning of the sequence of PH A, PH B, PH C and PH D signals with respect to the index signal, statically. Phase advance is used to further improve the torque ripple at different speeds. The start of the sequence of the four Phase signals can advanced, with respect to the index, proportionally with velocity of operation of the motor.

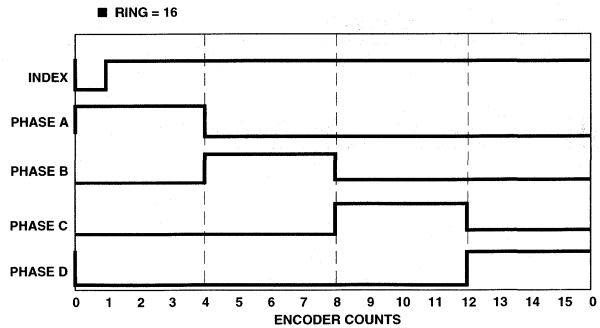


Figure 2. Basic Commutator Output.

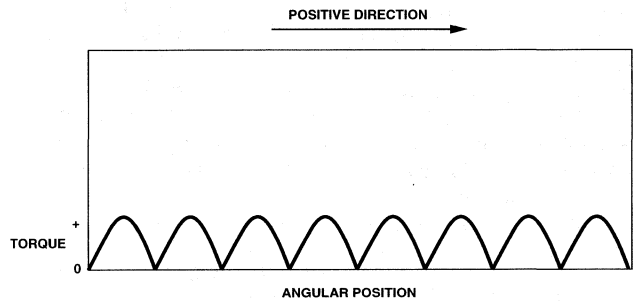


Figure 3. Torque Ripple of Step Motor with Basic Commutation.

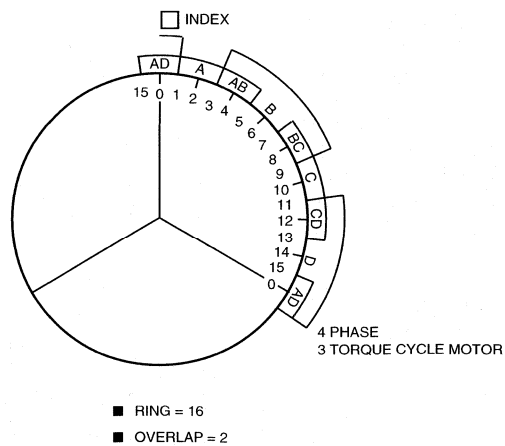


Figure 4. Phase Overlap Feature.

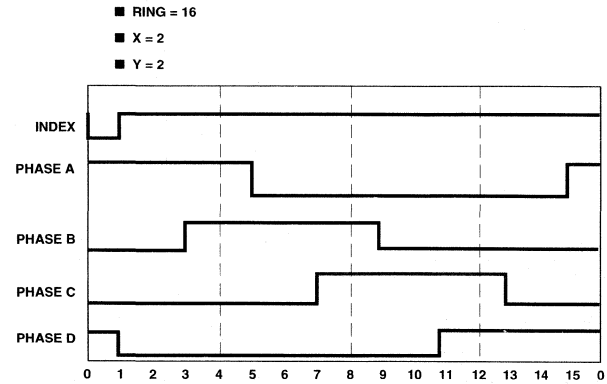


Figure 5. Commutator Output with Overlap.

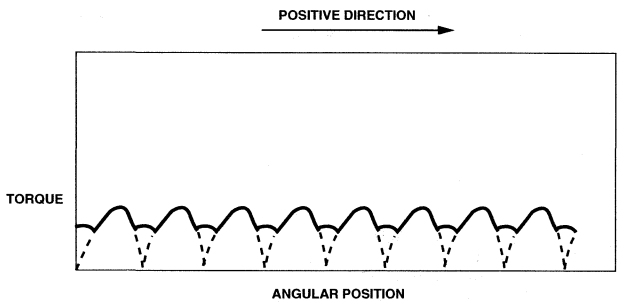


Figure 6. Torque Ripple with Phase Overlap Feature.

Example 3: This example uses register settings used in example 1 and illustrates the effect of programming the Phase Offset register to -3. The value of -3 causes the four Phase signals to be generated in the fashion illustrated in Figures 7 and 8.

Example 4: For the same register settings as in example 1, if the Maximum Phase Advance register is programmed to 2 and the Velocity Timer register is programmed so as to give a given phase advance at a given velocity using the equation as shown in the Figure 9, the PH A through PH D signals are gener-

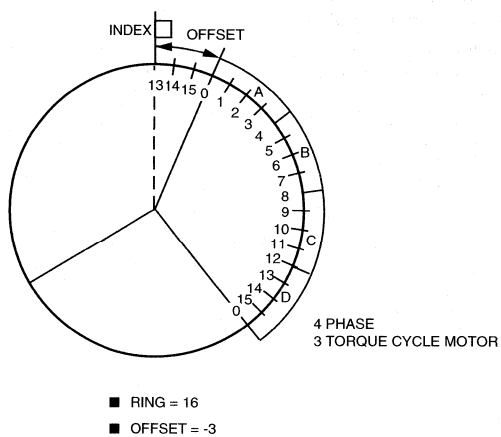


Figure 7. Phase Offset Feature.

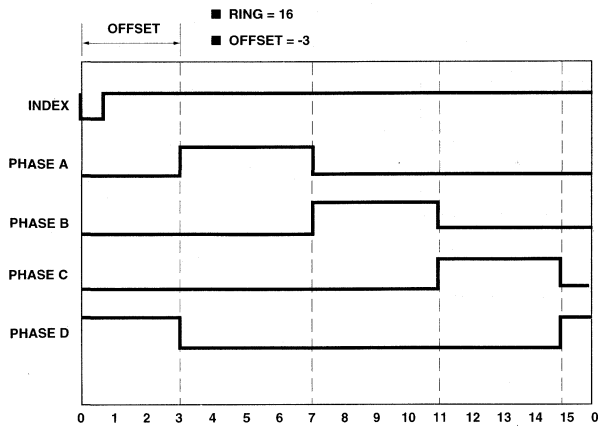


Figure 8. Commutator Output with Phase Offset.

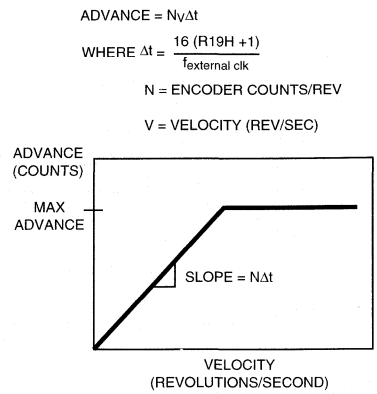


Figure 9. Phase Advance Equation and Graph.

ated in the fashion indicated in Figure 10.

There are certain constraints on the values that can be written into the commutator registers. These constraints are:

- Full counts per revolution should be an integer multiple of the motor steps per revolution, or number of commutation steps per revolution.

$$-128 \le \left(\frac{3}{2}\right) \text{ring} + \text{offset} \pm \text{max. advance} \le +127$$

- X register cannot have a value of zero.

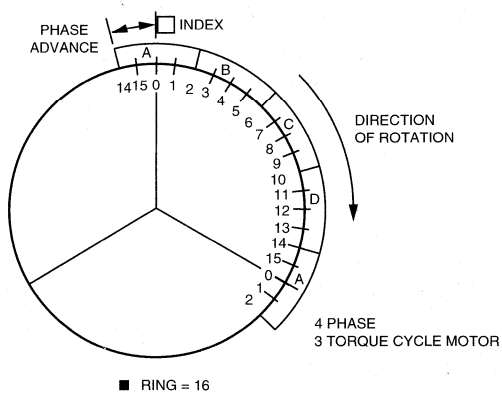


Figure 10. Phase Advance Feature.

Summary

Choose an encoder that satisfies the counts per revolution requirements for the motor and align the index pulse physically to the last phase torque detent of the motor. This is done during assembly of the encoder on the motor shaft as shown in Figure 11.

With the last phase of the motor energized, and the encoder module powered, the code wheel is attached to the shaft in such a way that the index pulse is active. An oscilloscope can be used to determine if the index is active. Even if the index pulse is not exactly aligned with the last phase torque detent fine tuning can be done using the phase offset register at a later time. Figures 12 and 13 show the location of the index pulse for a 4 phase motor.

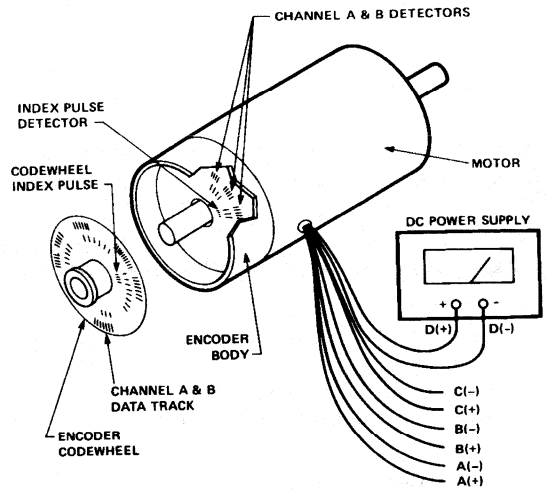


Figure 11. Index Channel Alignment.

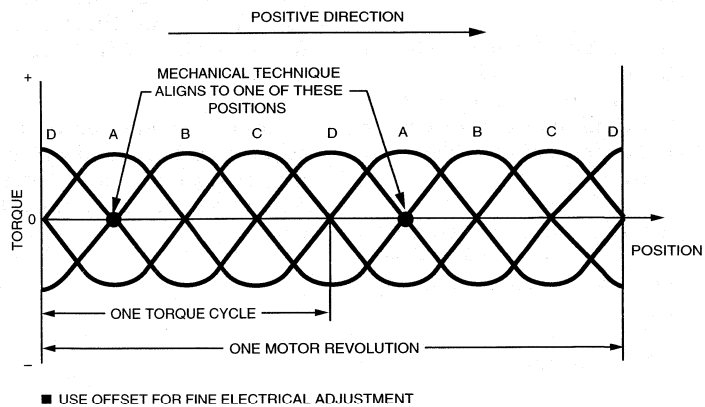


Figure 12. Index Channel Alignment — Motor Torque Cycle.

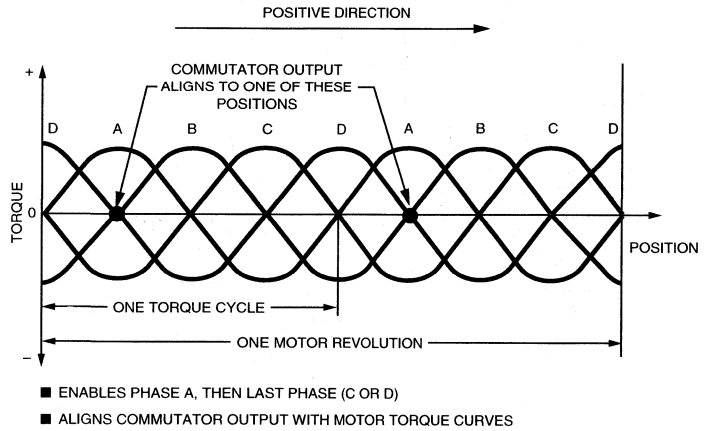


Figure 13. HCTL-1000 Align Mode.

To program the commutator follow these steps:

- Choose commutation based on full counts or quadrature counts and set the Status register.
- Choose Ring Register value to correspond to number of counts in one commutation cycle; full counts or quadrature counts depending on the status register.
- Choose X and Y register values to satisfy the firing sequence of the motor phases and such that,

  X+Y = Ring/(number of phases)

- "Align" the motor and adjust the Offset Register for optimum performance in both directions. Please refer to the data sheet for the HCTL-1100 for explanation of the "Align" mode.
- Check commutator constraints equation and correct the register programmed values if the constraints equation is not satisfied.

Interfacing the HCTL-1100 to the 8051

Application Brief M-015

HCTL-1100/8051 Interfaces

This application brief offers two different approaches to interfacing the HCTL-1100 to the 8051 microcontroller family. The first approach uses the 8051's address/data/control bus to communicate with the HCTL-1100 and the second approach uses the 8051's I/O ports to communicate with the HCTL-1100.

The choice of which interface is most appropriate for your application should be based on whether or not your current design is utilizing the 8051's bus structure. If your 8051 design is utilizing the bus, it makes sense to use the HCTL-1100 bus interface circuit. This approach requires only two additional TTL chips. If your 8051 design is completely I/O based with no external memory, it makes sense to use the I/O port interface. The I/O interface requires no additional glue logic.

The I/O routines are slightly more complicated for the I/O interface than for the bus interface. These routines can be seen in the software listings provided with this application brief. There is only a marginal performance difference between the two approaches. The execution times for these routines are listed in Table 1.

These execution times do not include stack operations and subroutine overhead.

The HCTL-1100 bus interface circuit is capable of supporting four HCTL-1100s with no additional logic. If an I/O port based design requires more than one HCTL-1100, the interface would require only two additional I/O port lines per chip. These lines would control OE (Output Enable) and CS (Chip Select) for each of the individual HCTL-1100s. If there is an inadequate number of I/O port lines available for this purpose, a separate decoder chip could be used. One such chip is the 74LS138 3-to-8 decoder which is capable of handling four HCTL-1100s.

Table 1. Execution Times

	Read Operation	Write Operation
I/O Port Interface	15 µs at 12 MHz 180 Clock Per.	13 µs at 12 MHz 156 Clock Per.
Bus Interface	12 µs at 12 MHz 144 Clock Per.	6 µs at 12 MHz 72 Clock Per.

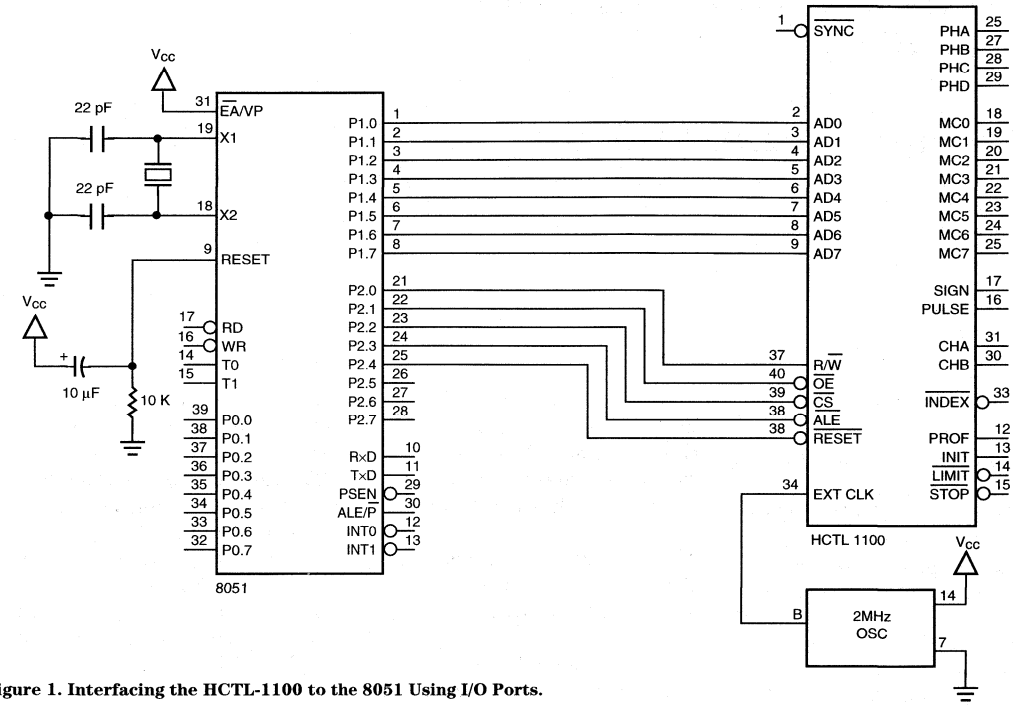
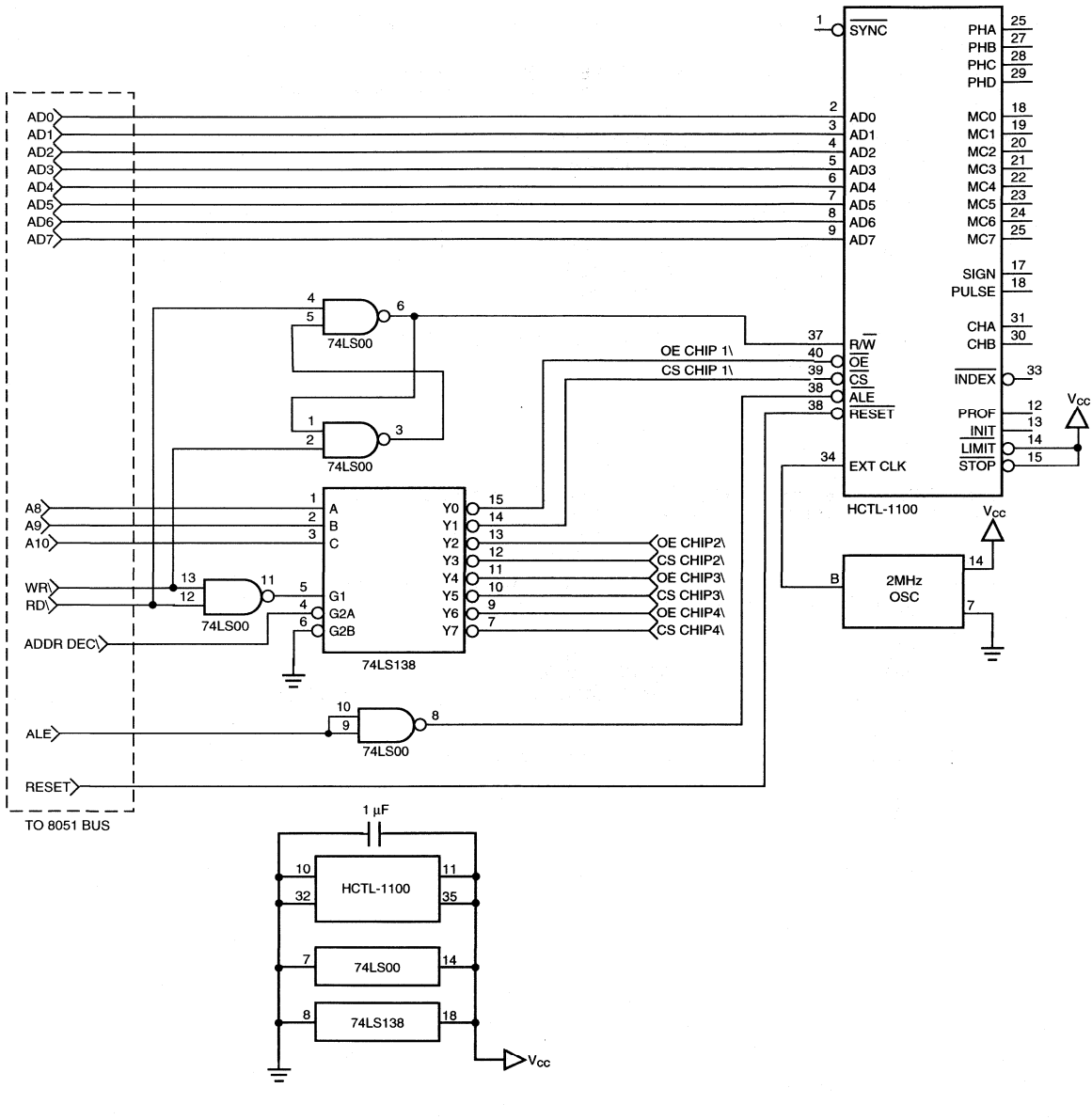


Figure 1. Interfacing the HCTL-1100 to the 8051 Using I/O Ports.

```
;*****************************************************************************
;HCTL-1100 READ/WRITE ROUTINES
;THIS SOFTWARE IS USED IN CONJUNCTION WITH THE HCTL-1100/8051 I/O
;PORT INTERFACE
;*****************************************************************************

;*****************************************************************************
;SUBROUTINE RD1100
;READS HCTL REG POINTED TO BY B AND RETURNS REG VALUE IN ACC
;*****************************************************************************
RD1100:  SETB    P2.0          ; SET R/W LINE TO READ

         MOV     P1,B          ; LATCH ADDRESS
         CLR     P2.3          ; PULSE ALE
         SETB    P2.3
         MOV     P1,#0FFH

         CLR     P2.2          ; PULSE CS
         SETB    P2.2
         NOP                   ; DELAY 4µS
         NOP                   ; ALLOW ENOUGH TIME FOR 1MHz
         NOP                   ; HCTL-1100 OR FASTER

         CLR     P2.1          ; SET OE=0
         MOV     A,P0          ; GET DATA FROM 1100
         SETB    P2.1          ; SET OE=1

         RET
```

(Continues)

```
;*************************************************************************
;SUBROUTINE WR1100
;LOADS HCTL-1100 REGISTER POINTED TO BY B WITH VALUE IN ACC
;*************************************************************************

WR1100:  MOV     P1,B          ; LATCH ADDR
         CLR     P2.3          ; PULSE ALE
         SETB    P2.3
         MOV     P1,#0FFH

         CLR     P2.0          ; SET R/W LINE TO WRITE
         MOV     P1,A          ; SEND DATA
         CLR     P2.2          ; PULSE CS
         SETB    P2.2
         SETB    P2.0          ; RETURN R/W TO READ MODE
         MOV     P1,#0FFH

         RET

;*************************************************************************
;SUBROUTINE RS1100
;THIS SUBROUTINE RESETS THE HCTL-1100 WITH A 5µS PULSE. THIS IS
;ENOUGH TIME TO RESET A 1MHz HCTL-1100 OR FASTER.
;*************************************************************************

RS1100:  ORL     P2,#0FH       ; SET R/W TO READ, OE=1, CS=1, AE=1
         MOV     P0,#0FFH      ; SET P1=HIGH

         CLR     P2.4          ; SET RESET LOW
         NOP                   ; PULSE FOR 5µS
         NOP                   ; CAN REMOVE 2 NOP'S FOR 2MHz HCTL-1100
         NOP
         NOP
         SETB    P2.4          ; BRING RESET LINE HIGH

         RET
```



\ DENOTES AN ACTIVE LOW SIGNAL

Figure 2. Interfacing the HCTL-1100 to the 8051 Using the Address/Data Bus.

```
;*****************************************************************************
;HCTL-1100 READ/WRITE ROUTINES
;THIS SOFTWARE IS USED IN CONJUNCTION WITH THE HCTL-1100
;BUS INTERFACE
;*****************************************************************************

; HCTL-1100 ADDRESS
OE1100    EQU     060H            ; BASE ADDRESS = 6000H
CS1100    EQU     061H            ; BASE ADDRESS = 6100H

;*****************************************************************************
;SUBROUTINE RD1100
;READS HCTL REG POINTED TO BY B AND RETURNS REG VALUE IN ACC
;*****************************************************************************

RD1100:   PUSH    DPL             ; SAVE DATA POINTER
          PUSH    DPH

          MOV     DPH,#CS1100     ; POINT TO BASE CS ADDRESS
          MOV     DPL,B           ; LOAD REG ADDRESS IN
                                  ; LOWER 8 BITS OF DATA POINTER
          MOVX    A,@DPTR         ; LATCH HCTL-1100 REG ADDRESS

          NOP                     ; ALLOW ENOUGH TIME FOR 1MHz CLK
          NOP                     ; (NOT REQUIRED FOR 2MHz HCTL-1100 CLK)
          MOV     DPH,#OE1100     ; POINT TO BASE OE ADDRESS
          MOVX    A,@DPTR         ; READ BYTE FROM HCTL-1100

          POP     DPH             ; RESTORE DATA POINTER
          POP     DPL
          RET


;*****************************************************************************
;SUBROUTINE WR1100
;LOADS HCTL-1100 REGISTER POINTED TO BY B WITH VALUE IN ACC
;*****************************************************************************

WR1100:   PUSH    DPL             ; SAVE DATA POINTER
          PUSH    DPH

          MOV     DPTR,#CS1100    ; POINT TO BASE CS ADDRESS
          MOV     DPL,B           ; LOAD REG ADDRESS IN
                                  ; LOWER 8 BITS OF DATA POINTER
          MOVX    @DPTR,A         ; WRITE BYTE TO HCTL-1100

          POP     DPH             ; RESTORE DATA POINTER
          POP     DPL
          RET
```

HEWLETT® PACKARD

Interfacing the HCTL-20XX to the Intel 8051

Application Brief M-017

Introduction

The HCTL-2000, 2016, and 2020 are CMOS ICs that provide a noise filter, quadrature decoder, counter, and bus interface on a single chip. This family of ICs is designed to improve system performance by removing the burden of quadrature decoding from the processor. The HCTL-2000 has a 12-bit counter and the HCTL-2016 and HCTL-2020 have 16-bit counters.

This application brief discusses what is required to interface the HCTL-20XX family to an Intel 8051 microcontroller bus. The hardware interface is shown in Figure 2. The address decoder in this circuit consists of a single 8-input NAND gate which is used to decode the base address of 0FEXXH. This address is purely arbitrary and the user could substitute their own address decoder circuitry to select any arbitrary address in the 8051's external address space. The SEL line can also be connected to any arbitrary address line.

The decoded address signal is ANDed together with the processor RD signal to form the HCTL-20XX OE signal. When this signal is active the HCTL-20XX places the selected count byte on the data bus. The timing for these signals is shown in Figure 1.

The HCTL-20XX has internal inhibit logic circuitry and latches to guarantee that the 16 bit count is held stable while both 8-bit halves of this count are read by the processor. For proper operation of this circuitry the processor should read the high byte first (SEL=0) and then the low byte (sel=1). This sequence can be seen in the code listings provided with this application brief.

The interfaces for the HCTL-2000, 2016, and 2020 are identical. The HCTL-2020 also provides additional signal for cascading external counters. This is helpful for designs which require more than a 16-bit counter. For more information on these ICs please see the HCTL-20XX data sheet.

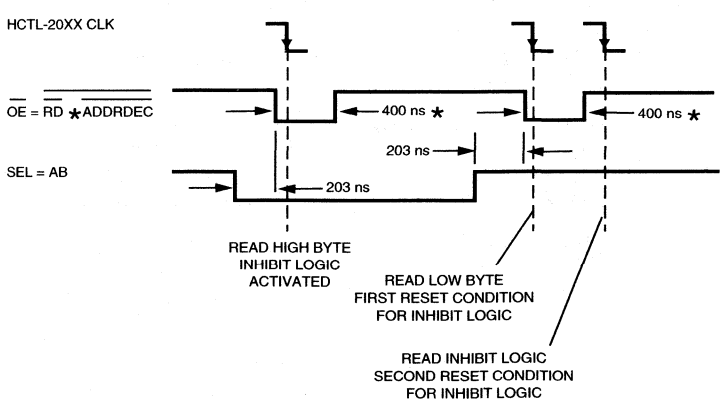


Figure 1. HCTL-20XX/8051 Read Cycle Timing.

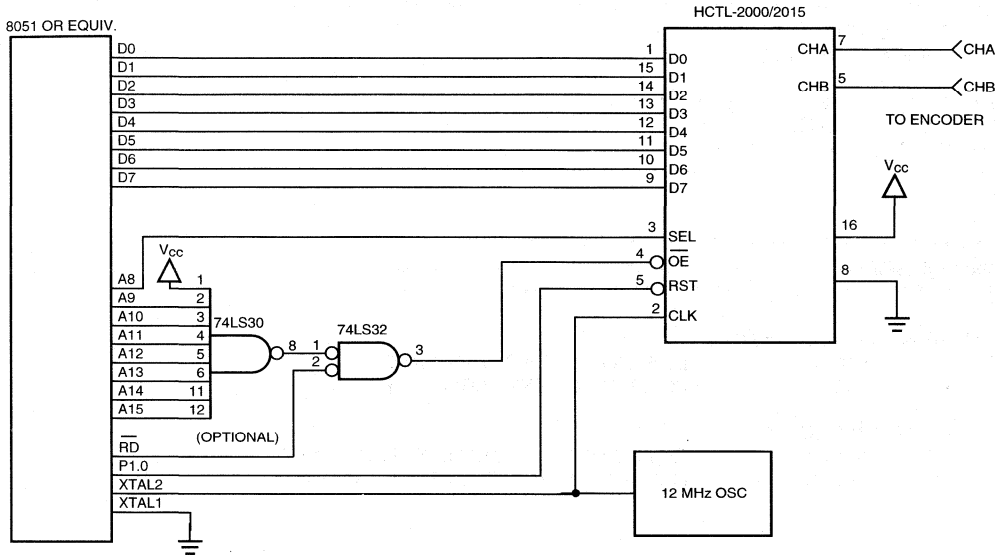


Figure 2. 8051/HCTL-2000 Bus Interface.

```
;*****************************************************************************
;HCTL-20XX INTERFACE ROUTINES
;THIS SOFTWARE ASSUMES THE FOLLOWING:
;
;1) THE HCTL-20XX BASE ADDRESS IS 0FE00H
;2) THE SEL LINE IS CONNECTED TO A8
:3) THE RESET LINE IS CONNECTED TO P1.0
;*****************************************************************************


;*****************************************************************************
;HCTL-2000 EQUATES
;*****************************************************************************

; INTERNAL MEMORY ALLOCATION
COUNTH   EQU     030H            ; POSITION COUNT - HIGH BYTE
COUNTL   EQU     031H            ; POSITION COUNT - LOW BYTE

; HCTL-2000 I/O ADDRESSES
H2000H   EQU     0FF00H          ; HCTL-2000 PORT ADDRESS - HIGH BYTE
H2000L   EQU     0FE00H          ; HCTL-2000 PORT ADDRESS - LOW BYTE



;*****************************************************************************
;SUBROUTINE RD2000
;THIS SUBROUTINE READS THE 16 BIT COUNT VALUE FROM THE
;HCTL-2000 AND STORES IT IN INTERNAL MEMORY LOCATIONS
;COUNTH AND COUNTL.
;*****************************************************************************

RD2000:  MOV     DPTR,#H2000H ; SELECT HIGH BYTE OF HCTL-2000
         MOVX    A,@DPTR
         MOV     COUNTH,A     ; STORE IN INTERNAL RAM
         MOV     DPTR,#H2000L ; SELECT LOW BYTE OF HCTL-2000
         MOVX    A,@DPTR
         MOV     COUNTL,A     ; STORE IN INTERNAL RAM
         RET



;*****************************************************************************
;SUBROUTINE RS2000
;THIS SUBROUTINE RESETS THE HCTL-2000
;THIS SUBROUTINE ASSUMES THAT THE HCTL-2000 RESET LINE IS ;CON-
NECTED TO P1.0 ON THE 8051
;*****************************************************************************

RS2000:  CLR     P1.0            ; BRING HCTL-2000 RESET LINE LOW
         SETB    P1.0            ; BRING HCTL-2000 RESET LINE HIGH
         RET
```

The Effects of High Frequency Noise on the HCTL-1100

Application Brief M-018

Introduction

In 1990 Hewlett-Packard obsoleted the HCTL-1000 and replaced it with the HCTL-1100. The HCTL-1100 is a pin for pin compatible enhanced replacement for the HCTL-1000. Among the enhancements was the process change from low speed NMOS to a high-speed, low-power CMOS. The speed of this new process is on the order of 10 to 30 times faster than the old process. This speed difference makes the HCTL-1100 much more susceptible to high speed noise glitches such as those generated by brush type motors. The HCTL-1000 was considerably less susceptible to this noise as a result of its low speed process. Figure 1 shows an example of the response of the HCTL-1000 and HCTL-1100 to this type of noise.

This Application Note describes two different approaches to dealing with HCTL-1100 noise problems. The first approach deals with how to reduce the noise susceptibility of the HCTL-1100 and the second approach deals with common sources of high frequency noise and how to eliminate it at the source.

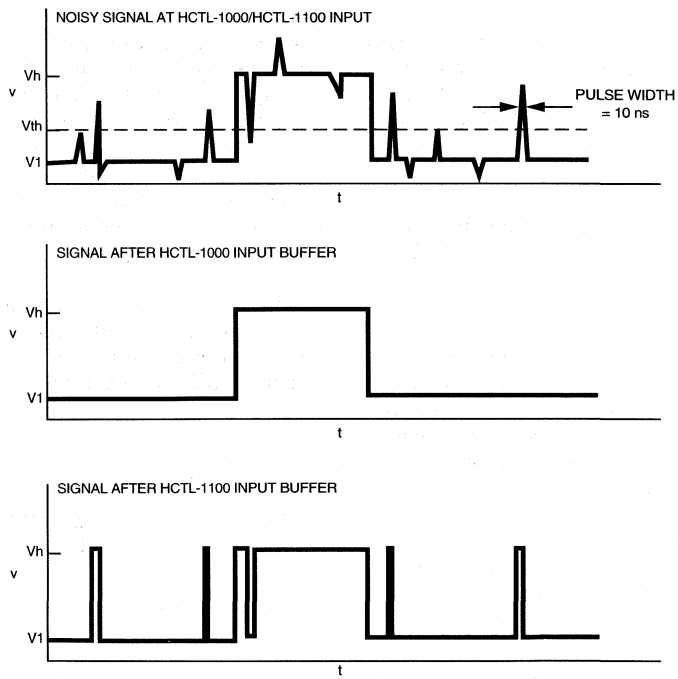


Figure 1. Effects of Noise on the HCTL-1000 and HCTL-1100.

Effects of Noise on the HCTL-1100

There are six inputs on the HCTL-1100 that are particularly susceptible to noise. These inputs are the edge triggered signals and bus control signals. They are CLK, RESET, OE, CS, ALE, and R/W. The typical effects of noise on each of these lines are described below.

CLK

1) The HCTL-1100 intermittently

drops out of control mode back to initialization idle mode.
2) The position counter freezes.
3) The sample timer freezes.
4) The HCTL-1100 completely fails and can only be revived with a hardware reset.

RESET
1) The HCTL-1100 completely fails and can only be revived with a proper hardware reset.
2) The HCTL-1100 will intermittently reset and return to initialization idle mode.

OE
1) The HCTL-1100 intermittently crashes the host processor as a result of the HCTL-1100's tri-state data bus buffers being enabled at the wrong time.

CS
1) Intermittent read and write errors occur during HCTL-1100 bus operations.

ALE
1) Intermittent read and write errors occur during HCTL-1100 bus operations. This is due to an invalid address being latched as a result of a noise spike.

R/W
1) Intermittent read and write errors occur during HCTL-1100 bus operations.

In extremely noisy environments, D7-D0, SYNC, LIMIT, and STOP may also be susceptible to noise; however, if the noise is severe enough to affect these lines, the host processor would more than likely be affected as well. In this situation it would be necessary to shield and isolate all of the control electronics from the source of noise.

Detecting high frequency noise glitches without the proper test equipment is very difficult. It is recommended that an oscilloscope having a bandwidth of 300 MHz or greater be used when tracing these types of problems. If an inadequate scope is used for this application, the sharp noise spikes will appear to be of a much lower amplitude and spread out in time. In many instances they will be invisible to a low speed oscilloscope.

If a 300 MHz or greater oscilloscope is unavailable it is still possible to debug these types of problems. The best way to do this is to try each of the solutions offered in this application note until the problem disappears. The most effective solution is to place filters in line with each sensitive input. The details of this solution are described in the next section.

In addition to noise coupled from external sources, the HCTL-1100 is also susceptible to other phenomenon such as ringing on signals. The line which is most susceptible to ringing is the clock line. Make certain that all ringing that occurs on sensitive signals such as the clock line remains outside the HCTL-1100 input threshold range (0.8 V to 2.0 V). Figure 2 shows an example of what the HCTL-1100 sees when unacceptable ringing crosses its input threshold.

The HCTL-1000 was less susceptible to this problem due to the slow response time of the old NMOS process.

In many instances the ringing may be so fast that it would be undetectable by a low bandwidth oscilloscope. It is also recommended for this test that an oscilloscope having a bandwidth of 300 MHz or greater be used.

Reducing the Noise Susceptibility of the HCTL-1100

The following is a list of solutions that help reduce the noise susceptibility of the HCTL-1100.

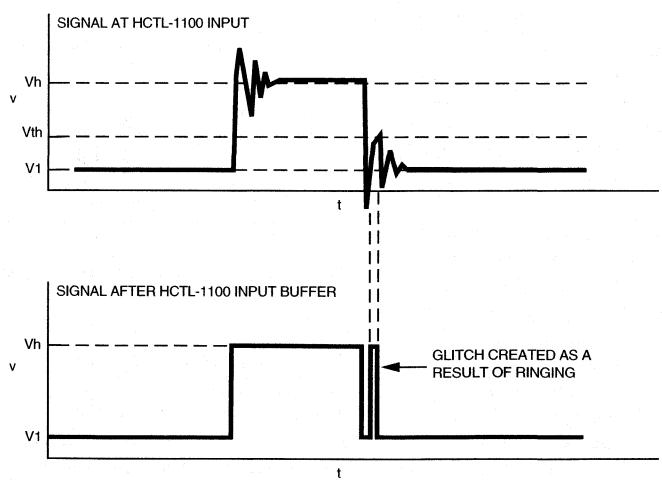


Figure 2. The HCTL-1100's Response to Excessive Ringing.

1) Place Filters on Sensitive Inputs

The most successful way to reduce the noise susceptibility of the HCTL-1100 is to protect the sensitive inputs from high frequency noise glitches. The best way to protect these inputs is to place a low pass filter in line with each of the inputs. Figure 3 shows the connection of these filters. The filters should be placed as physically close as possible to the protected input to minimize the amount of noise coupled onto the line after the filter. It is also important to minimize the trace length between the filter's ground terminal and the system's ground plane.

A variety of options are available in choosing a filter type. Some of these options are listed below in the order of most effective to least effective.

a) Ferrite Bead/Ceramic Capacitor EMI Filter Networks: These networks were originally designed for applications where it was necessary to reduce the amount of electromagnetic interference radiated from a high speed circuit. However, these networks are also very effective at removing fast noise glitches and transients. These devices are third order low pass filters. The schematic for this network is shown in Figure 4.

It is important when doing timing calculations to keep in mind that the additional capacitance will introduce timing delays in the circuit. In isolated cases it may be necessary to use a network with a

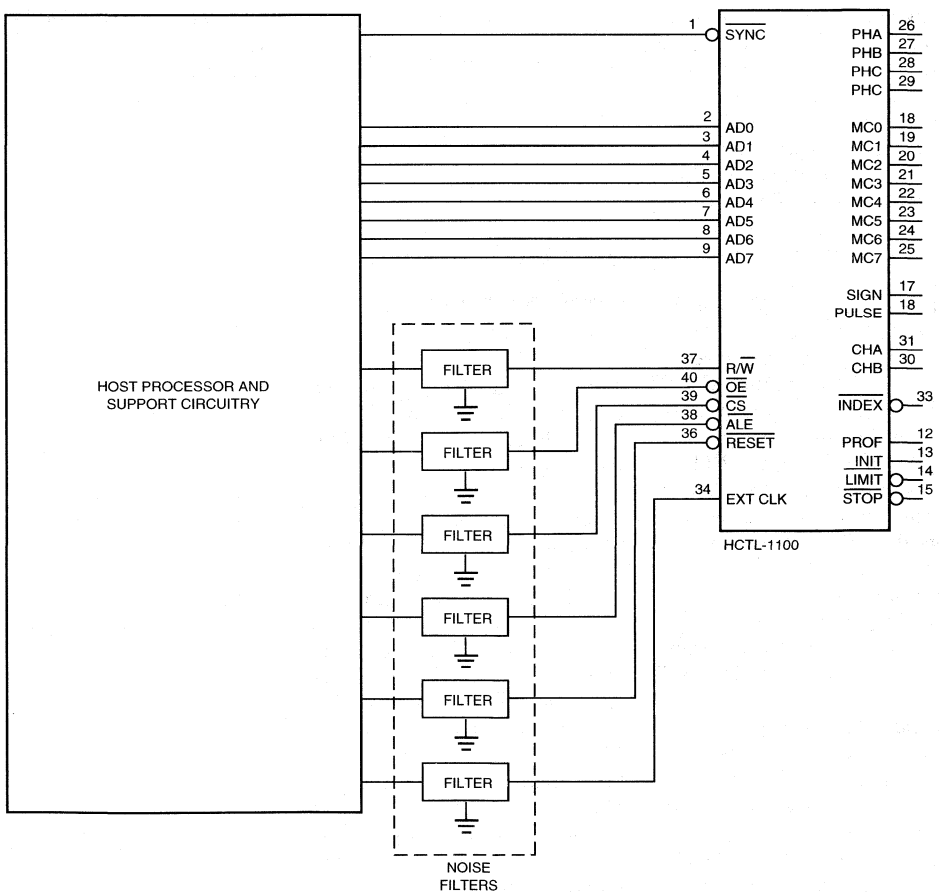
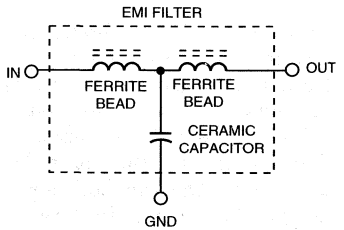


Figure 3. Noise Filter Placement for the HCTL-1100.

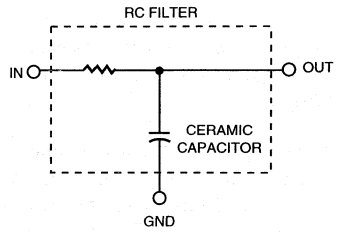


RECOMMENDED CAPACITANCE VALUE = 100 pF

RECOMMENDED TDK PART NUMBER = ZJSR 5101-101R (100 pF)

RECOMMENDED MURATA PART NUMBER = DSS306-55Y5S101M (100 pF)

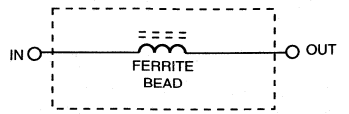
Figure 4. EMI Filter Network.



RECOMMENDED RESISTANCE VALUE = 100 Ω

RECOMMENDED CAPACITANCE VALUE = 100 pF

Figure 5. RC Filter Network.



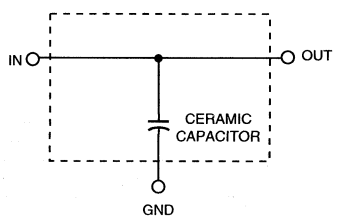
RECOMMENDED TDK PART NUMBERS:
ZBF503D-00 (TA)
ZBF504D-00 (TA)
ZBF506D-00 (TA)

Figure 7. Ferrite Bead.

lower capacitance in order to reduce this delay. To determine the additional delay due to the capacitive loading consult the data book of the part driving the HCTL-1100's inputs. For an LS TTL output the additional 100 pF capacitance will contribute a delay that is on the order of 5-10 ms.

b) RC Low Pass Filter Networks:
This filter type is a single pole filter which is fairly effective at reducing high frequency noise, but not as effective as the LC EMI suppressor described above. This network has a much slower roll-off characteristic than the EMI suppressor; however, this network would introduce less ringing in the signal than the EMI suppressor. Once again the delay introduced by this network should be taken into account when doing timing calculations. The diagram for this filter is shown in Figure 5.

c) Ceramic Capacitors:
This solution is the simplest and cheapest of all the solutions and in many applications this solution will suffice. The recommended capacitance value for most applications is on the order of 100 pF.



RECOMMENDED CAPACITANCE VALUE = 100 pF

Figure 6. Capacitive Filter.

The additional delay introduced by this method should be computed the same way as described for the EMI filter.

d) Ferrite Beads:
This solution is the least effective of all for this application due to the high impedance nature of the HCTL-1100's inputs. A more effective solution would be to use a capacitor to ground after the ferrite bead. This would give the same level of protection as the EMI filter described in section (a). Ferrite beads are much more effective in applications such as power supply filtering where the input and output impedances are much lower.

The delay contribution for the ferrite bead is in most cases negligible.

2) Power Supply Filtering

a) Place a ceramic bypass capacitor between V_{DD} and GND.

b) Use a ferrite bead on V_{DD} in conjunction with a ceramic capacitor. Figure 8 shows the placement of these components.

3) Resistive Termination of Long Traces

Resistive termination gives the noise a much lower impedance path to be coupled onto and greatly reduces ringing. As mentioned earlier, ringing can also cause problems if the amplitude is sufficient enough to cross the TTL threshold.

4) Shielding

a) Use shielded cables to carry sensitive signals. Do not mix high power signals with sensitive signals within the same shield.

b) Shield the HCTL-1100. In extreme situations it may be necessary to enclose the control electronics (including the HCTL-1100) in a shielded metal enclosure.

c) Use a multi-layer PC board with ground and power planes.

5) Cabling Techniques

a) Minimize cable lengths for sensitive signals.

b) Separate sensitive cables from cables carrying noisy signals or high power signals.

c) Shield cables carrying sensitive signals.

6) Isolation

In extremely noisy environments it may be necessary to isolate the HCTL-1100's encoder and motor control signals from the external world. An example of such an environment is in automatic welding machinery where very high levels of EMI are present. The most economical way to isolate the encoder and motor control signals would be to use optocouplers.

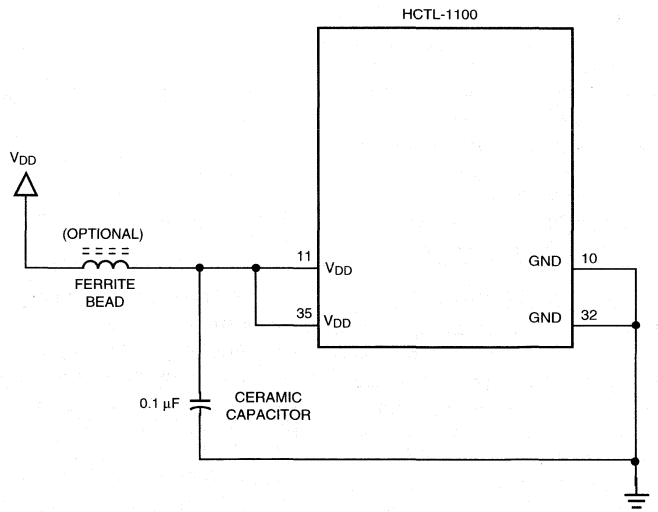


Figure 8. Power Supply Filtering.

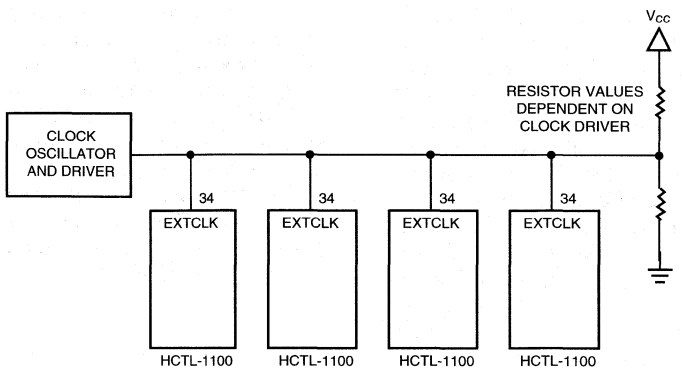


Figure 9. Example of Resistive Termination on the Clock Line.

Eliminating Noise at the Source

This section describes the most common sources of noise in an HCTL-1100 based servo system and the most effective ways to deal with them. This section is divided into three parts:

1) Motor Brush Noise
2) PWM Switching Noise
3) External Noise Sources

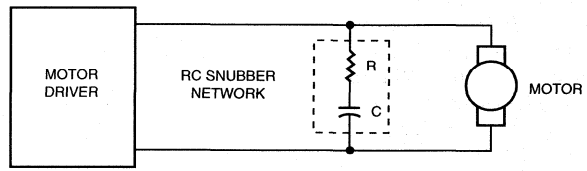


Figure 10. Application of an RC snubber Network to Reduce Motor Brush Noise.

1) Motor Brush Noise

If a servo system is using a brush type motor and the system is suffering from noise problems, the most likely cause is the motor brushes. A majority of the noise is generated from the breaking of the contact between the motor's brushes and the rotor contacts. This disconnection is done in series with the highly inductive rotor windings which causes a high voltage/high frequency noise spike to be generated every time the contact is broken. The radiated energy from this spike is transmitted from both the rotor windings and the wires leading to the motor. The energy radiated from the rotor windings is very effectively blocked by the metal motor housing, however, the energy radiated from the motor terminals and the wires leading to the motor are not. It is very easy for this noise to couple onto sensitive control signals such as those leading to the HCTL-1100. The most effective way to reduce this noise is to block it right at the motor terminals.

One effective way to block this high frequency noise is to place a capacitor across the motor terminals. The capacitor looks like a short circuit to this noise. One problem with this method is that a resonant circuit is formed with the capacitor and the inductance of the motor lead wires. This arrangement can produce long periods of ringing at the resonant frequency of this high Q circuit causing strong RF emissions at that resonant frequency. A second problem with this solution occurs when it is used in conjunction with PWM motor driver circuits. The capacitor causes excessive current spikes during switching times and may cause the PWM driver circuit to eventually fail. These spikes may also cause noise problems just as severe as the motor brush noise was itself.

A more effective way to eliminate motor brush noise is to place a series type RC snubber network across the motor terminals. Figure 10 shows the connection of this network. The resistor greatly reduces the level of current spikes and ringing that a capacitor alone would cause. It is recommended that a ceramic capacitor be used for this application.

In a DC drive system, component values are not critical. The larger the capacitor the more effective the snubber will be. The constraints are usually the cost and size of the capacitor and the effect it will have on system stability. The resistor may be optional in this application. This can be determined by viewing the duration of ringing at the motor terminals. If the ringing is less than a couple of cycles the resistor may not be necessary. In many DC drive applications it is not required.

In a PWM driven system there may be several constraints on component values and the series resistor will always be necessary. The two dominant constraints are the peak and average current through the snubber network. You can choose the optimal values based on these constraints using the equations below.

$$I_{AVG} = \frac{2CV_P}{T}\left(1-e^{\frac{-T}{2RC}}\right)$$

Where:

$$V_P = \left(\frac{1}{1+e^{\frac{-T}{2RC}}}\right)V_{PWM}$$

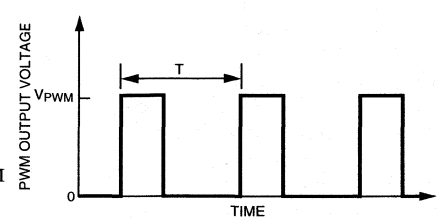


Figure 11. Average Current Through the Network.

Peak current through snubber network:

$$I_{PEAK} = \frac{V_{PWM}}{R}$$

The following three steps outline a procedure for determining the RC values for the network based on the peak and average current through the network.

Step 1:
Solve for R using the equation for peak current. This yields:

$$R = \frac{V_{PWM}}{I_{PEAK}}$$

Step 2:
The second step is to solve for C using the average current equations on the previous page. Since there is no way to derive a closed form solution for C from these equations, an iterative approach or an approximation would have to be used. In this application note, the approximation method is used. The following equation was derived using first order approximations for the average current equations.

$$C = \frac{T}{2} \quad \frac{I_{AVG}}{1.53\ V_{PWM} - 2\ RI_{AVG}}$$

A correction factor was added to guarantee that the actual average current will never exceed the initially specified average current.

Step 3:
Calculate the power rating for the snubber resistor. This can be done by calculating the worst case average current using the equation below. This equation assumes the worst case duty ratio of 50%.

$$P_{AVG} = \frac{CVp^2}{T}\ (1 - e^{\frac{-T}{RC}})$$

The calculations described above assume a PWM driver which is low impedance during the off-state. If the driver is open circuit during the off-state, the equations are no longer valid and the snubber network may have adverse effects on system stability. This potential instability occurs as a result of the capacitor discharging into the motor during the off-state. The additional charge stored in the capacitor can cause the motor and driver to have a non-linear transfer function with a much higher gain at lower duty ratios.

2) PWM Switching Noise
The second most likely source of noise in a PWM driven servo system is the motor power driver. The noise originates from the high speed switching of voltage on the driver's output. Fast current transients are usually minimal due to the inductive nature of the motor. However, if there is sufficient capacitive or parallel resistive loading, there may also be significant current transients as well. These high speed power signals are usually sent over lengthy cables to a motor. These cables can very effectively radiate this energy to the surrounding environment if precautions are not taken. One way to reduce this radiated energy is to route the motor wires as physically close together as possible. A grounded shield could be added to these wires as a second level of protection.

Another effective way to reduce this noise is to place ferrite beads in line with the driver's outputs. The beads slow down the fast switching edges of the PWM's output. The beads should be located as physically close to the driver as possible. A more effective but more expensive way to reduce this noise is to place a more complex low pass filter in line with the motor driver's outputs. Typically this filter would be an LC type filter. An example of this is shown in Figure 12. Keep in mind that this type of filter is only applicable for low impedance off-state drivers.

It is important to design the filter such that the motor in combination with the filter does not exceed the driver's peak current or average current ratings.

Using a motor driver which is high impedance in the off-state may also be a major source of noise in a servo control system. When the driver switches from

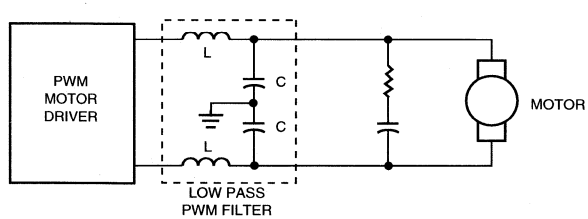


Figure 12. Example of a Low Pass PWM Filter.

the on-state to the off-state, a high voltage spike is generated as a result of the rapid interruption of current through the highly inductive motor windings. This high voltage spike and rapid interruption of current is the primary source of noise. In almost all applications this type of driver is more noisy than the low impedance off-state type driver. Where possible, it is highly recommended that a low impedance off-state driver be used.

3) Other Sources of Noise
In addition to the servo motor and driver, there may be other significant sources of noise in your system. The following is a list of some common sources of noise that may affect your HCTL-1100 based servo control system.

- Switching power supplies
- High power electromechanical actuators
- Noisy switches
- Electrostatic discharge
- Arcing of any sort
- SCRs and TRIACs
- Gas discharge tubes or displays

In general, high power/high speed electrical devices are likely to be a source of noise. The best way to minimize the high frequency RF energy radiated from these devices is to slow down any fast voltage or current transients created by these devices. EMI shielding is also an effective way to reduce this radiated energy.

Answers to Commonly Asked Questions About the HCTL-2020

Application Brief M-019

Question 1.

What is the maximum frequency on any one channel (A or B) of pulses that will be counted by the HCTL-2020?

Answer: 2.3 MHz.
The maximum frequency of the clock that can be used is 14 MHz. Each input qualified by the chip input filter is considered to be a valid level if it remains for at least three consecutive rising edges (3/14 microseconds). Therefore, for two valid levels (one cycle of the input) the minimum time should be 6/14 microseconds. The maximum frequency is 14/6 MHz. This maximum frequency will be reduced slightly in order to take into account the finite rise times, assymetry of the waveforms, and noise.

Question 2.

Is it possible to hold the SEL line LO and read the HI byte (a flow-through of the HI byte) like it is possible to hold the SEL line HI and read the LO byte (a flow-through of the LO byte)?

Answer: No.
With a negative clock edge the internal latch is inhibited and stops being updated. The HI byte value is not updated for subsequent reads.

Question 3.

If SEL and OE are LO but there is no negative clock edge during this time, does it mean that the inhibit will not be set?

Answer: No.
Internal to the chip SEL and OE being LO at the same time leads to an inhibit condition being satisfied. With the next negative clock edge the internal latch is inhibited from counting. In order to reset the inhibit two conditions should be satisfied in sequence:

1) a negative clock edge should see SEL being HI and OE being LO.

2) a negative clock edge should see the OE at HI. (SEL is a don't care for this.)

Note that a total of three clock edges – one to set the inhibit, one to start the reset, and one to complete the reset of the inhibit, is needed for the whole process.

Question 4.

Can the index pulse from a three channel encoder be used to reset the latch in the HCTL-2020?

Answer: Yes.
HP three channel encoders give a HI level index pulse every revolution of the code wheel and this index pulse occurs when both channel A and B are LO for a quarter period of a cycle. If this index pulse is inverted and connected to the reset (Pin 7 on HCTL-2020) it will reset the internal latch to zero as long as this signal is LO for 28 ns. Note that a reset also resets the inhibit.

Question 5.

Can the chip be reset at the end of every read?

Answer: Yes.
Since the chip was not designed with this purpose in mind, some timing constraints for doing this follow. It is assumed that the chip is being read at a negative going clock edge as explained in the data sheets. The chip can be reset if a delay can be introduced after the negative going clock edge at which the chip is read such that the data that is being read is stable in the internal latch (in

other words, it is not being reset to zero by the time it is read) and then a LO signal (duration = 28 ns and occuring before the next rising clock edge after the read) is input to the reset pin. It is necessary that the reset signal occur before the next rising clock edge after the read; otherwise a new count that could be coming in with the rising edge will be lost.

Question 6.

What is the quadrature relationship needed between signals on channel A and channel B?

Answer: At least one positive clock edge between any two valid quadrature states, which will be ensured if there is at least one clock period between two successive quadrature states. A good design will take into account the finite rise times of signals.

Question 7.

Is the up/down signal a level? HI when counting up and LO when counting down?

Answer: No.
The signal is at the correct level one positive clock edge before a count and stays at the correct level until the next rising edge after the count. Therefore, if there are quadrature counts every four positive edges (which is the fastest possible rate), then the signal stays at the correct level at all times. At all other times the level on the signal is not defined. Therefore, to use the signal, combine it with the CNT_{DCDR} signal.

A Simple Interface for the HCTL-2020 with a 16-bit DAC without Using a Processor

Application Brief M-020

Introduction

In certain applications it becomes necessary to interface the HCTL-2020 to a DAC (Digital Analog Converter) without having to use a processor or micro controller. A typical block diagram is shown in Figure 1.

A simple circuit with easily available components can be used. The *Analog Devices* AD 569 16-bit DAC is shown. It has an 8-bit interface and signals to control the loading of the high and low bytes from the HCTL-2020 called HBE (High Byte Enable) and LBE (Low Byte Enable) respectively. These signals are active LO signals. The LDAC signal on the AD 569 can be connected to ground or tied to LBE. The CS signal is tied to ground. Please refer to the data sheets for the DAC AD 569 for detailed timing diagrams. The different operations needed to achieve the interface can be described as shown in Table 1.

Table 1.

SEL	$\overline{OE}$	$\overline{HEB}$	$\overline{LBE}$	Remarks
LO	LO	LO	HI	;enable the HI byte from HCTL-2020, ;load the byte into the DAC with the ;HBE signal.
LO	LO	HI	HI	;complete the loading process.
HI	LO	HI	LO	;enable the LO byte from the HCTL- ;2020, load the byte into the DAC ;with the LBE signal.
HI	LO	HI	HI	;complete the loading process.
HI	HI	HI	HI	;pull OE high to complete inhibit ;reset of HCTL-2020.
HI	HI	HI	HI	;
HI	HI	HI	HI	;
HI	HI	HI	HI	;The above three sets of states have ;been added to get a total of 8 states.

The last three states in Table 1 simplify the design. They can be arbitrarily selected. For example, they can be used to reset the inhibit in the HCTL-2020 by dummy read. In order to simplify the design they have been chosen to be HI here. Note that LO on all cannot be used as it corresponds to enabling the HCTL-2020 and the AD 569. After this last state the circuit is made to start from the beginning and therefore repeat the read to the HCTL-2020, write to the DAC cycle.

Note: If you are using a 16-bit DAC with no 8-bit interface, but only a 16-bit interface, consider using the signals HBE and LBE to enable external latches connected to the HI and LO bytes of the DAC respectively as shown in Figure 1.

The design consists of dividing the main clock by 2, 4 and 8 using a 74LS193 counter, and combining the 8-states to give the sequence of steps described above for each signal. The diagrams shown in "Sequencer and Control Signals Timing Diagram" and

"Truth Table" are descriptive of the process. The SEL signal can be realized with an OR gate. In a similar manner the other signals can be constructed also. A logic gate diagram of the sequencer and control signals is shown in Figure 2.

The maximum rate at which the DAC is updated with a new count is equal to the main clock rate into the HCTL-2020 divided by 8.

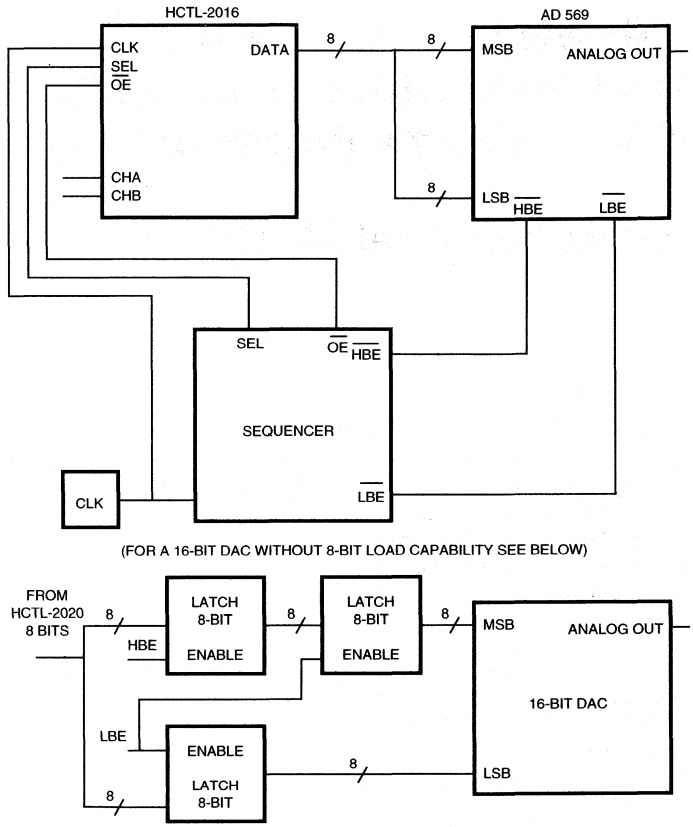
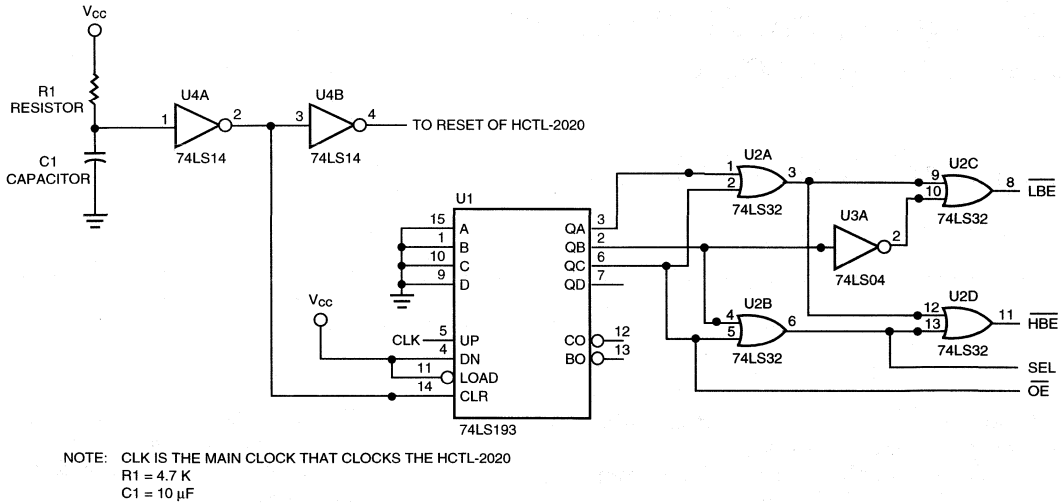


Figure 1. Interfacing the HCTL-2020 with the 16-bit DAC AD 569.

Truth Table

M3	M2	M1	SEL	$\overline{OE}$	$\overline{HBE}$	$\overline{LBE}$
0	0	0	0	0	0	1
0	0	1	0	0	1	1
0	1	0	1	0	1	0
0	1	1	1	0	1	1
1	0	0	1	1	1	1
1	0	1	1	1	1	1
1	1	0	1	1	1	1
1	1	1	1	1	1	1

Note: M1 = CLK/2
M2 = CLK/4
M3 = CLK/8



NOTE: CLK IS THE MAIN CLOCK THAT CLOCKS THE HCTL-2020
R1 = 4.7 K
C1 = 10 µF

Figure 2. Sequencer and Control Signals Logic Diagram.

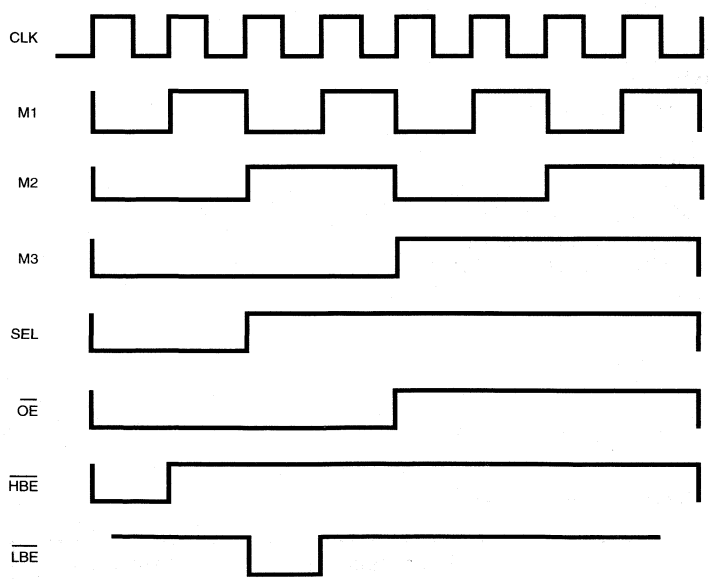


Figure 3. Sequencer and Control Signals Timing Diagram.

HEWLETT® PACKARD

Interfacing the HCTL-1100 to the MC68HC11

Application Brief M-021

Introduction

This application brief describes two interfaces to the HCTL-1100 with the MC68HC11E9. They are Port Interfacing and Bus Interfacing, respectively. Circuit diagrams for both cases are presented and code to read and write to the HCTL-1100 is supplied. A table showing the read and write cycle timing for both cases is presented for comparison purposes.

For the purpose of the port interfacing the 68HC11 is used in the single-chip mode. Port C is connected to the data/address pins of the HCTL-1100 and four pins on port B are used to control the reading and writing of data from and to the HCTL-1100. The E clock of the 68HC11 is connected to the clock input of the HCTL-1100. The frequency of the E clock is 2 MHz (1/4 the crystal frequency of the 68HC11). This is the highest clock frequency at which the HCTL-1100 can be run.

Port Interfacing

Connections:

E clock of the 68HC11 is connected to HCTL-1100 EXTCLK.

Port C pins PC0-PC5 are connected to the AD0-AD5 respectively.

PC6 to D6.
PC7 to D7.
PB0 to OE.
PB2 to CS.
PB4 to ALE.

PB6 to R/W, as shown in the schematic diagram in Figure 1, "68HC11 to HCTL-1100 Port Interface".

The table shown below compares the time taken by the read and write routines in the port and bus interfaces.

Table 1. Execution Times

	Read Operation	Write Operation
Port Interface	30.5 µs	26 µs
Bus Interface	14.5 µs	12.5 µs

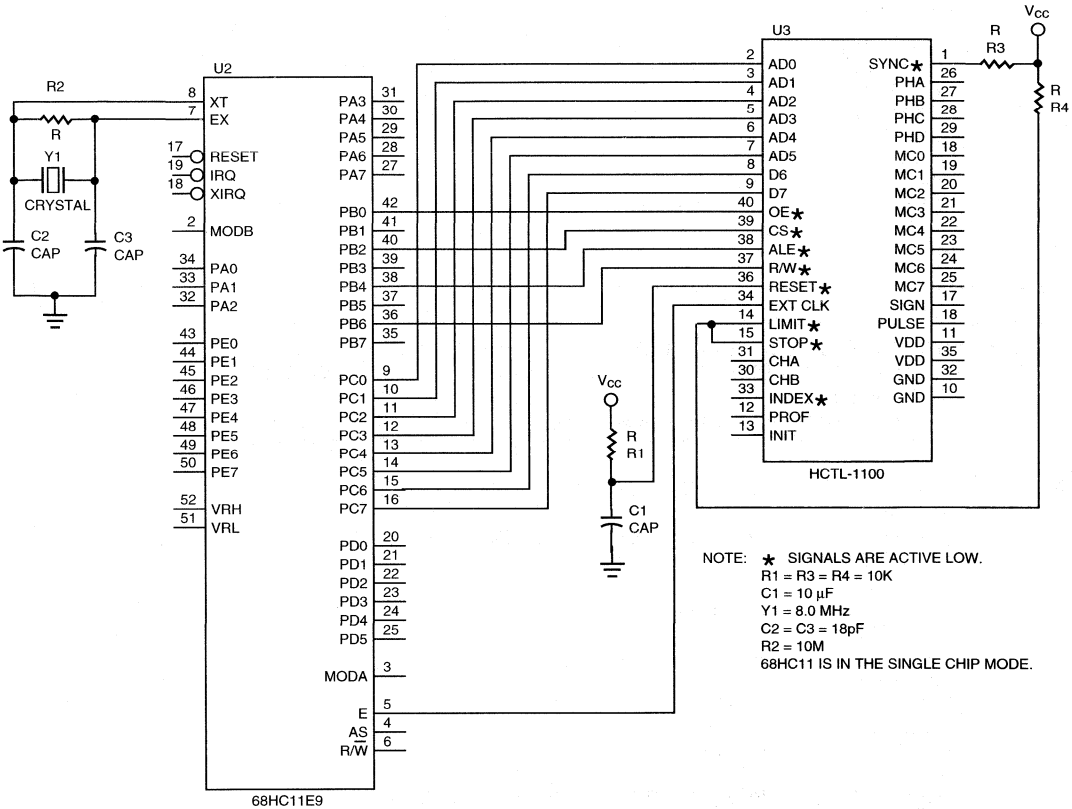


Figure 1. 68HC11 to HCTL-1100 Port Interface.

The following two subroutines to read and write to the HCTL-1100 assume that the non-overlapped mode of interfacing, as explained in the HCTL-1100 data sheet, is being used.

```
;*****************************************************************************
;THE FOLLOWING SUBROUTINE IS USED TO WRITE DATA TO THE HCTL-1100.
;THE SUBROUTINE IS CALLED WITH THE ADDRESS OF THE LOCATION TO BE
;WRITTEN TO IN REGISTER B. THE DATA TO BE WRITTEN IS IN A MEMORY
;LOCATION CALLED WRITEDTA.
;ADDRESS $1007 IS DATA DIRECTION CONTROL REGISTER FOR PORT C.
;ADDRESS $1003 IS PORT C.
;ADDRESS $1004 IS PORT B.
;*****************************************************************************

WR1100:  PSHA            ;SAVE THE ACCUMULATOR IN THE STACK.:
         LDAA#0FF
         STAA$1007       ;SET PORT C DIRECTION TO OUTPUT.
         STAB$1003       ;ADDRESS OUT.
         LDAA#0EF
         STAA$1004       ;ALE LOW
```

(Continues)

```
        LDAA#0BB
        STAA$1004       ;ALE HI, CS LO, R/W LOW
        LDAA WRITEDTA   ;DATA TO BE WRITTEN LOADED IN REGISTER A.
        STAA$1003       ;OUTPUT DATA.
        LDAA#0BF
        STAA$1004       ;CS HI.
        LDAA#0FF        ;
        STAA$1004       ;R/W HI.
        PULA            ;RETRIEVE THE VALUE OF ACCUMULATOR FROM
                        ;STACK.
        RTS


;*******************************************************************************
;THE FOLLOWING SUBROUTINE IS USED TO READ DATA FROM THE HCTL-1100.
;THE SUBROUTINE IS CALLED WITH THE ADDRESS OF THE LOCATION TO BE
;READ IN REGISTER B.
;THE SUBROUTINE RETURNS THE DATA BYTE READ IN REGISTER B.
;*******************************************************************************

RD1100: PSHA            ;SAVE THE ACCUMULATOR ON STACK.
        LDAA#0FF
        STAA$1007       ;PORT C IS SET TO OUTPUT MODE.
        STAB$1003       ;ADDRESS OUT.
        LDAA#0EF
        STAA$1004       ;ALE LO.
        LDAA#0FB
        STAA$1004       ;ALE HI, CS LO.
        LDAA#0FF
        STAA$1004       ;CS HI.
        LDAA#0FE
        STAA$1004       ;OE LO.
        LDAA#00
        STAA$1007       ;PORT C IS SET TO INPUT TO READ THE DATA.
        LDAB$1003       ;READ THE DATA INTO REGISTER B.
        LDAA#0FF
        STAA$1004       ;OE HI.
        PULA            ;RETRIEVE THE VALUE OF THE ACCUMULATOR A
                        ;FROM THE STACK
        RTS
```

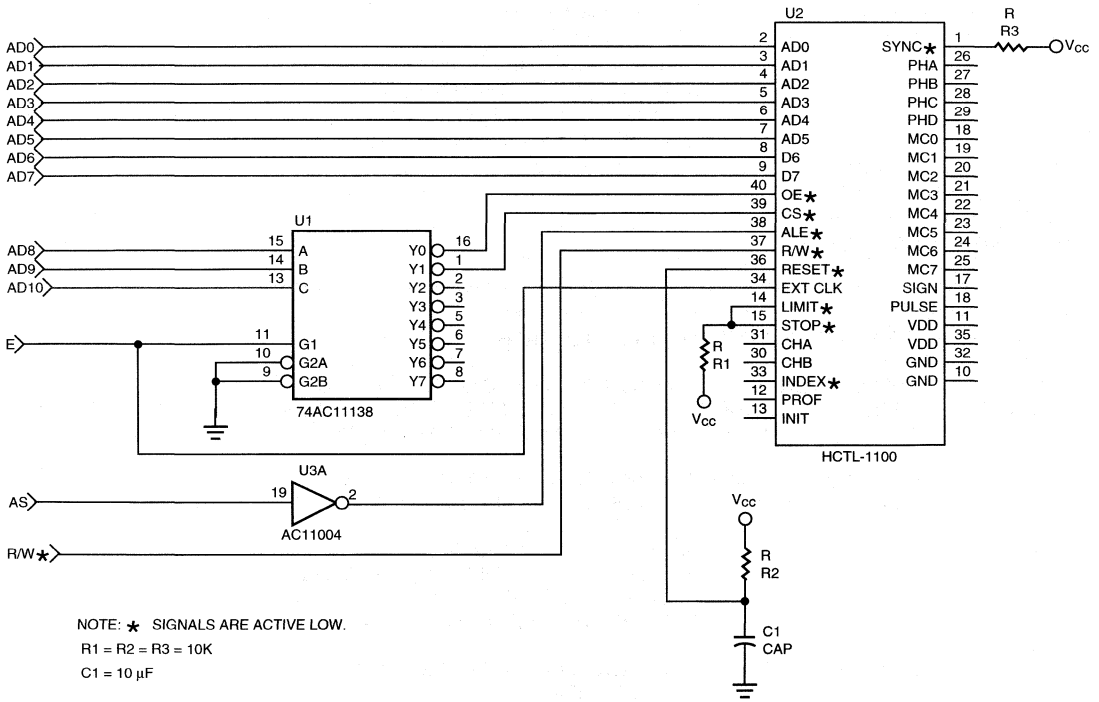


Figure 2. 68HC11 to HCTL-1100 Bus Interface.

Bus Interfacing

Connections:

E clock of the 68HC11 is connected to the HCTL-1100 EXT CLK.

AS of the 68HC11 is inverted and connected to the ALE signal of the HCTL-1100.

R/W of the 68HC11 is connected to the R/W of the HCTL-1100.

The rest of the connections are shown in the schematic diagram in Figure 2, "68HC11 to HCTL-1100 Bus Interface".

Note that all signals on this schematic with a "*" sign are active low signals.

For the bus interface, a 3-to-8 decoder 74AC11138 and an inverter 74AC11004 are needed. With these two chips, four HCTL-1100 ICs can be interfaced to the 68HC11 bus. The "68HC11 to HCTL-1100 Bus Interface" schematic shows how connections to one of the four HCTL-1100s can be made. The CS and OE signals of the other three HCTL-1100s can be connected to the outputs of the 74AC11138 in a similar manner to the connections made to the HCTL-1100 shown in the diagram.

The following two subroutines are used to write and read while using the 68HC11 bus to interface to the HCTL-1100.

Please note that all four routines assume that the clock frequency into the HCTL-1100 is equal to 2 MHz. If the HCTL-1100 clock frequency is less than 2 MHz, and the processor clock is at 2 MHz, NOPs may be inserted where it is required to produce more delay in the read routine as shown, to satisfy timing requirements given in the data sheet.

```
;*************************************************************************
;THIS SUBROUTINE IS USED TO WRITE DATA TO THE HCTL-1100 FOR THE
;BUS INTERFACE.
;THE DATA TO BE WRITTEN IS IN MEMORY LOCATION CALLED WRITEDTA
;REGISTER B CONTAINS THE ADDRESS OF THE LOCATION TO BE WRITTEN.
;*************************************************************************
;
            OE0  EQU  $0F000   ;ADDRESS HI BYTE FOR OE* SIGNAL.
            CS0  EQU  $0F100   ;ADDRESS HI BYTE FOR CS* SIGNAL.

WRITE1100:  PSHA               ;SAVE THE ACCUMULATOR
            LDX#CS0            ;HI BYTE ADDRESS IN INDEX REGISTER.
            ABX                ;ADD THE ADDRESS OF LOCATION TO BE
                               ;WRITTEN TO FORM COMPLETE ADDRESS.

            LDAA WRITEDTA      ;LOAD THE DATA TO WRITE IN THE
                               ;ACCUMULATOR.

            STAA 0,X           ;WRITE THE VALUE TO THE HCTL-1100
            PULA
            RTS

;*************************************************************************
;THIS SUBROUTINE IS USED TO READ DATA FROM THE HCTL-1100 FOR THE
;BUS INTERFACE.
;THE ADDRESS OF THE LOCATION TO BE READ IS IN REGISTER B.
;THE DATA READ IS RETURNED IN REGISTER B.
;*************************************************************************
;
RD1100:     PSHA
            LDX#CS0            ;HI BYTE OF ADDRESS WHICH PULSES CS*
                               ;IN INDEX REGISTER
            ABX                ;ADD REGISTER B TO FORM COMPLETE
                               ;ADDRESS.
            LDAA 0,X           ;LATCH THE ADDRESS IN HCTL-1100, BY
                               ;PERFORMING A DUMMY READ.
            ;NOP
            ;NOP               ;IF NEEDED.(SEE EXPLANATION ABOVE.)
                               ;NOT NEEDED IF HCTL-1100 HAS 2 MHz
                               ;CLOCK.

            LDX#OE0            ;LOAD THE HIGH BYTE OF THE ADDRESS
                               ;WHICH PULSES OE* IN INDEX REGISTER.

            LDAB 0,X           ;READ THE HCTL-1100. DATA IN REGISTER B.
            PULA
            RTS
```

Quasi-Absolute Encoding

Application Brief M-022

What is Quasi-Absolute Encoding?

It is a method using Incremental encoders to determine absolute position after a small change in position.

Applications:

- Throttle Valve Positioning
- Steering Angle Sensor

  Used in:
  - Power steering control
  - Suspension control
  - 4-wheel steering
  - Traction control

A.) First, let us look at a typical 3-Channel Incremental Encoder and Codewheel.

There are two channels which produce digital signals that are 90 degrees out of phase with each other, which provides direction information and allows discrimination into quadrature counts. See A and B in Figure 1. The third channel occurs once per revolution and is used as a reference to establish an absolute position. The index channel coincides with channels A and B both low. See I in Figure 1.

Why use incremental encoding instead of absolute encoding?

Encoder Type	Advantages	Disadvantages
Optical Absolute	Position known on power up Easy interface to controller Various output codes available High resolution	Large size Expensive 2^N counts requires N channels
Optical Incremental	Low cost Small size High resolution Index pulse for absolute reference	Position unknown on power up* May require interface circuitry

* Quasi-Absolute addresses the issue of unknown position on power up for optical incremental encoders.

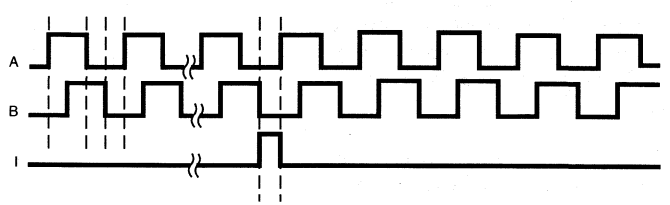


Figure 1.

B.) Now, let us look at the same 3-Channel Incremental Encoder used with a Special Codewheel to achieve Quasi-Absolute encoding: A coding scheme can be used with multiple index channels in order to determine the absolute position without a large movement of the

codewheel. A very simple scheme might use 1 index at 0 degree, 2 indexes at 90 degreees, 3 indexes at 180 degrees, and 4 indexes at 270 degrees. This would provide absolute position information within 1/4 turn. See I_1 in Figure 2.

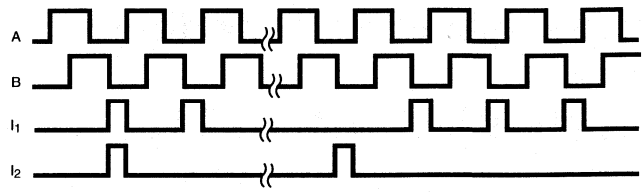


Figure 2.

Another method might use indexes spaced such that a specific number of counts on channels A and B happen between adjacent indexes. See I_2 in Figure 2.

More complex coding schemes can be used to provide absolute position detection in just a few mechanical degrees of movement.

Codewheels:

Quasi-Absolute codewheels may be developed in cooperation with Hewlett-Packard.

Encoders:

Special encoders may be required depending on desired resolution. For resolutions of 73 LPI or below, a standard 3-channel encoder may be used to provide up to 1 index pulse per electrical cycle. Higher resolutions using 1 index pulse per 10 or more cycles may also use a standard 3-channel encoder. High resolutions using 1 index pulse per 9 or less cycles requires a special encoder design and may be developed in cooperation with Hewlett-Packard.

For more information concerning your particular application, you may contact the Optoelectronics Applications Hot Line, 408-435-4444.

Interfacing the MC68HC11 to the HCTL-2020

Application Brief M-023

Introduction

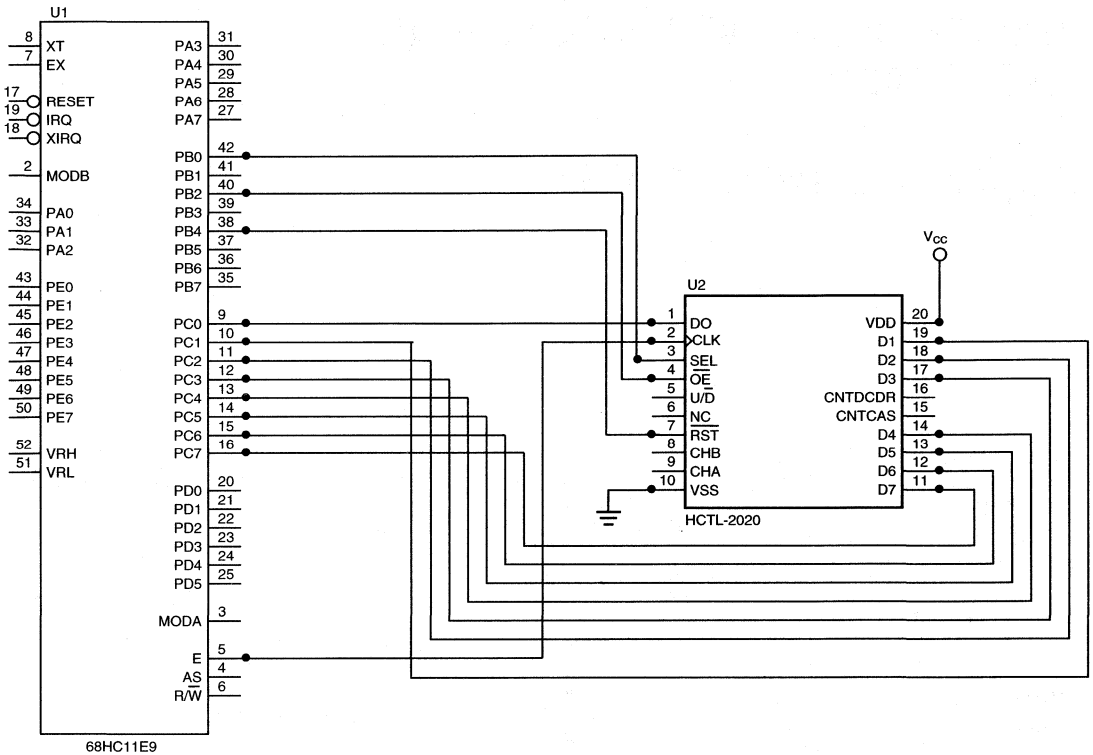
This application brief describes two interfaces for the HCTL-2020 to the MC68HC11. One is a port interface and the other is a bus interface.

Port Interface

The connections are shown in Figure 1, the schematic titled "Port Interface". Port C is used to read the data in and 3 pins on port B are used for the control signals to the HCTL-2020. The E clock from the 68HC11E9 is used to clock the HCTL-2020. In this interface it is assumed that the 68HC11E9 is in the single chip mode.

The subroutines to read from the HCTL-2020 and to reset the HCTL-2020 follow.

```
;*******************************************************************************
;THIS SUBROUTINE IS USED TO READ DATA FROM THE HCTL-2020
;FOR THE PORT INTERFACE.
;THE SUBROUTINE RETURNS THE 16 BIT DATA FROM THE HCTL-
;2020 IN REGISTER IX.
;* DENOTES ACTIVE LOW SIGNALS.
;*******************************************************************************

RD2020:  PSHA        ;SAVE REG A ON STACK.
         PSHB
         LDAA#00
         STAA$1007   ;PUT PORT C IN INPUT MODE.
         LDAA#0FA
         STAA$1004   ;SEL LO AND OE* LO.
         LDAA$1003   ;HIGH BYTE OF DATA IN REG. A.
         LDAB#0FB
         STAB$1004   ;SEL HI AND OE* LO.
         LDAB$1003   ;LO BYTE IN REG. B.
         XGDX        ;REGISTER IX HAS THE 16 BIT VALUE FROM
                     ;THE HCTL-2020
         LDAA#0FF
         STAA$1004   ;SEL HI AND OE* HI.
         PULB        ;RESTORE REG B FROM STACK.
         PULA        ;RESTORE REG A FROM STACK.
         RTS

;*******************************************************************************
;THIS SUBROUTINE IS USED TO RESET THE HCTL-2020 IN THE
;PORT INTERFACE.
;*******************************************************************************

RST2020: PSHA
         LDAA#0EF
         STAA$1004   ;RST*LO.
         LDAA#0FF
         STAA$1004   ;RST*HI.
         PULA
         RTS
```



NOTE: 68HC11E9 IS IN THE SINGLE CHIP MODE.
REFER TO THE 68HC11E9 REFERENCE MANUAL FOR DETAILS.

Figure 1. Port Interface Schematic.

Bus Interface

In applications where the expanded-mode is already being used, it is convenient to use the bus interface to the HCTL-2020. Figure 2, "Bus Interface Control Signals", is the schematic diagram to generate the control signals in the expanded mode.

The subroutines to read and reset follow.

```
;*******************************************************************************
;THIS SUBROUTINE READS A VALUE FROM THE HCTL-2020. THE HIGH
;BYTE OF DATA IS RETURNED IN REG IY IN THE CORRECT ORDER OF
;HIGH AND LOW BYTES.
;THE TWO BYTES ARE MAPPED AT THE MEMORY LOCATIONS AT 0CFFOh
;AND 0CFF1h RESPECTIVELY.
;*******************************************************************************

H2020 EQU $0C000

RD2020:  LDY H2020
         RTS


;*******************************************************************************
;THIS SUBROUTINE IS USED TO RESET THE HCTL-2020. THE RESET
;SIGNAL IS MAPPED TO MEMORY LOCATION 0CFF2h.
;*******************************************************************************

REST2020 EQU $0CFF2

RST2020:  PSHA
          LDAA REST2020      ;READ LOCATION $CFF2 TO CAUSE RESET
          PULA
          RTS
```

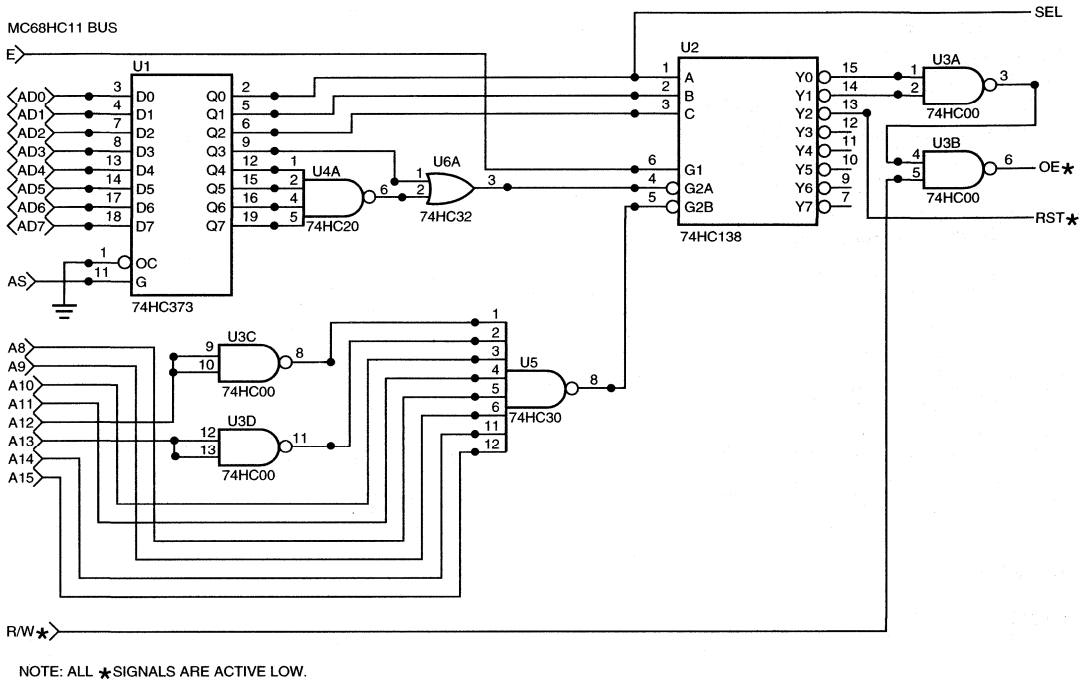


Figure 2. Bus Interface Control Signals.

Using the HCTL-1100 with DC Brush Motors

Application Brief M-024

Introduction

The HCTL-1100 general purpose motion control IC can be used for closed loop position and velocity control of DC Brush motors. A block diagram is shown in Figure 1.

A linear or PWM amplifier, host computer/microcontroller and an incremental optical encoder are the only other components needed to design and implement the closed loop control system.

Any one of four operating modes (two for position control and two for velocity control) can be used with DC Brush motors. Please refer to the technical data sheets for the HCTL-1100 for detailed information on the different modes of operation.

For more information on interfacing to a host please refer to Application Briefs M-015, M-016, M-021, and M-003. For more information on HP optical encoders please refer to Application Briefs M-101 and M-109.

Amplifiers compatible with the HCTL-1100s can be built from discrete components, are available as integrated half and full bridges and, from various vendors with special features. A list of some of the manufacturers of amplifiers follows:

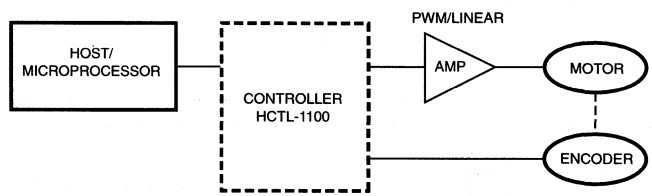


Figure 1. Closed Loop Position and Velocity Control of DC Brush Motor.

Name	Phone Number
Allegro	(508) 853-5000
SGS-Thomson	(602) 867-6100
Unitrode	(603) 424-2410
Harris	(407) 724-3000
TI	(800) 336-5236
Motorola	(708) 490-9500
International Rectifier	(310) 322-3331
Siliconix	(408) 970-5700

In many cases motor manufacturers supply amplifiers for their motors. A good reference for a list of amplifier vendors is the PCIM® (Power Conversion and Intelligent Motion) magazine issue dated December 1995.

PWM Interface

Figure 2 shows the glue logic for a PWM amplifier interface to the HCTL-1100 for a DC Brush motor using the L6203 IC made by SGS-Thomson.

Linear Amplifier Interface

Figure 3 shows an example of a linear amplifier interface to the HCTL-1100 for a DC Brush motor using the L165 made by SGS-Thomson. The circuit makes use of a digital to analog converter DAC-08.

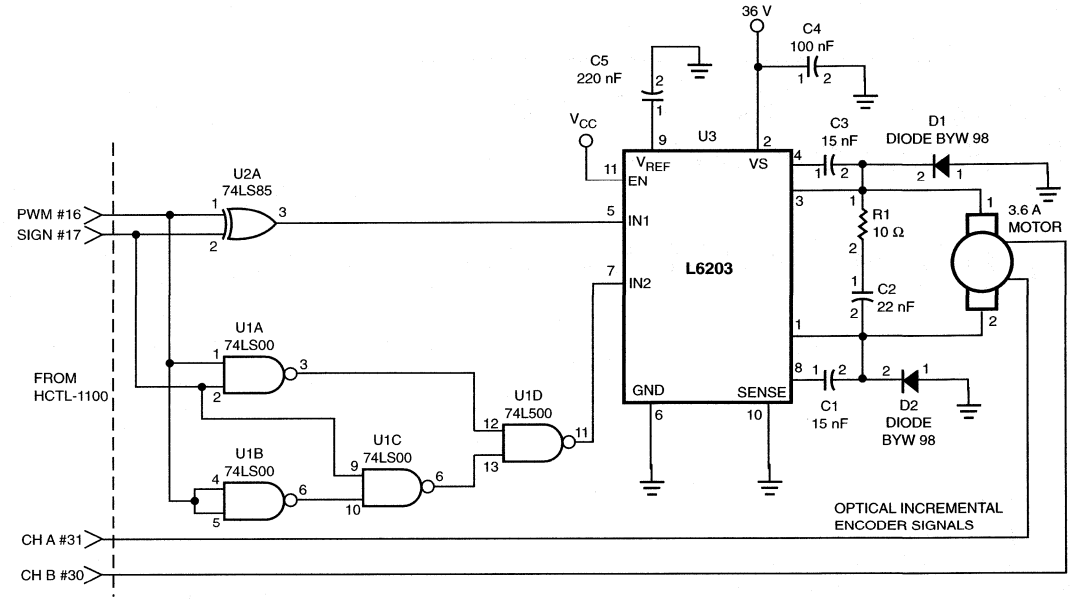


Figure 2.

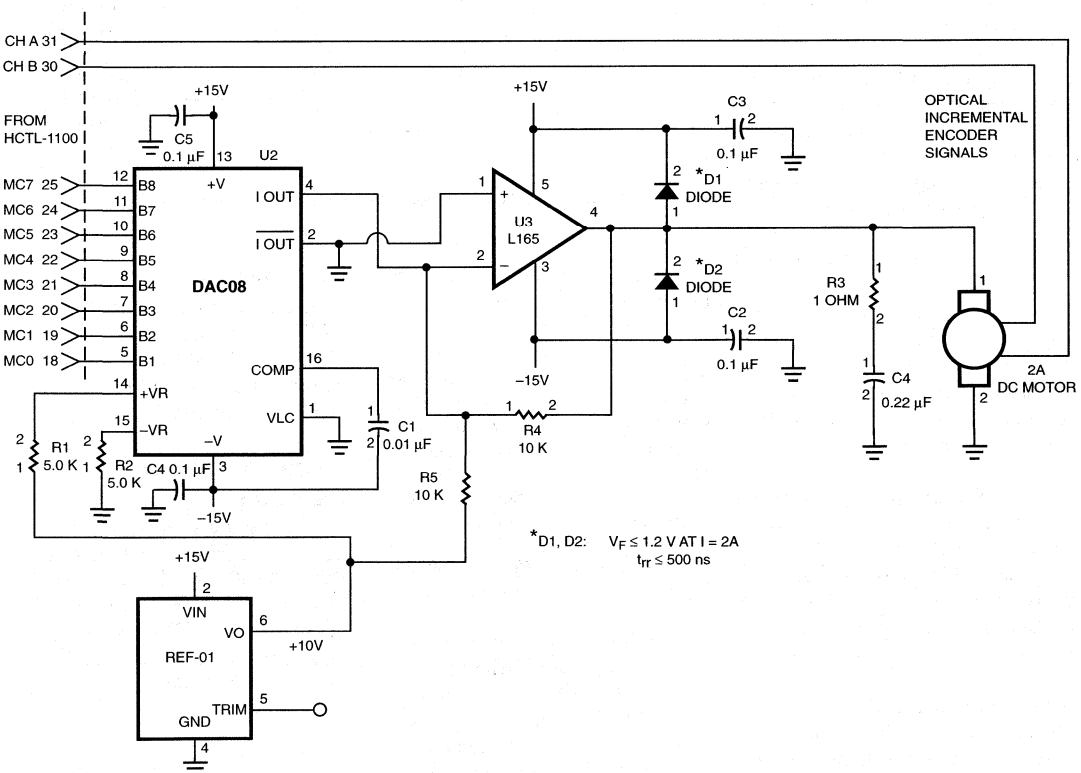


Figure 3.

Using the HCTL-1100 with DC Brushless Motors

Application Brief M-025

Introduction

The HCTL-1100 general purpose motion control IC can be used for closed loop position and velocity control of DC Brushless motors. A block diagram is shown in Figure 1.

A linear or PWM amplifier, host computer/microcontroller and an incremental optical encoder are the only other components needed to design and implement the closed loop control system.

Any one of four operating modes (two for position control and two for velocity control) can be used with DC Brushless motors. Please refer to the technical data sheets for the HCTL-1100 for detailed information on the different modes of operation.

For more information on interfacing to a host please refer to application briefs M015, M016, M021 and M003. For more information on HP optical encoders please refer to application briefs M101 and M109.

Amplifiers compatible with the HCTL-1100 can be built from discrete components, are available as integrated half and full bridges and, from various vendors with special features. A list of some of the manufacturers of amplifiers is:

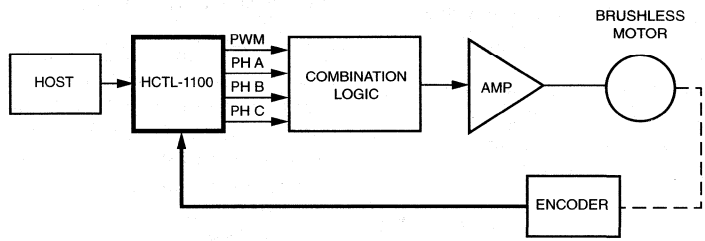


Figure 1.

Name	Phone Number
Allegro	(508) 853 5000
SGS-Thomson	(602) 867 6100
Unitrode	(603) 424 2410
Harris	(407) 724 3000
TI	(800) 336 5236
Motorola	(708) 490 9500
International Rectifier	(310) 322 3331
Siliconix	(408) 970 5700

In many cases motor manufacturers supply amplifiers for their motors. A good reference for a list of amplifier vendors is the PCIM® (Power Conversion and Intelligent Motion) magazine issue dated December 1995.

PWM Interface for DC Brushless motor without Hall effect sensors

Shown in Figure 2 is an example of a PWM amplifier interface to the HCTL-1100 for a 3 phase, 4 pole DC Brushless motor using the UC3657 IC made by Unitrode. This interface does not require the DC Brushless motor to have Hall effect sensors for commutation. The HCTL-1100 provides commutation signals based on the optical incremental encoder signals CH A, CH B and CH I.

A 192 CPR encoder is assumed to be installed on the DC Brushless motor and the HCTL-1100 commutator is assumed to be counting in full counts. For a description of the HCTL-1100

commutator please refer to application brief M012.

X Register is programmed to 16D and Y to 16D. The Ring register is programmed to 96D. All the other registers associated with the commutator are programmed to zero decimal.

For the purposes of this application brief it is assumed that the motor rotates in the clockwise direction when the currents in the three phases are commutated in the following order — AB, AC, BC, BA, CA, CB, AB .....
For the counter-clockwise direction of rotation, the currents are in the following order — BA, BC, AC, AB, CB, CA, BA .....

Table 1 is the truth table for the input signals needed for the UC3657 based on PH A, PH B and PH C signals and PWM signal from the HCTL-1100.

Based on this truth table, Figure 2 shows the schematic for the glue logic needed for interfacing the HCTL-1100 to the UC3657.

PWM Interface for DC Brushless motor with Hall effect sensors

Shown in Figure 3 is an example of a PWM amplifier interface to the HCTL-1100 for a 3 phase, 4 pole DC Brushless motor using the UC3657 IC made by Unitrode. This interface requires the DC Brushless motor to have Hall effect sensors for commutation, with 120 electrical degrees separation. The PAL16L8 is used to provide the control signals for the driver UC3657.

A 192 CPR encoder is assumed to be installed on the DC Brushless motor and the HCTL-1100 commutator is assumed to be counting in full counts. For a description of the HCTL-1100 commutator please refer to application brief M012.

X Register is programmed to 16D and Y to 16D. The Ring register is programmed to 96D. All the other registers associated with the commutator are programmed to zero decimal.

For the purposes of this application brief it is assumed that the motor rotates in the clockwise direction when the currents in the three phases are commutated in the following order — AB, AC, BC, BA, CA, CB, AB .....
For the counter-clockwise direction of rotation, the currents are in the following order — BA, BC, AC, AB, CB, CA, BA .....

Table 2 is the truth table for the input signals needed for the UC3657 based on HA, HB and HC Hall-effect sensor signals, and, SIGN and PWM signal from the HCTL-1100.

Based on the truth table as given in Table 2, the schematic for the interface is given in Figure 3.

Table 1.

PWM	PH A	PH B	PH C	A1	A2	B1	B2	C1	C2
1	1	0	0	0	0	1	1	1	0
1	1	1	0	0	0	1	0	1	1
1	0	1	0	1	0	0	0	1	1
1	0	1	1	1	1	0	0	1	0
1	0	0	1	1	1	1	0	0	0
1	1	0	1	1	0	1	1	0	0
0	1	0	0	0	0	1	0	1	0
0	1	1	0	0	0	1	0	1	0
0	0	1	0	1	0	0	0	1	0
0	0	1	1	1	0	0	0	1	0
0	0	0	1	1	0	1	0	0	0
0	1	0	1	1	0	1	0	0	0

Please note that the 16L8 has active low outputs, and therefore when programming the 16L8, the sum-of-product terms for programming should be those corresponding to /A1 (complement of A1).

eg /A1 = PWM*/SIGN*HA*/HB*/HC
+ PWM*/SIGN*HA*HB*/HC
+ PWM*SIGN*/HA*HB*HC
+ PWM*SIGN*/HA*/HB*HC

The INH input to the UC3657 is defined as,

/INH = HA*/HB
+ /HB*HC
+ /HA*HC
+ HB*/HC
+ HA*/HC
+ /HA*HB

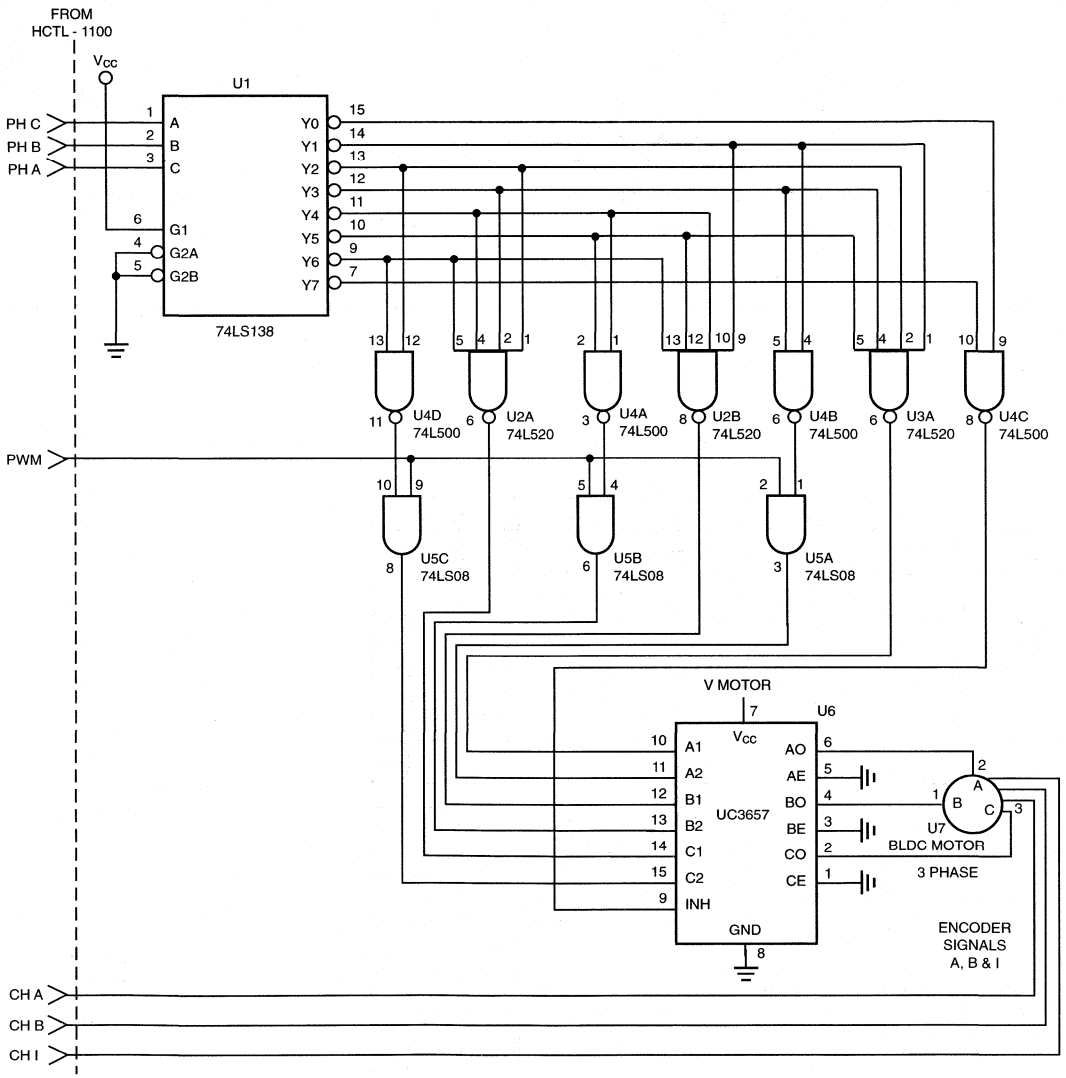


Figure 2.

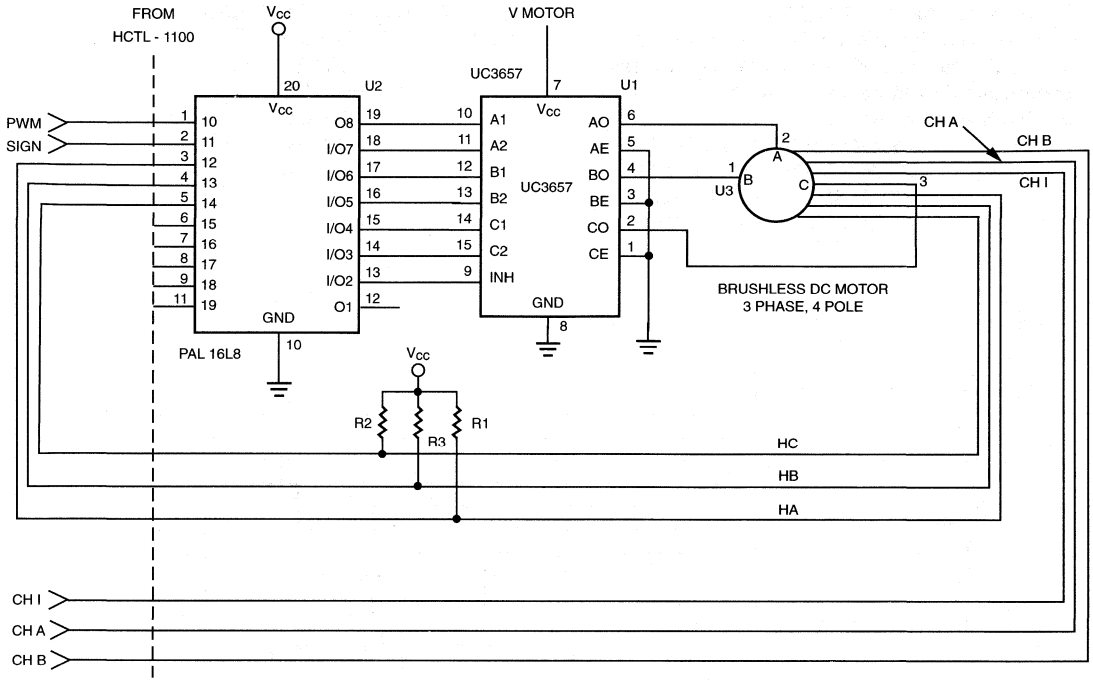


Figure 3.

Table 2.

PWM	SIGN	HA	HB	HC	A1	A2	B1	B2	C1	C2
1	0	1	0	0	0	0	1	1	1	0
1	0	1	1	0	0	0	1	0	1	1
1	0	0	1	0	1	0	0	0	1	1
1	0	0	1	1	1	1	0	0	1	0
1	0	0	0	1	1	1	1	0	0	0
1	0	1	0	1	1	0	1	1	0	0
1	1	1	0	0	1	1	0	0	1	0
1	1	1	1	0	1	1	1	0	0	0
1	1	0	1	0	1	0	1	1	0	0
1	1	0	1	1	0	0	1	1	1	0
1	1	0	0	1	0	0	1	0	1	1
1	1	1	0	1	1	0	0	0	1	1
0	0	1	0	0	1	0	1	1	1	0
0	0	1	1	0	1	0	1	0	1	1
0	0	0	1	0	1	0	1	0	1	1
0	0	0	1	1	1	1	1	0	1	0
0	0	0	0	1	1	1	1	0	1	0
0	0	1	0	1	1	0	1	1	1	0
0	1	1	0	0	1	1	1	0	1	0
0	1	1	1	0	1	1	1	0	1	0
0	1	0	1	0	1	0	1	1	1	0
0	1	0	1	1	1	0	1	1	1	0
0	1	0	0	1	1	0	1	0	1	1
0	1	1	0	1	1	0	1	0	1	1

Using the HCTL-1100 with Stepper Motors

Application Brief M-026

Introduction

The HCTL-1100 general purpose motion control IC can be used for closed loop position and velocity control of Stepper motors. A block diagram is shown in Figure 1.

A linear or PWM amplifier, host computer/microcontroller and an incremental optical encoder are the only other components needed to design and implement the closed loop control system.

Any one of four operating modes (two for position control and two for velocity control) can be used with stepper motors. Please refer to the technical data sheets for the HCTL-1100 for detailed information on the different modes of operation.

For more information on interfacing to a host please refer to application briefs M015, M016, M021 and M003. For more information on HP optical encoders please refer to application briefs M101 and M109.

Amplifiers compatible with the HCTL-1100 can be built from discrete components, are available as integrated half and full bridges and, from various vendors with special features. A list of some of the manufacturers of amplifiers follows:

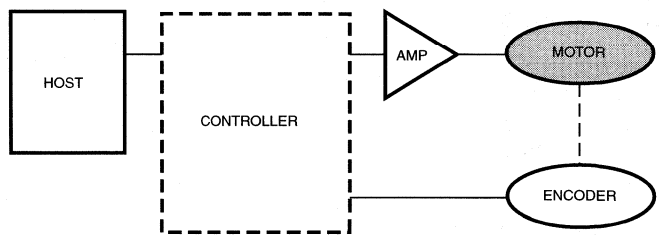


Figure 1. Step Motor Interface.

Name	Phone #
Allegro	(508) 853-5000
SGS-Thomson	(602) 867-6100
Unitrode	(603) 424-2410
Harris	(407) 724-3000
TI	(800) 336-5236
Motorola	(708) 490-9500
International Rectifier	(310) 322-3331
Siliconix	(408) 970-5700

In many cases motor manufacturers supply amplifiers for their motors. A good reference for a list of amplifier vendors is the PCIM® (Power Conversion and Intelligent Motion) magazine issue dated December 1995.

This application brief describes an interface to a 200 full steps per revolution stepper motor. A description of how the commutator needs to be configured to obtain half-stepping is described at the end.

Motor/Feedback Configuration:

1.8 degree per step, hybrid motor with 4 windings. 8 leads accessible to the user.
A pair of leads, as described in the motor data sheet, is connected in parallel giving two sets of windings. One set is called A1A2 and the other is called B1B2 for purposes of this application brief. Figure 2 describes the windings and the connections.

Number of steps/rev. = 200 full steps.
Encoder CPR = 400 CPR (1600 quadrature counts)
Number of torque cycles /rev = 50
Number of quadrature counts per torque cycle = 1600/50 = 32

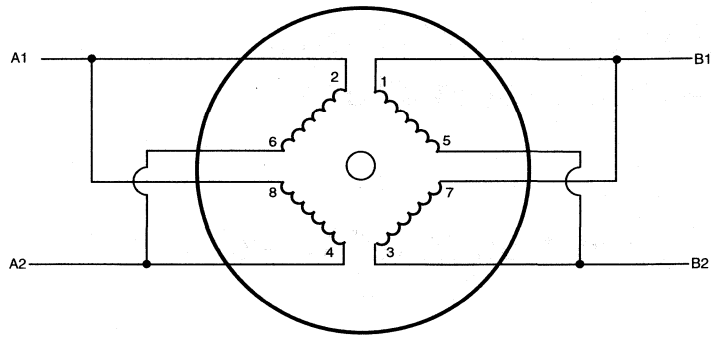


Figure 2. Motor Connections.

Phase Energizing Sequence:

CW ROTATION

A1A2*	B1B2
A2A1	B1B2
A2A1	B2B1
A1A2	B2B1

CCW ROTATION

A1A2	B1B2
A1A2	B2B1
A2A1	B2B1
A2A1	B1B2

Based on the motor/feedback configuration described, the commutator can be programmed as:

Status Register (R07H) = XXXX0011H
Commutator Ring (R18H) = 32
X Register (R1AH) = 8
Y Phase Overlap (R1BH) = 0
Offset (R1CH) = 0
Max. Phase Advance (R1FH) = 0
Velocity Timer (R19H) = 0

Application brief M012 describes the commutator operation in detail.

The hardware connections required for the stepper motor interface are shown in the schematic in Figure 3. For details on mounting a 3 channel encoder on a stepper motor for closed loop control please refer to the data sheet for the HCTL-1100.

*A1A2 means that positive direction of current flow is from the A1 terminal to the A2 terminal.

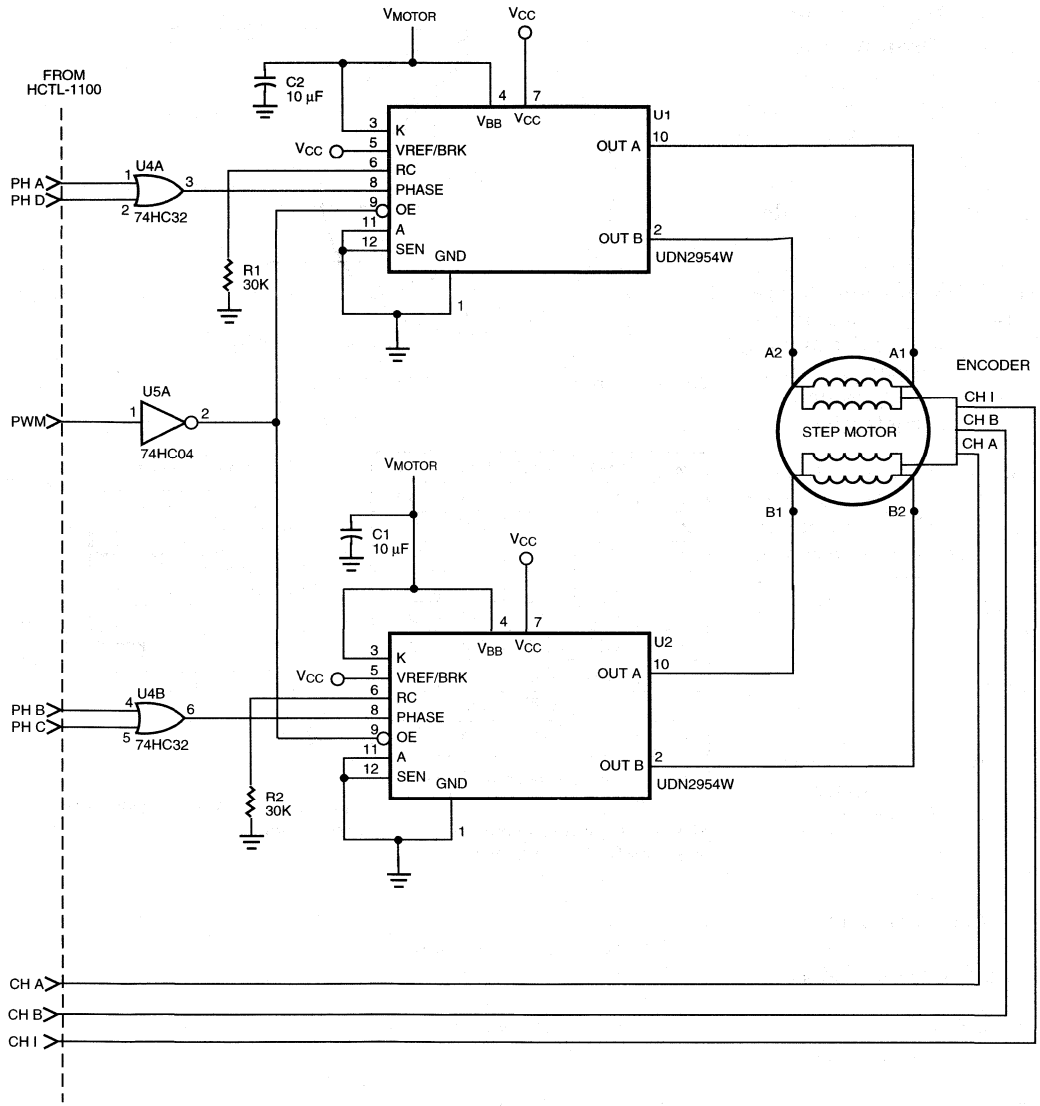


Figure 3. Stepper Interface Schematic.

Using the HCTL-1000/ 1100 with Step Motors: The Half-Step Sequence

The HCTL-1000 and HCTL-1100 can be used to commutate a step motor in half-step mode. In the half-step movement, the rotor moves half of its normal angle per step. For example, a 200 step per revolution (1.8° per step) motor would become a 400 step per revolution (0.9° per step) motor. Besides providing twice as many detent positions per revolution, half stepping also provides smoother running torque.

The commutator of the HCTL-1000/1100 can be programmed to generate a half-step switching sequence. The phase overlap feature of the commutator is used to generate the necessary logic sequence.

Example:

Motor: PM Step Motor
200 steps/rev, 1.8°/step
50 torque cycles/rev
(see Figure 4)

Encoder:
500 CPR
2000 quad counts

Full Step Sequence: 4 steps

Half-Step Sequence:
8 steps (see Figure 5)

Programming the HCTL-1000/1100:

Status Register:
Bit #1 = 1 4 phase config.
Bit #2 = 0 Rotor position measured in quad counts

Ring:
(2000 qd. cts.) / (50 torque cyc.) = 40 qd. cts./torque cyc.

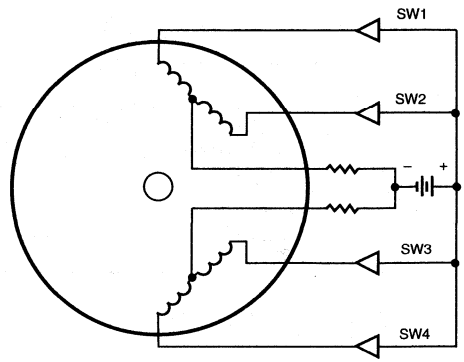


Figure 4. Permanent Magnet (PM) Step Motor.

Step	SW1	SW2	SW3	SW4
1	On	Off	On	Off
2	On	Off	Off	Off
3	On	Off	Off	On
4	Off	Off	Off	On
5	Off	On	Off	On
6	Off	On	Off	Off
7	Off	On	On	Off
8	Off	Off	On	Off
1	On	Off	On	Off

Note: To step in the opposite direction, the sequence is 1-8-7-6-5-4-3-2-1.

Figure 5. Eight-Step Switching Sequence for Half-Stepping.

X, Y:
Program for 50% overlap,
X = Y

X + Y = (Ring)/(# of phases)
= 40/4 = 10

X + Y = 10, X = Y

So X = 5, Y = 5

The resultant output from the HCTL-1000/1100 commutator is shown in Figure 6. By connecting PH A to SW1, PH B to SW4, PH C to SW2, and PH D to SW3, the eight-step half stepping sequence is achieved.

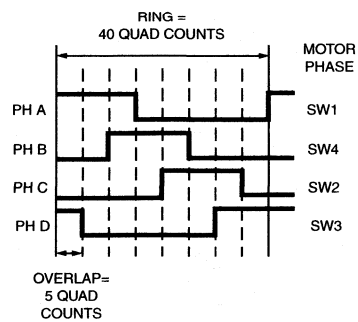


Figure 6. HCTL-1000/1100 Commutator Output.

Encoder Questions and Answers

Application Brief M-101

Introduction

This guide answers the most often-asked questions about encoders in general and Hewlett-Packard encoders in particular. It is organized into the following sections:

- General Encoding
- Output Waveforms
- Resolution
- Mounting
- Materials
- Reliability
- Electrical
- Miscellaneous

General Encoding

Question 1.
What is an encoder?

Answer. An encoder is a sensor of mechanical motion. It translates motion (such as position, velocity, and acceleration) into electrical signals.

Question 2. What kinds of encoders are available?

Answer. The three basic types of encoders are contact (also called resistive or potentiometers), magnetic, and optical. Contact encoders use either a wiper which picks off a voltage corresponding to its position, or has a brush or series of brushes which wipe along a codewheel with an alternating conductor/insulator pattern. The pattern of insulator and conductor corresponds to mechanical position. Magnetic encoders sense a magnetic field which changes according to mechanical position. Examples of magnetic encoders include synchros, resolvers, and Hall effect sensors. Optical encoders have a light source which shines through or reflects off a codewheel or codestrip to a photodetector. The photodetector sees a pattern of light and dark which corresponds to the mechanical position.

Encoders generate either analog or digital output signals. An analog encoder may put out a voltage or a series of voltages corresponding to position, velocity, etc. A digital encoder puts out signals which represent a binary 1 or 0 (logic level high or low). The coding of the 1's and 0's determines the position.

Question 3.
What is the difference between an absolute and an incremental encoder?

Answer. Absolute encoders have a unique value (voltage, binary count) for each mechanical position and thus the position is known "absolutely". At power up, the position of an absolute encoder is known. Incremental encoders have output signals which repeat over the range of motion and thus each mechanical position is not uniquely defined. The current position sensed is only incremental from the last position sensed. Thus at power up, the position of an incremental encoder is not known since the output signals are not unique to any singular position. Count and direction information can be obtained from both absolute and incremental encoders.

Question 4.
What is a channel?

Answer. A channel is an electrical output signal from an encoder. Typical high performance incremental encoders have either two or three channels.

Question 5. What is quadrature?

Answer. All HP encoders have channels A and B which output identical repeating square waves as motion occurs. Channel A is offset from channel B by half of a

high pulse of the square wave on either channel. Quadrature is the offset relationship between channel A and channel B.

Question 6. What is meant by 4X decoding?

Answer. The rising edge to rising edge (called the Cycle) on either channel A or B signifies that one window and bar pair of the codewheel has rotated by the photodetector array. Because A and B are in quadrature, four unique logic states are defined for each window and bar pair that mechanically passes. When these four unique logic states are decoded, the resolution obtained is 4 times (4X) the resolution of the codewheel. Thus a codewheel with 500 window and bar pairs can be decoded into 2000 quadrature states. See Figure 1 for more details.

Question 7. What is an index pulse?

Answer. An index pulse occurs on a third channel called channel I. A pulse occurs on this channel once for each full revolution of the codewheel. Essentially, this pulse marks a singular position of the codewheel. This is an absolute reference added to an incremental encoder.

Question 8. Of Cycle, Pulse Width, and State Width, which is the most consistent?

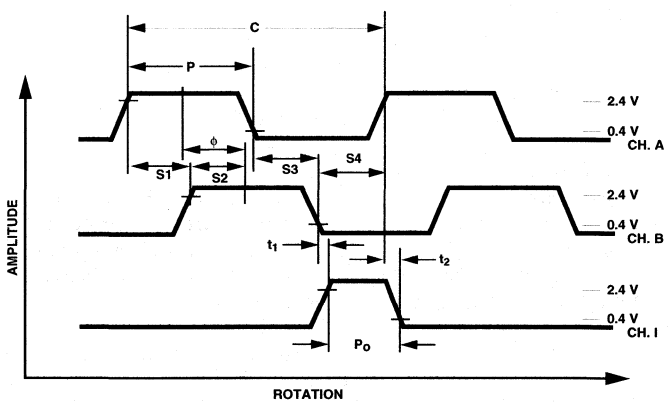
Answer. Cycle is the most consistent. If you are trying to measure velocity by timing between edges, use the rising to rising (or falling to falling) on either channel A or B. Pulse width and state width are not as consistent.

Question 9. What other terms are used within the industry to describe output waveforms?

Answer. Other terms in the industry include:
Phase: rising edge on A to rising edge on B. (This is equivalent to HP's State 1 width. HP defines phase as the center of the high state on A to the center of the high state on B.)
Flutter: variation from cycle to adjacent cycle.
Duty Jitter, Waterfall: variation from pulse width to adjacent pulse width.
Symmetry: ratio between pulse high and pulse low (nominally unity).
Edge to Edge Variation, Edge Separation, Phase Error: equivalent to State Width Error.
Phase Jitter: variation from rising edge on A to rising edge on B.

Question 10. Do HP encoders provide analog outputs (sinusoidal or quasi-sinusoidal signals)?

Answer. No. HP encoders provide only digital incremental output waveforms.



C = CYCLE (1 WINDOW AND BAR PAIR, 360°e)
S1 . . . S4 = LOGIC STATE WIDTH (4 STATES PER WINDOW AND BAR PAIR, EACH STATE IS 90°e)
P = PULSE WIDTH (RISING TO FALLING ON CH. A OR B, 180°e)
CH. I = INDEX CHANNEL (ONE PULSE PER FULL CODEWHEEL REVOLUTION)

Figure 1. Output Waveforms.

Resolution

Question 11. How does HP define resolution?

Answer. We typically talk in terms of line density, which is the number of window and bar pairs per unit length. Line density is expressed either as lines per inch (LPin) or lines per mm (LPmm). For a rotary encoder, the line density is given by:

$$\text{LPin (LPmm)} = \frac{\text{Counts per Revolution}}{(2\,\pi)\,(\text{Rop})}$$

This gives the number of window and bar pairs per unit arc length at a given optical radius (Rop).

For linear encoder modules, the resolution is the number of window and bar pairs per unit of linear length.

Alternative to line density is the counts per revolution (CPR) with a specified optical radius (for rotary encoders).

Question 12. What are the minimum and maximum resolutions available with HP encoder modules?

Answer. HP can make encoder modules with resolutions from 30 LPin to 360 LPin (1.18 LPmm to 14.17 LPmm).

Question 13. How can I get a rotary encoder resolution that is not one of the standard resolutions?

Answer. Custom resolutions can be obtained by one of two ways. One way is to use a standard encoder module and design a custom codewheel. The line density of the module and the codewheel must match, but the optical radius can be varied to make a larger or smaller diameter codewheel which has a custom number of window and bar pairs.

Example: Customer wants 220 CPR encoder, which is between HEDS-9100 standard resolutions of 200 CPR and 256 CPR.

Steps:

a.) Use HEDS-9100 #E00 (200 CPR at 11.00 mm Rop, LPmm = 2.89 lines/mm).

b.) Match the LPmm of the module with the LPmm of the new codewheel and solve for a new optical radius:

$$LPmm = \frac{CPR}{(2\pi)(Rop)} \rightarrow Rop = \frac{CPR}{(2\pi)(LPmm)}$$

$$Rop = \frac{220\ CPR}{(2\pi)(2.89\ lines/mm)} = 12.1\ mm$$

Thus the custom codewheel will be slightly larger than the standard codewheel to accommodate 20 extra window and bar pairs (Rop = 12.1 mm vs. Rop = 11.00 mm) but have the same line density. The modules are robust enough to handle the difference in optical radius.

The other way to get a custom resolution is to have HP make a custom photodetector IC with the desired custom resolution. A custom codewheel is still required to work with the custom IC. Contact your local HP sales representative for more information.

Question 14. Will any codewheel work with any encoder module?

Answer. No. The line densities of the module and codewheel must match. Thus a 200 LPin module will not work with a 120 LPin module.

Question 15. How closely does the line density of the codewheel or codestrip have to match the line density of the module?

Answer. For modules with less than 200 LPI resolution, a general rule of thumb is that the line densities must match within 5 lines/inch for the module to function (0.2 lines/mm). Encoding performance degrades with mismatch and thus HP cannot guarantee encoding specifications when significant mismatch occurs.

Question 16. Can I use an encoder module to detect the presence or absence of an object?

Answer. No. The module is looking for a certain light/dark pattern. The passing of an opaque or transparent material past the photodetector array may or may not cause a transition on either channel. The result is not predictable.

Mounting

Question 17. How are the encoder module mounting tolerances referenced?

Answer. For the HEDS-9000, 9100, and 9200 series encoder modules, the tolerances are referenced from the centers of the aligning recesses. For the HEDS-9700 series modules, the tolerances are referenced from the aligning post on the underside of the module.

Question 18. Three channel encoders and modules require use of an alignment tool or other aligning aid. Do you need an alignment tool for two channel encoders and modules?

Answer. With the exception of the HEDS-9000/9100 Extended Resolution Series, alignment aids are not required. However, using alignment aids will result in better performance and are recommended. The Extended Resolution modules, which are the HEDS-9000 Options T and U and the HEDS-9100 Options B and J, do require the use of alignment aids. In some cases, alignment aids can also improve assembly times.

Question 19. Can adhesives be used instead of screws?

Answer. Yes. A common adhesive used is RTV, made by GE or Dow Corning (GE 162, Dow Corning 3145) among others.

Question 20. What is meant by "artwork side of codewheel?"

Answer. The artwork side only refers to codewheels that are made of glass or mylar (plastic). On these codewheels, the "art" or window/bar pattern appears only on one side. Generally, it is better to have the artwork side closer to the photodetector array to cast a cleaner, sharper shadow. With metal codewheels, both sides are equivalent since the window is an absence of material. The artwork side does not apply here.

Question 21. How will the gap between the codewheel and the detector side of the encoder module affect the output?

Answer. In general, HP encoders are not that sensitive to the codewheel gap. This is because the lens collimates the LED light into a parallel beam and keeps the light/dark pattern fairly uniform. However, as the codewheel gets closer to the detector, the shadows cast by the codewheel get cleaner and sharper. This results in better light/dark contrast and subsequently somewhat better performance.

Question 22. Does HP provide mounting screws?

Answer. No.

Question 23. What is TIR?

Answer. TIR stands for Total Indicated Runout and is the total movement that the codewheel window/bar pattern will have in a radial direction. Thus it is the total eccentricity of the codewheel. The factors which contribute to TIR are:

- Shaft eccentricity
- Shaft undersize relative to hub
- Off-center placement of hub relative to codewheel
- Shaft radial play due to bearing tolerance and uneven loading

TIR contributes directly to the cycle error and position error of the encoder.

Question 24. Can HP bend the leads of the encoder modules?

Answer. Yes. The standard part numbers are HEDS-9001 (an HEDS-9000 with bent leads), HEDS-9101, HEDS-9041, HEDS-9141, HEDS-9701, and HEDS-9721.

Question 25. How do you remove an HEDS-5500 series encoder?

Answer. The HEDS-5500 series encoders were not designed to be removed. However, it is possible to do so if done carefully. The procedure to remove one is essentially the assembly procedure in reverse. The steps are as follows:

a.) Turn the encoder cap from the two-dot position to the one-dot position.
b.) Insert hex wrench into side hole by the one-dot mark.
c.) Push down on the hex wrench, and rotate the shaft slowly until you feel the setscrew. Insert wrench into hole and loosen setscrew. (This may take more than one attempt.)
d.) *Carefully* unsnap the encoder housing from the encoder baseplate. Gently lift the encoder housing up off the shaft. If the housing is pulled off too quickly, the codewheel may be damaged.
e.) Remove baseplate screws.

Question 26. In the HEDS-5500 series assembly procedure, Step 4 calls for using the screwdriver slot to turn the encoder cap from the one-dot position to the two-dot position. If the encoder has an optional through-hole with no screwdriver slot, how do you turn from the one-dot to the two-dot positon?

Answer. Insert the hex wrench into one of the two side slots on the top of the encoder housing and rotate clockwise from the one-dot to the two-dot positon.

Materials

Question 27. What is the material of the encoder module housing?

Answer. For the HEDS-90XX/91XX/92XX, the material is Ryton R-4, a polyphenylene sulfide which contains 40% glass fiber. For the HEDS-9700 series, the housing material is a 30% glass-

filled polyester with the trade name of Valox.

Question 28. What is the material of the HEDS-5500 series housing?

Answer. The HEDS-5500 series housing is also made of Valox.

Question 29. What is the lens made of?

Answer. The lens is polycarbonate.

Question 30. What are the codewheels made of?

Answer. Codewheels are made either of nickel, nickel-plated copper, or stainless steel. The hubs are made of aluminum. The codewheel setscrew is made of black anodized high-carbon steel.

Reliability

Question 31. Is there a reliability data sheet for HP encoders?

Answer. Yes, reliability data sheets are available for the HEDS-9000, HEDS-9100, HEDS-9200, HEDS-5500, HEDS-5000, and HEDS-6000 series encoders and encoder modules.

Question 32. Will HP encoders work in a vacuum?

Answer. Our encoders are not characterized nor were they intended to work in a vacuum. Customers have tried with varying amounts of success.

Question 33. Will HP encoders work in a radioactive environment?

Answer. Again, they were not characterized or intended for such conditions. Customers have tried this also, again with different amounts of success.

Question 34. Will HP encoders work in a fluid?

Answer. No. Fluids ruin the optics, potentially cause electrical problems, and, depending on the fluid, may destroy the materials of the encoder.

Question 35. How well do HP encoders work in a dusty environment?

Answer. HP encoders are fairly robust to dusty environments. The encoders look at multiple sets of window and bar pairs. Thus a speck of dust at any one window will be averaged out by the other sets of windows and bars. Because of this averaging effect, a number of windows can be covered completely and the module will still not lose a count.

Question 36. What solvents can be used to clean in the vicinity of the encoder modules?

Answer. HP has found that almost all solvents (besides water) will attack some part of the encoder module. This includes alcohols and freon-based cleaners. HP has not qualified any solvent to be compatible with the encoder modules.

Electrical

Question 37. What kind of output drives do HP encoders have?

Answer. HP encoders have a current source output of 125 microamps typical, 40 microamps minimum in the high state. The outputs can sink up to 3.2 mA under Recommended Operating Conditions (3.86 mA for three channel HEDS-9040/9140, HEDS-5540/5640).

Question 38. I am trying to drive a fairly long length of cable. What kind of additional circuitry should I consider?

Answer. For cable in the 6 to 10 foot range, pull-up resistors to +5 Volts on each output channel may suffice (3.3 K for two channel, 2.7 K for three channel). For longer lengths of cable, either a buffer or a line driver may be necessary.

Question 39. I am having some problems with noise affecting my encoder signals. What should I do?

Answer. There are several ways to improve noise immunity. Be careful to separate motor driver wires from encoder wires, and be sure to separate encoder channels from each other (i.e., do not twist CH A with CH B or CH I). Shielded twisted pair cable is recommended for encoder lines. Also, be sure to separate the ground lines of the motor/amplifier and the encoder since high current switching in the motor can cause noise in the encoder output lines.

Pull-up resistors help somewhat with noise rejection. Additional circuitry, such as line drivers/receivers and optocouplers, is much more effective in rejecting noise. In really noisy environments, additional circuitry may be the only way to totally eliminate a noise problem.

Question 40. Does HP provide line driver outputs?

Answer. Yes. HP has made available the HEDL-55XX/56XX encoders, which are HEDS-55XX/56XX encoders with a line driver board. This board uses an industry standard 26LS31 line driver IC. The line driver outputs are RS-422 compatible and provide complementary outputs on a 19 inch twisted pair ribbon cable. Both two and three channel encoders are available with the line driver option. Contact your local HP representative for further information.

Question 41. What is meant by "push-pull" circuitry?

Answer. In determining the output for Channel A, the encoder photodetector is looking for signals for A and its complement A'. These signals are sent to a comparator such that when A receives more light than A', Ch. A is high. If A' receives more light than A, Ch. A is low. This arrangement is called "push-pull" circuitry.

The advantage is that the Ch. A output is insensitive to variation in the LED light level since A and A' are affected equally by the light source. Channels B and I are configured similarly.

Question 42. Typically, how much current do the LED and photodetector IC draw?

Answer. In the two channel modules and encoders, the LED typically draws about 15 mA and the IC draws about 2 mA. In the three channel modules and encoders, the LED draws about 45 mA and the IC draws about 10 to 12 mA.

Miscellaneous

Question 43. Does HP provide codestrips?

Answer. Only as samples. HP does not sell codestrips, but we can provide a list of codestrip and codewheel vendors.

Question 44. How thick is an HP codewheel?

Answer. Codewheels are between 0.0007 inches (0.018 mm) and 0.003 inches (0.076 mm) in thickness.

Question 45. On the HEDS-9000/9100/9200 encoder modules, there are two metal straps on either side of the five pinouts. What are they for? Can they be cut or removed?

Answer. These are the Ground and V_{CC} lines which carry current to the LED light source. The pinouts, where the user connects Ground and V_{CC}, are on the detector side of the module. The "straps" carry current to the emitter side of the module. If these lines are cut, the LED will not light up and the module will obviously not function.

Question 46. What does "HEDS" stand for?

Answer. Hewlett-Packard Emitter Detector System

Incremental Encoder Errors: Causes and Methods to Reduce Them

Application Brief M-109

Introduction

Optical incremental encoders are an inexpensive, reliable, and accurate way to sense position or velocity. However, the acuracy of these devices depends on the mechanical, electrical, and optical properties of the fully assembled encoder. This paper examines the individual causes of error and ways that error can be reduced. Examples of actual encoder performance are provided. The methods for reducing error involve either features built into the encoder or correct assembly of the device. A list of performance features is provided for use when selecting an optical incremental encoder, as well as key considerations to be aware of when designing the device into the end system.

Optical incremental encoders are used to sense position and velocity in applications ranging from computer peripherals to industrial robotics to medical equipment. What makes these devices appealing to all industries are their high accuracy, low cost, high reliability, and ease of use.

The major considerations when using an optical incremental encoder are resolution and accuracy. The resolution is determined by the codewheel used with the encoder and by the method of decoding. The accuracy depends on a number of mechanical, optical, and electrical considerations. If the encoder design accounts for these considerations, high accuracy, repeatability, and small variation from encoder to encoder can be obtained.

Optical Encoder Basics

The basic components of an optical incremental encoder are a light source, a codewheel or codestrip, and a photodetector. (A codewheel is used to sense rotational movement while a codestrip is used to measure linear movement.) The codewheel has a pattern of windows and bars which either blocks light or allows light to pass through. In a slot interrupter configuration, the light source (typically an LED) shines through the codewheel and, as the codewheel rotates, an alternating pattern of light and dark is seen by the photodetector. In a reflective configuration, the light source reflects off the codewheel and is received by the photodetector. An alternating light/dark pattern is developed as light is reflected or not reflected by the codewheel.

Circuitry attached to the photodetector turns the light/dark pattern into electrical output signals. These signals repeat many times for each revolution of the codewheel. If the outputs are digital, the signals are square waves with logic high and logic low levels corresponding to light detected or not detected. The number of high or low pulses gives position information, and the rate of the pulses gives velocity information. If the outputs are analog, the signals are sinusoidal or quasi-sinusoidal waves corresponding to the amount of light detected.

Output Waveforms

Typical high performance encoders have two output signals (called "channels") which produce identical periodic waveforms. These signals are offset from each other in an arrangement called quadrature. In one direction of rotation, channel A leads channel B; in the other direction of rotation, channel B leads channel A. Quadrature provides direction information in addition to positional count information.

For digital outputs, these waveforms are identical repeating square waves. Because of the quadrature relationship, four

unique logic states are generated per window and bar pair. If each of these logic states is decoded and counted, the final resolution to the user is four times the resolution of the codewheel (called "4X" decoding). If the codewheel has 360 window and bar pairs, the signals can be decoded to 1440 quadrature states. This gives a final resolution of 1/4 of a mechanical degree. The user has a choice of whether to decode once, twice, or four times the codewheel resolution.

Figure 1 shows the typical two channel incremental encoder output waveforms. Below are some definitions associated with these waveforms.

Counts Per Revolution (CPR): The number of window and bar pairs per revolution.

Cycle (C): Length of time from rising edge to adjacent rising edge on either Channel A or Channel B, denoted as 360 electrical degrees (°e). This corresponds to the passing of one window and bar pair past the photodetector.

Pulse Width (P1, P2): Number of electrical degrees that a channel is high during a cycle. This is nominally 180 electrical degrees, or half of the cycle.

State Width (S1, S2, S3, S4): Number of electrical degrees between a transition on Channel A and the neighboring transition on Channel B. There are four states per cycle, each nominally 90 electrical degrees.

Phase (ϕ): Number of electrical degrees between the center of the high state on Channel A to the center of the high state on Channel B. The phase is typically 90 electrical degrees.

Position Error ($\Delta\theta$): The angular difference between the actual shaft position and the position indicated by the encoder cycle count. The position error is normalized about zero.

Optical Radius (Rop): The distance from the codewheel's center of rotation to the optical center of the encoder.

Cycle error, pulse width error, state width error, and phase error are simply the deviation of each parameter from their nominal value.

The accuracy of the encoder is a direct function of the waveform errors. Foremost is the position error, which is the difference between the actual shaft location and the location as determined by the encoder. Position error shows up in the waveforms as an integration of the cycle error. As the cycle error accumulates, the position error increases.

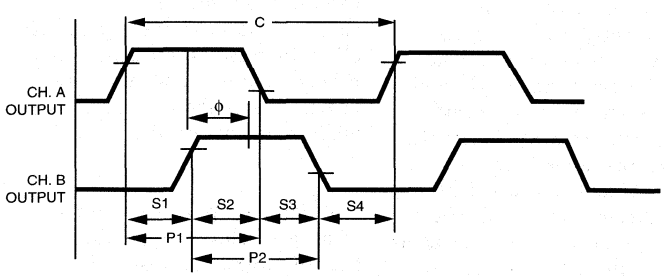


Figure 1. Digital Incremental Output Waveforms.

If decoding is done according to the state width (4X decoding), then state width error will also affect the accuracy. The three contributors to state width error are cycle error, phase error, and pulse width error. Cycle error results in state error because the rising edges on both channels are off of the nominal locations. Phase error results in state width error because the relationship between the two channels is off. Pulse width error results in state width error because the length of the high state is not equal to the length of the low state and thus the rising and falling edges are inconsistent with each other.

Causes of Encoder Error and Ways to Reduce Error

The accuracy of the waveforms depends on the optical, mechanical, and electrical design of the encoder. The design of the encoder and, at times, the system, can be optimized to provide more accurate and reliable performance. The factors that affect the output waveforms are:

- Variation in Light Level
- Codewheel Point Defects
- Mounting Misalignment
- Eccentricity
- Axial Play
- Frequency
- Mechanical Linkage Errors

Each of the individual causes is listed and described below.

Variation in Light Level: The simplest way to implement an optical encoder is to have a threshold level asssociated with the photodetector current. The current

is proportional to the amount of light received at the photodetector, and switching from logic low to high (or vice versa) occurs when the current crosses over the threshold. If there is some variation in the amount of light received, then the crossing points on the threshold level are going to vary as well. This leads to non-uniformity in the output waveforms, most notably in the pulse width and the state width.

The light level may vary in a single part over time and temperature. LED light sources degrade over years of use and experience reduced light output. LED light output is also affected by increases or decreases in temperature. In addition, the amount of light seen by the photodetector is affected by the opacity and transmissivity of the codewheel. Codewheels constructed from mylar or glass may not have perfectly opaque bars or perfectly transparent windows.

It is also difficult to maintain uniformity over a large number of LEDs. LEDs vary in intensity even with tight production controls. Thus it is difficult to set a photocurrent threshold that will provide consistent waveforms from part to part. Some adjustment in the final assembly process, such as determining the resistance of a current-limiting potentiometer, may be required.

Figure 2 demonstrates the effect of light level variation. It shows the square wave outputs from a slot interrupter with an open-collector threshold circuit. (When the phototransistor is exposed to light, the output is low). In Figure 2(a), the LED light source is driven at 8.1 mA and the resulting pulse width error is $\Delta P = +12°e$. In Figure 2(b), the LED light source was driven at 17 mA with a pulse width error of $\Delta P = -54°e$. The threshold circuit shows a large change in pulse width for the change in LED current.

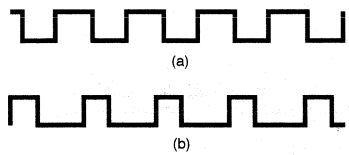


Figure 2. Waveforms of slot interrupter with threshold circuitry: (a) LED current is 8.1 mA. (b) LED current is 17.0 mA.

"Push-pull" or differential circuitry eliminates the sensitivity to variations of light level [1]. In a push-pull system, Channel A is determined from two separate signals, A and its complement, A'. When the detector generating the A signal is exposed to the light source by a codewheel window, A' is blocked by a codewheel bar and vice versa. The switching from logic low to high occurs when the A signal goes above A'; high to low occurs when A' goes above A.

If the light level varies for any of the reasons mentioned above, both A and A' are affected equally (assuming close proximity of the separate detectors) and the switching points remain the same. The same technique is used to generate the Channel B output. In actual tests, an HP HEDS-9100 series module with the LED driven at 15 mA and at 30 mA had a pulse width difference of less than 1 °e.

Codewheel Point Defects:
The quality of the codewheel is a critical factor in an encoder's performance. Seemingly small imperfections in a codewheel's window/bar pattern can significantly degrade the performance of a high resolution encoder. Imperfections may arise from defects in production or simply from the appearance of dust or dirt at a codewheel window. It is typical to see a housing around an encoder to protect it from particles and other potential harm.

If the encoder is designed with only a single photodiode per output channel, then a defect at any window or bar will cause an error at the output. If, for example, a window is completely covered with dust, a pulse will be missed altogether. An encoder with multiple photodiodes per output channel will average out the effects at any one window or bar. If there are ten photodetectors that contribute to Channel A, then an imperfection at any one window or bar constitutes only 10% of the overall signal. Error will result, but the pulse train will be maintained.

Figure 3(a) shows the output from a slot interrupter encoder with a single phototransistor looking at one window or bar. A single window was covered with opaque material resulting in a missed count. Figure 3(b) shows the cycle error over the full rotation of a 500 CPR encoder which looks at 13 window and bar pairs simultaneously. A section of five consecutive codewheel windows were covered with opaque material. Although there was a discontinuity when the opaque material passed by the detectors, all electrical cycles were maintained. The cycle error increased in the covered section from $\Delta C = 2°e$ to $\Delta C = 6°e$. A small error resulted, but the quadrature relationship was not lost. Even though the codewheel had only 495 windows, 500 cycles were counted.

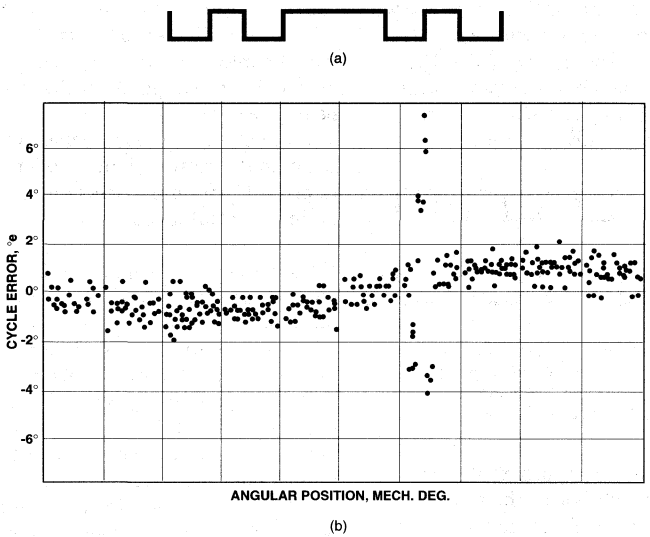


Figure 3. (a) Output of Slot Interrupter with Single Phototransistor and 1 Codewheel Window Covered. (b) HEDS-9100 Plot of Cycle Error vs. Angular Position. Detector Array Looks at 13 Sets of Windows and Bars. Five Codewheel Windows Were Covered.

Mounting Misalignment

Consider two detectors, one for channel A and one for channel B, separated by a distance S. These detectors are centered on the optical radius (Rop) and offset by (N + 1/4) cycles where N is an integer. Assuming perfect alignment and a good codewheel, channels A and B will nominally be 90 electrical degrees out of phase.

Now consider a misalignment d between the codewheel and the detectors in the radial direction from the shaft center as shown in Figure 4. As the codewheel rotates in the direction shown, the channel A detector sees each window/bar edge earlier than if at the desired location. Likewise, the channel B detector sees each window/bar edge later than if at the desired location. This results in a phase error in the offset relationship between the two channels. The phase error is given by the following equation[2]:

$$\Delta\phi = \frac{(d)\,(S)\,(CPR)}{(Rop)^2}\ \frac{(360)}{(2\pi)}\ \text{elec. deg.} \qquad (1)$$

The dependency of the error on the separation distance between the detectors is evident here. Thus it is better to design an encoder with a smaller distance S between the detectors so that the encoder will be more tolerant to the misalignment d.

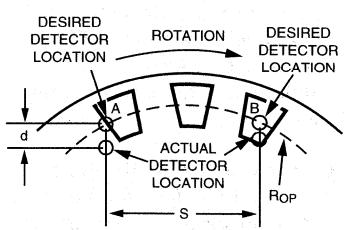


Figure 4. Radial Misalignment of Channel A and B Detectors.

Figures 5(a) and 5(b) show the misalignment effect on an HP HEDS-5000 series encoder with 500 CPR at Rop = 11.00 mm. In Figure 5(a), the encoder is placed at its nominal location with an average phase error $\Delta\phi$ = 0.4 °e. In Figure 5(b), the encoder is misaligned in the radial direction by d = 0.076 mm (0.003 in.). An average phase error of $\Delta\phi$ = 38.7°e resulted. With the separation of the channel A and B detectors S = 2.1 mm, the predicted phase error from equation (1) is 37.9 °e.

Figures 6(a) and 6(b) show the misalignment insensitivity of an HP HEDS-9100 encoder module used with the same 500 CPR codewheel at Rop = 11.00 mm. The separation of the channel A and B detectors is 0.034 mm. In Figure 6(a), the encoder module is placed at its nominal location with an average phase error of $\Delta\phi$ = -2.8 °e. In Figure 6(b), the encoder module is misaligned in the radial direction by d = 0.076 mm (0.003 in.) as in the previous example. The resulting phase error was $\Delta\phi$ = -2.7 °e, virtually no different than in Figure 6(a). The predicted phase error from equation (1) is $\Delta\phi$ = 0.6 °e.

A misalignment in the direction tangential to the shaft center will not result in any phase error. Transitions on channel A may be early or late, but the transitions on channel B will be identical. The only restriction on tangential misalignment is to not be so great so as to actually lose the output waveforms.

Eccentricity

Eccentricity is the total cyclic off-axis motion of the codewheel. Several factors contribute to eccentricity:

- Shaft eccentricity

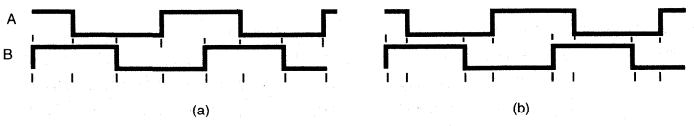


Figure 5. HEDS-5000 ch. A and B waveforms. (a) Nominal Radial Alignment, ΔΦ = 0.4 °e. (b) Radial Misalignment of 0.076 mm (0.003 in.), ΔΦ = 38.7 °e.

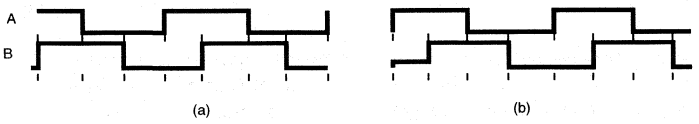


Figure 6. HEDS-9100 ch. A and B waveforms. (a) Nominal Radial Alignment, ΔΦ = -2.8 °e. (b) Radial Misalignment of 0.076 mm (0.003 in.), ΔΦ = -2.7 °e.

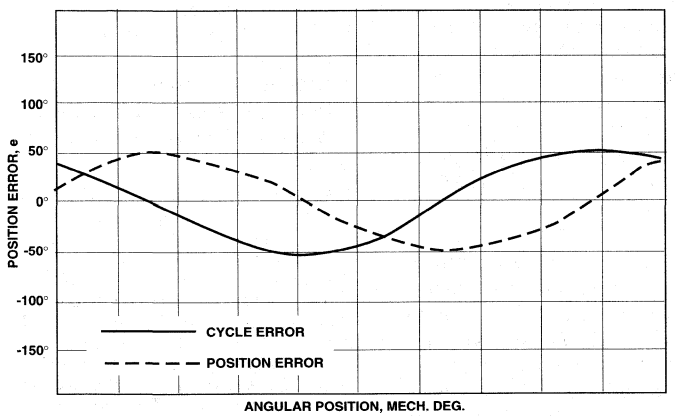


Figure 7. Position error as a function of angular position over one full codewheel rotation.

- Radial play (from bearing tolerances or uneven loading)
- Shaft undersize tolerance (relative to codewheel)
- Codewheel/hub assembly misalignment

The eccentricity is a function of the rotational angle θ. Some amount of eccentricity e (q) at the detectors looks like a radial misalignment. Thus eccentricity will cause a phase error described in equation (1) with the value e (θ) substituted for d. In addition, a cycle error ΔC will result and is calculated as:

$$\Delta C = \frac{e}{\text{max. Rop}} (360°e), \quad \text{for } e << \text{Rop} \qquad (2)$$

The accuracy of the encoder in terms of detecting the true shaft position is affected by the cycle error.

Position error is the accumulation of the cycle error, so as the cycle error builds up, the error between the detected and actual shaft position increases. Figure 7 shows a graph of position error vs. rotation for a full revolution of the codewheel. The position error is shown to be sinusoidal with respect to the angular position.

Frequency

Every transition in state has an associated rise or fall time. Rise and fall times are characteristic of the electronic circuitry used to produce these outputs. Rise times may or may not be equal to fall times, and the difference between the two becomes accentuated as the frequency of the channel A and B square waves increases. This may lead to significant error in the output.

At a frequency f with a logic level switching rise time t_r and a fall time t_f, a pulse width error ΔP results and is given by:

$$\Delta P = (t_r - t_f)\,(f)\,(360°e) \qquad (3)$$

For instance, if f = 10 kHz, t_r = 300 ns and t_f = 50 ns, the pulse width error is 0.9 electrical degrees. Given the same t_r and t_f at a frequency of 100 kHz, the pulse width error is 9 electrical degrees. At very high frequency, the quadrature relationship between Channel A and B can be lost. Figure 8 shows a channel A encoder output at 60 kHz with significant pulse width error due to a rise time which is substantially longer than the fall time.

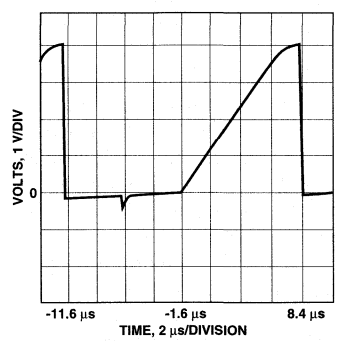


Figure 8. 60 kHz Channel A encoder Waveform with no Pull-up Resistor.

Rise times can be improved with additional circuitry. Pull-up resistors on the outputs can help significantly (the encoder in Figure 8 had no pull-up resistors). Where long cables are being used, a line driver/receiver pair such as the 26LS31/32 may be required which has fast and nearly uniform rise and fall times.

Axial Positioning and Play. The codewheel rotates in the gap between the light source and the photodetector circuitry. The position of the codewheel in this gap can potentially affect the output waveforms. This positioning is in the axial direction of the shaft.

With just a single photodetector per output channel and an unlensed light source, the codewheel gap greatly affects the output. The closer the codewheel is positioned to the light source, the greater the spread of light is on the detector. Thus the "on" time of the detector lengthens as the codewheel gets closer to the light source. This leads to errors in pulse width.

A lens placed over the light source can collimate the light into a parallel beam. The dependence of the geometric spread of light is eliminated. Hence, the codewheel gap is lessened as a contribution to error.

Even with a lens, it is still more desirable to have the codewheel closer to the detector. Shadows are not as well-defined the further away the codewheel is from the detector. A clean, sharp-contrast shadow results in more uniform output waveforms.

Mechanical Linkage Errors. A common use of a motor is to drive an object or platform in a linear direction. Some common examples are industrial X-Y stages, printer head movement, and conveyor belts. This necessitates a transmission from the rotary motion of the motor to the end linear motion. Belts, gears, and ballscrews are common apparatus for such applications.

If the optical encoder is placed at the motor, then any positioning errors due to mechanical linkages will not get detected. Gears and ballscrews have backlash, and belts stretch and slip. The encoder senses the rotational position of the motor, not the linear end movement. This is a situation where it may be wise to use a linear encoder at the output. Sensing the true end motion is important for maintaining good closed-loop control.

If the transmission from rotary to linear motion is precise, then placing the encoder at the motor may provide a significant advantage in resolution. For instance, a preloaded ballscrew with a pitch of 0.197 in./revolution (5 mm/rev) and a 1000 CPR encoder provides 5080 counts per inch (counts per 25.4 mm). With 4X decode from quadrature, the resolution is 20,320 logic states per inch of linear travel. A linear encoder with the same line density (number of window/bar pairs per unit length) as the 1000 CPR encoder may have a resolution an order of magnitude less. Thus a tradeoff exists between a higher resolution with transmission error or lower resolution with direct measurement of the position. If the transmission error is significant relative to the resolution, then no advantage is gained by using a rotary encoder at the motor.

Summary

This paper has shown that the accuracy of an optical incremental encoder depends on the mechanical, optical, and electrical design. A well-designed encoder has some or all of the following attributes:

- Push-pull detector circuitry
- Multiple sets of photodiodes per channel
- Small separation between channel A and B detectors
- Collimating lens

The effects that are outside the design of the encoder's light source and detector are:

- The total eccentricity of the codewheel
- External electronic circuitry (pull-up resistors, line drivers)
- Errors in the mechanical linkage

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4. H. Epstein, M. Leonard, and J. Uebbing, "An Incremental Optical Shaft Encoder Kit with Integrated Optoelectronics," Hewlett-Packard Journal, Vol. 32, no. 10, October 1981, pp. 10-15.
5. "Design and Operational Considerations for the HEDS-5000 and HEDS-6000 Incremental Shaft Encoders," *Hewlett-Packard Application Note 1011,* December 1983.

Applications

The following abstracts represent application notes that are not published in this catalog. These application notes can be obtained from your local Hewlett-Packard sales office or authorized HP distributor or representative (see section 5).

AN1011
Design and Operational Considerations for the HEDS-5000 Incremental Shaft Encoder

This application note is directed toward the system designer using the HEDS-5000 and HEDS-6000 modular incremental shaft encoders. First the note briefly analyzes the theory of design and operation of the HEDS-5000 and HEDS-6000. A practical approach to design considerations and an error analysis provide an in depth treatment of the relationship between motor mechanical parameter and encoding error accumulation. Several design examples demonstrate the analysis techniques presented. Operation considerations for assembly, test, trouble shooting and repair are presented. Finally, some circuits and software concepts are introduced which will be useful in interfacing the shaft encoder to a digital or microprocessor based system. Appendix A summarizes the uses and advantages of various encoder technologies while Appendix B provides guidance for selecting DC motors suitable for use with the HEDS-5000 and HEDS-6000

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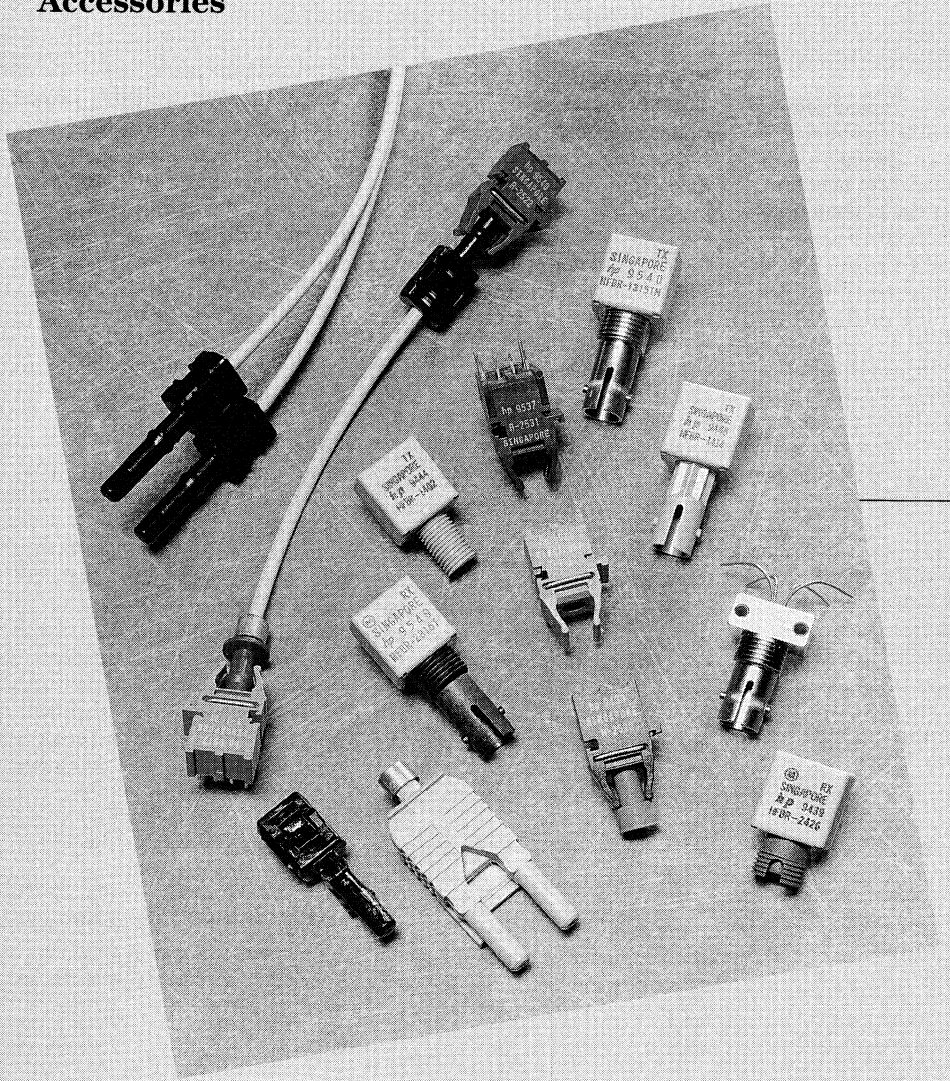

Fiber Optics

Introduction

Optical fiber as a transmission medium is gaining acceptance in many areas of technology because of its inherent benefits over copper media, and continuing efforts to reduce the cost of fiber optic links are making them cost competitive with wire assemblies.

In the market for factory automation and industrial control, fiber-optic link assemblies have been found to be cost-comparative with typical grades of twisted pair and coax cable.

Furthermore, fiber provides other advantages to wire such as voltage isolation and electromagnetic immunity, which are common problems in industrial environments.

Benefits of Optical Fiber over Copper Wire

For industrial applications, many problems arise when using copper wire assemblies which can be eliminated with fiber-optic cable. The following is a list of benefits a fiber optic link assembly will provide:

Electromagnetic Immunity/ Transmission

Copper transmission media are susceptible to electromagnetic fields and emit EM noise (which may interfere with other instrumentation.) Fiber optic links neither emit nor receive these signals. Because there is no crosstalk between lines, the signal is clearer and bit error rate (BER) is reduced.

Voltage Isolation

While optocouplers will often isolate high voltage interfaces from delicate CMOS circuitry up to 600 Volts, fiber is needed for higher voltages. Fiber also is used for isolation in longer distance links between equipment where ground loop problems may occur due to differences in potential. Furthermore, fiber provides voltage isolation to the operator and eliminates the risk of I/O board destruction due to a lightning strike or power surge.

Data Rate/Distance

While copper links perform well at low data rates for industrial applications, some control applications may require higher data rates and longer distances. For instance, a factory PLC might run on an ethernet LAN (20 MBd). At this data rate, category 5 UTP limits the distance obtainable to 185 meters, but with Spectran's HCS® (hard clad silica) fiber and 650 nm LED technology, the link can run up to 1 kilometer. If you need even longer distance, 62.5 µm core, graded-index glass fiber and low-cost 820 nm LED technology will run the link up to 2.7 kilometers.

Ease of Handling

Many people have the misconception that fiber is a lot harder to use than wire. In reality, fiber is actually easier to handle. First of all, fiber is a lot lighter than wire, that's a big deal to the workers doing the installation. Also, the bend radius of fiber is tighter than that of wire, giving more flexiblity. These benefits, along with the distance you can achieve with fiber, give the installer a lot of choices. Different rooms, different floors, even different buildings can easily be linked with fiber- optic cable.

Details of Industrial Fiber

A fiber-optic link assembly consists of an LED transmitter, a

PIN photodiode receiver, fiber optic cable and connectors, and related circuitry, integrated or discrete. The LED transmitter has a lens designed to efficiently couple light into the specific fiber you are using. The wavelength of the LED also is optimized for the fiber. Different fibers may give you different data rates and distances, so it is important to choose carefully which fiber to use in order to achieve required performance, while minimizing cost.

Fortunately, for the industrial market, data rates and distances tend to be low compared to the LAN market. Therefore, industrial customers are able to use the lowest cost fiber link available to meet their specifications. The fiber-optic links typically used in these applications fall in the 650 to 665 nm wavelength spectrum, and operate over plastic, 1 mm diameter fiber.

The technology, design, and manufacturing techniques implemented by Hewlett Packard make their fiber-optic products efficient, durable and low cost. HP has been in the forefront of fiber-optic communications from the very beginning as the largest independent supplier of communication products in the world. We are committed to using our unique combination of in-house, high-technology development along with our high-volume manufacturing processes to meet all of your fiber-optic datacom and telecom needs for data rates from DC to gigabit speeds and distances from 0 to Long-haul telecommunications.*

*Please contact your local sales office for further information on HP's high-performance fiber-optic data communications and telecommunications products to meet any standard.

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Fiber Optic Link Selection Guide

dc to 10 MBd

(data taken from 0 to 70°C unless specified.)

Signal Rate	Distance 25°C	Distance	Transmitter	Receiver	Fiber Type	Wavelength (nm)	Eval. Kit	Page No.
40 kBd	120 m	110 m	HFBR-1523	HFBR-2523	Plastic	660		3-6
1 MBd	20 m	10 m	HFBR-1524	HFBR-2524	Plastic	660	HFBR-0501	3-6
1 MBd	55 m	45 m	HFBR-1522	HFBR-2522	Plastic	660		3-6
1 MBd	75 m	70 m	HFBR-1528	HFBR-2522	Plastic	650		3-6, 3-36
1 MBd	650 m	550 m	HFBR-1528	HFBR-2522	HCS	650		3-6, 3-36
2 MBd	35 m	32 m	HFBR-1602	HFBR-2602	Plastic	660		3-43
2 MBd	45 m	42 m	HFBR-1604	HFBR-2602	Plastic	660		3-43
5 MBd	30 m	20 m	HFBR-1521	HFBR-2521	Plastic	660		3-6
5 MBd	1400 m	1100 m	HFBR-14X2	HFBR-24X2	HCS	820		3-85
5 MBd	2400 m	1700 m	HFBR-14X4	HFBR-24X2	62.5/125 Glass	820	HFBR-04X0	3-85
10 MBd	60 m	55 m	HFBR-1528	HFBR-2528	Plastic	650	HFBR-0528	3-36
10 MBd	500 m	300 m	HFBR-1528	HFBR-2528	HCS	650		3-36

10 MBd to 175 MBd

(data taken from 0 to 70°C unless specified.)

Data Rate	Distance	Transmitter	Receiver	Fiber Type	Wavelength (nm)	Evaluation Kit	Page No.
20 MBd	2700 m	HFBR-14X4	HFBR-24X6	62.5/125 Glass	820	HFBR-0414, HFBR-0463	3-85
20 MBd	5000 m	HFBR-1312T	HFBR-2316T	62.5/125 Glass	1300	HFBR-0310	3-68
20 MBd	1000 m	HFBR-1527	HFBR-2526	HCS	650	HFBR-0527H	3-24
20 MBd	14 Km	HFBR-1315TM	HFBR-2315T	9/125 Glass	1300	–	3-75
32 MBd	75 m	HFBR-1527	HFBR-2526	Plastic	650	HFBR-0527P	3-24
32 MBd	700 m	HFBR-1527	HFBR-2526	HCS	650	HFBR-0527H	3-24
32 MBd	2200 m	HFBR-14X4	HFBR-24X6	62.5/125 Glass	820	HFBR-0414	3-85
32 MBd	3200 m	HFBR-1312T	HFBR-2316T	62.5/125 Glass	1300	HFBR-0310	3-68
51 MBd	1400 m	HFBR-14X4	HFBR-24X6	62.5/125 Glass	820	HFBR-0414	3-85
51 MBd	3200 m	HFBR-1312T	HFBR-2316T	62.5/125 Glass	1300	HFBR-0310	3-68
51 MBd	60 m	HFBR-1527	HFBR-2526	Plastic	650	HFBR-0527P	3-24
51 MBd	240 m	HFBR-1527	HFBR-2526	HCS	650	HFBR-0527H	3-24
125 MBd	50 m	HFBR-1527	HFBR-2526	Plastic	650	HFBR-0527P	3-24
125 MBd	100 m	HFBR-1527	HFBR-2526	HCS	650	HFBR-0527H	3-24
125 MBd	700 m	HFBR-14X4	HFBR-24X6	62.5/125 Glass	820	HFBR-0416	3-85
125 MBd	2800 m	HFBR-1312T	HFBR-2316T	62.5/125 Glass	1300	HFBR-0310	3-68
155 MBd	50 m	HFBR-1527	HFBR-2526	Plastic	650	HFBR-0527P	3-24
155 MBd	600 m	HFBR-14X4	HFBR-24X6	62.5/125 Glass	820	HFBR-0416	3-85
155 MBd	2700 m	HFBR-1312T	HFBR-2316T	62.5/125 Glass	1300	HFBR-0310	3-68
175 MBd	500 m	HFBR-14X4	HFBR-24X6	62.5/125 Glass	820	HFBR-0416	3-85
175 MBd	2000 m	HFBR-1312T	HFBR-2316T	62.5/125 Glass	1300	HFBR-0310	3-68

HFBR-RXXYYY	Plastic Optical Fiber/HCS Fiber Cable and Connectors for Versatile Link	3-49
HFBR-4531/4532	Crimpless Connectors for POF and Versatile Link	3-63

HEWLETT® PACKARD

Versatile Link
The Versatile Fiber Optic Connection

Technical Data

HFBR-0501 Series

Features

- **Low Cost Fiber Optic Components**
- **Enhanced Digital Links dc-5 MBd**
- **Extended Distance Links up to 120 m at 40 kBd**
- **Low Current Link: 6 mA Peak Supply Current**
- **Horizontal and Vertical Mounting**
- **Interlocking Feature**
- **High Noise Immunity**
- **Easy Connectoring Simplex, Duplex, and Latching Connectors**
- **Flame Retardant**
- **Transmitters Incorporate a 660 nm Red LED for Easy Visibility**
- **Compatible with Standard TTL Circuitry**

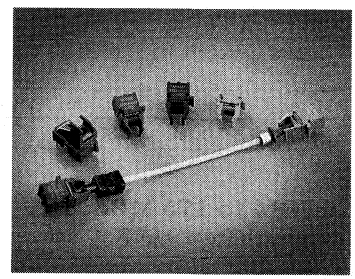
Applications

- **Reduction of Lightning/Voltage Transient Susceptibility**
- **Motor Controller Triggering**
- **Data Communications and Local Area Networks**
- **Electromagnetic Compatibility (EMC) for Regulated Systems: FCC, VDE, CSA, etc.**
- **Tempest-Secure Data Processing Equipment**
- **Isolation in Test and Measurement Instruments**
- **Error Free Signalling for Industrial and Manufacturing Equipment**
- **Automotive Communications and Control Networks**
- **Noise Immune Communication in Audio and Video Equipment**

Description

The Versatile Link series is a complete family of fiber optic link components for applications requiring a low cost solution. The HFBR-0501 series includes transmitters, receivers, connectors and cable specified for easy design. This series of components is ideal for solving problems with voltage isolation/insulation, EMI/RFI immunity or data security. The optical link design is simplified by the logic compatible receivers and complete specifications for each component. The key optical and electrical parameters of links configured with the HFBR-0501 family are fully guaranteed from 0° to 70°C.

A wide variety of package configurations and connectors provide the designer with numerous mechanical solutions to meet application requirements. The



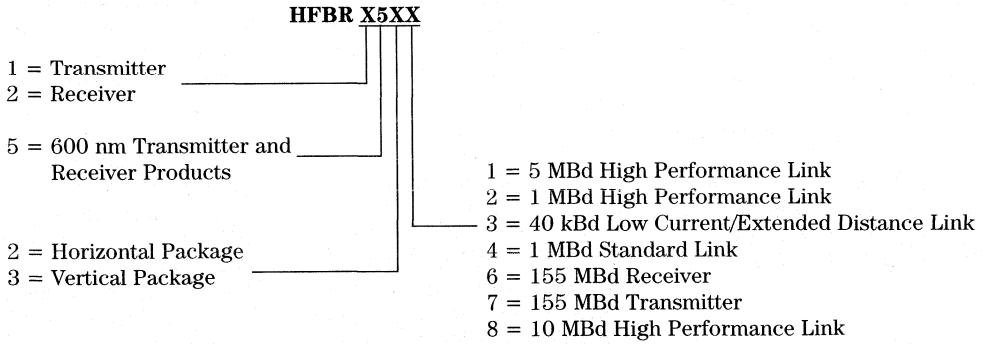
transmitter and receiver components have been designed for use in high volume/low cost assembly processes such as auto insertion and wave soldering.

Transmitters incorporate a 660 nm LED. Receivers include a monolithic dc coupled, digital IC receiver with open collector Schottky output transistor. An internal pullup resistor is available for use in the HFBR-25X1/2/4 receivers. A shield has been integrated into the receiver IC to provide additional, localized noise immunity.

Internal optics have been optimized for use with 1 mm diameter plastic optical fiber. Versatile Link specifications incorporate all connector interface losses. Therefore, optical calculations for common link applications are simplified.

5965-1657E

HFBR-0501 Series Part Number Guide



Link Selection Guide

(Links specified from 0 to 70°C, for plastic optical fiber unless specified.)

Signal Rate	Distance (m) 25°C	Distance (m)	Transmitter	Receiver
40 kBd	120	110	HFBR-1523	HFBR-2523
1 MBd	20	10	HFBR-1524	HFBR-2524
1 MBd	55	45	HFBR-1522	HFBR-2522
5 Mbd	30	20	HFBR-1521	HFBR-2521

Evaluation Kit

HFBR-0501 1 MBd Versatile Link:

This kit contains: HFBR-1524 Tx, HFBR-2524 Rx, polishing kit, 3 styles of plastic connectors, Bulkhead feedthrough, 5 meters of 1 mm diameter plastic cable, lapping film and grit paper, and HFBR-0501 data sheet.

Application Literature

Application Note 1035 (Versatile Link)

Package and Handling Information

The compact Versatilie Link package is made of a flame retardant VALOX® UL V-0 material (UL file # E121562) material and uses the same pad layout as a standard, eight pin dual-in-line package. Vertical and horizontal mountable parts are available. These low profile Versatile Link packages are stackable and are enclosed to provide a dust resistant seal. Snap action simplex, simplex latching, duplex, and duplex latching connectors are offered with simplex or duplex cables.

Package Orientation

Performance and pinouts for the vertical and horizontal packages are identical. To provide additional attachment support for the vertical Versatile Link housing, the designer has the option of using a self-tapping screw through a printed circuit board into a mounting hole at the bottom of the package. For most applications this is not necessary.

Package Housing Color

Versatile Link components and simplex connectors are color coded to eliminate confusion

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when making connections. Receivers are blue and transmitters are gray, except for the HFBR-15X3 transmitter, which is black.

All of the above transmitters and receivers are also available in black versions for applications where improved housing opacity is required due to very bright ambient light or bright flashes of light.

Handling

Versatile Link components are auto-insertable. When wave soldering is performed with Versatile Link components, the optical port plug should be left in to prevent contamination of the port. Water soluble fluxes, not rosin based fluxes, are recommended for use with Versatile Link components.

Versatile Link components are moisture sensitive devices and are shipped in a moisture sealed bag. If the components are exposed to air for an extended period of time, they may require a baking step before the soldering process. Refer to the special labeling on the shipping tube for details.

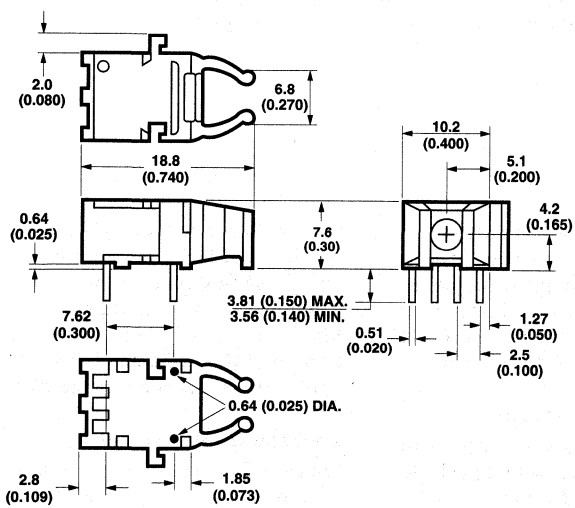
Recommended Chemicals for Cleaning/Degreasing

Alcohols: methyl, isopropyl, isobutyl. *Aliphatics:* hexane, heptane, *Other:* soap solution, naphtha.

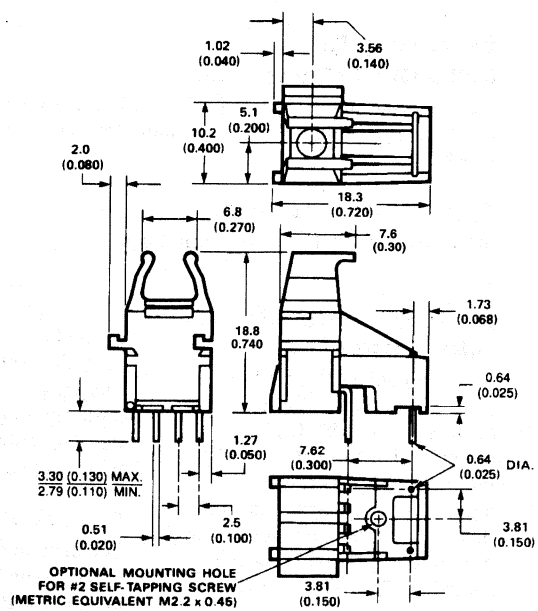
Do not use partially halogenated hydrocarbons such as 1,1.1 trichloroethane, ketones such as MEK, acetone, chloroform, ethyl acetate, methylene dichloride, phenol, methylene chloride, or N-methylpyrolldone. Also, HP does not recommend the use of cleaners that use halogenated hydrocarbons because of their potential environmental harm.

Mechanical Dimensions

Horizontal Modules

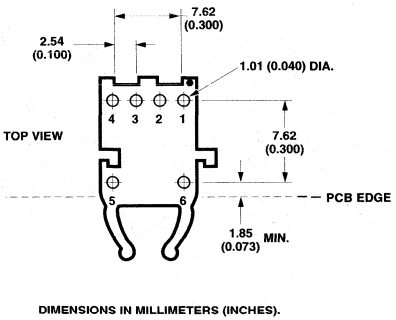


Vertical Modules



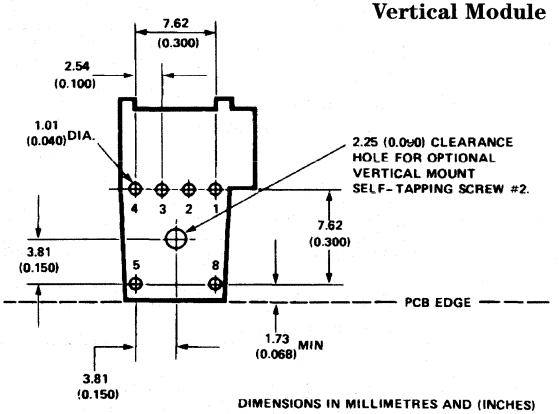
Versatile Link Printed Board Layout Dimensions

Horizontal Module



DIMENSIONS IN MILLIMETERS (INCHES).

Vertical Module



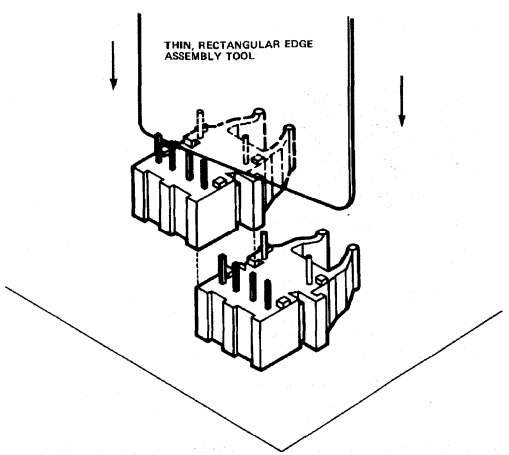
DIMENSIONS IN MILLIMETRES AND (INCHES)

Interlocked (Stacked) Assemblies (refer to Figure 1)

Horizontal packages may be stacked by placing units with pins facing upward. Initially engage the interlocking mechanism by sliding the L bracket body from above into the L slot body of the lower package. Use a straight edge, such as a ruler, to bring all stacked units into uniform alignment. This technique prevents potential harm that could occur to fingers and hands of assemblers from the package pins. Stacked horizontal packages can be disengaged if necessary. Repeated stacking and unstacking causes no damage to individual units.

To stack vertical packages, hold one unit in each hand, with the pins facing away and the optical ports on the bottom. Slide the L bracket unit into the L slot unit. The straight edge used for horizontal package alignment is not needed.

Stacking Horizontal Modules



Stacking Vertical Modules

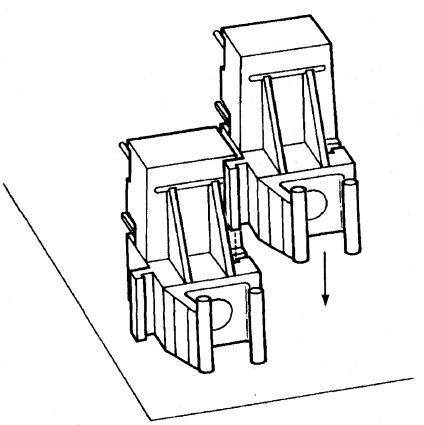


Figure 1. Interlocked (Stacked) Horizontal or Vertical Packages.

5 MBd Link (HFBR-15X1/25X1)

System Performance 0 to 70°C unless otherwise specified.

	Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions	Ref.
High Performance 5 MBd	Data Rate		dc		5	MBd	BER ≤ 10^{-9}, PRBS:2^7-1	
	Link Distance (Standard Cable)	ℓ	19 27	 48		m m	I_{Fdc} = 60 mA I_{Fdc} = 60 mA, 25°C	Fig. 3 Note 3
	Link Distance (Improved Cable)	ℓ	22 27	 53		m m	I_{Fdc} = 60 mA I_{Fdc} = 60 mA, 25°C	Fig. 4 Note 3
	Propagation Delay	t_{PLH} t_{PHL}		80 50	140 140	ns ns	R_L = 560 Ω, C_L = 30 pF fiber length = 0.5 m -21.6 ≤ P_R ≤ -9.5 dBm	Fig. 5, 8 Notes 1, 2
	Pulse Width Distortion t_{PLH}-t_{PHL}	t_D		30		ns	P_R = -15 dBm R_L = 560 Ω, C_L = 30 pF	Fig. 5, 7

Notes:

1. The propagation delay for one metre of cable is typically 5 ns.
2. Typical propagation delay is measured at P_R = -15 dBm.
3. Estimated typical link life expectancy at 40°C exceeds 10 years at 60 mA.

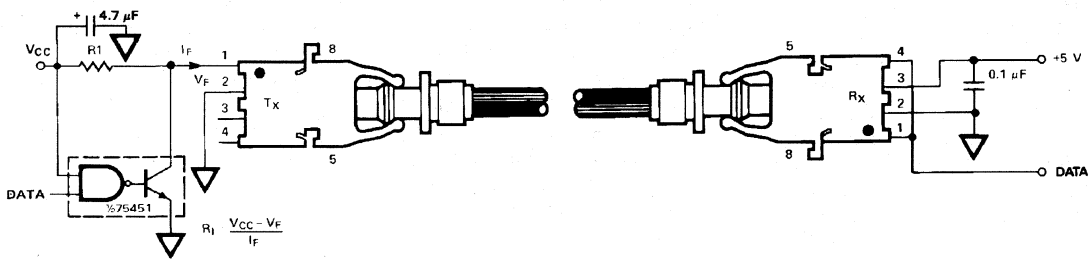


Figure 2. Typical 5 MBd Interface Circuit.

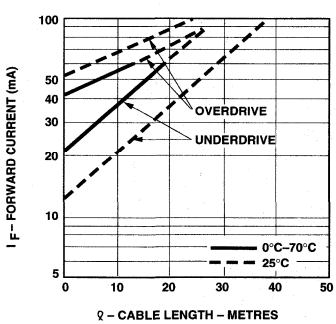


Figure 3. Guaranteed System Performance with Standard Cable (HFBR-15X1/25X1).

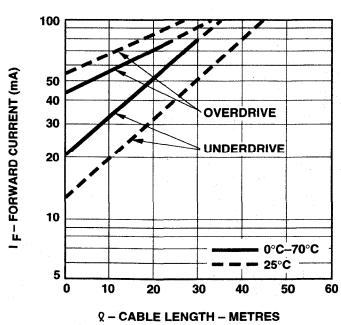


Figure 4. Guaranteed System Performance with Improved Cable (HFBR-15X1/25X1).

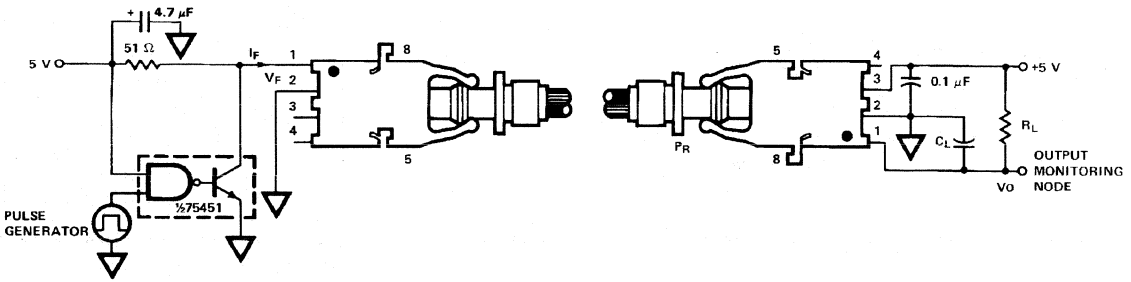


Figure 5. 5 MBd Propagation Delay Test Circuit.

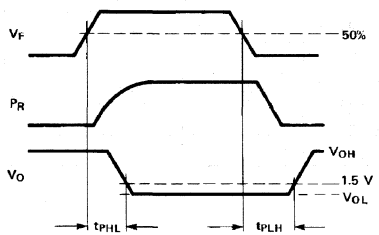


Figure 6. Propagation Delay Test Waveforms.

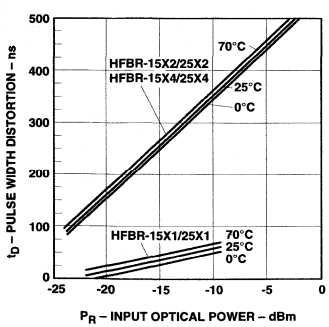


Figure 7. Typical Link Pulse Width Distortion vs. Optical Power.

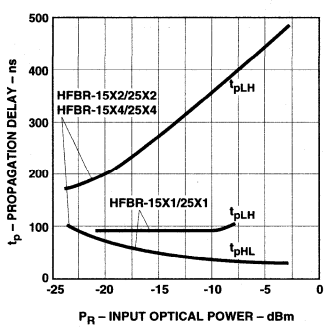
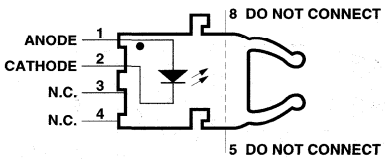


Figure 8. Typical Link Propagation Delay vs. Optical Power.

HFBR-15X1 Transmitter



Pin #	Function
1	Anode
2	Cathode
3	Open
4	Open
5	Do not connect
8	Do not connect

Note: Pins 5 and 8 are for mounting and retaining purposes only. Do not electrically connect these pins.

Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Units	Reference
Storage Temperature		T_S	-40	+75	°C	
Operating Temperature		T_A	0	+70	°C	
Lead Soldering Cycle	Temp.			260	°C	Note 1
	Time			10	sec	
Forward Input Current		I_{FPK}		1000	mA	Note 2, 3
		I_{Fdc}		80		
Reverse Input Voltage		V_{BR}		5	V	

Notes:
1. 1.6 mm below seating plane.
2. Recommended operating range between 10 and 750 mA.
3. 1 µs pulse, 20 µs period.

All HFBR-15XX LED transmitters are classified as IEC 825-1 Accessible Emission Limit (AEL) Class 1 based upon the current proposed draft scheduled to go into effect on January 1, 1997. AEL Class 1 LED devices are considered eye safe. Contact your local Hewlett-Packard sales representative for more information.

Transmitter Electrical/Optical Characteristics 0°C to 70°C unless otherwise specified

Parameter	Symbol	Min.	Typ.[5]	Max.	Units	Conditions	Ref.
Transmitter Output Optical Power	P_T	-16.5		-7.6	dBm	I_{Fdc} = 60 mA	Notes 1, 2
		-14.3		-8.0	dBm	I_{Fdc} = 60 mA, 25°C	
Output Optical Power Temperature Coefficient	$\Delta P_T/\Delta T$		-0.85		%/°C		
Peak Emission Wavelength	λ_{PK}		660		nm		
Forward Voltage	V_F	1.45	1.67	2.02	V	I_{Fdc} = 60 mA	
Forward Voltage Temperature Coefficient	$\Delta V_F/\Delta T$		-1.37		mV/°C		Fig. 9
Effective Diameter	D		1		mm		
Numerical Aperture	NA		0.5				
Reverse Input Breakdown Voltage	V_{BR}	5.0	11.0		V	I_{Fdc} = 10 µA, T_A = 25°C	
Diode Capacitance	C_O		86		pF	V_F = 0, f = MHz	
Rise Time	t_r		80		ns	10% to 90%, I_F = 60 mA	Note 3
Fall Time	t_f		40		ns		

Notes:
1. Measured at the end of 0.5 m standard fiber optic cable with large area detector.
2. Optical power, P (dBm) = 10 Log [P(µW)/1000 µW].
3. Rise and fall times are measured with a voltage pulse driving the transmitter and a series connected 50 Ω load. A wide bandwidth optical to electrical waveform analyzer, terminated to a 50 Ω input of a wide bandwidth oscilloscope, is used for this response time measurement.

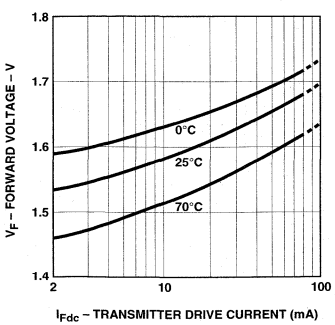


Figure 9. Typical Forward Voltage vs. Drive Current.

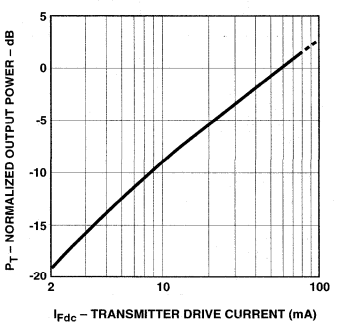
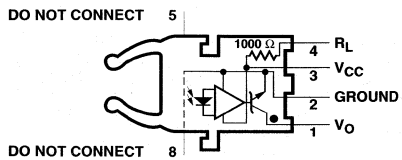


Figure 10. Normalized Typical Output Power vs. Drive Current.

HFBR-25X1 Receiver



Pin #	Function
1	V_O
2	Ground
3	V_{CC}
4	R_L
5	Do not connect
8	Do not connect

Note: Pins 5 and 8 are for mounting and retaining purposes only. Do not electrically connect these pins.

Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Units	Reference
Storage Temperature		T_S	-40	+75	°C	
Operating Temperature		T_A	0	+70	°C	
Lead Soldering Cycle	Temp.			260	°C	Note 1
	Time			10	sec	
Supply Voltage		V_{CC}	-0.5	7	V	Note 2
Output Collector Current		I_{OAV}		25	mA	
Output Collector Power Dissipation		P_{OD}		40	mW	
Output Voltage		V_O	-0.5	18	V	
Pull-up Voltage		V_P	-5	V_{CC}	V	
Fan Out (TTL)		N		5		

Notes:
1. 1.6 mm below seating plane.
2. It is essential that a bypass capacitor 0.01 µF be connected from pin 2 to pin 3 of the receiver. Total lead length between both ends of the capacitor and the pins should not exceed 20 mm.

Receiver Electrical/Optical Characteristics

0°C to 70°C, 4.75 V ≤ V_{CC} ≤ 5.25 V unless otherwise specified

Parameter	Symbol	Min.	Typ.[5]	Max.	Units	Conditions	Ref.
Input Optical Power Level for Logic "0"	$P_{R(L)}$	-21.6		-9.5	dBm	V_{OL} = 0.5 V I_{OL} = 8 mA	Notes 1, 2, 4
		-21.6		-8.7		V_{OL} = 0.5 V I_{OL} = 8 mA, 25°C	
Input Optical Power Level for Logic "1"	$P_{R(H)}$			-43	dBm	V_{OL} = 5.25 V I_{OH} ≤ 250 µA	Note 1
High Level Output Current	I_{OH}		5	250	µA	V_O = 18 V, P_R = 0	Note 3
Low Level Output Current	V_{OL}		0.4	0.5	V	I_{OL} = 8 mA, P_R = $P_{R(L)MIN}$	Note 3
High Level Supply Current	I_{CCH}		3.5	6.3	mA	V_{CC} = 5.25 V, P_R = 0	Note 3
Low Level Supply Current	I_{CCL}		6.2	10	mA	V_{CC} = 5.25 V P_R = -12.5 dBm	Note 3
Effective Diameter	D		1		mm		
Numerical Aperture	NA		0.5				
Internal Pull-up Resistor	R_L	680	1000	1700	Ω		

Notes:
1. Optical flux, P (dBm) = 10 Log [P (µW)/1000 µW].
2. Measured at the end of the fiber optic cable with large area detector.
3. R_L is open.
4. Pulsed LED operation at I_F > 80 mA will cause increased link t_{PLH} propagation delay time. This extended t_{PLH} time contributes to increased pulse width distortion of the receiver output signal.

1 MBd Link

(High Performance HFBR-15X2/25X2, Standard HFBR-15X4/25X4)

System Performance Under recommended operating conditions unless otherwise specified.

	Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions	Ref.
High Performance 1 MBd	Data Rate		dc		1	MBd	BER ≤ 10^{-9}, PRBS:2^7-1	
	Link Distance (Standard Cable)	ℓ	39 47	70		m m	I_{Fdc} = 60 mA I_{Fdc} = 60 mA, 25°C	Fig. 14 Notes 1, 3, 4
	Link Distance (Improved Cable)	ℓ	45 56	78		m m	I_{Fdc} = 60 mA I_{Fdc} = 60 mA, 25°C	Fig. 15 Notes 1, 3, 4
	Propagation Delay	t_{PLH} t_{PHL}		180 100	250 140	ns ns	R_L = 560 Ω, C_L = 30 pF I = 0.5 metre P_R = -24 dBm	Fig. 16, 18 Notes 2, 4
	Pulse Width Distortion t_{PLH}-t_{PHL}	t_D		80		ns	P_R = -24 dBm R_L = 560 Ω, C_L = 30 pF	Fig. 16, 17 Note 4

	Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions	Ref.
Standard 1 MBd	Data Rate		dc		1	MBd	BER ≤ 10^{-9}, PRBS:2^7-1	
	Link Distance (Standard Cable)	ℓ	8 17	43		m m	I_{Fdc} = 60 mA I_{Fdc} = 60 mA, 25°C	Fig. 12 Notes 1, 3, 4
	Link Distance (Improved Cable)	ℓ	10 19	48		m m	I_{Fdc} = 60 mA I_{Fdc} = 60 mA, 25°C	Fig. 13 Notes 1, 3, 4
	Propagation Delay	t_{PLH} t_{PHL}		180 100	250 140	ns ns	R_L = 560 Ω, C_L = 30 pF I = 0.5 metre P_R = -20 dBm	Fig. 16, 18 Notes 2, 4
	Pulse Width Distortion t_{PLH}-t_{PHL}	t_D		80		ns	P_R = -20 dBm R_L = 560 Ω, C_L = 30 pF	Fig. 16, 17 Note 4

Notes:

1. For I_{FPK} > 80 mA, the duty factor must be such as to keep I_{Fdc} ≤ 80 mA. In addition, for I_{FPK} > 80 mA, the following rules for pulse width apply:
   I_{FPK} ≤ 160 mA: Pulse width ≤ 1 ms
   I_{FPK} > 160 mA: Pulse width ≤ 1 μS, period ≥ 20 μS.
2. The propagation delay for one meter of cable is typically 5 ns.
3. Estimated typical link life expectancy at 40°C exceeds 10 years at 60 mA.
4. Pulsed LED operation at I_{FPK} > 80 mA will cause increased link t_{PLH} propagation delay time. This extended t_{PLH} time contributes to increased pulse width distortion of the receiver output signal.

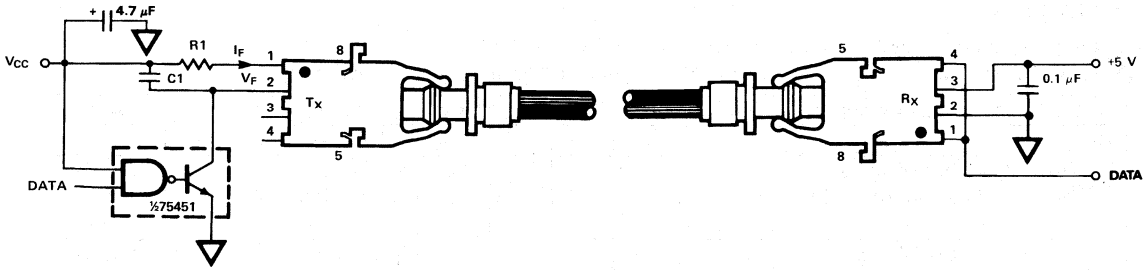


Figure 11. Required 1 MBd Interface Circuit.

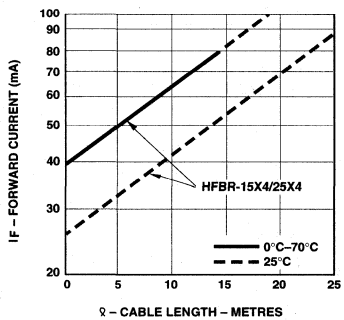


Figure 12. Guaranteed System Performance for the HFBR-15X4/25X4 Link with Standard Cable.

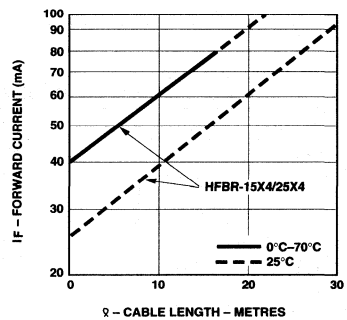


Figure 13. Guaranteed System Performance for the HFBR-15X4/25X4 Link with Improved Cable.

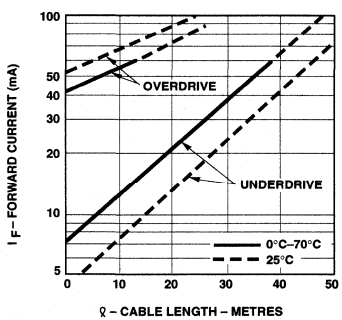


Figure 14. Guaranteed System Performance for the HFBR-15X2/25X2 Link with Standard Cable.

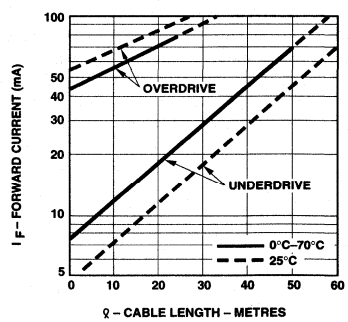


Figure 15. Guaranteed System Performance for the HFBR-15X2/25X2 Link with Improved Cable.

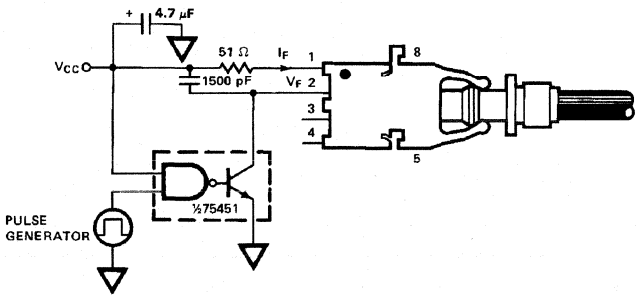


Figure 16. 1 MBd Propagation Delay Test Circuit.

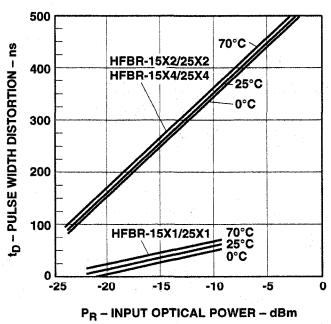


Figure 17. Pulse Width Distortion vs. Optical Power.

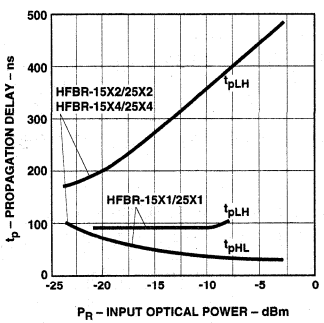


Figure 18. Typical Link Propagation Delay vs. Optical Power.

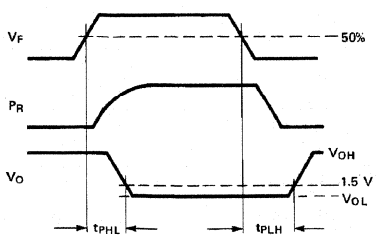
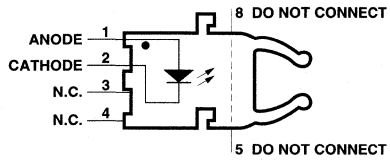


Figure 19. Propagation Delay Test Waveforms.

HFBR-15X2/15X4 Transmitters



Pin #	Function
1	Anode
2	Cathode
3	Open
4	Open
5	Do not connect
8	Do not connect

Note: Pins 5 and 8 are for mounting and retaining purposes only. Do not electrically connect these pins.

Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Units	Reference
Storage Temperature		T_S	-40	+75	°C	
Operating Temperature		T_A	0	+70	°C	
Lead Soldering Cycle	Temp.			260	°C	Note 1
	Time			10	sec	
Forward Input Current		I_{FPK}		1000	mA	Note 2, 3
		I_{Fdc}		80		
Reverse Input Voltage		V_{BR}		5	V	

Notes:
1. 1.6 mm below seating plane.
2. Recommended operating range between 10 and 750 mA.
3. 1 µs pulse, 20 µs period.

All HFBR-15XX LED transmitters are classified as IEC 825-1 Accessible Emission Limit (AEL) Class 1 based upon the current proposed draft scheduled to go into effect on January 1, 1997. AEL Class 1 LED devices are considered eye safe. Contact your Hewlett-Packard sales representative for more information.

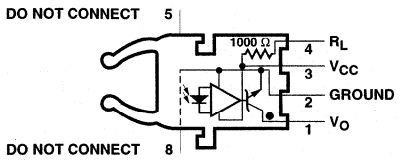
Transmitter Electrical/Optical Characteristics 0°C to 70°C unless otherwise specified

FOR FORWARD VOLTAGE AND OUTPUT POWER VS. DRIVE CURRENT GRAPHS.

Parameter		Symbol	Min.	Typ.[5]	Max.	Units	Conditions	Ref.
Transmitter Output Optical Power	HFBR-15X2	P_T	-13.6 -11.2		-4.5 -5.1	dBm	I_{Fdc} = 60 mA I_{Fdc} = 60 mA, 25°C	
	HFBR-15X4	P_T	-17.8 -15.5		-4.5 -5.1	dBm	I_{Fdc} = 60 mA I_{Fdc} = 60 mA, 25°C	
Output Optical Power Temperature Coefficient		$\Delta P_T/\Delta T$		-0.85		%/°C		
Peak Emission Wavelength		λ_{PK}		660		nm		
Forward Voltage		V_F	1.45	1.67	2.02	V	I_{Fdc} = 60 mA	
Forward Voltage Temperature Coefficient		$\Delta V_F/\Delta T$		-1.37		mV/°C		Fig. 11
Effective Diameter		D_T		1		mm		
Numerical Aperture		NA		0.5				
Reverse Input Breakdown Voltage		V_{BR}	5.0	11.0		V	I_{Fdc} = 10 µA, T_A = 25°C	
Diode Capacitance		C_O		86		pF	V_F = 0, f = 1 MHz	
Rise Time		t_r		80		ns	10% to 90%,	Note 1
Fall Time		t_f		40		ns	I_F = 60 mA	

Note:
1. Rise and fall times are measured with a voltage pulse driving the transmitter and a series connected 50 Ω load. A wide bandwidth optical to electrical waveform analyzer, terminated to a 50 Ω input of a wide bandwidth oscilloscope, is used for this response time measurement.

HFBR-25X2/25X4 Receivers



Pin #	Function
1	V_O
2	Ground
3	V_{CC}
4	R_L
5	Do not connect
8	Do not connect

Note: Pins 5 and 8 are for mounting and retaining purposes only. Do not electrically connect these pins.

Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Units	Reference
Storage Temperature		T_S	-40	+75	°C	
Operating Temperature		T_A	0	+70	°C	
Lead Soldering Cycle	Temp.			260	°C	Note 1
	Time			10	sec	
Supply Voltage		V_{CC}	-0.5	7	V	Note 2
Output Collector Current		I_{OAV}		25	mA	
Output Collector Power Dissipation		P_{OD}		40	mW	
Output Voltage		V_O	-0.5	18	V	
Pull-up Voltage		V_P	-5	V_{CC}	V	
Fan Out (TTL)		N		5		

Notes:
1. 1.6 mm below seating plane.
2. It is essential that a bypass capacitor 0.01 µF be connected from pin 2 to pin 3 of the receiver. Total lead length between both ends of the capacitor and the pins should not exceed 20 mm.

Receiver Electrical/Optical Characteristics 0°C to 70°C, 4.75 V ≤ V_{CC} ≤ 5.25 V unless otherwise specified

Parameter		Symbol	Min.	Typ.[5]	Max.	Units	Conditions	Ref.
Receiver Optical Input Power Level Logic 0	HFBR-2522	$P_{R(L)}$	-24			dBm	V_{OL} = 0 V I_{OL} = 8 mA	Notes 1, 2, 3
	HFBR-2524		-20					Note 4
Optical Input Power Level Logic 1		$P_{R(H)}$			-43	dBm	V_{OH} = 5.25 V I_{OH} = ≤ 250 µA	
High Level Output Current		I_{OH}		5	250	µA	V_O = 18 V, P_R = 0	Note 5
Low Level Output Voltage		V_{OL}		0.4	0.5	V	I_{OL} = 8 mA P_R = $P_{R(L)MIN}$	Note 5
High Level Supply Current		I_{CCH}		3.5	6.3	mA	V_{CC} = 5.25 V, P_R = 0	Note 5
Low Level Supply Current		I_{CCL}		6.2	10	mA	V_{CC} = 5.25 V, P_R = -12.5 dBm	Note 5
Effective Diameter		D		1		mm		
Numerical Aperture		NA		0.5				
Internal Pull-up Resistor		R_L	680	1000	1700	Ω		

Notes:
1. Measured at the end of the fiber optic cable with large area detector.
2. Pulsed LED operation at I_F > 80 mA will cause increased link t_{PLH} propagation delay time. This extended t_{PLH} time contributes to increased pulse width distortion of the receiver output signal.
3. The LED drive circuit of Figure 11 is required for 1 MBd operation of the HFBR-25X2/25X4.
4. Optical flux, P (dBm) = 10 Log [P(µW)/1000 µW].
5. R_L is open.

40 kBd Link

System Performance Under recommended operating conditions unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions	Ref.
Data Rate		dc		40	kBd	BER ≤ 10^{-9}, PRBS: 2^7 - 1	
Link Distance	ℓ	13	41		m	I_{Fdc} = 2 mA	Fig. 21
(Standard Cable)		94	138		m	I_{Fdc} = 60 mA	Note 1
Link Distance	ℓ	15	45		m	I_{Fdc} = 2 mA	Fig. 22
(Improved Cable)		111	154		m	I_{Fdc} = 60 mA	Note 1
Propagation	t_{PLH}		4		µs	R_L = 3.3 kΩ, C_L = 30 pF	Fig. 22, 25
Delay	t_{PHL}		2.5		µs	P_R = -25 dBm, 1 m fiber	Note 2
Pulse Width	t_D			7	µs	-39 ≤ P_R ≤ - 14 dBm	Fig. 23, 24
Distortion t_{PLH}-t_{PHL}						R_L = 3.3 kΩ, C_L = 30 pF	

Notes:

1. Estimated typical link life expectancy at 40°C exceeds 10 years at 60 mA.
2. The propagation delay for one metre of cable is typically 5 ns.

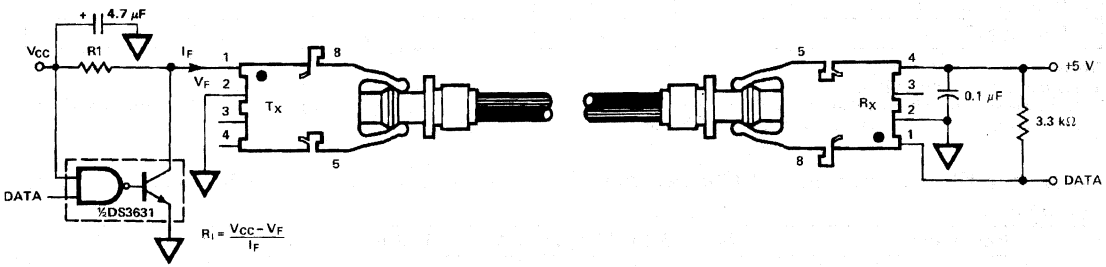


Figure 20. Typical 40 kBd Interface Circuit.

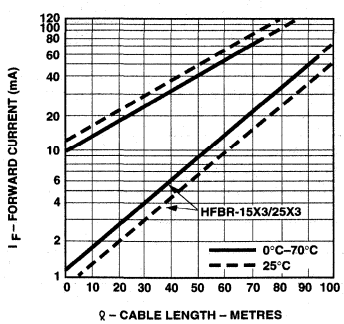


Figure 21. Guaranteed System Performance with Standard Cable.

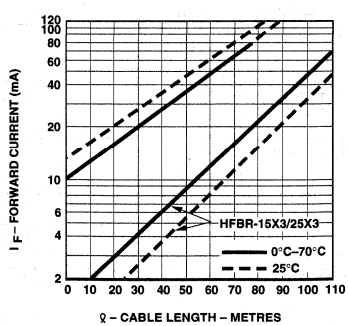


Figure 22. Guaranteed System Performance with Improved Cable.

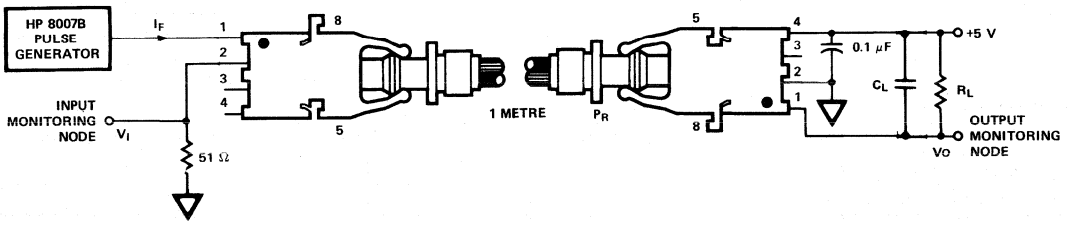


Figure 23. 40 kBd Propagation Delay Test Circuit.

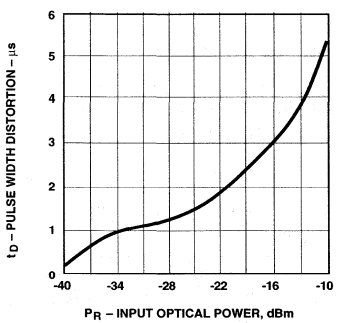


Figure 24. Typical Link Pulse Width Distortion vs. Optical Power.

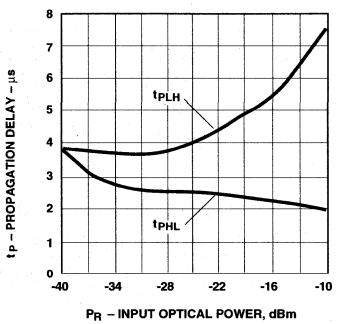


Figure 25. Typical Link Propagation Delay vs. Optical Power.

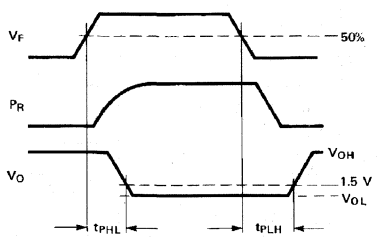
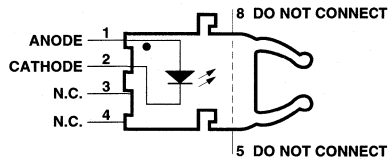


Figure 26. Propagation Delay Test Waveforms.

HFBR-15X3 Transmitter



Pin #	Function
1	Anode
2	Cathode
3	Open
4	Open
5	Do not connect
8	Do not connect

Note: Pins 5 and 8 are for mounting and retaining purposes only. Do not electrically connect these pins.

Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Units	Reference
Storage Temperature		T_S	-40	+75	°C	
Operating Temperature		T_A	0	+70	°C	
Lead Soldering Cycle	Temp.			260	°C	Note 1
	Time			10	sec	
Forward Input Current		I_{FPK}		1000	mA	Note 2, 3
		I_{Fdc}		80		
Reverse Input Voltage		V_{BR}		5	V	

Notes:
1. 1.6 mm below seating plane.
2. Recommended operating range between 10 and 750 mA.
3. 1 µs pulse, 20 µs period.

All HFBR-15XX LED transmitters are classified as IEC 825-1 Accessible Emission Limit (AEL) Class 1 based upon the current proposed draft scheduled to go into effect on January 1, 1997. AEL Class 1 LED devices are considered eye safe. Contact your Hewlett-Packard sales representative for more information.

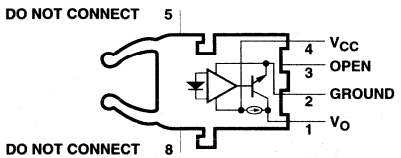
Transmitter Electrical/Optical Characteristics 0°C to 70°C unless otherwise specified.

FOR FORWARD VOLTAGE AND OUTPUT POWER VS. DRIVE CURRENT GRAPHS.

Parameter	Symbol	Min.	Typ.[5]	Max.	Units	Conditions	Ref.
Transmitter Output Optical Power	P_T	-11.2 -13.6 -35.5		-5.1 -4.5	dBm	I_{Fdc} = 60 mA, 25°C I_{Fdc} = 60 mA I_{Fdc} = 2 mA, 0-70°C	Notes 3, 4 Fig. 9, 10
Output Optical Power Temperature Coefficient	$\Delta P_T/\Delta T$		-0.85		%/°C		
Peak Emission Wavelength	λ_{PK}		660		nm		
Forward Voltage	V_F	1.45	1.67	2.02	V	I_{Fdc} = 60 mA	
Forward Voltage Temperature Coefficient	$\Delta V_F/\Delta T$		-1.37		mV/°C		Fig. 18
Effective Diameter	D		1		mm		
Numerical Aperture	NA		0.5				
Reverse Input Breakdown Voltage	V_{BR}	5.0	11.0		V	I_{Fdc} = 10 µA, T_A = 25°C	
Diode Capacitance	C_O		86		pF	V_F = 0, f = 1 MHz	
Rise Time	t_r		80		ns	10% to 90%,	Note 1
Fall Time	t_f		40			I_F = 60 mA	

Notes:
1. Rise and fall times are measured with a voltage pulse driving the transmitter and a series connected 50 Ω load. A wide bandwidth optical to electrical waveform analyzer, terminated to a 50 Ω input of a wide bandwidth oscilloscope, is used for this response time measurement.

HFBR-25X3 Receiver



Pin #	Function
1	V_O
2	Ground
3	Open
4	V_{CC}
5	Do not connect
8	Do not connect

Note: Pins 5 and 8 are for mounting and retaining purposes only. Do not electrically connect these pins.

Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Units	Reference
Storage Temperature		T_S	-40	+75	°C	
Operating Temperature		T_A	0	+70	°C	
Lead Soldering Cycle	Temp.			260	°C	Note 1
	Time			10	sec	
Supply Voltage		V_{CC}	-0.5	7	V	Note 2
Average Output Collector Current		I_O	-1	5	mA	
Output Collector Power Dissipation		P_{OD}		25	mW	
Output Voltage		V_O	-0.5	7	V	

Notes:
1. 1.6 mm below seating plane.
2. It is essential that a bypass capacitor 0.01 µF be connected from pin 2 to pin 3 of the receiver.

Receiver Electrical/Optical Characteristics 0°C to 70°C, 4.5 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions	Ref.
Input Optical Power	$P_{R(L)}$	-39		-13.7	dBm	$V_O = V_{OL}$, I_{OL} = 3.2 mA	Notes 1, 2, 3
Level Logic 0		-39		-13.3		$V_O = V_{OL}$, I_{OH} = 8 mA, 25°C	
Input Optical Power Level Logic 1	$P_{R(H)}$			-53	dBm	V_{OH} = 5.5 V I_{OH} = ≤ 40 µA	Note 3
High Level Output Voltage	V_{OH}	2.4			V	I_O = -40 µA, P_R = 0 µW	
Low Level Output Voltage	V_{OL}			0.4	V	I_{OL} = 3.2 mA $P_R = P_{R(L)MIN}$	Note 4
High Level Supply Current	I_{CCH}		1.2	1.9	mA	V_{CC} = 5.5 V, P_R = 0 µW	
Low Level Supply Current	I_{CCL}		2.9	3.7	mA	V_{CC} = 5.5 V, $P_R = P_{RL}$ (MIN)	Note 4
Effective Diameter	D		1		mm		
Numerical Aperture	NA		0.5				

Notes:
1. Measured at the end of the fiber optic cable with large area detector.
2. Optical flux, P (dBm) = 10 Log P(µW)/1000 µW.
3. Because of the very high sensitivity of the HFBR-25X3, the digital output may switch in response to ambient light levels when a cable is not occupying the receiver optical port. The designer should take care to filter out signals from this source if they pose a hazard to the system.
4. Including current in 3.3 k pull-up resistor.

HEWLETT® PACKARD

125 Megabaud Versatile Link The Versatile Fiber Optic Connection

Technical Data

HFBR-0507 Series
HFBR-15X7 Transmitters
HFBR-25X6 Receivers

Features

- **Data Transmission at Signal Rates of 1 to 125 MBd over Distances of 100 Meters**
- **Compatible with Inexpensive, Easily Terminated Plastic Optical Fiber, and with Large Core Silica Fiber**
- **High Voltage Isolation**
- **Transmitter and Receiver Application Circuit Schematics and Recommended Board Layouts Available**
- **Interlocking Feature for Single Channel or Duplex Links, in a Vertical or Horizontal Mount Configuration**

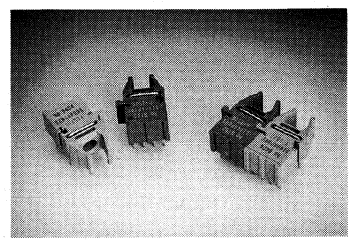
Applications

- **Intra-System Links: Board-to-Board, Rack-to-Rack**
- **Telecommunications Switching Systems**
- **Computer-to-Peripheral Data Links, PC Bus Extension**
- **Industrial Control**
- **Proprietary LANs**
- **Digitized Video**
- **Medical Instruments**
- **Reduction of Lightning and Voltage Transient Susceptibility**

Description

The 125 MBd Versatile Link (HFBR-0507 Series) is the most cost-effective fiber-optic solution for transmission of 125 MBd data over 100 meters. The data link consists of a 650 nm LED transmitter, HFBR-15X7, and a PIN/preamp receiver, HFBR-25X6. These can be used with low-cost plastic or silica fiber. One mm diameter plastic fiber provides the lowest cost solution for distances under 25 meters. The lower attenuation of silica fiber allows data transmission over longer distance, for a small difference in cost. These components can be used for high speed data links without the problems common with copper wire solutions, at a competitive cost.

The HFBR-15X7 transmitter is a high power 650 nm LED in a low cost plastic housing designed to efficiently couple power into 1 mm diameter plastic optical fiber



and 200 µm Hard Clad Silica (HCS®) fiber. With the recommended drive circuit, the LED operates at speeds from 1-125 MBd. The HFBR-25X6 is a high bandwidth analog receiver containing a PIN photodiode and internal transimpedance amplifier. With the recommended application circuit for 125 MBd operation, the performance of the complete data link is specified for of 0-25 meters with plastic fiber and 0-100 meters with 200 µm HCS® fiber. A wide variety of other digitizing circuits can be combined with the HFBR-0507 Series to optimize performance and cost at higher and lower data rates.

HCS® is a registered trademark of Spectran Corporation.

5965-6114E

HFBR-0507 Series
125 MBd Data Link

Data link operating conditions and performance are specified for the HFBR-15X7 transmitter and HFBR-25X6 receiver in the recommended applications circuits shown in Figure 1. This circuit has been optimized for 125 MBd operation. The Applications Engineering Department in the Hewlett-Packard Optical Communication Division is available to assist in optimizing link performance for higher or lower speed operation.

Recommended Operating Conditions for the Circuits in Figures 1 and 2.

Parameter	Symbol	Min.	Max.	Unit	Reference
Ambient Temperature	T_A	0	70	°C	
Supply Voltage	V_{CC}	+4.75	+5.25	V	
Data Input Voltage – Low	V_{IL}	V_{CC} -1.89	V_{CC} -1.62	V	
Data Input Voltage – High	V_{IH}	V_{CC} -1.06	V_{CC} -0.70	V	
Data Output Load	R_L	45	55	Ω	Note 1
Signaling Rate	f_S	1	125	MBd	
Duty Cycle	D.C.	40	60	%	Note 2

Link Performance: 1-125 MBd, BER ≤ 10^{-9}, under recommended operating conditions with recommended transmit and receive application circuits.

Parameter	Symbol	Min.[3]	Typ.[4]	Max.	Unit	Condition	Reference
Optical Power Budget, 1 m POF	OPB_{POF}	11	16		dB		Note 5,6,7
Optical Power Margin, 20 m Standard POF	$OPM_{POF,20}$	3	6		dB		Note 5,6,7
Link Distance with Standard 1 mm POF	l	20	27		m		
Optical Power Margin, 25 m Low Loss POF	$OPM_{POF,25}$	3	6		dB		Note 5,6,7
Link Distance with Extra Low Loss 1 mm POF	l	25	32		m		
Optical Power Budget, 1 m HCS	OPB_{HCS}	7	12		dB		Note 5,6,7
Optical Power Margin, 100 m HCS	$OPM_{HCS,100}$	3	6		dB		Note 5,6,7
Link Distance with HCS Cable	l	100	125		m		

Notes:

1. If the output of U4C in Figure 1, page 4 is transmitted via coaxial cable, terminate with a 50 Ω resistor to V_{CC} - 2 V.
2. Run length limited code with maximum run length of 10 µs.
3. Minimum link performance is projected based on the worst case specifications of the HFBR-15X7 transmitter, HFBR-25X6 receiver, and POF cable, and the typical performance of other components (e.g. logic gates, transistors, resistors, capacitors, quantizer, HCS cable).
4. Typical performance is at 25°C, 125 MBd, and is measured with typical values of all circuit components.
5. Standard cable is HFBR-RXXYYY plastic optical fiber , with a maximum attenuation of 0.24 dB/m at 650 nm and NA = 0.5. Extra low loss cable is HFBR-EXXYYY plastic optical fiber, with a maximum attenuation of 0.19 dB/m at 650 nm and NA = 0.5. HCS cable is HFBR-H/VXXYYY glass optical fiber, with a maximum attenuation of 10 dB/km at 650 nm and NA = 0.37.
6. Optical Power Budget is the difference between the transmitter output power and the receiver sensitivity, measured after 1 meter of fiber. The minimum OPB is based on the limits of optical component performance over temperature, process, and recommended power supply variation.
7. The Optical Power Margin is the available OPB after including the effects of attenuation and modal dispersion for the minimum link distance: OPM = OPB - (attenuation power loss + modal dispersion power penalty). The minimum OPM is the margin available for longterm LED LOP degradation and additional fixed passive losses (such as in-line connectors) in addition to the minimum specified distance.

Plastic Optical Fiber (1 mm POF) Transmitter Application Circuit:

Performance of the HFBR-15X7 transmitter in the recommended application circuit (Figure 1) for POF; 1-125 MBd, 25°C.

Parameter	Symbol	Typical	Unit	Condition	Note
Average Optical Power 1 mm POF	P_{avg}	-9.7	dBm	50% Duty Cycle	Note 1, Fig 3
Average Modulated Power 1 mm POF	P_{mod}	-11.3	dBm		Note 2, Fig 3
Optical Rise Time (10% to 90%)	t_r	2.1	ns	5 MHz	
Optical Fall Time (90% to 10%)	t_f	2.8	ns	5 MHz	
High Level LED Current (On)	$I_{F,H}$	19	mA		Note 3
Low Level LED Current (Off)	$I_{F,L}$	3	mA		Note 3
Optical Overshoot - 1 mm POF		45	%		
Transmitter Application Circuit Current Consumption - 1 mm POF	I_{CC}	110	mA		Figure 1

Hard Clad Silica Fiber (200 µm HCS) Transmitter Application Circuit: Performance of the HFBR-15X7 transmitter in the recommended application circuit (Figure 1) for HCS; 1-125 MBd, 25°C.

Parameter	Symbol	Typical	Unit	Condition	Note
Average Optical Power 200 µm HCS	P_{avg}	-14.6	dBm	50% Duty Cycle	Note 1, Fig 3
Average Modulated Power 200 µm HCS	P_{mod}	-16.2	dBm		Note 2, Fig 3
Optical Rise Time (10% to 90%)	t_r	3.1	ns	5 MHz	
Optical Fall Time (90% to 10%)	t_f	3.4	ns	5 MHz	
High Level LED Current (On)	$I_{F,H}$	60	mA		Note 3
Low Level LED Current (Off)	$I_{F,L}$	6	mA		Note 3
Optical Overshoot - 200 µm HCS		30	%		
Transmitter Application Circuit Current Consumption - 200 µm HCS	I_{CC}	130	mA		Figure 1

Notes:

1. Average optical power is measured with an average power meter at 50% duty cycle, after 1 meter of fiber.
2. To allow the LED to switch at high speeds, the recommended drive circuit modulates LED light output between two non-zero power levels. The modulated (useful) power is the difference between the high and low level of light output power (transmitted) or input power (received), which can be measured with an average power meter as a function of duty cycle (see Figure 3). Average Modulated Power is defined as one half the slope of the average power versus duty cycle:

$$\text{Average Modulated Power} = \frac{[P_{avg} \text{ @ 80\% duty cycle} - P_{avg} \text{ @ 20\% duty cycle}]}{(2)\,[0.80 - 0.20]}$$

3. High and low level LED currents refer to the current through the HFBR-15X7 LED. The low level LED "off" current, sometimes referred to as "hold-on" current, is prebias supplied to the LED during the off state to facilitate fast switching speeds.

Plastic and Hard Clad Silica Optical Fiber Receiver Application Circuit:

Performance[4] of the HFBR-25X6 receiver in the recommended application circuit (Figure 1); 1-125 MBd, 25°C unless otherwise stated.

Parameter	Symbol	Typical	Unit	Condition	Note
Data Output Voltage - Low	V_{OL}	V_{CC} -1.7	V	R_L = 50 Ω	Note 5
Data Output Voltage - High	V_{OH}	V_{CC} -0.9	V	R_L = 50 Ω	Note 5
Receiver Sensitivity to Average Modulated Optical Power 1 mm POF	P_{min}	-27.5	dBm	50% eye opening	Note 2
Receiver Sensitivity to Average Modulated Optical Power 200 µm HCS	P_{min}	-28.5	dBm	50% eye opening	Note 2
Receiver Overdrive Level of Average Modulated Optical Power 1 mm POF	P_{max}	-7.5	dBm	50% eye opening	Note 2
Receiver Overdrive Level of Average Modulated Optical Power 200 µm HCS	P_{max}	-10.5	dBm	50% eye opening	Note 2
Receiver Application Circuit Current Consumption	I_{CC}	85	mA	R_L = ∞	Figure 1

Notes:

4. Performance in response to a signal from the HFBR-15X7 transmitter driven with the recommended circuit at 1-125 MBd over 1 meter of HFBR-R/EXXYYY plastic optical fiber or 1 meter of HFBR-H/VXXYYY hard clad silica optical fiber.
5. Terminated through a 50 Ω resistor to V_{CC} - 2 V.
6. If there is no input optical power to the receiver, electrical noise can result in false triggering of the receiver. In typical applications, data encoding and error detection prevent random triggering from being interpreted as valid data. Refer to Applications Note 1066 for design guidelines.

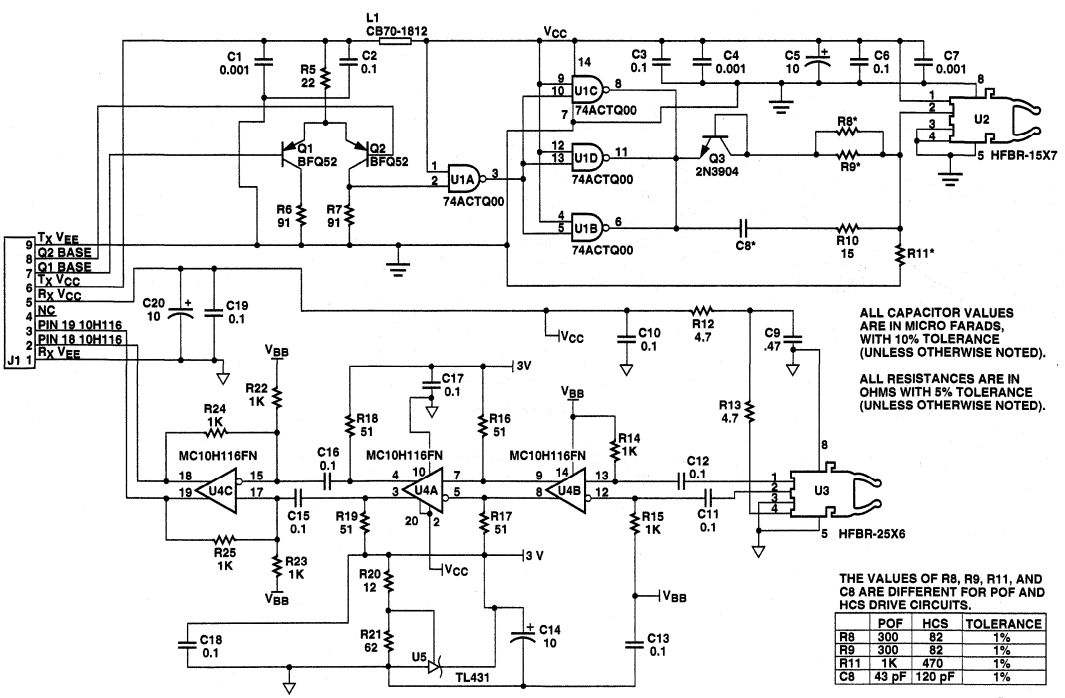


Figure 1. Transmitter and Receiver Application Circuit with +5 V ECL Inputs and Outputs.

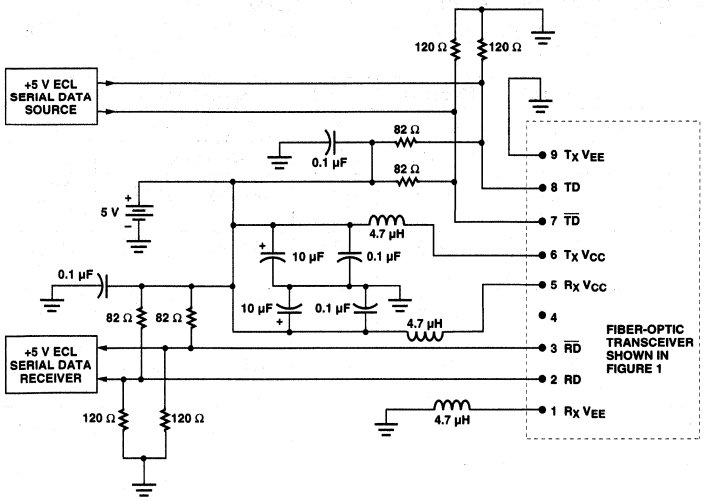


Figure 2. Recommended Power Supply Filter and +5 V ECL Signal Terminations for the Transmitter and Receiver Application Circuit of Figure 1.

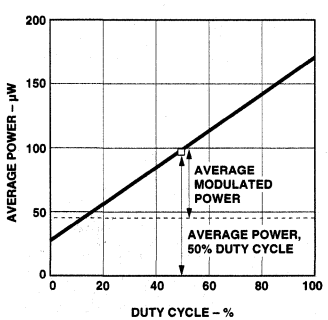


Figure 3. Average Modulated Power.

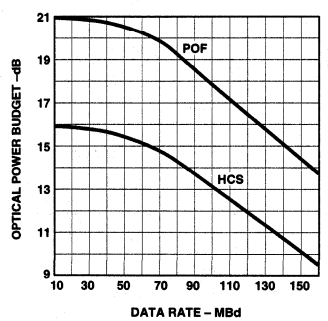


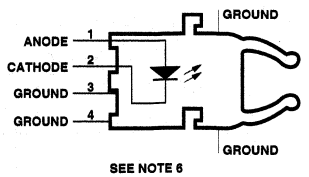
Figure 4. Typical Optical Power Budget vs. Data Rate.

125 Megabaud Versatile Link Transmitter

HFBR-15X7 Series

Description

The HFBR-15X7 transmitters incorporate a 650 nanometer LED in a horizontal (HFBR-1527) or vertical (HFBR-1537) gray housing. The HFBR-15X7 transmitters are suitable for use with current peaking to decrease response time and can be used with HFBR-25X6 receivers in data links operating at signal rates from 1 to 125 megabaud over 1 mm diameter plastic optical fiber or 200 µm diameter hard clad silica glass optical fiber. Refer to Application Note 1066 for details for recommended interface circuits.



Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Reference
Storage Temperature	T_S	-40	85	°C	
Operating Temperature	T_O	-40	70	°C	
Lead Soldering Temperature			260	°C	Note 1
Cycle Time			10	s	
Transmitter High Level Forward Input Current	$I_{F,H}$		120	mA	50% Duty Cycle ≥ 1 MHz
Transmitter Average Forward Input Current	$I_{F,AV}$		60	mA	
Reverse Input Voltage	V_R		3	V	

CAUTION: The small junction sizes inherent to the design of this component increase the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

WARNING: WHEN VIEWED UNDER SOME CONDITIONS, THE OPTICAL PORT MAY EXPOSE THE EYE BEYOND THE MAXIMUM PERMISSIBLE EXPOSURE RECOMMENDED IN ANSI Z136.2, 1993. UNDER MOST VIEWING CONDITIONS THERE IS NO EYE HAZARD.

Electrical/Optical Characteristics 0 to 70°C, unless otherwise stated.

Parameter	Symbol	Min.	Typ.[2]	Max.	Unit	Condition	Note
Transmitter Output Optical Power, 1 mm POF	P_T	-9.5 -10.4	-7.0	-4.8 -4.3	dBm	$I_{F,dc}$ = 20 mA, 25°C 0-70°C	Note 3
Transmitter Output Optical Power, 1 mm POF	P_T	-6.0 -6.9	-3.0	-0.5 -0.0	dBm	$I_{F,dc}$ = 60 mA, 25°C 0-70°C	Note 3
Transmitter Output Optical Power, 200 µm HCS®	P_T	-14.6 -15.5	-13.0	-10.5 -10.0	dBm	$I_{F,dc}$ = 60 mA, 25°C 0-70°C	Note 3
Output Optical Power Temperature Coefficient	$\frac{\Delta P_T}{\Delta T}$		-0.02		dB/°C		
Peak Emission Wavelength	λ_{PK}	640	650	660	nm		
Peak Wavelength Temperature Coefficient	$\frac{\Delta \lambda}{\Delta T}$		0.12		nm/°C		
Spectral Width	FWHM		21		nm	Full Width, Half Maximum	
Forward Voltage	V_F	1.8	2.1	2.4	V	I_F = 60 mA	
Forward Voltage Temperature Coefficient	$\frac{\Delta V_F}{\Delta T}$		-1.8		mV/°C		
Transmitter Numerical Aperture	NA		0.5				
Thermal Resistance, Junction to Case	θ_{jc}		140		°C/W		Note 4
Reverse Input Breakdown Voltage	V_{BR}	3.0	13		V	$I_{F,dc}$ = -10 µA	
Diode Capacitance	C_O		60		pF	V_F = 0 V, f = 1 MHz	
Unpeaked Optical Rise Time, 10% - 90%	t_r		12		ns	I_F = 60 mA f = 100 kHz	Figure 1 Note 5
Unpeaked Optical Fall Time, 90% - 10%	t_f		9		ns	I_F = 60 mA f = 100 kHz	Figure 1 Note 5

Notes:

1. 1.6 mm below seating plane.
2. Typical data is at 25°C.
3. Optical Power measured at the end of 0.5 meter of 1 mm diameter plastic or 200 µm diameter hard clad silica optical fiber with a large area detector.
4. Typical value measured from junction to PC board solder joint for horizontal mount package, HFBR-1527. θ_{jc} is approximately 30°C/W higher for vertical mount package, HFBR-1537.
5. Optical rise and fall times can be reduced with the appropriate driver circuit; refer to Application Note 1066.
6. Pins 5 and 8 are primarily for mounting and retaining purposes, but are electrically connected; pins 3 and 4 are electrically unconnected. It is recommended that pins 3, 4, 5, and 8 all be connected to ground to reduce coupling of electrical noise.
7. Refer to the Versatile Link Family Fiber Optic Cable and Connectors Technical Data Sheet for cable connector options for 1 mm plastic optical fiber and 200 µm HCS fiber.
8. The LED current peaking necessary for high frequency circuit design contributes to electromagnetic interference (EMI). Care must be taken in circuit board layout to minimize emissions for compliance with governmental EMI emissions regulations. Refer to Application Note 1066 for design guidelines.

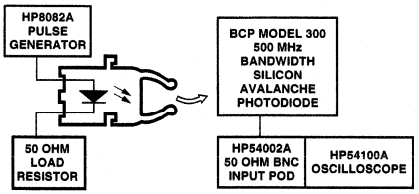


Figure 1. Test Circuit for Measuring Unpeaked Rise and Fall Times.

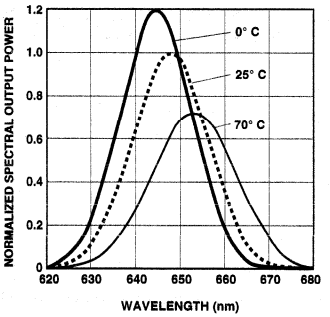


Figure 2. Typical Spectra Normalized to the 25°C Peak.

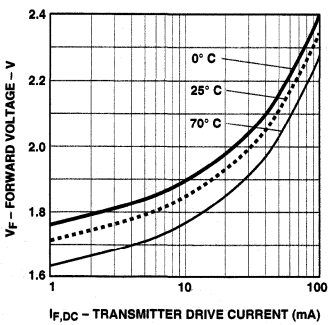


Figure 3. Typical Forward Voltage vs. Drive Current.

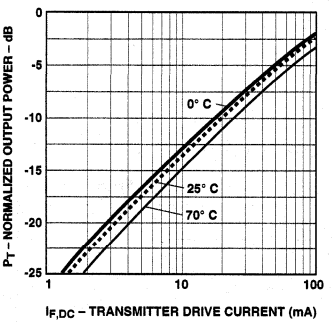


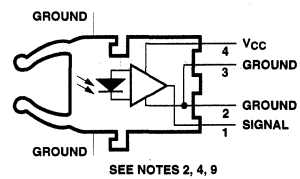
Figure 4. Typical Normalized Output Optical Power vs. Drive Current.

125 Megabaud Versatile Link Receiver

HFBR-25X6 Series

Description

The HFBR-25X6 receivers contain a PIN photodiode and transimpedance pre-amplifier circuit in a horizontal (HFBR-2526) or vertical (HFBR-2536) blue housing, and are designed to interface to 1mm diameter plastic optical fiber or 200 μm hard clad silica glass optical fiber. The receivers convert a received optical signal to an analog output voltage. Follow-on circuitry can optimize link performance for a variety of distance and data rate requirements. Electrical bandwidth greater than 65 MHz allows design of high speed data links with plastic or hard clad silica optical fiber. Refer to Application Note 1066 for details for recommended interface circuits.



Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Reference
Storage Temperature	T_S	-40	+75	°C	
Operating Temperature	T_A	0	+70	°C	
Lead Soldering Temperature			260	°C	Note 1
Cycle Time			10	s	
Signal Pin Voltage	V_O	-0.5	V_{CC}	V	
Supply Voltage	V_{CC}	-0.5	6.0	V	
Output Current	I_O		25	mA	

CAUTION: The small junction sizes inherent to the design of this component increase the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Electrical/Optical Characteristics 0 to 70°C; 5.25 V ≥ V_{CC} ≥ 4.75 V; power supply must be filtered (see Figure 1, Note 2).

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition	Note
AC Responsivity 1 mm POF	$R_{P,APF}$	1.7	3.9	6.5	mV/μW	650 nm	Note 4
AC Responsivity 200 μm HCS	$R_{P,HCS}$	4.5	7.9	11.5	mV/μW		
RMS Output Noise	V_{NO}		0.46	0.69	mV_{RMS}		Note 5
Equivalent Optical Noise Input Power, RMS - 1 mm POF	$P_{N,RMS}$		- 39	-36	dBm		Note 5
Equivalent Optical Noise Input Power, RMS - 200 μm HCS	$P_{N,RMS}$		-42	-40	dBm		Note 5
Peak Input Optical Power - 1 mm POF	P_R			-5.8 -6.4	dBm dBm	5 ns PWD 2 ns PWD	Note 6
Peak Input Optical Power - 200 μm HCS	P_R			-8.8 -9.4	dBm dBm	5 ns PWD 2 ns PWD	Note 6
Output Impedance	Z_O		30		Ω	50 MHz	Note 4
DC Output Voltage	V_O	0.8	1.8	2.6	V	P_R = 0 μW	
Supply Current	I_{CC}		9	15	mA		
Electrical Bandwidth	BW_E	65	125		MHz	-3 dB electrical	
Bandwidth * Rise Time			0.41		Hz * s		
Electrical Rise Time, 10-90%	t_r		3.3	6.3	ns	P_R = -10 dBm peak	
Electrical Fall Time, 90-10%	t_f		3.3	6.3	ns	P_R = -10 dBm peak	
Pulse Width Distortion	PWD		0.4	1.0	ns	P_R = -10 dBm peak	Note 7
Overshoot			4		%	P_R = -10 dBm peak	Note 8

Notes:

1. 1.6 mm below seating plane.
2. The signal output is an emitter follower, which does not reject noise in the power supply. The power supply must be filtered as in Figure 1.
3. Typical data are at 25°C and V_{CC} = +5 Vdc.
4. Pin 1 should be ac coupled to a load ≥ 510 Ω with load capacitance less than 5 pF.
5. Measured with a 3 pole Bessel filter with a 75 MHz, -3dB bandwidth.
6. The maximum Peak Input Optical Power is the level at which the Pulse Width Distortion is guaranteed to be less than the PWD listed under Test Condition. $P_{R,Max}$ is given for PWD = 5 ns for designing links at ≤ 50 MBd operation, and also for PWD = 2 ns for designing links up to 125 MBd (for both POF and HCS input conditions).
7. 10 ns pulse width, 50% duty cycle, at the 50% amplitude point of the waveform.
8. Percent overshoot is defined at:

$$\frac{(V_{PK} - V_{100\%})}{V_{100\%}} \times 100\%$$

9. Pins 5 and 8 are primarily for mounting and retaining purposes, but are electrically connected. It is recommended that these pins be connected to ground to reduce coupling of electrical noise.
10. If there is no input optical power to the receiver (no transmitted signal) electrical noise can result in false triggering of the receiver. In typical applications, data encoding and error detection prevent random triggering from being interpreted as valid data. Refer to Application Note 1066 for design guidelines.

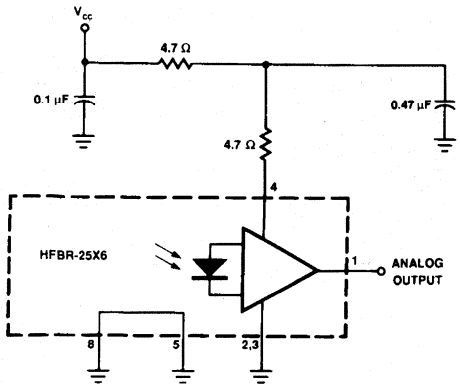


Figure 1. Recommended Power Supply Filter Circuit.

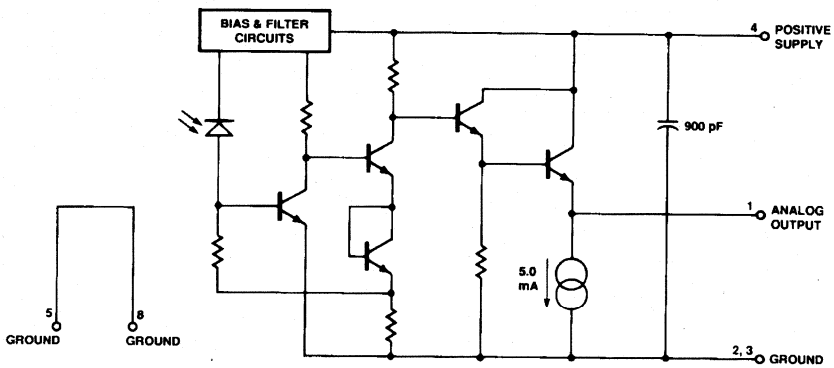


Figure 2. Simplified Receiver Schematic.

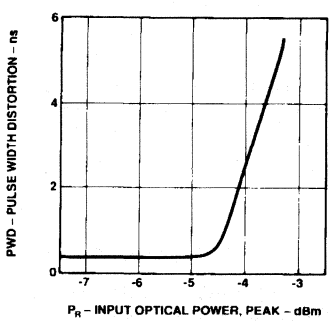


Figure 3. Typical Pulse Width Distortion vs. Peak Input Power.

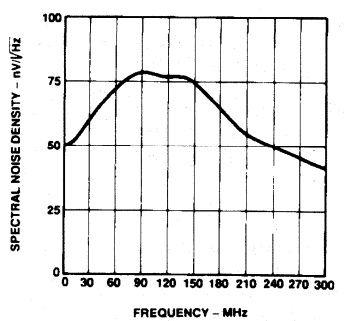


Figure 4. Typical Output Spectral Noise Density vs. Frequency.

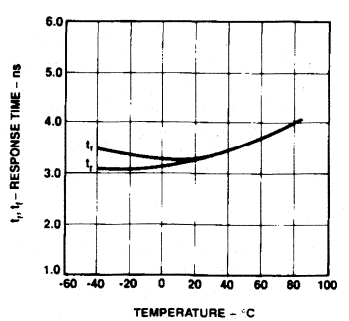
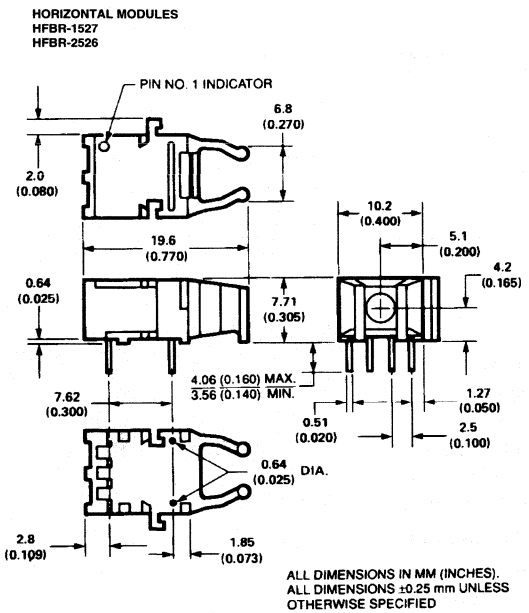
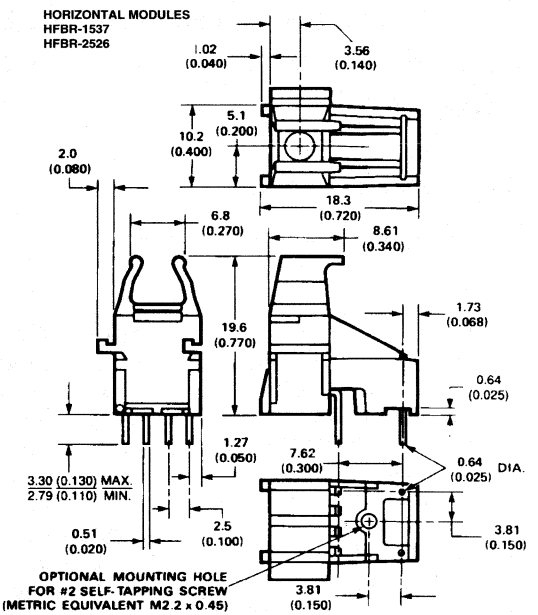


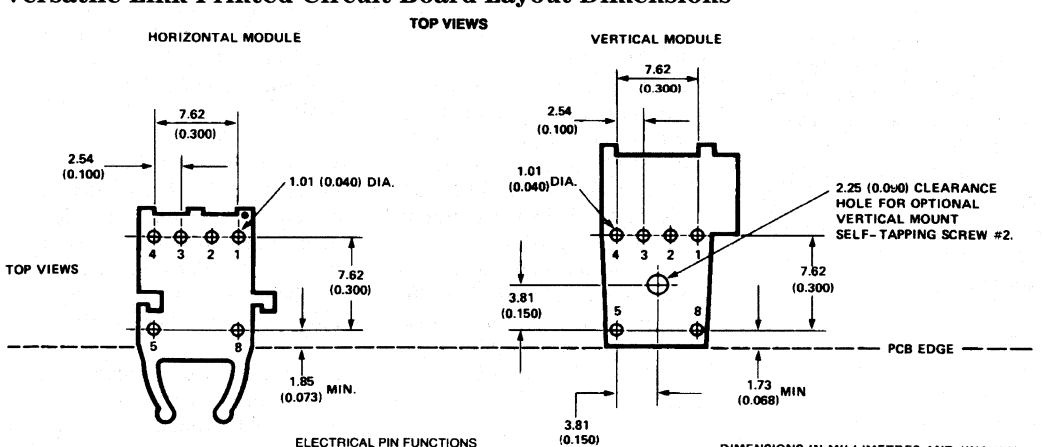
Figure 5. Typical Rise and Fall Time vs. Temperature..

Versatile Link Mechanical Dimensions





Versatile Link Printed Circuit Board Layout Dimensions



ELECTRICAL PIN FUNCTIONS

PIN NO.	TRANSMITTERS HFBR-15X7	RECEIVERS HFBR-25X6
1	ANODE	SIGNAL
2	CATHODE	GROUND
3	GROUND*	GROUND
4	GROUND*	V_{CC} (+5 V)
5	GROUND**	GROUND**
8	GROUND**	GROUND**

*NO INTERNAL CONNECTION.
**PINS 5 AND 8 CONNECTED INTERNALLY TO EACH OTHER ONLY.

DIMENSIONS IN MILLIMETRES AND (INCHES)

HEWLETT® PACKARD

10 Megabaud Versatile Link Fiber Optic Transmitter and Receiver for 1 mm POF and 200 µm HCS®

Technical Data

HFBR-0508 Series
HFBR-1528 Transmitter
HFBR-2528 Receiver

Features

- **Data Transmission at Signal Rates of dc to 10 MBd**
- **Up to 50 Meters Distances with 1 mm Plastic Optical Fiber (POF)**
- **Up to 500 Meters Distances with 200 µm Hard Clad Silica (HCS®)**
- **Wide Dynamic Range Receiver Allows Operation from Zero to Maximum Link Distance with a Single Transmitter Drive Current**
- **Link Distances Specified for Variations in Temperature, Power Supply, and Fiber Attenuation**
- **DC Coupled Receiver with CMOS/TTL Output for Easy Designs: No Data Encoding or Digitizing Circuitry Required**
- **Pulse Width Distortion Controlled to Limit Distortion from Low Duty Cycle or Burst Mode Data**
- **High Noise Immunity**
- **Compatible with HP's Versatile Link Family of Connectors, for Easy Termination of Fiber**

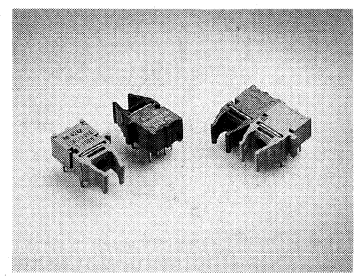
Applications

- **Industrial Control and Factory Automation**
- **Serial Field Buses**
- **Intra-System Links; Board-to-Board, Rack-to-Rack**
- **Extension of RS-232, RS-485**
- **Elimination of Ground Loops**
- **High Voltage Isolation**
- **Reduces Voltage Transient Susceptibility**

Description

The HFBR-0508 Series consists of a fiber-optic transmitter and receiver operating at a 650 nm wavelength (red). The HFBR-1528 transmitter is an LED in a low cost plastic housing designed to efficiently couple power into 200 µm diameter HCS and 1 mm diameter POF. The HFBR-2528 receiver incorporates a PIN detector and digital output IC compatible with CMOS and TTL logic families.

HFBR-0508 links operate from DC to 10 MBd at distances up to 50 meters with 1 mm POF and up to 500 meters with 200 µm HCS®. No minimum link distances are required when using recommended circuits, simplifying design.



Versatile Link components can be interlocked (N-plexed together) to minimize space and to provide dual connections with the duplex connectors. Up to eight packages can be interlocked and inserted into a printed circuit board.

POF and HCS are available in preconnectored lengths or can be easily field-terminated. A single transmitter drive current for POF and HCS allows both fibers to be used with a single design.

HCS® is a registered trademark of SpecTran Corporation.

CAUTION:. It is advised that normal static precautions be taken in handling and assembly of these components to prevent damage and/or degradation which may be induced by ESD.

HFBR-0508 Series 10 MBd Data Link

Typical Link Performance, T_A = +25°C

Parameter	Symbol	Typ.[1]	Unit	Condition	Note
Signaling Rate	f_S	15	Mb/s	NRZ	2
Link Distance with Extra Low Loss POF Cable	ℓ	100	m	10 MBd	2, 3, 5
Link Distance with 200 µm HCS Cable	ℓ	900	m	10 MBd	2, 4, 5

Specified Link Performance, T_A = -20° to +85°C, DC to 10 MBd, unless otherwise noted

Parameter	Symbol	Min.	Max.	Unit	Condition	Note
Signaling Rate	f_S	DC	10	Mb/s	NRZ	2
Link Distance with Extra Low Loss POF Cable	ℓ	0.1 0.1 0.1	50 40 30	m	+25°C 0 to +70°C -20 to +85°C	2, 3, 5
Link Distance with 200 µm HCS Cable	ℓ	0.1 0.1 0.1	500 300 100	m	+25°C 0 to +70°C -20 to +85°C	2, 4, 5
Pulse Width Distortion	PWD	-30	+30	ns	25 – 75% Duty Cycle	2
		-50	+50	ns	Arbitrary Duty Cycle	

Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Unit	Note
Storage and Operating Temperature, Transmitter		$T_{S,O}$	-40	+85	°C	
Storage and Operating Temperature, Receiver		$T_{S,O}$	-20	+85	°C	
Receiver Supply Voltage		V_{CC}	-0.5	+5.5	V	
Receiver Average Output Current		$I_{O,AVG}$	-16	+16	mA	
Receiver Output Power Dissipation		P_{OD}		80	mW	
Transmitter Peak Forward Input Current		$I_{F,PK}$		90	mA	6
Transmitter Average Forward Input Current		$I_{F,AVG}$		60	mA	
Transmitter Reverse Input Voltage		V_R		3	V	
Lead Soldering Cycle	Temp	T_{SOL}		+260	°C	7
	Time			10	sec	7

Recommended Operating Conditions

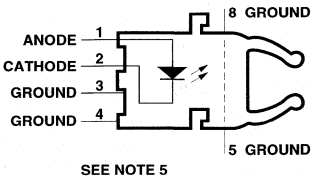
Parameter	Symbol	Min.	Max.	Unit	Condition	Note
Ambient Temperature	T_A	-20	+85	°C		
Power Supply Voltage	V_{CC}	4.75	5.25	V	<100 mV_{p-p} Noise	
Transmitter Peak Forward Current	$I_{F,PK}$	20	90	mA		6
Transmitter Average Forward Current	$I_{F,AV}$		60	mA		
Fanout (7400 Series TTL)	N		1			

Notes:

1. Typical data at 25°C, V_{CC} = 5 V.
2. With recommended transmitter and receiver application circuits (60 mA nominal drive current).
3. POF is HFBR-R/EXXYYY plastic (1 mm) optical fiber. Worst case attenuation used (0.23 dB/m from -40°C to +85°C at 660 nm).
4. HCS is HFBR-H/VXXYYY hard clad silica (200/230 µm) fiber. Worst case attenuation is used (10 dB/km from 0°C to +70°C and 12 dB/km from -40°C to +85°C at 650 nm).
5. BER ≤ 10^{-9}, 2^{23} - 1 PRBS NRZ 10 MBd.
6. For $I_{F,PK}$ > 60 mA, the duty factor must maintain $I_{F,AV}$ ≤ 60 mA and pulse with ≤ 1 µs.
7. 1.6 mm below seating plane.

HFBR-1528 Transmitter

The HFBR-1528 transmitter incorporates a 650 nm LED in a light gray, nonconductive plastic housing. The high light output power enables the use of both plastic optical fiber (POF) and Hard Clad Silica (HCS) fiber. This transmitter can be operated up to 10 MBd using a simple driver circuit. The HFBR-1528 is compatible with all Versatile Link connectors.



HFBR-1528 Transmitter, Top View

Electrical and Optical Characteristics: T_A = -40° to +85°C unless otherwise noted.

Parameter	Symbol	Min.	Typ.[1]	Max.	Units	T_A (°C)	Conditions	Note
Peak Output Power 1 mm POF, 60 mA	P_T	-6.0	-3.5	0.0	dBm	+25	$I_{F,dc}$ = 60 mA	2, 3 Fig. 2
		-6.9		+0.5		0 to +70		
		-7.2		+1.3		-40 to +85		
Peak Output Power 1 mm POF, 20 mA	P_T	-15.6	-9.0	-2.0	dBm	+25	$I_{F,dc}$ = 20 mA	2, 3 Fig. 2
		-16.5		-1.5		0 to +70		
		-16.8		-0.7		-40 to +85		
Peak Output Power 200 µm HCS, 60 mA	P_T	-16.1	-12.5	-8.5	dBm	+25	$I_{F,dc}$ = 60 mA	2, 3 Fig. 2
		-17.0		-8.0		0 to +70		
		-17.3		-7.2		-40 to +85		
Optical Power Temperature Coefficient	$\Delta P_T/\Delta T$		-0.40		%/°C			
			-0.02		dB/°C			
Peak Emission Wavelength	λ_P	640	650	660	nm	0 to +70		Fig. 3
		635		662		-40 to +85		
Peak Wavelength Temperature Coefficient	$\Delta\lambda/\Delta T$		0.12		nm/°C			
Spectral Width	FWHM		21		nm			Fig. 3
Forward Voltage	V_F	1.8	2.1	2.65	V		$I_{F,dc}$ = 60 mA	Fig. 1
Forward Voltage Temperature Coefficient	$\Delta V_F/\Delta T$		-1.8		mV/°C			Fig. 1
Reverse Input Breakdown Voltage	V_{BR}	3.0	13		V		$I_{F,dc}$ = -10 µA	
Diode Capacitance	C_O		60		pF		V_F = 0 V, f = 1 MHz	
Transmitter Numerical Aperture	NA		0.5					
Thermal Resistance, Junction to Case	θ_{jc}		140		°C/W			4
50 Ω Optical Rise Time	t_r		13		ns		10% to 90%, I_F = 60 mA	
50 Ω Optical Fall Time	t_f		10		ns			

Notes:

1. Typical data are at 25°C.
2. Optical power measured at the end of 0.5 meters of 1 mm diameter plastic or 200 µm diameter hard clad silica fiber with a large area detector.
3. Minimum and maximum values for P_T over temperature are based on a fixed drive current. The recommended drive circuit has temperature compensation which reduces the variation in P_T over temperature; refer to Figures 4 and 6.
4. Typical value measured from junction to PC board solder joint for horizontal mount package, HFBR-1528.
5. Pins 5 and 8 are for mounting and retaining purposes, but are electrically connected; pins 3 and 4 are electrically isolated. It is recommended that pins 3, 4, 5 and 8 all be connected to ground to reduce coupling of electrical noise.
6. Refer to the "Plastic Optical Fiber and HCS Fiber Cable and Connectors for Versatile Link" Technical Data Sheet for cable connector options for 1 mm plastic and 200 µm HCS optical fiber.

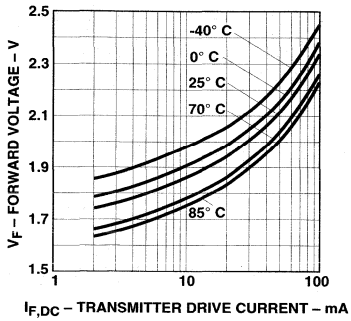


Figure 1. Typical Forward Voltage vs. Drive Current.

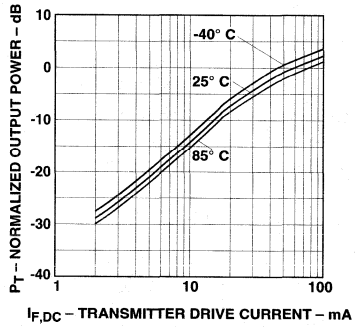


Figure 2. Typical Normalized Optical Power vs. Drive Current.

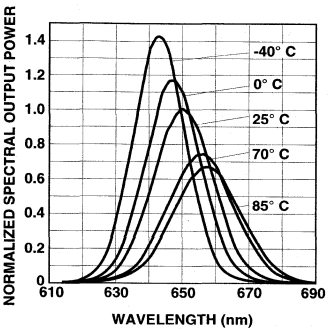


Figure 3. Typical Normalized Optical Spectra.

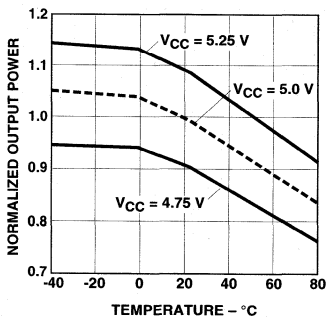


Figure 4. Typical Normalized Optical Power vs. Temperature (in Recommended Drive Circuit).

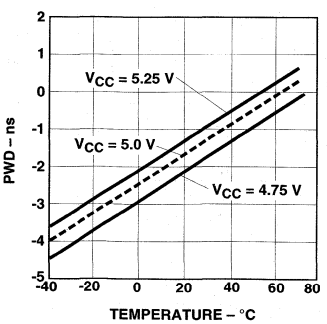


Figure 5. Typical Optical Pulse Width Distortion vs. Temperature and Power Supply Voltage (in Recommended Drive Circuit).

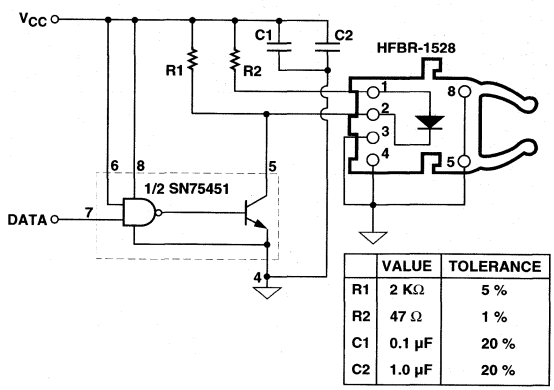


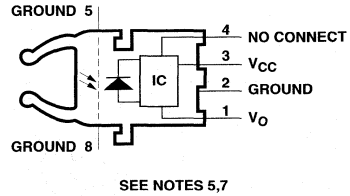
Figure 6. Recommended Transmitter Drive Circuit ($I_{F,on}$ = 60 mA Nominal at T_A = 25°C).

WARNING: WHEN VIEWED UNDER SOME CONDITIONS, THE OPTICAL PORT MAY EXPOSE THE EYE BEYOND THE MAXIMUM PERMISSIBLE EXPOSURE RECOMMENDED IN ANSI Z136.2, 1993. UNDER MOST VIEWING CONDITIONS THERE IS NO EYE HAZARD.

HFBR-2528 Receiver

The HFBR-2528 receiver consists of a silicon PIN photodiode and digitizing IC to produce a logic compatible output. The IC includes a unique circuit to correct the pulse width distortion of the first bit after a long idle period. This enables operation from DC to 10 MBd with low PWD for arbitrary data patterns.

The receiver output is a "push-pull" stage compatible with TTL and CMOS logic. The receiver housing is a dark, conductive plastic, compatible with all Versatile Link connectors.



SEE NOTES 5,7

HFBR-2528 Receiver, Top View

Electrical and Optical Characteristics: T_A = -20° to +85°C, 4.75 V < V_{CC} < 5.25 V, unless otherwise noted.

Parameter	Symbol	Min.	Typ.[1]	Max.	Unit	T_A (°C)	Condition	Note	Fig.
Peak POF Sensitivity: Minimum Input for Logic "0"	$P_{RL,min}$		-23.0	-21.0 -20.0 -19.5	dBm	+25 0 to +70 -20 to +85	1 mm POF, |PWD| < 30 ns	2,6	2,4
Peak POF Overdrive Limit:Maximum Input for Logic "0"	$P_{RL,max}$	+1.0 +0.0 -1.0	+5.0		dBm	+25 0 to +70 -20 to +85	1 mm POF, |PWD| < 30 ns	2,3, 6	1,2, 3
Peak POF Off State Limit: Maximum Input for Logic "1"	$P_{RH,max}$			-42	dBm		1 mm POF	2,6, 8	
Peak HCS Sensitivity: Minimum Input for Logic "0"	$P_{RL,min}$		-25.0	-23.0 -22.0 -21.5	dBm	+25 0 to +70 -20 to +85	200 µm HCS, |PWD| < 30 ns	2,6	
Peak HCS Overdrive Limit: Maximum Input for Logic "0"	$P_{RL,max}$	-1.0 -2.0 -3.0	+3.0		dBm	+25 0 to +70 -20 to +85	200 µm HCS, |PWD| < 30 ns	2,3, 6	
Peak HCS Off State Limit: Maximum Input for Logic "1"	$P_{RH,max}$			-44	dBm		200 µm HCS	2,6, 8	
Supply Current	I_{CC}		27	45	mA		V_O = Open		
High Level Output Voltage	V_{OH}	4.2	4.7		V		I_O = -40 µA		
Low Level Output Voltage	V_{OL}		0.22	0.4	V		I_O = +1.6 mA		
Output Rise Time	t_r		12	30	ns		C_L = 10 pF	6	
Output Fall Time	t_f		10	30	ns		C_L = 10 pF	6	
Thermal Resistance, Junction to Case	θ_{jc}		200		°C/W			4	
Electric Field Immunity	E_{MAX}		8		kV/m		Near Field, Electrical Field Source	5	
Power Supply Noise Immunity	PSNI	0.1	0.4		V_{pp}		Sine Wave DC - 10 MHz	6	

Notes:

1. Typical data are at 25°C, V_{CC} = 5.0 V.
2. Input power levels are for peak (not average) optical input levels. For 50% duty cycle data, peak optical power is twice the average optical power.
3. Receiver overdrive ($P_{RL,max}$) is specified as the limit where |PWD| will not exceed 30 ns. The receiver will be in the correct state (logic "0") for optical powers above $P_{RL,max}$. However, it may not meet a 30% symbol period PWD if the overdrive limit is exceeded. Refer to Figure 2 for PWD performance at high received optical powers.
4. Typical value measured from junction to PC board solder joint for horizontal mount package, HFBR-2528.
5. Pins 5 and 8 are electrically connected to the conductive housing and are also used for mounting and retaining purposes. It is required that pins 5 and 8 be connected to ground to maintain conductive housing shield effectiveness.
6. In recommended receiver circuit, with an optical signal from the recommended transmitter circuit.
7. Pin 4 is electrically isolated internally. Pin 4 may be externally connected to pin 1 for board layout compatibility with HFBR-25X1, HFBR-25X2 and HFBR-25X4. Otherwise it is recommended pin 4 be grounded as in Figure 5.
8. BER ≤ 10E-9, includes a 10.8 dB margin below the receiver switching threshold level (signal to noise ratio = 12).

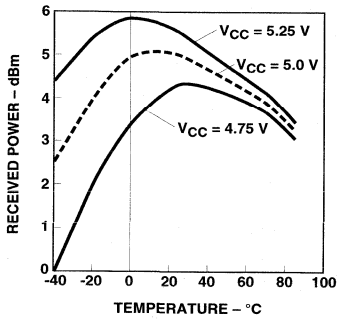


Figure 1. Typical POF Receiver Overdrive, $P_{RL,max}$, at 10 MBd, vs. Temperature and Power Supply Voltage.

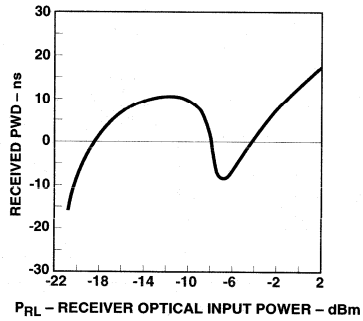


Figure 2. Typical POF Receiver Pulse Width Distortion vs. Optical Power at 10 MBd.

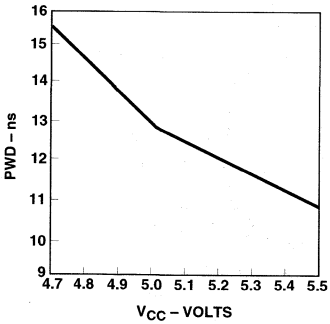


Figure 3. Typical POF Receiver Pulse Width Distortion vs. Power Supply Voltage at High Optical Power (0 dBm,pk, 10 MBd).

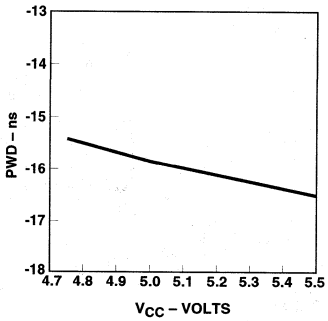
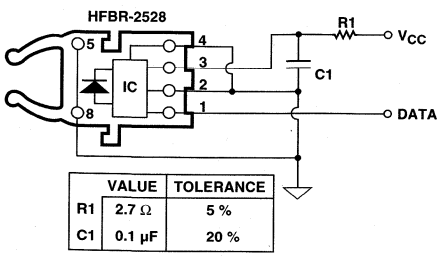


Figure 4. Typical POF Receiver Pulse Width Distortion vs. Power Supply Voltage at Low Optical Power, (-21 dBm,pk, 10 MBd).



	VALUE	TOLERANCE
R1	2.7 Ω	5 %
C1	0.1 µF	20 %

Figure 5. Recommended Receiver Application Circuit.

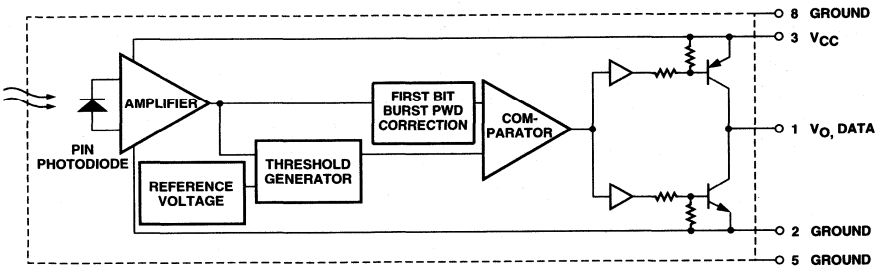
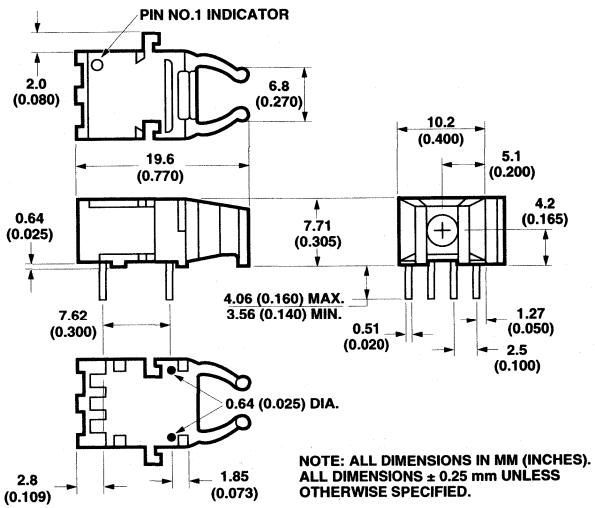


Figure 6. HFBR-2528 Receiver Block Diagram.

Versatile Link Mechanical Dimensions



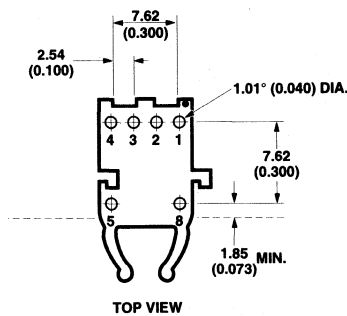
NOTE: ALL DIMENSIONS IN MM (INCHES).
ALL DIMENSIONS ± 0.25 mm UNLESS OTHERWISE SPECIFIED.

ELECTRICAL PIN FUNCTIONS

PIN NO.	TRANSMITTER HFBR-1528	RECEIVER HFBR-2528
1	ANODE	SIGNAL, V_O
2	CATHODE	GROUND
3	GROUND*	V_{CC} (+5 V)
4	GROUND*	GROUND*
5	GROUND**	GROUND**
8	GROUND**	GROUND**

* NO INTERNAL CONNECTION, GROUND CONNECTION RECOMMENDED.
** PINS 5 AND 8 CONNECTED INTERNALLY TO EACH OTHER.

Versatile Link Printed Circuit Board Layout Dimensions



HEWLETT® PACKARD

SERCOS Fiber Optic Transmitters and Receiver

Technical Data

HFBR-0600 Series

Features

- **Fully Compliant to SERCOS Optical Specifications**
- **Optimized for 1 mm Plastic Optical Fiber**
- **Compatible with SMA Connectors**
- **Auto-Insertable and Wave Solderable**
- **Data Transmission at Symbol Rates from DC to over 2 MBd for Distances from 0 to over 20 Metres**

Applications

- **Industrial Control Data Links**
- **Reduction of Lightning and Voltage Transient Susceptibility**
- **Tempest-Secure Data Processing Equipment**
- **Isolation in Test and Measurement Instruments**
- **Robotics Communication**

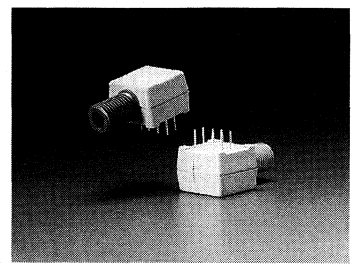
SERCOS

SERCOS is a SErial Realtime COmmunication System, a standard digital interface for communication between controls and drives for numerically controlled machines. The SERCOS interface specification was written by a joint working group of the VDW (German Machine Tool Builders Association) and ZVEI (German Electrical and Electronic Manufacturer's Association) to allow data exchange between NC controls and drives via fiber optic rings, with isolation and noise immunity. The HFBR-0600 family of fiber optic transmitters and receivers comply to the SERCOS specifications for transmitter and receiver optical characteristics and connector style (SMA).

Description

The HFBR-0600 components are capable of operation at symbol rates from DC to over 2 MBd and distances from 0 to over 20 metres. The HFBR-1602 and HFBR-1604 transmitters contain a 655-nm AlGaAs emitter capable of efficiently launching optical power into 1000 µm plastic optical fiber. The optical output is specified at the end of 0.5 m of plastic optical fiber.

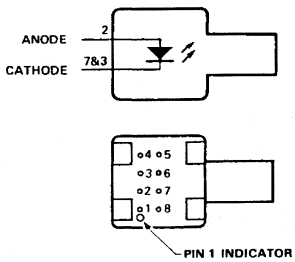
The HFBR-1604 is a selected version of the HFBR-1602, with power specified to meet the SERCOS high attenuation specifications.



The HFBR-2602 receiver incorporates an integrated photo IC containing a photodetector and dc amplifier driving an open-collector Schottky output transistor. The HFBR-2602 is designed for direct interfacing to popular logic families. The absence of an internal pull-up resistor allows the open-collector output to be used with logic families such as CMOS requiring voltage excursions higher than V_{CC}. The HFBR-2602 has a dynamic range of 15 dB.

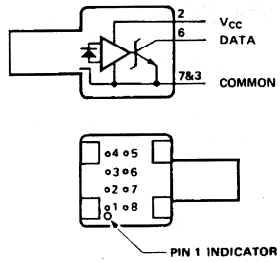
CAUTION: The small junction sizes inherent to the design of this component increase the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

HFBR-160X Transmitters



Pin	Function
1*	N.C.
2	ANODE
3	CATHODE
4*	N.C.
5*	N.C.
6	N.C.
7**	CATHODE
8*	N.C

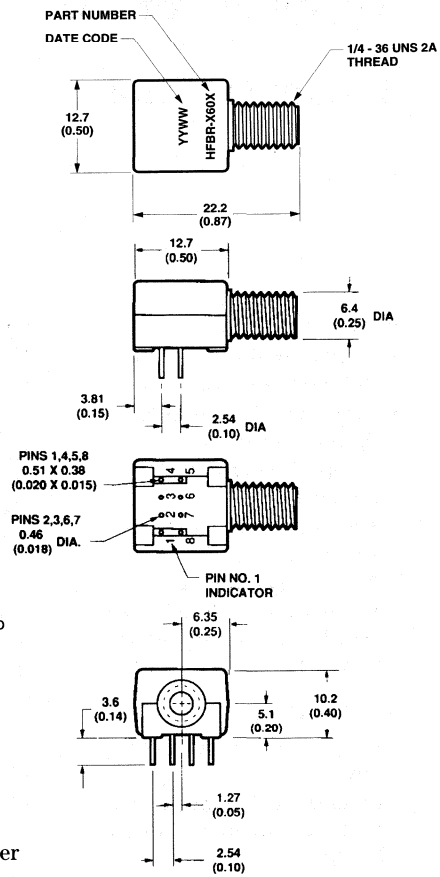
HFBR-2602 Receiver



Pin	Function
1*	N.C.
2	V_{CC} (5 V)
3	COMMON
4*	N.C.
5*	N.C.
6	DATA
7	COMMON
8*	N.C.

*Pins 1, 4, 5, and 8 are isolated from the internal circuitry, but electrically connected to one another.
**Transmitter Pin 7 may be left unconnected if necessary.

HFBR-0600 SMA Series Mechanical Dimensions



In the receiver, both the open-collector "Data" output Pin 6 and V_{CC} Pin 2 are referenced to "Common" Pin 3 and 7. It is essential that a bypass capacitor (0.1 µF ceramic) be connected from Pin 2 (V_{CC}) to Pin 3 (circuit common) of the receiver.

SMA is an industry standard fiber optic connector, available from many fiber optic connector suppliers. HFBR-4401 is a kit consisting of 100 nuts and 100 washers for panel mounting the HFBR-0600 components.

HFBR-1602/1604 Transmitters

Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Unit	Reference
Storage Temperature		T_S	-55	85	°C	
Operating Temperature		T_A	-40	85	°C	
Lead Soldering Cycle	Temp.			260	°C	Note 1
	Time			10	s	Note 1
Forward Input Current Peak		I_{FPK}		120	mA	
Forward Input Current Average		I_{Favg}		60	mA	
Reverse Input Voltage		V_{BR}		-5	V	

Electrical/Optical Characteristics 0 to 55°C, unless otherwise stated

Parameter	Symbol	Min.	Typ.[2]	Max.	Unit	Condition	Reference
Forward Voltage	V_F	1.5	1.9	2.2	V	I_F = 35 mA	
Forward Voltage Temp. Coefficient	$\Delta V_F/\Delta T$		-1.2		mV/°C	I_F = 35 mA	
Reverse Input Voltage	V_{BR}	-5.0	-18		V	I_R = 100 µA	
Peak Emission Wavelength	λ_P	640	655	675	nm		
Full Width Half Maximum	FWHM		20	30	nm	25°C	
Diode Capacitance	C_T		30		pF	V_F = 0 f = 1 MHz	
Optical Power Temp. Coefficient	$\Delta P_T/\Delta T$		- 0.01		dBm/°C	I_F = 35 mA	
Thermal Resistance	θ_{JA}		330		°C/W		Notes 3, 4
Peak Optical Output Power of HFBR-1602	P_{T1602}	-10.5		-5.5	dBm	I_F = 35 mA	Notes 5, 6, 11
Peak Optical Output Power of HFBR-1604	P_{T1604}	-7.5 -10.5		-3.5 -5.5	dBm dBm	I_F = 60 mA I_F = 35 mA	Notes 5, 6, 11
Rise Time (10% to 90%)	t_r		57 50		ns ns	I_F = 60 mA I_F = 35 mA	
Fall Time (90% to 10%)	t_f		40 27		ns ns	I_F = 60 mA I_F = 35 mA	

HFBR-2602 Receiver

Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Unit	Reference
Storage Temperature		T_S	-55	85	°C	
Operating Temperature		T_A	-40	85	°C	
Lead Soldering Cycle	Temp.			260	°C	Note 1
	Time			10	s	Note 1
Supply Voltage		V_{CC}	-0.5	7.0	V	
Output Current		I_O		25	mA	
Output Voltage		V_O	-0.5	18.0	V	
Output Collector Power Dissipation		$P_{O\,AVG}$		40	mW	
Fan Out (TTL)		N		5		Note 8

Electrical/Optical Characteristics 0 to 55°C;
Fiber core diameter ≤ 1.0 mm, fiber N.A. ≤ 0.5, 4.75 V ≤ V_{CC} ≤ 5.25 V

Parameter	Symbol	Min.	Typ.[2]	Max.	Unit	Condition	Reference
High Level Output Current	I_{OH}		5	250	µA	V_{OH} = 18 V P_R < -31.2 dBm	
Low Level Output Voltage	V_{OL}		0.4	0.5	V	I_{OL} = 8 mA P_R > -20.0 dBm	
High Level Supply Current	I_{CCH}		3.5	6.3	mA	V_{CC} = 5.25 V P_R < -31.2 dBm	
Low Level Supply Current	I_{CCL}		6.2	10	mA	V_{CC} = 5.25 V P_R > -20.0 dBm	

Dynamic Characteristics 0 to 55°C unless otherwise specified; 4.75 V ≤ V_{CC} ≤ 5.25 V; BER ≤ 10^{-9}

Parameter	Symbol	Min.	Typ.[2]	Max.	Unit	Condition	Reference
Peak Input Power Level Logic HIGH	P_{RH}			-31.2	dBm	λ_P = 655 nm	Note 7
Peak Input Power Level Logic LOW	P_{RL}	-20.0		-5.0	dBm	I_{OL} = 8 mA	Note 7
Propagation Delay LOW to HIGH	t_{PLH}		60		ns	P_R = -20 dBm 2 MBd	Note 8, 9
Propagation Delay HIGH to LOW	t_{PHL}		110		ns	P_R = -20 dBm 2 MBd	Note 8, 9
Pulse Width Distortion, $t_{PLH} - t_{PHL}$	PWD		50 -50		ns ns	P_R = -5 dBm P_R = -20 dBm	Note 10 Figure 6

Notes:

1. 2.0 mm from where leads enter case.
2. Typical data at T_A = 25°C.
3. Thermal resistance is measured with the transmitter coupled to a connector assembly and fiber, and mounted on a printed circuit board.
4. Pins 2, 6, and 7 are welded to the cathode header connection to minimize the thermal resistance from junction to ambient. To further reduce the thermal resistance, the cathode trace should be made as large as is consistent with good RF circuit design.
5. P_T is measured with a large area detector at the end of 0.5 metre of plastic optical fiber with 1 mm diameter and numerical aperture of 0.5.
6. When changing µW to dBm, the optical power is referenced to 1 mW (1000 µW). Optical Power P(dBm) = 10 log [P (µW)/1000 µW].
7. Measured at the end of 1mm plastic fiber optic cable with a large area detector.
8. 8 mA load (5 x 1.6 mA), R_L = 560 Ω.
9. Propagation delay through the system is the result of several sequentially occurring phenomena. Consequently it is a combination of data-rate-limiting effects and of transmission-time effects. Because of this, the data-rate limit of the system must be described in terms of time differentials between delays imposed on falling and rising edges. As the cable length is increased, the propagation delays increase. Data-rate, as limited by pulse width distortion, is not affected by increasing cable length if the optical power level at the receiver is maintained.
10. Pulse width distortion is the difference between the delay of the rising and falling edges.
11. Both HFBR-1602 and HFBR-1604 meet the SERCOS "low attenuation" specifications when operated at 35 mA; only HFBR-1604 meets the SERCOS "high attenuation" limits when operated at 60 mA.

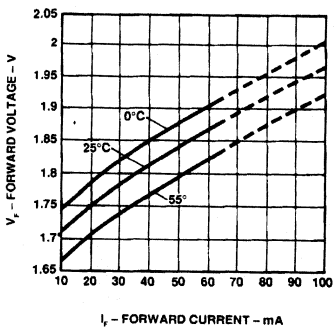


Figure 1. Forward Voltage and Current Characteristics.

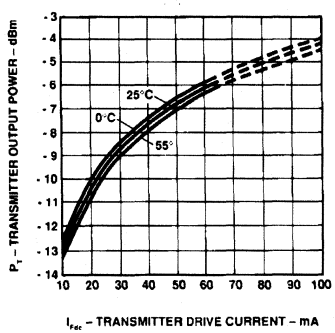


Figure 2. Typical Transmitter Output vs. Forward Current.

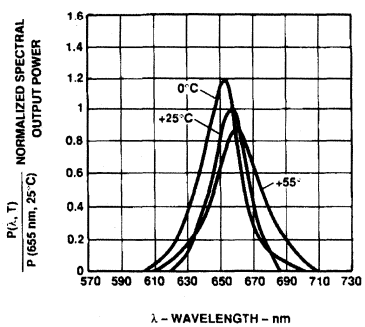


Figure 3. Transmitter Spectrum Normalized to the Peak at 25°C.

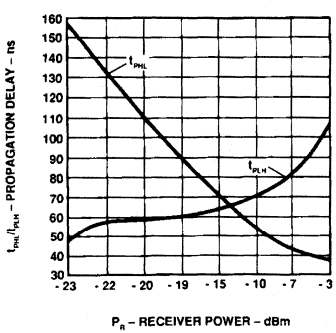


Figure 4. Typical Propagation Delay through System with 0.5 Metre of Cable.

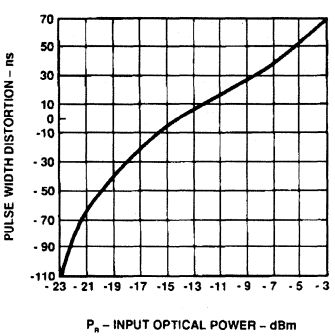


Figure 5. Typical HFBR-160X/2602 Link Pulsewidth Distortion vs Optical Power.

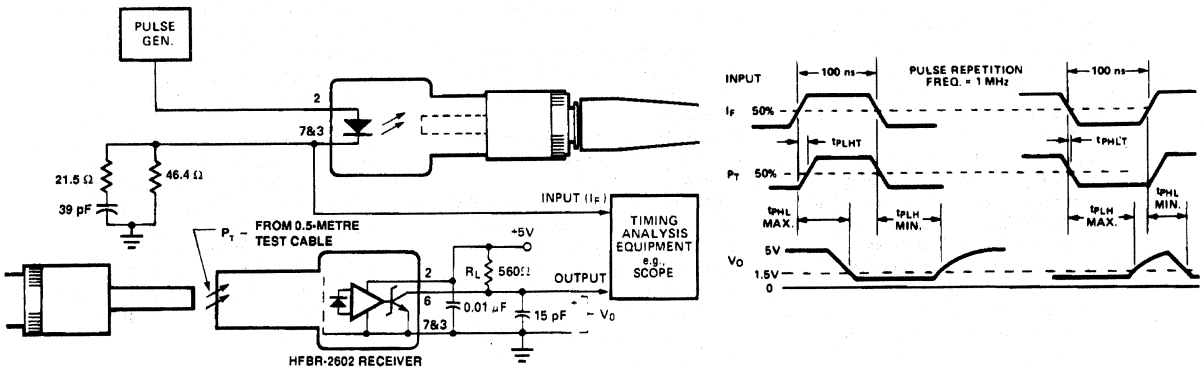


Figure 6. System Propagation Delay Test Circuit and Waveform Timing Definitions.

HEWLETT® PACKARD

Plastic Optical Fiber and HCS® Fiber Cable and Connectors for Versatile Link

Technical Data

HFBR-RXXYYY Series (POF)
HFBR-EXXYYY Series (POF)
HFBR-HXXYYY Series (HCS)
HFBR-VXXYYY Series (HCS)

Features

- **Compatible with HP Versatile Link Family of Connectors and Fiber Optic Components**
- **1 mm Diameter Plastic Optical Fiber (POF) in Two Grades: Low Cost Standard POF with 0.22 dB/m Typical Attenuation, or High Performance Extra Low Loss POF with 0.19 dB/m Typical Attenuation**
- **200 μm Diameter Hard Clad Silica (HCS®) Fiber with 8 dB/km Typical Attenuation, Riser or Plenum Rated Jackets, Superior Mechanical Strength**

Applications

- **Industrial Data Links for Factory Automation and Plant Control**
- **Intra-System Links; Board-to-Board, Rack-to-Rack**
- **Telecommunications Switching Systems**
- **Computer-to-Peripheral Data Links, PC Bus Extension**
- **Proprietary LANs**
- **Digitized Video**
- **Medical Instruments**
- **Reduction of Lightning and Voltage Transient Susceptibility**
- **High Voltage Isolation**

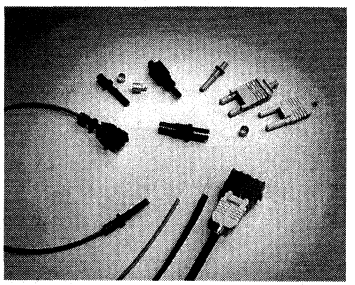
Cable Description

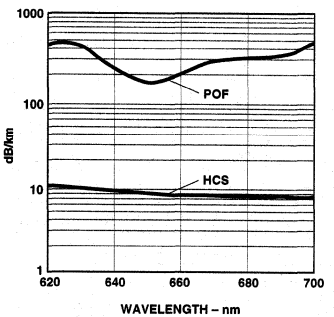
The HFBR-R/EXXYYY series of plastic fiber optic cables are constructed of a single step-index fiber sheathed in a black polyethylene jacket. The duplex fiber consists of two simplex fibers joined with a zipcord web.

Standard attenuation and extra low loss POF cables are identical except for attenuation specifications.

The HFBR-H/VXXYYYY series of hard clad silica fiber optic cables are constructed of a single step index pure silica HCS® fiber sheathed in a blue polyvinyl chloride jacket. The duplex fiber consists of two simplex fibers joined with a zipcord web. Riser and Plenum rated HCS® fiber cables are identical except for jacket materials.

Polyethylene jackets on all plastic fiber cables comply with UL VW-1 flame retardant specifications.





Typical POF and HCS Attenuation

PVC jackets on HCS® cables are either UL Riser rated or UL Plenum rated.

All series of cables are available in unconnectored or connectored options. Refer to the Ordering Guide for part number information.

HCS® is a registered trademark of SpecTran Corporation.

Plastic Optical Fiber Specifications: HFBR-R/EXXYYY

Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Unit	Note
Storage and Operating Temperature		$T_{S,O}$	-55	+85	°C	
Recommended Operating Temperature		T_O	-40	+85	°C	
Installation Temperature		T_I	-20	+70	°C	1
Short Term Tensile Force	Single Channel	F_T		50	N	2
	Dual Channel	F_T		100	N	
Short Term Bend Radius		r	25		mm	3, 4
Long Term Bend Radius		r	35		mm	
Long Term Tensile Load		F_T		1	N	
Flexing				1000	Cycles	4

Mechanical/Optical Characteristics, T_A = -40 to +85°C unless otherwise specified

Parameter		Symbol	Min.	Typ.[5]	Max.	Unit	Condition
Cable Attenuation	Standard Cable, Type "R"	α_O	0.15	0.22	0.27	dB/m	Source is HFBR-15XX (660 mm LED, 0.5 NA) ℓ = 50 meters
	Extra Low Loss, Type "E"		0.15	0.19	0.23		
Reference Attenuation	Standard Cable, Type "R"	α_R	0.12	0.19	0.24	dB/m	Source is 650 nm, 0.5 NA monochrometer, ℓ = 50 meters Note 7, Figure 1
	Extra Low Loss, Type "E"		0.12	0.16	0.19		
Numerical Aperture		NA	0.46	0.47	0.50		>2 meters
Diameter, Core and Cladding		D_C	0.94	1.00	1.06	mm	
Diameter, Jacket		D_J	2.13	2.20	2.27	mm	Simplex Cable
Propagation Delay Constant		l/v		5.0		ns/m	Note 6
Mass per Unit Length/Channel				5.3		g/m	Without Connectors
Cable Leakage Current		I_L		12		nA	50 kV, ℓ = 0.3 meters
Refractive Index	Core	n		1.492			
	Cladding			1.417			

Notes:

1. Installation temperature is the range over which the cable can be bent and pulled without damage. Below -20°C the cable becomes brittle and should not be subjected to mechanical stress.
2. Short Term Tensile Force is for less than 30 minutes.
3. Short Term Bend Radius is for less than 1 hour nonoperating.
4. 90° bend on 25 mm radius mandrel. Bend radius is the radius of the mandrel around which the cable is bent.
5. Typical data are at 25°C.
6. Propagation delay constant is the reciprocal of the group velocity for propagation delay of optical power. Group velocity is v=c/n where c is the velocity of light in free space ($3x10^8$ m/s) and n is the effective core index of refraction.
7. Note that α_R rises at the rate of about 0.0067 dB/°C, where the thermal rise refers to the LED temperature changes above 25°C. Please refer to Figure 1 which shows the typical plastic optical fiber attenuation versus wavelength at 25°C.

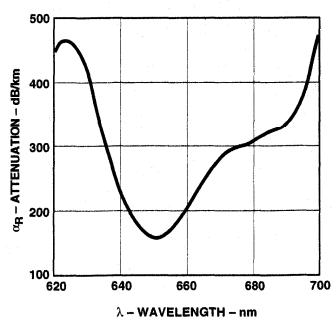


Figure 1. Typical POF Attenuation vs. Wavelength.

Plastic Fiber Connector Styles

Connector Description

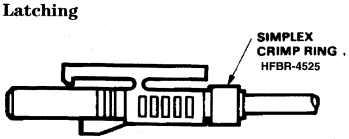
Four connector styles are available for termination of plastic optical fiber: simplex, simplex latching, duplex and duplex latching. All connectors provide a snap-in action when mated to Versatile Link components. Simplex connectors are color coded to facilitate identification of transmitter and receiver connections. Duplex connectors are keyed so that proper orientation is ensured during insertion. If the POF cable/connector will be used at extreme operating temperatures or experience frequent and wide temperature cycling effects, the cable/connector attachment can be strengthened with an RTV adhesive (see Plastic Connectoring Instructions for more detail).

SIMPLEX CONNECTOR STYLES

HFBR-4501/4511/4501B — Simplex

The simplex connector provides a quick and stable connection for applications that require a component-to-connector retention force of 8 Newtons (1.8 lb.). These connectors are available in gray (HFBR-4501), blue (HFBR-4511), or black (HFBR-4501B).

HFBR-4503/4513/4503B — Simplex Latching

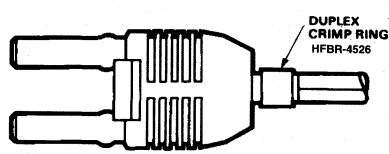


The simplex latching connector is designed for rugged applications requiring a greater retention force — 80 Newtons (18 lb.) — than provided by a simplex nonlatching connector. When inserting the simplex latching connector into a module, the connector latch mechanism should be aligned with the top surface of the horizontal modules, or with the tall vertical side of the vertical modules. Misalignment of an inserted latching connector into either module will not result in a positive latch. The connector is released by depressing the rear section of the connector lever, and then pulling the connector assembly away from the module housing.

The simplex latching connector is available in gray (HFBR-4503), blue (HFBR-4513), or black (HFBR-4503B).

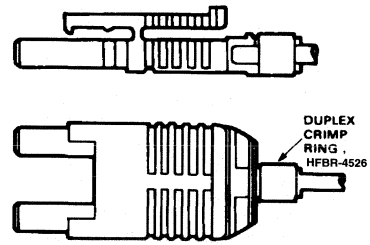
DUPLEX CONNECTOR STYLES

HFBR-4506/4506B — Duplex



Duplex connectors provide convenient duplex cable termination and are keyed to prevent incorrect insertion into duplex configured modules. The duplex connector is compatible with dual combinations of horizontal or vertical Versatile Link components (e.g., two horizontal transmitters, two vertical receivers, a horizontal transmitter with a horizontal receiver, etc.). The duplex nonlatching connector is available in parchment, off-white (HFBR-4506) or black (HFBR-4506B).

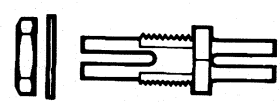
HFBR-4516/4516B — Duplex Latching



The duplex latching connector is designed for rugged applications requiring greater retention force than the nonlatching duplex connector. When inserting the duplex latching connector into a module, the connector latch mechanism should be aligned with the top surface of the dual combination of horizontal or vertical Versatile Link components. The duplex latching connector is available in gray (HFBR-4516) or black (HFBR-4516B).

Feedthrough/Splice

HFBR-4505/4515/4506B Bulkhead Adapter



The HFBR-4505/4515 adapter mates two simplex connectors for panel/bulkhead feedthrough of HFBR-4501/4511 terminated plastic fiber cable. Maximum panel thickness is 4.1 mm (0.16 inch). This adapter can serve as a cable in-line splice using two simplex connectors. The adapters are available in gray (HFBR-4505), blue (HFBR-4515), and black (HFBR-4505B). This adapter is currently not compatible with POF duplex, POF simplex latching, or HCS connectors.

Plastic Optical Fiber Connector Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Note
Storage and Operating Temperature	$T_{S,O}$	-40	85	°C	1
Recommended Operating Temperature	T_O	-40	85	°C	1
Installation Temperature	T_I	0	70	°C	1
Nut Torque HFBR-4505/4515 Adapter	T_N		0.7	N-m	2
			100	OzF-in.	

Notes:
1. Storage and Operating Temperatures refer to the ranges over which the connectors can be used when not subjected to mechanical stress. Installation Temperature refers to the ranges over which connectors may be installed onto the fiber and over which connectors can be connected and disconnected from transmitter and receiver modules.
2. Recommended nut torque is 0.57 N-m.

Plastic Optical Fiber Connector Mechanical/Optical Characteristics

T_A = -40 to +85°C, Unless Otherwise Specified

Parameter	Part Number	Symbol	Min.	Typ.[1]	Max.	Units	Temp. °C	Note
Retention Force, Connector to Versatile Link Transmitters and Receivers	Simplex, HFBR-4501/4511	$F_{R\text{-}C}$	7 3	8		N	+25 -40 to +85	2
	Simplex Latching, HFBR-4503/4513		47 11	80			+25 -40 to +85	
	Duplex, HFBR-4506		7 4	12			+25 -40 to +85	
	Duplex Latching, HFBR-4516		50 15	80			+25 -40 to +85	
Tensile Force, Connector to Cable	Simplex, HFBR-4501/4511	F_T	8.5	22		N		3
	Simplex Latching, HFBR-4503/4513		8.5	22				
	Duplex, HFBR-4506		14	35				
	Duplex Latching, HFBR-4516		14	35				
Adapter Connector to Connector Loss	HFBR-4505/4515 with HFBR-4501/4511	α_{CC}	0.7	1.5	2.8	dB	25	4, 5
Retention Force Connector to Adapter	HFBR-4505/4515 with HFBR-4501/4511	$F_{R\text{-}B}$	7	8		N		
Insertion Force, Connector to Versatile Link Transmitters and Receivers	Simplex, HFBR-4501/4511	F_I		8	30	N		6
	Simplex Latching, HFBR-4503/4513			16	35			
	Duplex, HFBR-4506			13	46			
	Duplex Latching HFBR-4516			22	51			

Notes:
1. Typical data are at +25°C.
2. No perceivable reduction in retention force was observed after 2000 insertions. Retention force of non-latching connectors is lower at elevated temperatures. Latching connectors are recommended for applications where a high retention force at high temperatures is desired.
3. For applications where frequent temperature cycling over temperature extremes is expected, please contact Hewlett-Packard for alternate connectoring techniques.
4. Minimum and maximum limit for α_{CC} for 0°C to +70°C temperature range. Typical value of α_{CC} is at +25°C.
5. Factory polish or field polish per recommended procedure.
6. Destructive insertion force was typically at 178 N (40 lb.).

Step-by-Step Plastic Cable Connectoring Instructions

The following step-by-step guide describes how to terminate plastic fiber optic cable. It is ideal for both field and factory installation. Connectors can be easily installed on cable ends with wire strippers, cutters and a crimping tool.

Finishing the cable is accomplished with the Hewlett-Packard HFBR-4593 Polishing Kit, consisting of a Polishing Fixture, 600 grit abrasive paper and 3 µm pink lapping film (3M Company, OC3-14). The connector can be used immediately after polishing.

Materials needed for plastic fiber termination are:

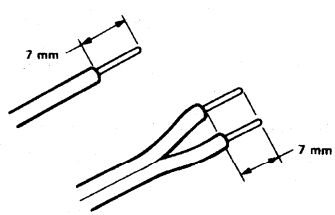
1. Hewlett-Packard Plastic Optical Fiber Cable (Example: HFBR-RUS500, HFBR-RUD500, HFBR-EUS500, or HFBR-EUD500)
2. Industrial Razor Blade or Wire Cutters
3. 16 Gauge Latching Wire Strippers (Example: Ideal Stripmaster™ type 45-092).
4. HFBR-4597 Crimping Tool
5. HFBR-4593 Polishing Kit
6. One of the following connectors:
   a) HFBR-4501/4503 Gray Simplex/Simplex Latching Connector and HFBR-4525 Simplex Crimp Ring
   b) HFBR-4511/4513 Blue Simplex/Simplex Latching Connector and HFBR-4525 Simplex Crimp Ring
   c) HFBR-4506 Parchment (off-white) Duplex Connector and HFBR-4526 Duplex Crimp Ring
   d) HFBR-4516 Gray Latching Duplex Connector and HFBR-4526 Duplex Crimp Ring

Step 1

The zip cord structure of the duplex cable permits easy separation of the channels. The channels should be separated approximately 50 mm (2.0 in) back from the ends to permit connectoring and polishing.

After cutting the cable to the desired length, strip off approximately 7 mm (0.3 in.) of the outer jacket with the 16 gauge wire strippers. Excess webbing on the duplex cable may have to be trimmed to allow the simplex or simplex latching connector to slide over the cable.

When using the duplex connector and duplex cable, the separated duplex cable must be stripped to equal lengths on each cable. This allows easy and proper seating of the cable into the duplex connector.



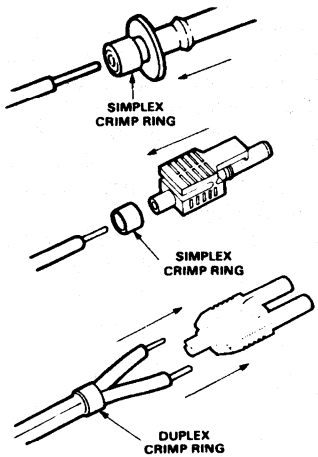
Step 2

Place the crimp ring and connector over the end of the cable; the fiber should protrude about 3 mm (0.12 in.) through the end of the connector. Carefully position the ring so that it is entirely on the connector with the rim of the crimp ring flush with the connector, leaving a small space between the crimp ring and the flange. Then crimp the ring in place with the crimping tool. One crimp tool is used for all POF connector crimping requirements.

For applications with extreme temperature operation or frequent temperature cycling, improved connector to cable attachment can be achieved with the use of an RTV (GE Company, RTV-128 or Dow Corning 3145-RTV) adhesive. The RTV is placed into the connector prior to insertion of the fiber and the fiber is crimped normally. The connector can be polished after the RTV has cured and is then ready for use.

Note: *By convention, place the gray connector on the transmitter cable end and the blue connector on the receiver cable end to maintain color coding (different color connectors are mechanically identical).*

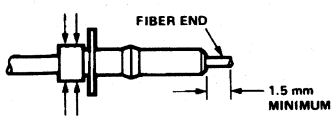
Simplex connector crimp rings cannot be used with duplex connectors and duplex connector crimp rings cannot be used with simplex connectors because of size differences. The simplex crimp has a dull luster appearance; the duplex ring is glossy and has a thinner wall.



Step 3

Any excess fiber protruding from the connector end may be cut off; however, the trimmed fiber should extend at least 1.5 mm (0.06 in) from the connector end.

Insert the connector fully into the polishing fixture with the trimmed fiber protruding from the bottom of the fixture. This plastic polishing fixture can be used to polish two simplex connectors or simplex latching connectors simultaneously, or one duplex connector.



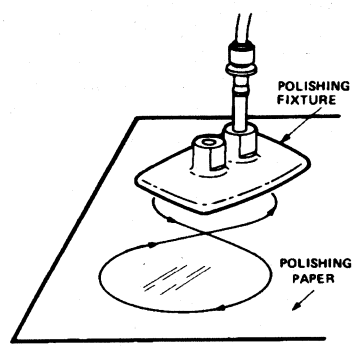
Note: *The four dots on the bottom of the polishing fixture are wear indicators. Replace the polishing fixture when any dot is no longer visible. Typically, the polishing fixture can be used 10 times; 10 duplex connectors or 20 simplex connectors, two at a time.*

Place the 600 grit abrasive paper on a flat smooth surface, pressing down on the connector, polish the fiber and the connector using a figure eight pattern of strokes until the connector is flush with the bottom of the polishing fixture. Wipe the connector and fixture with a clean cloth or tissue.

Step 4

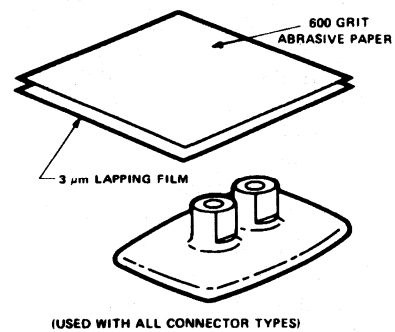
Place the flush connector and polishing fixture on the dull side of the 3 μm pink lapping film and continue to polish the fiber and connector for approximately 25 strokes. The fiber end should be flat, smooth and clean.

This cable is now ready for use.



Note: *Use of the pink lapping film fine polishing step results in approximately 2 dB improvement in coupling performance of either a transmitter-receiver link or a bulkhead/splice over a 600 grit polish alone. This fine polish is comparable to the Hewlett-Packard factory polish. The fine polishing step may be omitted where an extra 2 dB of optical power is not essential, as with short link lengths. Proper polishing of the tip of the fiber/connector face results in a tip diameter between 2.5 mm (0.098 in.) minimum and 3.2 mm (0.126 in.) maximum..*

HFBR-4593 Polishing Kit



Hard Clad Silica Fiber Specifications: HFBR-H/VXXYYY

Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Unit	Note
Storage/Operating Temperature		$T_{S,O}$	-40	85	°C	
Recommended Operating Temperature		T_O	-40	85	°C	
Installation Temperature		T_I	-20	85	°C	1
Short Term Tensile Force	Single Channel	F_T		101	N	2
	Dual Channel	F_T		202	N	2
Short Term Bend Radius		r	9		mm	3, 4
Long Term Bend Radius		r	15		mm	
Long Term Tensile Load		F_T		21	N	
Flexing				50,000	Cycles	4

Mechanical/Optical Characteristics, T_A = -40 to +85°C

Parameter		Symbol	Min.	Typ.[5]	Max.	Unit	Condition
Cable Attenuation	HCS® Cable	α_O	5	7	10	dB/km	Source is HFBR-15X7 (650 nm LED, 0.5 NA) 0 to +70°C
Cable Attenuation	HCS® Cable	α_O	5	7	12	dB/km	-40 to +85°C
Reference Attenuation	HCS® Cable	α_R	6.0	8.0	10.0	dB/km	Source is 650 nm, 0.37 NA monochrometer -40 to +85°C
Numerical Aperture		NA	0.35	0.37	0.39		ℓ = 2 meters
Diameter, Core		D_{CORE}	196	200	204	µm	
Diameter, Cladding		D_{CLAD}	220	230	230	µm	
Diameter, Buffer		D_{BUFF}	470	500	530	µm	
Diameter, Jacket		D_J	2.1	2.2	2.3	mm	Simplex Cable
Propagation Delay Constant		l/v		4.8		ns/m	Note 6
Mass per Unit Length/Channel				6.1		g/m	Without Connectors
Refractive Index	Core	n		1.457			
	Cladding			1.407			

Notes:

1. Installation temperature is the range over which the cable can be bent and pulled without damage. Below -20°C the cable becomes brittle and should not be subjected to mechanical stress.
2. Less than 1 hour.
3. Less than 1 hour, non-operating.
4. 90° bend on 9 mm radius.
5. Typical data are at +25°C.
6. Propagation delay constant is the reciprocal of the group velocity for propagation delay of optical power. Group velocity is v = c/n, where c is the velocity of light in free space ($3x10^8$ m/s) and n is the effective core index of refraction.

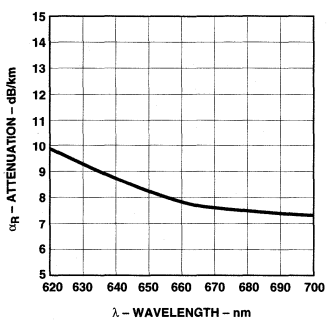


Figure 1. Typical HCS Attenuation vs. Wavelength.

Hard Clad Silica Optical Fiber Connector Styles

Simplex Connector Style, HFBR-4521

The simplex connector provides a quick and stable connection for applications that require a component to provide a retention force of 8 Newtons (1.8 lb.). This connector is available only in black.

Hard Clad Silica Glass Optical Fiber Connector

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Note
Storage and Operating Temperature	$T_{S,O}$	-40	85	°C	1
Recommended Operating Temperature	T_O	-40	85	°C	
Installation Temperature	T_A	0	85	°C	

Note:

1. Storage and Operating Temperatures refer to the ranges over which the connectors can be used when not subjected to mechanical stress. Installation Temperature refers to the ranges over which connectors may be installed onto the fiber and over which connectors can be connected and disconnected from transmitter and receiver modules.

Hard Clad Silica Glass Optical Fiber Connector

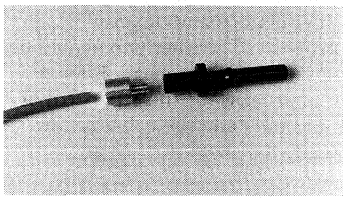
Mechanical/Optical Characteristics; T_A = -40 to +85 °C

Parameter	Part Number		Sym.	Min.	Typ.[1]	Max.	Units	Note
Retention Force Connector to Versatile Link Transmitters and Receivers	Simplex	HFBR-4521	F_{R-C}	3	8		N	2
Tensile Force Connector to Cable	Simplex	HFBR-4521	F_T	40	45		N	
Insertion Force Connector to Versatile Link Transmitters and Receivers	Simplex	HFBR-4521	F_I		8	30	N	3

Notes:

1. Typical data are at 25°C.
2. No perceivable reduction in retention force was observed after 2000 insertions.
3. Destructive insertion forces was typically at 178 N (40 lb.).

Instructions for Step-by-Step Connector Installation for HCS® Cable

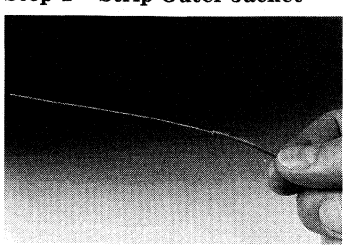


The following step-by-step guide describes how to terminate hard clad silica fiber optic cable. It is ideal for both field and factory installation. Connectoring the cable is accomplished with the Hewlett-Packard HFBR-4521 Crimp and Cleave Kit consisting of a Cable Stripper Tool, Fiber Stripper Tool, Crimp Tool, and Diamond Cleave Tool. No adhesive material is needed to secure the cable in the connector, and the connector can be used immediately after cleaving. Connectors may be easily installed on the cable ends with the Crimp and Cleave Kit.

Materials needed for the terminating procedure are:

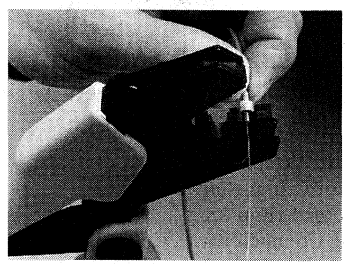
1. Hewlett-Packard HCS® Fiber Optic Cable: (Example: HFBR-HUS500, HFBR-HUD500, HFBR-VUS500)
2. HFBR-4584 Crimp and Cleave Kit
3. HFBR-4521 Black Simplex Connector and Crimp Ring (HFBR-4527)

Step 1 – Strip Outer Jacket



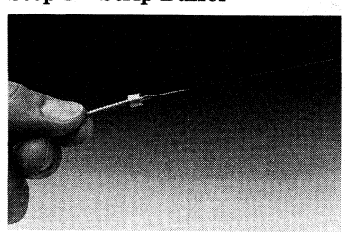
The zipcord structure of the duplex cable permits easy separation of the channels. The channels should be separated approximately 75 mm (3.0 in) back from the ends to permit connectoring and cleaving. After cutting the cable to the desired length, strip off approximately 75 mm (3 in) of the outer jacket with the cable stripper tool, selecting the 1.6 cutting hole labeled on the cable stripper tool. This is done by applying a quick squeezing action to cut the cable jacket. Remove the cut cable jacket portion.

Step 2 – Install Crimp Ring (HFBR-4527) to Fiber



Place the crimp ring over the end of the cable and rest the larger end against the unstripped cable jacket. Selecting the smaller crimp hole (front die nest), align the crimp ring in the crimp tool jaws and fully squeeze the tool handles together and release. This crimps the crimp ring to the fiber buffer.

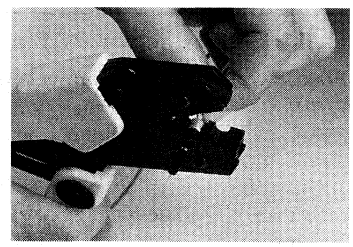
Step 3 – Strip Buffer



Insert the stripped cable through the guide hole of the fiber stripper tool, inserting the crimp ring until it is fully seated in the guide tube. Holding the unstripped cable securely, squeeze the handles of the fiber stripper to cut the fiber buffer and pull straight to slightly separate the buffer.

Release the fiber stripper handles, remove the tool and carefully slide the buffer off the fiber by hand. Inspect the fiber for cladding damage (i.e., white dusty appearance). If damage has occurred, cut the damaged portion of the fiber and repeat the Strip Outer Jacket procedure. If the fiber stripper tool blade is worn, replace the tool immediately.

Step 4 — Install Ferrule (Connector)



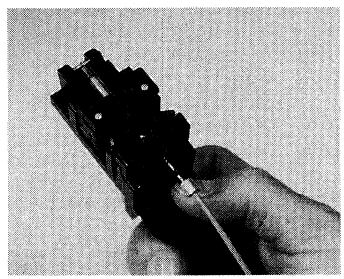
Slide the ferrule onto the fiber and into the crimp ring, carefully aligning the ferrule fully within the crimp ring. The fiber should protrude at least 35 mm (1.4 in) through the end of the ferrule. Selecting the large hole on the crimp tool (rear die nest), crimp the ring to the ferrule by fully squeezing the crimp tool handles together and releasing.

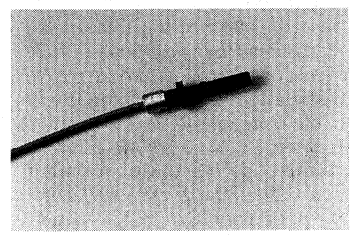
Step 5 – Cleave Fiber

Carefully insert the ferrule into the slot on the diamond cleave tool until the ferrule rests securely in the cleave tool connector adapter.

Check to see that the fiber is positioned between the two fiber clamps and that the connector face is in proximity to the cleaving blade. If the ferrule or the fiber is not positioned correctly, remove the cable assembly and reinsert the ferrule.

Holding the cleave tool horizontally, grip the handle, leaving the index finger free. Release the ferrule, and, using the index finger, slowly depress the cleave tool trigger until the trigger is completely down. This motion activates the fiber clamp and the diamond cleave blade to complete the fiber termination; the ferrule will snap back slightly after the cleave process. Remove the cleaved ferrule (connector assembly) from the adapter slot and release the cleave tool trigger. Remove the fiber remnant from the cleave tool fiber clamps and dispose of properly. The fiber end should be flat, smooth and clean. Repeat this process for the other end of the cable, and the cable is now ready for use.





Ordering Guide for POF and HCS Connectors and Accessories

Plastic Optical Fiber Connectors

HFBR-4501	Gray Simplex Connector/Crimp Ring
HFBR-4511	Blue Simplex Connector/Crimp Ring
HFBR-4501B	Black Simplex Connector/Crimp Ring
HFBR-4503	Gray Simplex Latching Connector with Crimp Ring
HFBR-4513	Blue Simplex Latching Connector with Crimp Ring
HFBR-4503B	Black Simplex Latching Connector with Crimp Ring
HFBR-4506	Parchment Duplex Connector with Crimp Ring
HFBR-4506B	Black Duplex Connector with Crimp Ring
HFBR-4516	Gray Duplex Latching Connector with Crimp Ring
HFBR-4516B	Black Duplex Latching Connector with Crimp Ring
HFBR-4505	Gray Adapter (Bulkhead/Feedthrough)
HFBR-4515	Blue Adapter (Bulkhead/Feedthrough)
HFBR-4505B	Black Adapter (Bulkhead/Feedthrough)

Plastic Optical Fiber Accessories

HFBR-4525	1000 Simplex Crimp Rings
HFBR-4526	500 Duplex Crimp Rings
HFBR-4593	Polishing Kit (one polishing tool, two pieces 600 grit abrasive paper, and two pieces 3 μm pink lapping film)
HFBR-4597	Plastic Fiber Crimping Tool

HCS® Fiber Connectors

HFBR-4521	Black Simplex Connector/Crimp Ring

HCS® Fiber Accessories

HFBR-4527	100 Simplex Crimp Rings
HFBR-4584	Crimp and Cleave Termination Kit (one Fiber Strip tool, one Cable Strip tool, one Crimp tool, one Scissors and one Diamond Cleave Tool)

Ordering Guide for POF and HCS Cable

Four steps are required to determine the proper part number for a desired cable.

Step 1
Select the cable type.

POF: Standard (**R**) or Extra Low Loss (**E**) Attenuation Cable.

HCS: Riser (**H**) or Plenum (**V**) rated cable.

Step 2
Select the connector style.

POF: Simplex, Simplex Latching, Duplex, or Duplex Latching.

HCS: Simplex only (non-latching).

Step 3
Select Simplex or Duplex cable.

Step 4
Determine the cable length.

To determine the appropriate part number, select the letter corresponding to your selection and fill in the appropriate information, as in the chart below.

For Example:

HFBR-RUD500 is a Standard Attenuation, Unconnectored, Duplex, 500 meter cable.

HFBR-ELS001 is an Extra Low Loss Attenuation, Latching Simplex Connectored, Simplex, 1 meter cable.

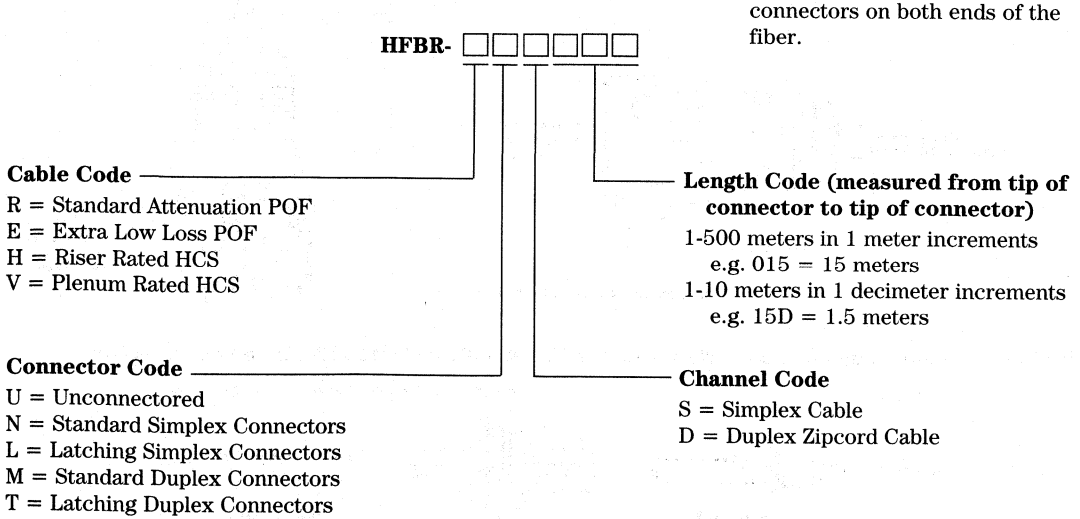
HFBR-RMD010 is a Standard Attenuation, Standard Duplex Connectored, Duplex, 10 meter cable.

HFBR-RND100 is a Standard Attenuation, Standard Simplex Connectored, Duplex, 100 meter cable.

Cable Length Tolerances:
The plastic cable length tolerances are: +10%/-0%.

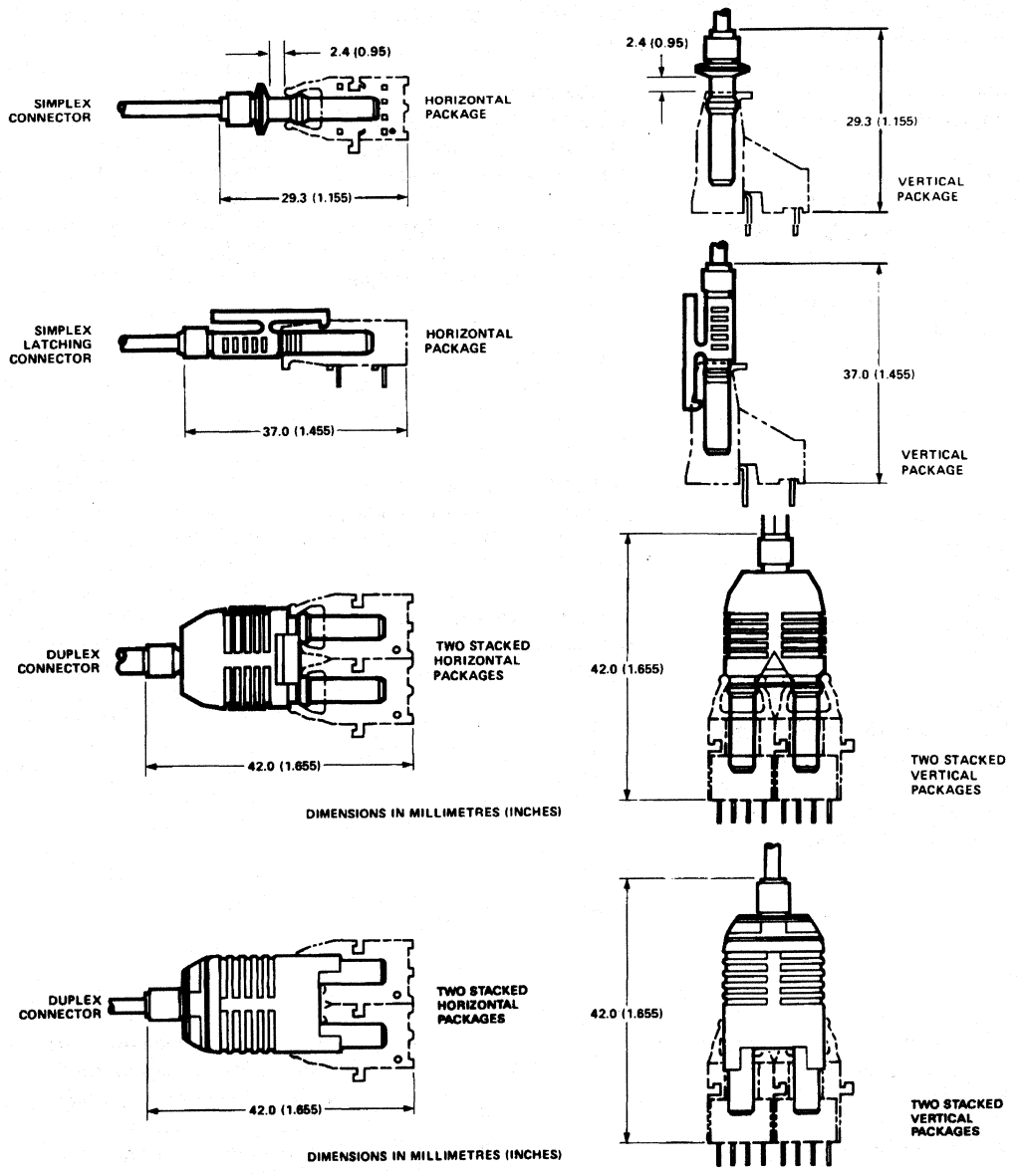
Note: 0.1 meter Standard Attenuation Simplex lengths are available: 0.5 meter Standard Attenuation Simplex and Duplex lengths are also available. The lengths are ordered as HFBR-xxx1DM or HFBR-xxx5DM. Cables of 1 to 10 meter lengths in 1 decimeter increments are also available. This cable is ordered as HFBR-xxxyyD where "yy" is the length of the cable. For example, a 1.5 meter Standard Attenuation, Standard Simplex Connectored, Simplex cable would be ordered as HFBR-RNS15D.

NOTE: By convention, pre-connectored simplex POF cables have gray and blue colored connectors on the opposite ends of the same fiber; although oppositely colored, the connectors are mechanically identical. For duplex POF cables with simplex connectors, the same rule applies to each fiber and adjacent terminations use complimentary colored connectors. For duplex POF cables with duplex connectors similar rules apply using color coded markings on the duplex fiber cable. Pre-connectored simplex HCS cables have identically colored BLACK connectors on both ends of the fiber.

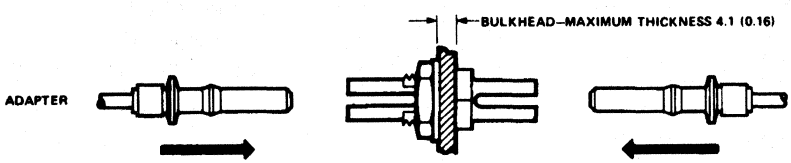


Connector Applications

Attachment to Hewlett-Packard Versatile Link Fiber Optic Components



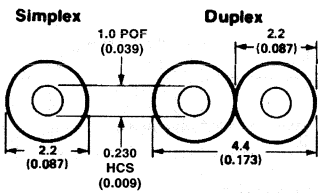
Bulkhead Feedthrough or Panel Mounting for HFBR-4501/4511/4501B Simplex Connectors



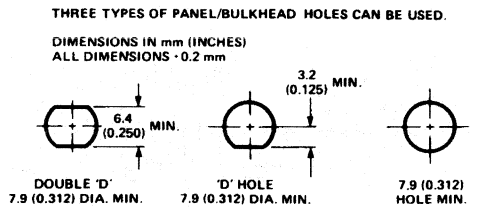
Versatile Link Mechanical Dimensions

All dimensions in mm (inches).
All dimensions ± 0.25 mm unless otherwise specified.

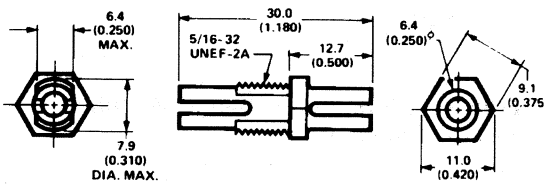
Fiber Optic Cable Dimensions



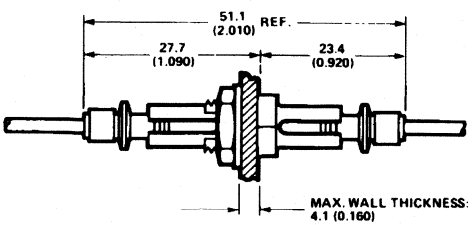
Panel Mounting – Bulkhead Feedthrough



HFBR-4505 (Gray)/4515 (Blue)/4505B (Black) Adapters

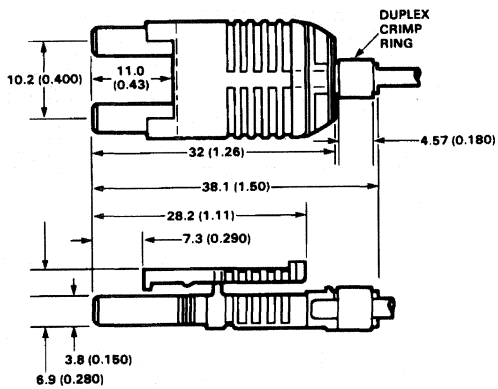


Bulkhead Feedthrough with Two HFBR-4501/ 4511/4501B Connectors

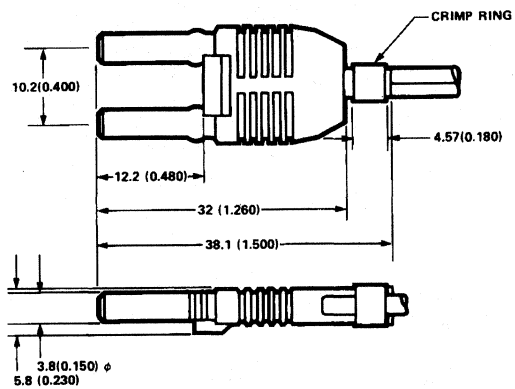


Versatile Link Mechanical Dimensions, continued

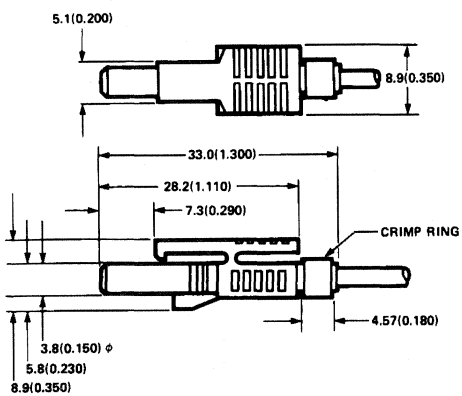
HFBR-4516 (Parchment)/4516B (Black) Duplex Latching Connector



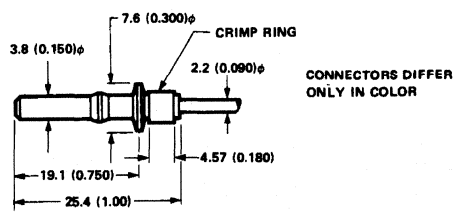
HFBR-4506 (Parchment)/4506B (Black) Duplex Connector



HFBR-4503 (Gray)/4513 (Blue/4503 (Black) Simplex Latching Connector



HFBR-4501 (Gray)/4511 (Blue)/4501 (Black) Simplex Connector



HEWLETT® PACKARD

Crimpless Connectors for Plastic Optical Fiber and Versatile Link

Technical Data

HFBR-4531
HFBR-4532

Features

- **Requires No Crimp Ring or Crimping Tool**
- **Durable ULTEM® Plastic Material (UL File #E121562)**
- **Same Low Cost as HFBR-4501/4503 Series Connectors**
- **Excellent Retention Force**
- **Symmetry in Nonlatching Connector Gives Simplex/Duplex Functionality with the Same Part**

Applications

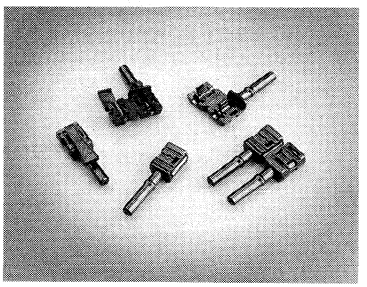
These connectors can be used for any application in which plastic optical fiber is used including:

- **Industrial Control and Voltage Isolation**
- **Automotive Networks**
- **Proprietary System Interconnects**
- **Gaming Equipment**
- **Medical Equipment**
- **Telecommunications**
- **Datacommunications**

Description

The HFBR-453X series connectors are an enhanced version of the HFBR-4501 and HFBR-4503 low-cost connectors for plastic optical fiber, which are compatible with HP's versatile link series transmitters and receivers. The innovative design uses a simple, snap-together concept which eliminates the need for crimping. This connector not only saves the user labor and tool cost, but reduces the yield loss due to installation error.

The HFBR-453X series connectors are available in two styles: latching and non-latching. For a duplex connector, two nonlatching simplex connectors can be snapped together. The connectors are made of a rugged, flame retardant plastic which is good for industrial and other harsh environments. The HFBR-453X series connectors are for use with Plastic Optical Fiber only.



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Termination Guide

Step-by-Step Plastic Cable Connectoring Instructions

The following step-by-step guide describes how to terminate plastic fiber optic cable. It is ideal for both field and factory installations. Connectors can be easily installed on cable ends with standard tools such as wire strippers and cutters.

Finishing the cable is accomplished with the Hewlett-Packard HFBR-4593 Polishing Kit, consisting of a polishing fixture, 600 grid abrasive paper and 3 μm pink lapping film (3M Company, OC3-14). The connector can be used immediately after polishing.

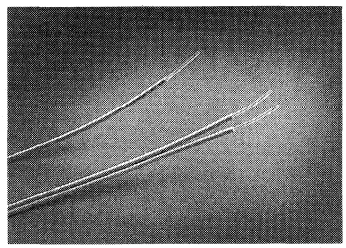
The following materials are needed for plastic fiber termination:

1. Plastic optical fiber cable (Example: HFBR-RUD500)
2. Wire cutters or scissors
3. 16 gauge wire stripper (Example: Ideal Stripmaster type 45-092)
4. HFBR-4593 polishing kit (optional)
5. Crimpless connectors

Step 1: Stripping the Fiber

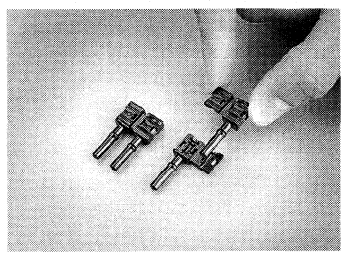
The zip cord structure of the duplex cable permits easy separation of the channels. The channels should be separated a minimum of 100 mm (4 in) to a maximum of 150 mm (6 in) back from the ends to permit connectoring, polishing and cable end flexibility.

After cutting the cable to the desired length, strip off approximately 7 mm (0.3 in) of the outer jacket with the 16 gauge wire strippers.



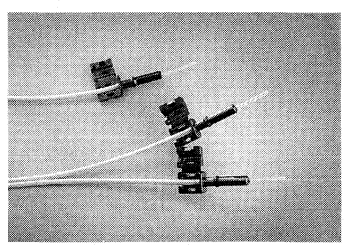
When using the duplex connector arrangement, the separated duplex cable should be stripped to roughly equal lengths on each cable end.

For the non-latching version (HFBR-4531), the same connector is used for simplex and duplex arrangement. No crimping is necessary. The top half of the connector will snap into the ferrule half to secure the fiber.



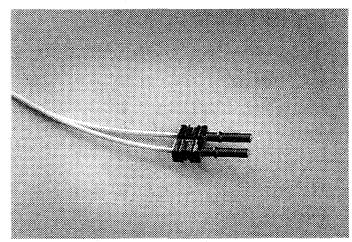
Step 2: Putting on the Connector

Place the connector on each end of the fiber, and slide the connector down until the fiber jacket stops it. The fiber should protrude *no less* than 1.5 mm (0.06 in) from the end of the connector.



To install *simplex* connectors flip the top half of the connector over and snap it into the ferrule half (with your fingers). When the top half latches inside the body of the ferrule half, proper connector-to-cable attachment is achieved.

For *duplex* connector installation place one connector on top of the other, so that the top half of each connector is over the ferrule half of the opposite connector.

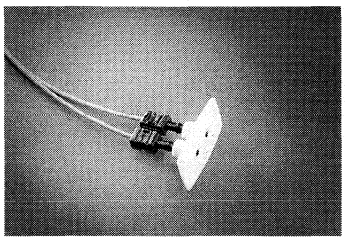


Manually press connectors together in the center of the arrangement. Then latch by pressing on the sides of each connector. As with the simplex version, connectors are secured when top halves latch into the ferrule halves.

Step 3: Trimming and Polishing

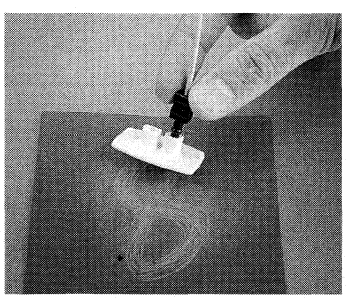
Any fiber in excess of 1.5 mm (0.06 in) protruding from the connector end should be cut off with wire cutters or scissors.

Insert the connector fully into the polishing fixture with the trimmed fiber protruding from the bottom of the fixture. This plastic polishing fixture can be used to polish two simplex connectors simultaneously or one duplex connector.



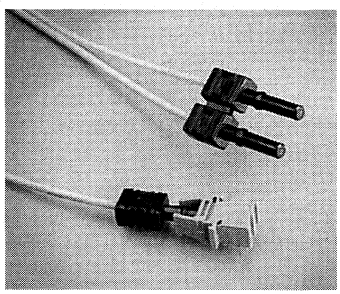
Note: *The four dots on the bottom of the polishing fixture are wear indicators. Replace the polishing fixture when any dot is no longer visible.*

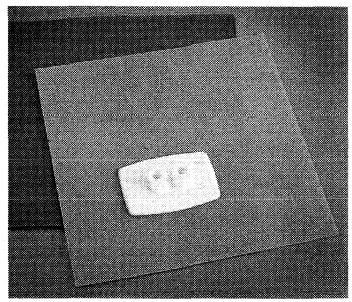
Press the polishing tool down on the 600 grit abrasive paper. Polish the fiber using a figure eight pattern until the connector is flush with the bottom of the polishing fixture. Wipe the connector and fixture with a clean cloth or tissue.



Step 4: Finishing

Place the flush connector and polishing fixture on the dull side of the 3 µm pink lapping film and continue to polish the fiber in the same figure eight pattern for approximately 25 strokes. The fiber end should be flat, smooth and clean.





HFBR-4593 Polishing Kit

Note: *Use of the pink lapping film fine polishing step results in approximately 2 dB improvement in coupling performance of either a transmitter-receiver link or a bulkhead/splice over a 600 grit polish alone. This fine polish is comparable to the Hewlett-Packard factory polish. The fine polishing step may be omitted for short link lengths.*

HFBR-4531/4532
Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Note
Storage Temperature	T_S	-40	85	°C	1
Operating Temperature	T_O	-40	85	°C	1
Installation Temperature	T_I	0	70	°C	1

Connector Mechanical Characteristics

Parameter	Part Number	Symbol	Min.	Typ.	Units	Temp. (°C)
Retention Force to HFBR-0501 Series	HFBR-4531	F_{R-C}	3	8	N	+25
	HFBR-4532		47	80		
Retention Force to HFBR-0508 Series	HFBR-4531		8	12		
Tensile Force, Connector to Cable	HFBR-4531	F_T	40	50		-40 to +85
	HFBR-4532					

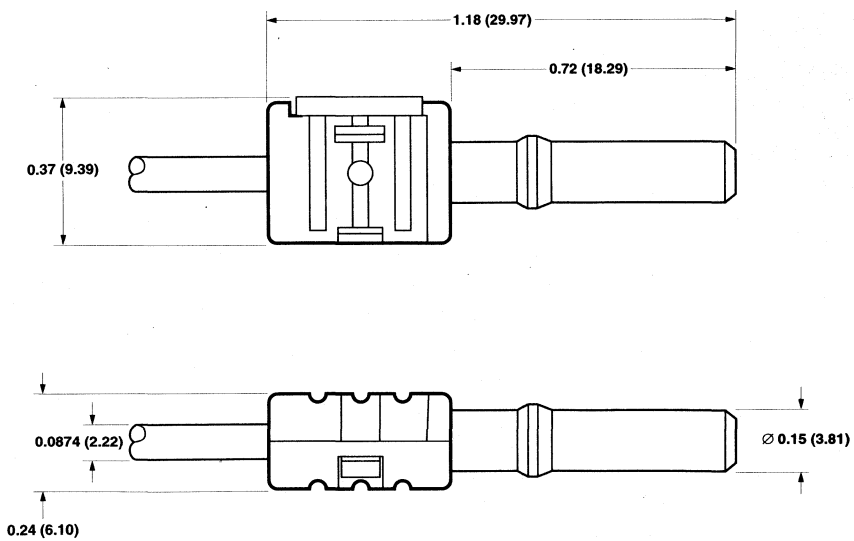
Note:

1. Storage and operating temperatures refer to the ranges over which the connectors can be used when not subjected to mechanical stress. Installation temperature refers to the ranges over which connectors may be installed onto the fiber and over which connectors can be connected and disconnected from the transmitter and receiver modules.

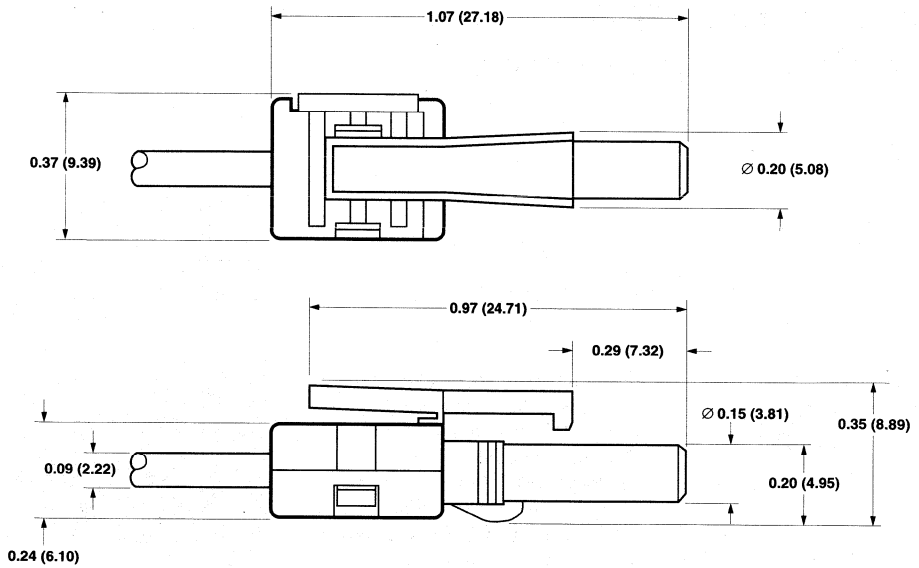
Mechanical Dimensions

All dimensions are in inches and (millimeters)

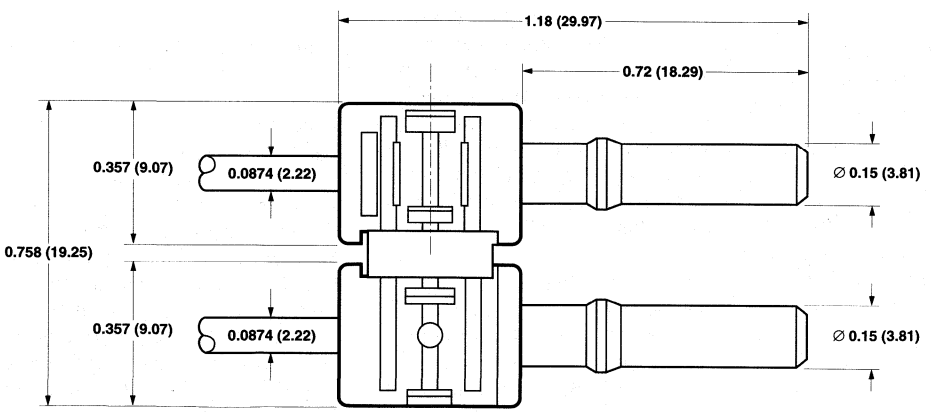
HFBR-4531 (Nonlatching):



HFBR-4532 (Latching):



HFBR-4531 in Duplex Configuration



HEWLETT® PACKARD

1300 nm Fiber Optic Transmitter and Receiver

Technical Data

HFBR-0300 Series:
HFBR-1312T Transmitter
HFBR-2316T Receiver

Features

- **Low Cost Fiber Optic Link**
- **Signal Rates over 155 Megabaud**
- **1300 nm Wavelength**
- **Link Distances over 5 km**
- **Dual-in-line Package Panel-Mountable ST* and SC Connector Receptacles**
- **Auto-Insertable and Wave-Solderable**
- **Specified with 62.5/125 µm and 50/125 µm Fiber**
- **Compatible with HFBR-0400 Series**

Applications

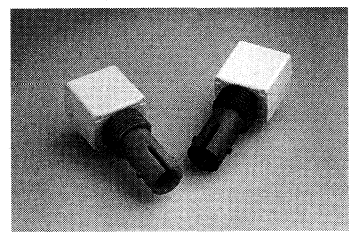
- **Desktop Links for High Speed LANs**
- **Distance Extension Links**
- **Telecom Switch Systems**
- **TAXIchip® Compatible**

Description

The HFBR-0300 Series is designed to provide the most cost-effective 1300 nm fiber optic links for a wide variety of data communication applications from low-speed distance extenders up to SONET OC-3 signal rates. Pinouts identical to Hewlett-Packard HFBR-0400 Series allow designers to easily upgrade their 820 nm links for farther distance. The transmitter and receiver are compatible with two popular optical fiber sizes: 50/125 µm and 62.5/125 µm diameter. This allows flexibility in choosing a fiber size. The 1300 nm wavelength is in the lower dispersion and attenuation region of fiber, and provides longer distance capabilities than 820 nm LED technology. Typical distance capabilities are 2 km at 125 MBd and 5 km at 32 MBd.

Transmitter

The HFBR-1312T fiber optic transmitter contains a 1300 nm InGaAsP light emitting diode capable of efficiently launching optical power into 50/125 µm and 62.5/125 µm diameter fiber. Converting the interface circuit from a HFBR-14XX 820 nm transmitter to the HFBR-1312T requires only the removal of a few passive components.

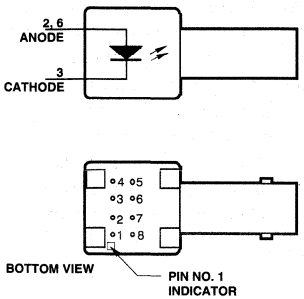


Receiver

The HFBR-2316T receiver contains an InGaAs PIN photodiode and a low-noise transimpedance preamplifier that operate in the 1300 nm wavelength region. The HFBR-2316T receives an optical signal and converts it to an analog voltage. The buffered output is an emitter-follower, with frequency response from DC to typically 125 MHz. Low-cost external components can be used to convert the analog output to logic compatible signal levels for a variety of data formats and data rates. The

*ST is a registered trademark of AT&T Lightguide Cable Connectors

HFBR-1312T Transmitter

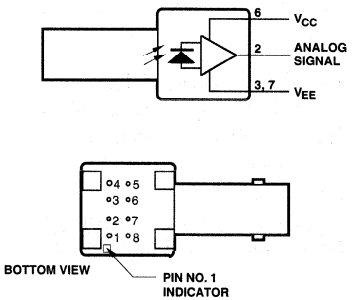


PIN	FUNCTION
1†	N.C.
2	ANODE
3	CATHODE
4†	N.C.
5†	N.C.
6	ANODE
7*	N.C.
8†	N.C.

* PIN 7 IS ELECTRICALLY ISOLATED FROM PINS 1, 4, 5, AND 8, BUT IS CONNECTED TO THE HEADER.

† PINS 1, 4, 5, AND 8 ARE ISOLATED FROM THE INTERNAL CIRCUITRY, BUT ARE ELECTRICALLY CONNECTED TO EACH OTHER.

HFBR-2316T Receiver



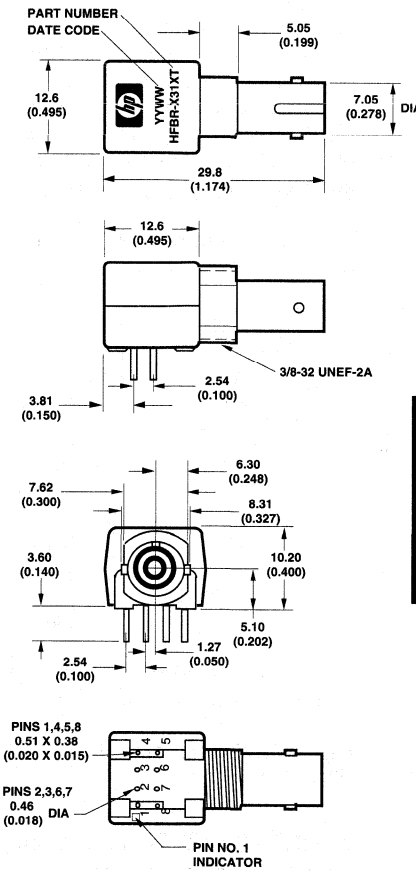
PIN	FUNCTION
1†	N.C.
2	SIGNAL
3*	V_{EE}
4†	N.C.
5†	N.C.
6	V_{CC}
7*	V_{EE}
8†	N.C.

* PINS 3 AND 7 ARE ELECTRICALLY CONNECTED TO THE HEADER.

† PINS 1, 4, 5, AND 8 ARE ISOLATED FROM THE INTERNAL CIRCUITRY, BUT ARE ELECTRICALLY CONNECTED TO EACH OTHER.

HFBR-0300 Series

Mechanical Dimensions



HFBR-2316T is pin compatible with HFBR-24X6 receivers and can be used to extend the distance of an existing application by substituting the HFBR-2316T for the HFBR-2416.

Package Information

HFBR-0300 Series transmitters and receivers are housed is a dual-in-line package made of high strength, heat resistant, chemically resistant, and UL V-0 flame retardant plastic. Transmitters are identified by the brown port color; receivers have black ports. The package is auto-insertable and wave solderable for high volume production applications.

Note: The "T" in the product numbers indicates a Threaded ST connector (panel mountable), for both transmitter and receiver.

Handling and Design Information

When soldering, it is advisable to leave the protective cap on the unit to keep the optics clean. Good system performance requires clean port optics and cable ferrules to avoid obstructing the optical path. Clean compressed air is often sufficient to remove particles of dirt; methanol on a cotton swab also works well.

Panel Mounting Hardware

The HFBR-4411 kit consists of 100 nuts and 100 washers with dimensions as shown in Figure 1. These kits are available from HP or any authorized distributor. Any standard size nut and washer will work, provided the total thickness of the wall, nut, and washer does not exceed 0.2 inch (5.1mm).

When preparing the chassis wall for panel mounting, use the mounting template in Figure 2. When tightening the nut, torque should not exceed 0.8 N-m (8.0 in-lb).

Recommended Chemicals for Cleaning/Degreasing HFBR-0300 Products

Alcohols (methyl, isopropyl, isobutyl)
Aliphatics (hexane, heptane)
Other (soap solution, naphtha)

Do not use partially halogenated hydrocarbons (such as 1.1.1 trichloroethane), ketones (such as MEK), acetone, chloroform, ethyl acetate, methylene dichloride, phenol, methylene chloride, or N-methylpyrolldone. Also, HP does not recommend the use of cleaners that use halogenated hydrocarbons because of their potential environmental harm.

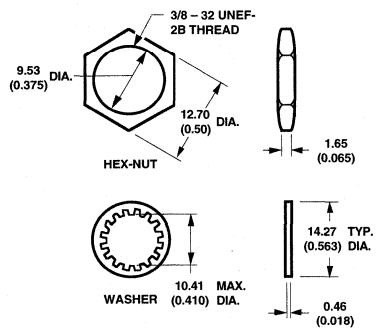


Figure 1. HFBR-4411 Mechanical Dimensions.

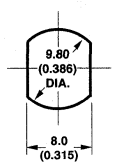


Figure 2. Recommended Cut-out for Panel Mounting.

HFBR-1312T Transmitter Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Reference
Storage Temperature	T_S	-55	85	°C	
Operating Temperature	T_A	-40	85	°C	
Lead Soldering Cycle Temperature			260	°C	Note 8
Lead Soldering Cycle Time			10	sec	
Forward Input Current DC	I_{FDC}		100	mA	
Reverse Input Voltage	V_R		1	V	

CAUTION: The small junction sizes inherent to the design of this bipolar component increase the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

HFBR-1312T Transmitter Electrical/Optical Characteristics

0 to 70°C unless otherwise specified

Parameter	Symbol	Min.	Typ.[1]	Max.	Unit	Condition	Ref.
Forward Voltage	V_F	1.1	1.4	1.7	V	I_F = 75 mA	Fig. 1
			1.5			I_F = 100 mA	
Forward Voltage Temperature Coefficient	$\Delta V_F/\Delta T$		-1.5		mV/°C	I_F = 75 - 100 mA	
Reverse Input Voltage	V_R	1	4		V	I_R = 100 µA	
Center Emission Wavelength	λ_C	1270	1300	1370	nm		
Full Width Half Maximum	FWHM		130	185	nm		
Diode Capacitance	C_T		16		pF	V_F = 0 V, f = 1 MHz	
Optical Power Temperature Coefficient	$\Delta P_T/\Delta T$		-0.03		dB/°C	I_F = 75 - 100 mA DC	
Thermal Resistance	Θ_{JA}		260		°C/W		Note 2

HFBR-1312T Transmitter Output Optical Power and Dynamic Characteristics

Parameter	Symbol	Min.	Typ.[1]	Max.	Unit	Condition		Ref.
						T_A	$I_{F, peak}$	
Peak Power 62.5/125 µm NA = 0.275	P_{T62}	-16.0	-14.0	-12.5	dBm	25°C	75 mA	Notes 3, 4, 5 Fig. 2
		-17.5		-11.5		0-70°C	75 mA	
		-15.5	-13.5	-12.0		25°C	100 mA	
		-17.0		-11.0		0-70°C	100 mA	
Peak Power 50/125 µm NA = 0.20	P_{T50}	-19.5	-17.0	-14.5	dBm	25°C	75 mA	Notes 3, 4, 5 Fig. 2
		-21.0		-13.5		0-70°C	75 mA	
		-19.0	-16.5	-14.0		25°C	100 mA	
		-20.5		-13.0		0-70°C	100 mA	
Optical Overshoot	OS		5	10	%	0-70°C	75 mA	Note 6 Fig. 3
Rise Time	t_r		1.8	4.0	ns	0-70°C	75 mA	Note 7 Fig. 3
Fall Time	t_f		2.2	4.0	ns	0-70°C	75 mA	Note 7 Fig. 3

Notes:

1. Typical data are at T_A = 25°C.
2. Thermal resistance is measured with the transmitter coupled to a connector assembly and mounted on a printed circuit board; $\Theta_{JC} < \Theta_{JA}$.
3. Optical power is measured with a large area detector at the end of 1 meter of mode stripped cable, with an ST* precision ceramic ferrule (MIL-STD-83522/13), which approximates a standard test connector. Average power measurements are made at 12.5 MHz with a 50% duty cycle drive current of 0 to $I_{F,peak}$; $I_{F,average} = I_{F,peak}/2$. Peak optical power is 3 dB higher than average optical power.
4. When changing from µW to dBm, the optical power is referenced to 1 mW (1000 µW).
   Optical power P(dBm) = 10*log[P(µW)/1000µW].
5. Fiber NA is measured at the end of 2 meters of mode stripped fiber using the far-field pattern. NA is defined as the sine of the half angle, determined at 5% of the peak intensity point. When using other manufacturer's fiber cable, results will vary due to differing NA values and test methods.
6. Overshoot is measured as a percentage of the peak amplitude of the optical waveform to the 100% amplitude level. The 100% amplitude level is determined at the end of a 40 ns pulse, 50% duty cycle. This will ensure that ringing and other noise sources have been eliminated.
7. Optical rise and fall times are measured from 10% to 90% with 62.5/125 µm fiber. LED response time with recommended test circuit (Figure 3) at 25 MHz, 50% duty cycle.
8. 2.0 mm from where leads enter case.

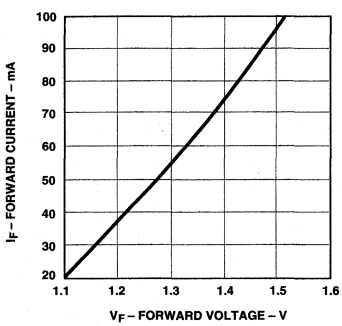


Figure 1. Typical Forward Voltage and Current Characteristics.

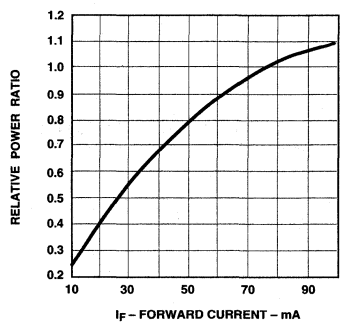


Figure 2. Normalized Transmitter Output Power vs. Forward Current.

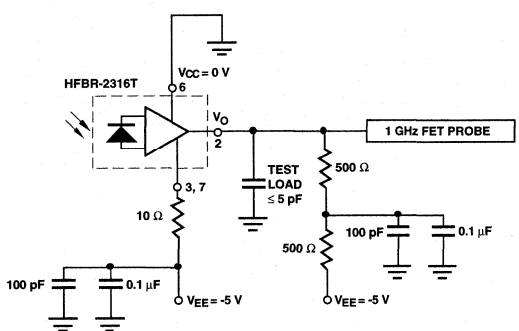


Figure 3. Recommended Transmitter Drive and Test Circuit.

HFBR-2316T Receiver Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Reference
Storage Temperature	T_S	-55	85	°C	
Operating Temperature	T_A	-40	+85	°C	
Lead Soldering Temperature			260	°C	Note 1
Cycle Time			10	s	
Signal Pin Voltage	V_O	-0.5	V_{CC}	V	
Supply Voltage	V_{CC} - V_{EE}	-0.5	6.0	V	Note 2
Ouptut Current	I_O		25	mA	

CAUTION: The small junction sizes inherent to the design of this bipolar component increase the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

HFBR-2316T Receiver Electrical/Optical and Dynamic Characteristics

0 to 70°C; 4.75 V < V_{CC} - V_{EE} < 5.25 V; power supply must be filtered (see note 2).

Parameter	Symbol	Min.	Typ.[3]	Max.	Unit	Condition	Ref.
Responsitivity	R_P	6.5	13	19	mV/µW	λ_p = 1300 nm, 50 MHz	Note 4 Fig. 1, 5
RMS Output Noise Voltage	V_{NO}		0.4	0.59	mV_{RMS}	100 MHz bandwidth, P_R = 0 µW	Note 5 Fig. 2
				1.0	mV_{RMS}	Unfiltered Bandwidth P_R = 0 µW	
Equivalent Optical Noise Input Power (RMS)	$P_{N,\,RMS}$		-45	-41.5	dBm	@ 100 MHz, P_R = 0 µW	Note 5
			0.032	0.071	µW		
Peak Input Optical Power	P_R			-11.0	dBm	50 MHz, 1 ns PWD	Note 6
				80	µW		Fig. 3
Output Resistance	R_O		30		Ohm	f = 50 MHz	
DC Output Voltage	$V_{O,DC}$	0.8	1.8	2.6	V	V_{CC} = 5 V, V_{EE} = 0 V P_R = 0 µW	
Supply Current	I_{CC}		9	15	mA	R_{LOAD} = ∞	
Electrical Bandwidth	BW_E	75	125		MHz	-3 dB electrical	Note 7
Bandwidth * Rise Time Product			0.41		Hz *s		
Electrical Rise, Fall Times, 10-90%	t_r,t_f		3.3	5.3	ns	P_R = -15 dBm peak, @ 50 MHz	Note 8 Fig. 4
Pulse-Width Distortion	PWD		0.4	1.0	ns	P_R = -11 dBm, peak	Note 6,9 Fig. 3
Overshoot			2		%	P_R = -15 dBm, peak	Note 10

Notes:

1. 2.0 mm from where leads enter case.
2. The signal output is referred to V_{CC}, and does not reject noise from the V_{CC} power supply. Consequently, the V_{CC} power supply must be filtered. The recommended power supply is +5 V on V_{CC} for typical usage with +5 V ECL logic. A -5 V power supply on V_{EE} is used for test purposes to minimize power supply noise.
3. Typical specifications are for operation at T_A = 25°C and V_{CC} = +5 V_{DC}.
4. The test circuit layout should be in accordance with good high frequency circuit design techniques.
5. Measured with a 9-pole "brick wall" low-pass filter [Mini-Circuits™, BLP-100*] with -3 dB bandwidth of 100 MHz.
6. -11.0 dBm is the maximum peak input optical power for which pulse-width distortion is less than 1 ns.
7. Electrical bandwidth is the frequency where the responsivity is -3 dB (electrical) below the responsivity measured at 50 MHz.
8. The specifled rise and fall times are referenced to a fast square wave optical source. Rise and fall times measured using an LED optical source with a 2.0 ns rise and fall time (such as the HFBR-1312T) will be approximately 0.6 ns longer than the specifled rise and fall times. E.g.: measured $t_{r,f} \simeq [(\text{specifled } t_{r,f})^2 + (\text{test source optical } t_{r,f})^2]^{1/2}$.
9. 10 ns pulse width, 50% duty cycle, at the 50% amplitude point of the waveform.
10. Percent overshoot is defined as: $((V_{PK} - V_{100\%})/V_{100\%}) \times 100\%$. The overshoot is typically 2% with an input optical rise time ≤ 1.5 ns.
11. The bandwidth*risetime product is typically 0.41 because the HFBR-2316T has a second-order bandwidth limiting characteristic.

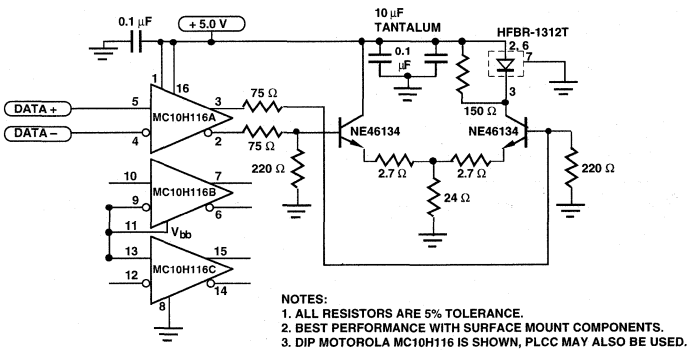


Figure 1. HFBR-2316T Receiver Test Circuit.

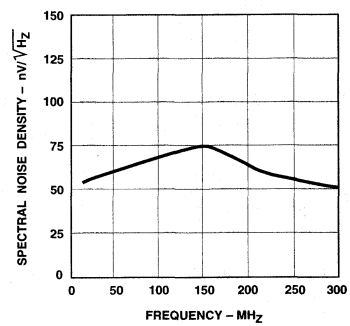


Figure 2. Typical Output Spectral Noise Density vs. Frequency.

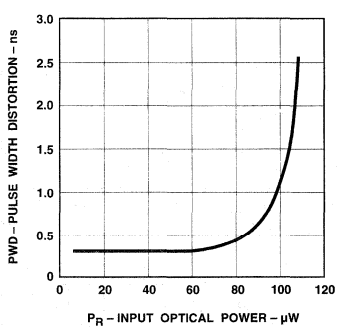


Figure 3. Typical Pulse Width Distortion vs. Peak Input Power.

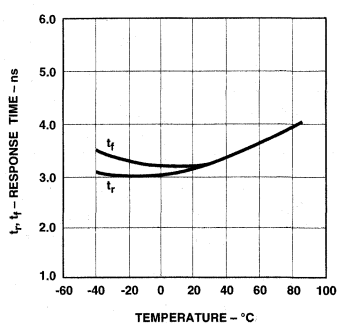


Figure 4. Typical Rise and Fall Times vs. Temperature.

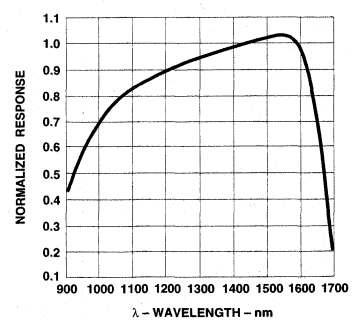


Figure 5. Normalized Receiver Spectral Response.

*Mini-Circuits Division of Components Corporation.

HEWLETT® PACKARD

1300 nm E-LED Transmitter and PIN/Preamp Receiver for Single-Mode Fiber

Technical Data

HFBR-0305 Series

Features

- **Distances Up to 14 km at Signal Rates of 20 MBd**
- **Performance Specified With Single-Mode Fiber Cables**
- **Wave Solder and Aqueous Wash Process Compatible**
- **Panel Mount ST Connectors**
- **Pinout Compatible With HFBR-0400 Series Parts**

Applications

- **Single-Mode Extensions to Ethernet (10Base-F) Links**
- **Proprietary Links Using Single-Mode Fiber**

Description

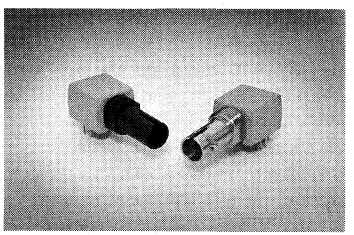
The HFBR-0305 Series is designed to provide the most cost-effective single-mode solution, and is pin-compatible with HP's HFBR-0400 and HFBR-0300 families of 820 and 1300 nm fiber optic links for multimode fiber. This allows designers to use a single circuit and board layout for 820 nm multimode fiber links, 1300 nm multimode fiber links, and 1300 nm single-mode fiber links. Upgrading a multimode solution to single-mode fiber is as simple as switching components on a board.

Transmitter

The HFBR-1315TM/1315M single-mode fiber-optic transmitter contains a 1300 nm edge-emitting LED (E-LED) capable of efficiently launching optical power into single-mode fiber. Because it is an LED, and not a laser, the drive circuit is simple and compatible with drive circuits for multimode LED transmitters.

Receiver

The HFBR-2315T/2315M receiver contains an InGaAs PIN photodiode and a low-noise transimpedance preamplifier operating in the 1300 nm wavelength region. The HFBR-2315T/2315M receives an optical signal and converts it to an analog voltage. The buffered output is an emitter-follower, with a frequency response from dc to typically 125 MHz.



Package

HFBR-0305 Series transmitters and receivers are housed in a dual-in-line package made of high strength, heat resistant, chemical resistant, and UL V-0 flame retardant plastic. The HFBR-1315TM/1315M is a stainless steel, threaded ST port (panel mountable); the HFBR-1315M is a stainless steel, unthreaded ST port. The HFBR-2315T is a black, non-conductive plastic threaded ST port (panel mountable); the HFBR-2315M is a stainless steel, unthreaded ST port.

Package Options

	Metal Port	Plastic Port
Transmitter:		
Threaded	HFBR-1315TM	N/A
Unthreaded	HFBR-1315M	N/A
Receiver:		
Threaded	N/A	HFBR-2315T
Unthreaded	HFBR-2315M	N/A

ESD Handling Precautions

The HFBR-0305 Series products are MIL-STD 883C Method 3015.4 Class 1 devices. Normal static precautions should be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by electrostatic discharge (ESD)

Solder Processing

The HFBR-0305 Series products are compatible with either hand or wave solder processes. When soldering, it is advisable to leave the protective cap on the port to keep the optics clean. Good system performance requires clean port optics and cable ferrules to avoid obstructing the optical path. Clean compressed air is often sufficient to remove particles of dirt; methanol on a cotton swab also works well.

Wash Processing - Chemical Resistance

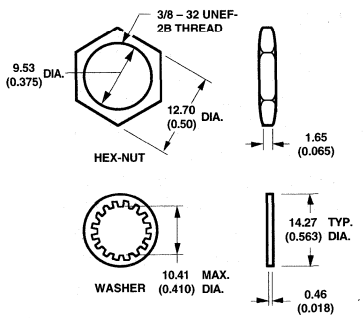
The HFBR-0305 Series package is compatible with the following chemicals for cleaning and degreasing:

- Aqueous Wash
- Naptha
- Alcohol (methyl, isopropyl, isobutyl)
- Aliphatics (hexane, heptane)

The following chemicals are not recommended as they will damage the package: Partially halogenated hydrocarbons such as 1,1,1 Trichloroethane, Ketones such as MEK, Acetone, Chloroform, Ethyl Acetate, Methylene Dichloride and N-methylpyroldone.

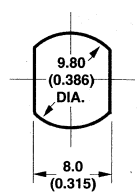
Panel Mounting of Threaded ST Package Style

Any standard 3/8 - 32 UNEF-2B threaded nut and washer can be used to secure the threaded ST receptacle to the chassis wall, provided the overall thickness of the chassis wall, washer and nut are less than 5.1 mm (0.2 inch). Hewlett-Packard supplies the HFBR-4411 kit which consists of 100 each, nuts and washers per the figure below.



NOTE: ALL DIMENSIONS IN MILLIMETRES AND (INCHES).

When preparing the chassis wall for panel mounting, use the mounting template in the figure below. When tightening the nut, torque should not exceed 0.8 N-m (8.0 in-lb). Note that the maximum nut dimension exceeds the width of the port package, so approximately 2 mm of space between device packages is required to allow nuts to be mounted on adjacent ports.



Flame Resistance

The HFBR-0305 Series package is made with UL V-0 flame retardant plastic material.

Electrostatic Discharge (ESD)

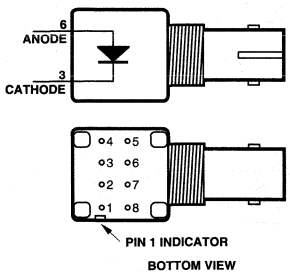
Static discharges can occur to the exterior of the equipment chassis containing the HFBR-0305 Series parts. To the extent that their connector receptacles are exposed to the outside of the equipment chassis, they may be subject to whatever ESD system level test criteria that the equipment is intended to meet.

Radiated Susceptibility

Equipment utilizing these products will be subject to EMI fields in some environments. These HFBR-0305 Series products are expected to withstand fields of up to 10 volts per meter, when tested on a circuit card in free space without an equipment chassis, with no measurable effect on their performance. A suggested test method is based on the equipment procedure specified in IEC 801-3.

Pinout Description

HFBR-1315TM/1315M Transmitters

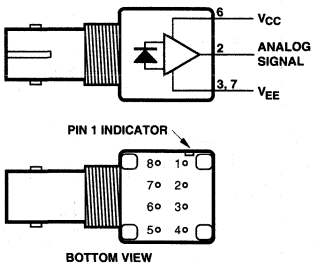


PIN	FUNCTION
1†	N.C.
2*	N.C.
3	CATHODE
4†	N.C.
5†	N.C.
6	ANODE
7	N.C.
8†	N.C.

* THERE IS NO PIN 2. I.E., IN THE NUMBER 2 PIN POSITION, THERE IS NO PHYSICAL PIN.

† PINS 1, 4, 5, AND 8 ARE ISOLATED FROM THE INTERNAL CIRCUITRY, BUT ARE ELECTRICALLY CONNECTED TO EACH OTHER AND TO THE METAL PORT.

HFBR-2315T/2315M Receivers



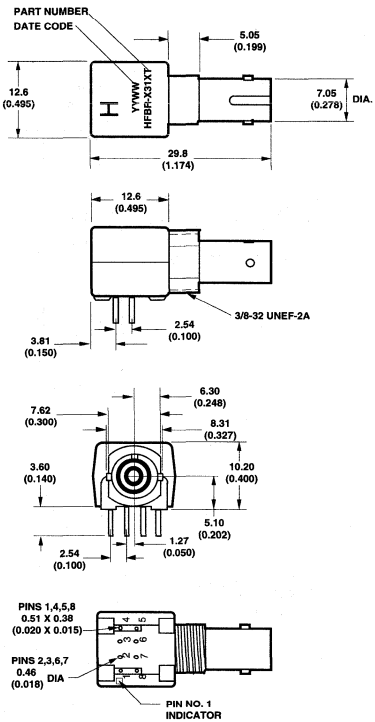
PIN	FUNCTION
1†	N.C.
2	SIGNAL
3*	VEE
4†	N.C.
5†	N.C.
6	VCC
7*	VEE
8†	N.C.

* PINS 3 AND 7 ARE ELECTRICALLY CONNECTED TO THE HEADER.

† PINS 1, 4, 5, AND 8 ARE ISOLATED FROM THE INTERNAL CIRCUITRY, BUT ARE ELECTRICALLY CONNECTED TO EACH OTHER (AND TO THE PORT IF METAL).

Mechanical Dimensions

All dimensions are in millimeters and (inches)



Recommended Operating Conditions for HFBR-0305 Series Products

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Operating Temperature - Ambient	T_A	0		70	°C	
Supply Voltage	V_{CC}	4.75		5.25	V	Note 1

Note:

1. The HFBR-2315T/2315M signal output is referenced to V_{CC}, and does not reject noise from the V_{CC} power supply. Consequently, the V_{CC} power supply must be filtered.

Link Performance: At Data Rates 1-20 MBd

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Reference
Optical Power Budget with Single-Mode Fiber Cables	OPB	9	18		dB	0 to 70°C	Note 1
Link Distance with Single-Mode Fiber Cables	ℓ	14			km	0 to 70°C	Note 2

Notes:

1. Optical Power Budget applies to HFBR-1315TM/1315M and HFBR-2315T/2315M in the recommended application circuit (Figures 1 and 2). Worst case transmitter coupled power (P_T) is -27 dBm peak, -30 dBm average. Worst case receiver sensitivity is -36 dBm peak, -39 dBm average. Refer to Application Note 1082 for details.
2. Link distance is based on fiber with 0.5 dB/km attenuation, and assumes 1 dB for loss of in-line splices or connectors, and 1 dB margin for LED aging: (9 dB OPB - 1 dB in-line splice loss - 1 dB aging margin)/(0.5 dB/km) = 14 km.

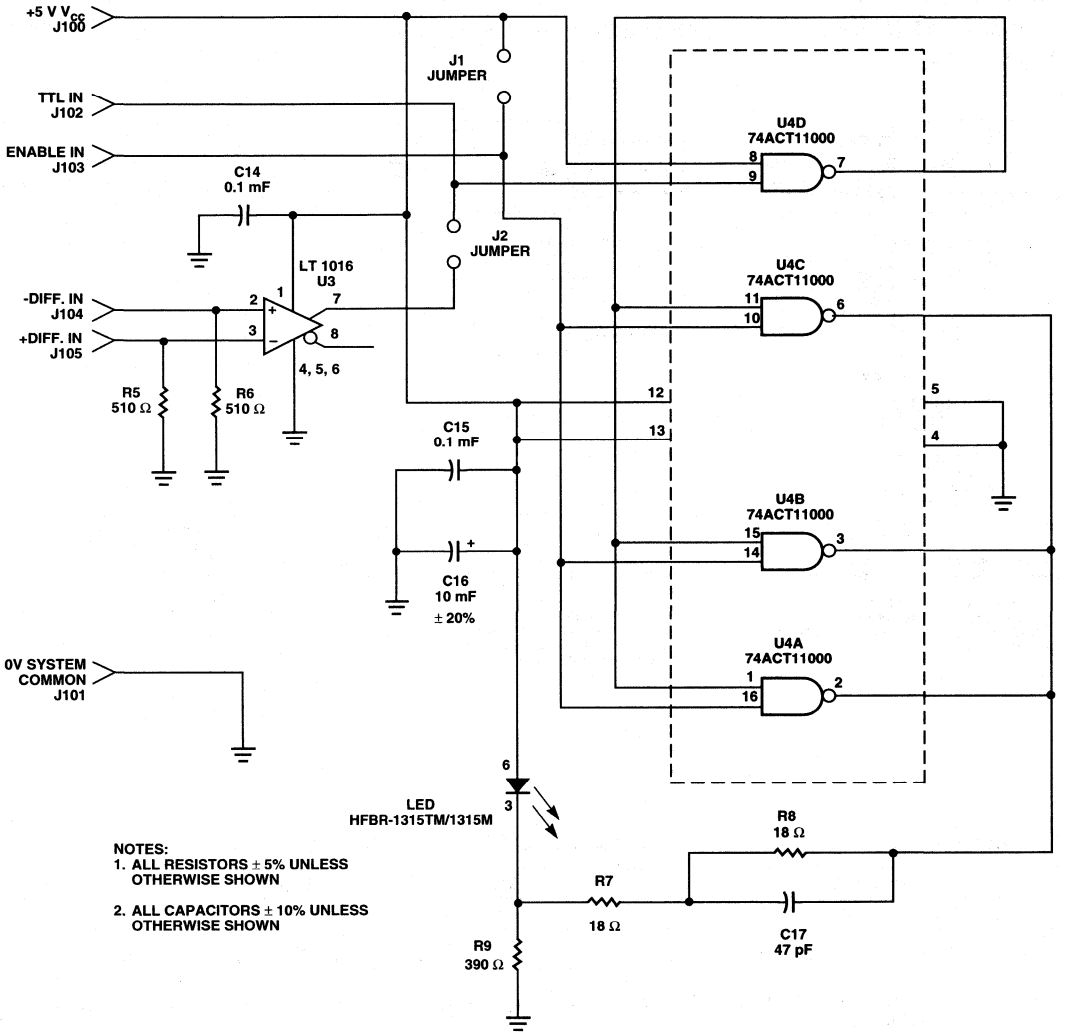


Figure 1. Recommended Transmitter Circuit.

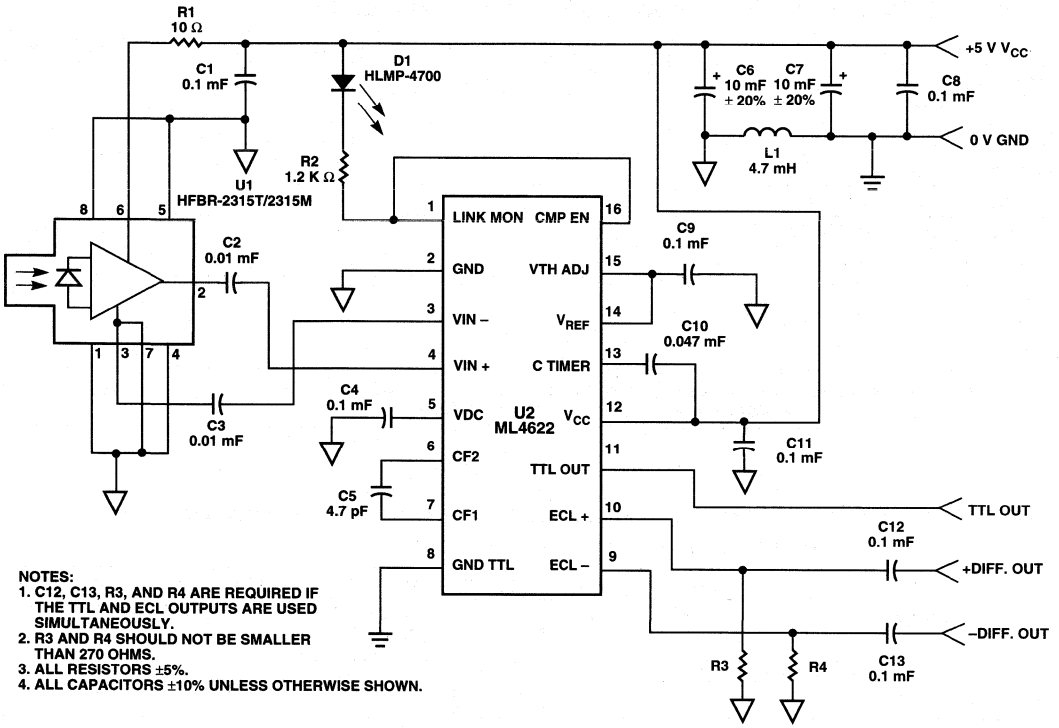


Figure 2. Recommended Receiver Circuit.

HFBR-1315TM/1315M - Transmitter Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Condition
Storage Temperature	T_S	-40	85	°C	
Operating Temperature	T_A	-40	85	°C	
Lead Soldering Cycle Temperature			260	°C	Note 1
Lead Soldering Cycle Time			10	sec	
Forward Input Current dc	I_{FDC}		100	mA	
Forward Input Current, Peak	I_{FPK}		175	mA	1 sec pulse
Reverse Input Voltage	V_R		2	V	

Notes:
1. 2.0 mm from where leads enter case.

CAUTION: It is advised that normal static precautions be taken in handling or assembly of these components to prevent damage and/or degradation which may be induced by ESD.

HFBR-1315TM/1315M - Transmitter Electrical/Optical Characteristics

(T_A = 0°C to 70°C, I_F = 100 mA unless otherwise specified)

Parameter	Symbol	Min.	Typ.[1]	Max.	Unit	Condition	Reference
Forward Voltage	V_F	1.1	1.5	1.9	V	T_A = 25°C	Figure 3
		1.0		2.0			
Forward Voltage Temperature Coefficient	$\Delta V_F/\Delta T$		-3.4		mV/°C		
Center Emission Wavelength	λ_C	1265	1310	1380	nm		
Spectral Width - FWHM	$\Delta\lambda$		95	125	nm	T_A = 25°C	
				140			
Optical Power Temperature Coefficient	$\Delta P_T/\Delta T$		-0.07		dB/°C		
Reverse Leakage Current	I_R			200	µA	T_A = 25°C, V_R = -2 V	
Thermal Resistance	θ_{JA}		105		°C/W		Note 2

Notes:
1. Typical data are at T_A = 25°C.
2. Thermal resistance is measured with the transmitter coupled to a connector assembly and mounted on a printed circuit board; $\theta_{JC} < \theta_{JA}$.

HFBR-1315TM/1315M - Transmitter Optical Output Power and Dynamic Characteristics

Parameter	Symbol	Min.	Typ.[1]	Max.	Unit	Conditions		Reference
						T_A	$I_{F,peak}$	
Peak Power	P_T	-23	-21	-17	dBm	25°C	100 mA	Note 2
Single-mode		-27		-15		0-70°C	100 mA	Figure 4
Rise, Fall Time (10% to 90%)	t_r, t_f			4.5	ns	0-70°C	100 mA, No Pre-bias	Note 4 Figure 5
Rise, Fall Time (10% to 90%)	t_r, t_f		2.6 1.6		ns	0-70°C	100 mA, With Pre-bias	Note 4 Figure 1

Notes:

1. Typical data are at T_A = 25°C.
2. Optical power is measured with a large area detector at the end of 1 meter of single-mode cable, with an ST* precision ceramic ferrule (MIL-STD-83522/13), which approximates a standard test connector.
3. When changing from µW to dBm, the optical power is referenced to 1 mW (1000 µW). Optical power P(dBm) = 10*log[P(µW)/1000µW].
4. Optical rise and fall times are measured from 10% to 90% with single-mode fiber. The "No Pre-bias" response time is measured in the recommended test circuit (50 ohm load, Figure 5) at 25 MHz, 50% duty cycle. The response time "With Pre-bias" is measured in the recommended application circuit (Figure 1).

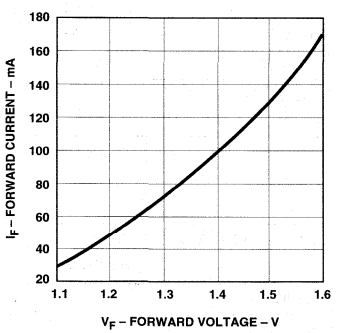


Figure 3. Typical Forward Voltage and Current Characteristics, 25°C.

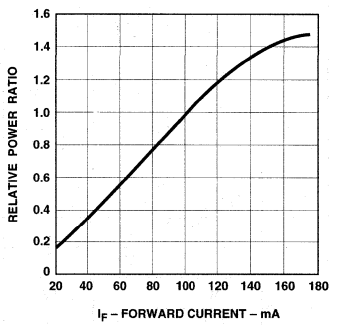


Figure 4. Normalized Transmitter Output Power vs. Forward Current, 25°C.

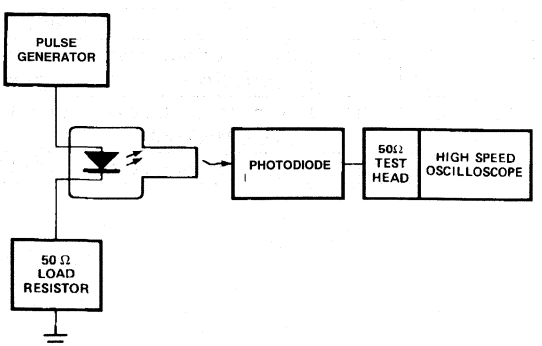


Figure 5. Test Circuit for Measuring t_r, t_f Without Pre-Bias.

HFBR-2315TM/2315M - Receiver Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Condition
Storage Temperature	T_S	-55	85	°C	
Operating Temperature	T_A	-40	+85	°C	
Lead Soldering Cycle Temperature			260	°C	Note 1
Lead Soldering Cycle Time			10	sec	
Signal Pin Voltage	V_O	-0.5	V_{CC}	V	
Supply Voltage	(V_{CC} - V_{EE})	-0.5	6.0	V	Note 2
Output Current	I_O		25	mA	

CAUTION: It is advised that normal static precautions be taken in handling or assembly of these components to prevent damage and/or degradation which may be induced by ESD.

HFBR-2315T/2315M - Electrical/Optical and Dynamic Characteristics

(T_A = 0°C to 70°C; 4.75 V < (V_{CC} - V_{EE}) < 5.25 V; power supply must be filtered per note 2)

Parameter	Symbol	Min.	Typ.[3]	Max.	Unit	Condition	Reference
Responsivity, Single-Mode Fiber	R_P	8.5	17	24	mV/μW	λ_p = 1300 nm, 50 MHz	Note 4, Figures 6, 10
RMS Output Noise Voltage	V_{NO}		0.4	0.59	mV_{RMS}	@100 MHz, P_R = 0 mW	Note 5 Figure 7
				1.0	mV_{RMS}	Unfiltered Bandwidth P_R = 0 mW	
Equivalent Optical Noise Input Power (RMS)	$P_{N,RMS}$		-45	-41.5	dBm	@100 MHz, P_R = 0 mW	Note 5
			0.032	0.071	μW		
Peak Input Optical Power, Single-Mode	P_R			-14	dBm	50 MHz, 1 ns PWD	Note 6 Figure 8
				40	μW		
Output Impedance	Z_O		30		Ω	f = 50 MHz	
DC Output Voltage	$V_{O,DC}$	0.8	1.8	2.6	V	V_{CC} = 5 V, V_{EE} = 0 V P_R = 0 mW	
Supply Current	I_{CC}		9	15	mA	R_{LOAD} = ∞	
Electrical Bandwidth	BW_E	75	125		MHz	-3 dB electrical	Note 7
Bandwidth * Rise Time			0.41		Hz * s		Note 8
Electrical Rise, Fall Times, 10-90%	$t_{r,f}$		3.3	5.3	ns	P_R = -21 dBm Peak, @ 50 MHz	Note 9 Figure 9
Pulse-Width Distortion	PWD		0.4	1.0	ns	P_R = -14 dBm, Peak, Single-Mode Fiber	Note 10 Figure 8
Overshoot			2		%	P_R = -21 dBm, Peak	Note 11

Notes:

1. 2.0 mm from where leads enter case.
2. The signal output is an emitter follower, which does not reject noise from V_{CC}. Consequently, the power supply must be filtered. The recommended supply is +5 V on V_{CC} for typical usage with +5 V ECL logic. A -5 V supply on V_{EE} is used for test purposes to minimize supply noise.
3. Typical specifications are for operation at T_A = 25°C, V_{CC} = +5 V_{DC}, V_{EE} = 0 V.
4. The test circuit layout should be in accordance with good high frequency circuit design techniques.
5. Measured with a Mini-Circuits 9-pole "brick wall" low-pass filter, BLP-100, with -3 dB bandwidth of 100 MHz.
6. -14 dBm is the maximum peak input optical power from single-mode fiber for which pulse-width distortion is less than 1 ns.
7. Electrical bandwidth is the frequency where the responsivity is -3 dB (electrical) below the responsivity measured at 50 MHz.
8. The bandwidth * risetime product is typically 0.41 because the HFBR-2315T/2315M has a second-order bandwidth limiting characteristic.
9. The specified rise and fall times are referenced to a fast square wave optical source. Rise and fall times measured using an LED optical source with a 2.0 ns rise and fall time (such as the HFBR-1315TM/1315M) will be approximately 0.6 ns longer than the specified rise and fall times. E.g.: measured $t_{r,f} \cong [(\text{specified } t_{r,f})^2 + (\text{test source optical } t_{r,f})^2]^{1/2}$
10. 10 ns pulse width, 50% duty cycle, at the 50% amplitude point of the waveform.
11. Percent overshoot is defined as: $((V_{PK} - V_{100\%})/V_{100\%}) \times 100\%$. The overshoot is typically 2% with an input optical rise time < 1.5 ns.

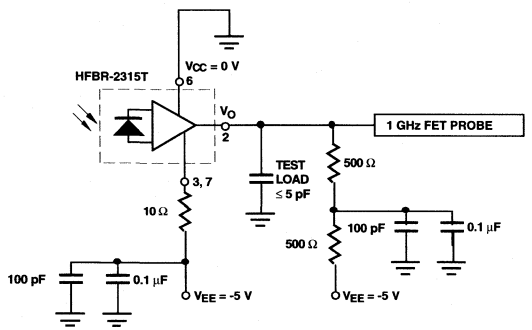


Figure 6. HFBR-2315T/2315M Receiver Test Circuit.

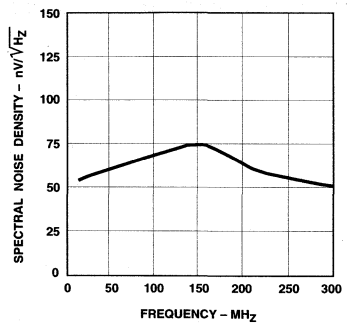


Figure 7. Typical Output Spectral Noise Density vs. Frequency.

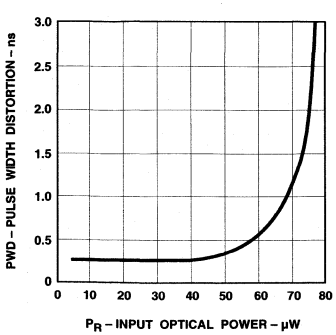


Figure 8. Typical Pulse Width Distortion vs. Peak Input Power.

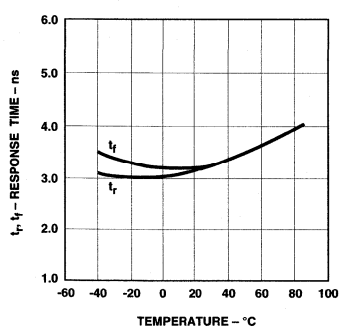


Figure 9. Typical Rise and Fall Times vs. Temperature.

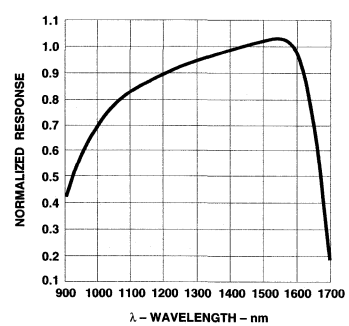


Figure 10. Normalized Receiver Spectral Response.

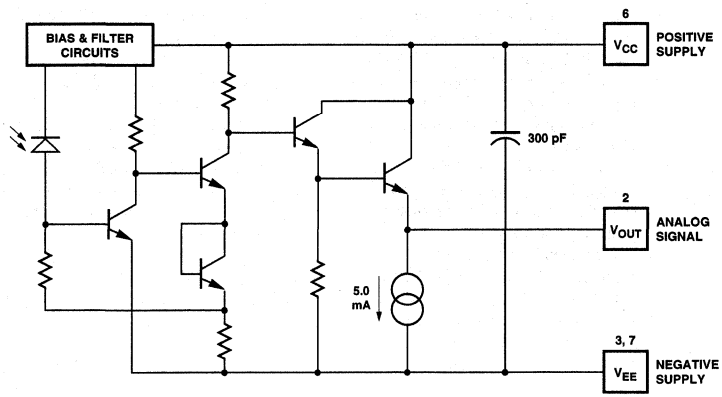


Figure 11. HFBR-2315T Simplified Schematic Diagram.

HEWLETT® PACKARD

Low Cost, Miniature Fiber Optic Components with ST®, SMA, SC and FC Ports

Technical Data

HFBR-0400 Series

Features

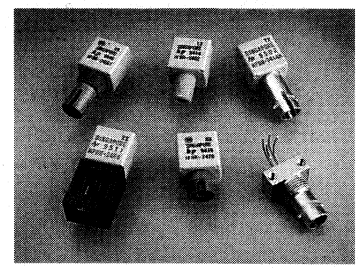
- **Meets IEEE 802.3 Ethernet and 802.5 Token Ring Standards**
- **Low Cost Transmitters and Receivers**
- **Choice of ST®, SMA, SC or FC Ports**
- **820 nm Wavelength Technology**
- **Signal Rates up to 175 Megabaud**
- **Link Distances Up to 4 km**
- **Specified with 50/125 µm, 62.5/125 µm, 100/140 µm, and 200 µm HCS® Fiber**
- **Repeatable ST Connections within 0.2 dB Typical**
- **Unique Optical Port Design for Efficient Coupling**
- **Auto-Insertable and Wave Solderable**
- **No Board Mounting Hardware Required**
- **Wide Operating Temperature Range -40°C to 85°C**
- **AlGaAs Emitters 100% Burn-In Ensures High Reliability**
- **Conductive Port Option with the SMA and ST Threaded Port Styles**

Applications

- **Local Area Networks**
- **Computer to Peripheral Links**
- **Computer Monitor Links**
- **Digital Cross Connect Links**
- **Central Office Switch/PBX Links**
- **Video Links**
- **Modems and Multiplexers**
- **Suitable for Tempest Systems**
- **Industrial Control Links**

Description

The HFBR-0400 Series of components is designed to provide cost effective, high performance fiber optic communication links for information systems and industrial applications with link distances of up to 4 kilometers. With the HFBR-24X6, the 125 MHz analog receiver, data rates of up to 175 megabaud are attainable.



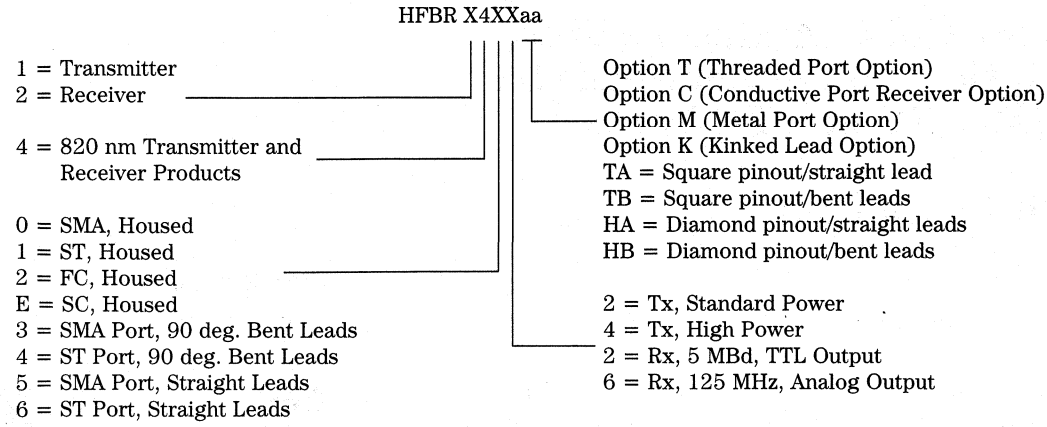
Transmitters and receivers are directly compatible with popular "industry-standard" connectors: ST, SMA, SC and FC. They are completely specified with multiple fiber sizes; including 50/125 µm, 62.5/125 µm, 100/140 µm, and 200 µm.

Complete evaluation kits are available for ST and SMA product offerings; including transmitter, receiver, connectored cable, and technical literature. In addition, ST and SMA connectored cables are available for evaluation.

FIBER OPTICS

ST® is a registered trademark of AT&T.
HCS® is a registered trademark of the SpecTran Corporation.

HFBR-0400 Series Part Number Guide



LINK SELECTION GUIDE

Data Rate (MBd)	Distance (m)	Transmitter	Receiver	Fiber Size (μm)	Evaluation Kit
5	1500	HFBR-14X2	HFBR-24X2	200 HCS	N/A
5	2000	HFBR-14X4	HFBR-24X2	62.5/125	HFBR-04X0
20	2700	HFBR-14X4	HFBR-24X6	62.5/125	HFBR-0414, HFBR-0463
32	2200	HFBR-14X4	HFBR-24X6	62.5/125	HFBR-0414
55	1400	HFBR-14X4	HFBR-24X6	62.5/125	HFBR-0414
125	700	HFBR-14X4	HFBR-24X6	62.5/125	HFBR-0416
155	600	HFBR-14X4	HFBR-24X6	62.5/125	HFBR-0416
175	500	HFBR-14X4	HFBR-24X6	62.5/125	HFBR-0416

For additional information on specific links see the following individual link descriptions. Distances measured over temperature range from 0 to 70°C.

Applications Support Guide

This section gives the designer information necessary to use the HFBR-0400 series components to make a functional fiber-optic transceiver. HP offers a wide selection of evaluation kits for hands-on experience with fiber-optic products as well as a wide range of application notes complete with circuit diagrams and board layouts. Furthermore, HP's application support group is always ready to assist with any design consideration.

Application Literature

Title	Description
HFBR-0400 Series Reliability Data	Transmitter & Receiver Reliability Data
Application Bulletin 73	Low Cost Fiber Optic Transmitter & Receiver Interface Circuits
Application Bulletin 78	Low Cost Fiber Optic Links for Digital Applications up to 155 MBd
Application Note 1038	Complete Fiber Solutions for IEEE 802.3 FOIRL, 10Base-FB and 10 Base-FL
Application Note 1065	Complete Solutions for IEEE 802.5J Fiber-Optic Token Ring
Application Note 1073	HFBR-0319 Test Fixture for 1X9 Fiber Optic Transceivers
Application Note 1086	Optical Fiber Interconnections in Telecommunication Products

HFBR-0400 Series Evaluation Kits

HFBR-0410 ST Evaluation Kit

Contains the following :

- One HFBR-1412 transmitter
- One HFBR-2412 five megabaud TTL receiver
- Three meters of ST connectored 62.5/125 (μm fiber optic cable with low cost plastic ferrules.
- Related literature

HFBR-0414 ST Evaluation Kit

Includes additional components to interface to the transmitter and receiver as well as the PCB to reduce design time.

Contains the following:

- One HFBR-1414T transmitter
- One HFBR-2416T receiver
- Three meters of ST connectored 62.5/125 μm fiber optic cable
- Printed circuit board
- ML-4622 CP Data Quantizer
- 74ACTllOOON LED Driver
- LT1016CN8 Comparator
- 4.7 μH Inductor
- Related literature

HFBR-0400 SMA Evaluation Kit

Contains the following :

- One HFBR-1402 transmitter
- One HFBR-2402 five megabaud TTL receiver
- Two meters of SMA connectored 1000 μm plastic optical fiber
- Related literature

HFBR-0416 Evaluation Kit

Contains the following:

- One fully assembled 1x9 transceiver board for 155 MBd evaluation including:
  -HFBR-1414 transmitter
  -HFBR-2416 receiver
  -circuitry
- Related literature

HFBR-0463 Ethernet MAU Evaluation Kit

Contains the following:

- One fully assembled Media Attachment Unit (MAU) board which includes:
  -HFBR-1414 transmitter
  -HFBR-2416 receiver
  -HFBR-4663 IC
- Related literature

Note: Cable not included. Order HFBR-BXS010 seperately (2 pieces)

Package and Handling Information

Package Information

All HFBR-0400 Series transmitters and receivers are housed in a low-cost, dual-inline package that is made of high strength, heat resistant, chemically resistant, and UL 94V-O flame retardant ULTEM® (plastic (UL File #E121562). The transmitters are easily identified by the light grey color connector port. The receivers are easily identified by the dark grey color connector port. (Black color for conductive port.) The package is designed for auto-insertion and wave soldering so it is ideal for high volume production applications.

Handling and Design Information

Each part comes with a protective port cap or plug covering the optics. These caps/plugs will vary by port style. When soldering, it is advisable to leave the protective cap on the unit to keep the optics clean. Good system performance requires clean port optics and cable ferrules to avoid obstructing the optical path. Clean compressed air often is sufficient to remove particles of dirt; methanol on a cotton swab also works well.

Recommended Chemicals for Cleaning/Degreasing HFBR-0400 Products

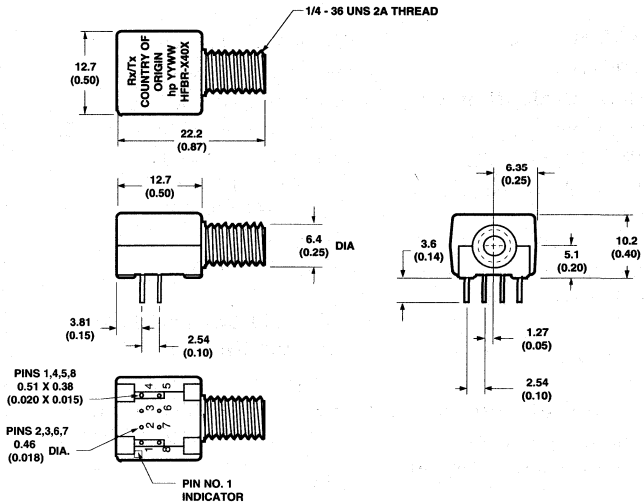
Alcohols: methyl, isopropyl, isobutyl. Aliphatics: hexane, heptane, Other: soap solution, naphtha.

Do not use partially halogenated hydrocarbons such as 1,1.1 trichloroethane, ketones such as MEK, acetone, chloroform, ethyl acetate, methylene dichloride, phenol, methylene chloride, or N-methylpyrolldone. Also, HP does not recommend the use of cleaners that use halogenated hydrocarbons because of their potential environmental harm.

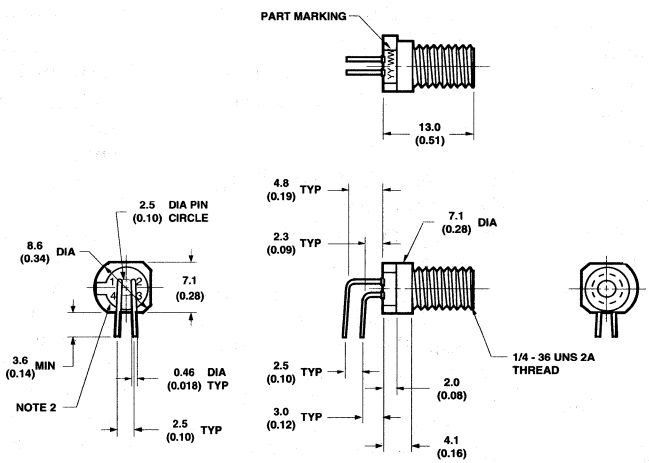
Ultem® is a registered Trademark of the GE corporation.

Mechanical Dimensions
HFBR-0400 SMA Series

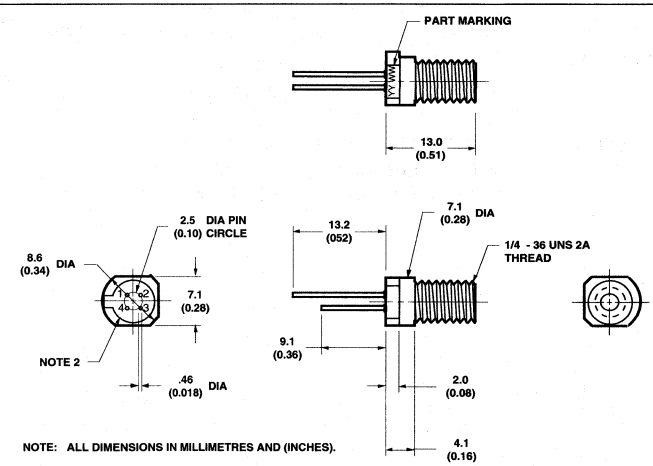
HFBR-X40X



HFBR-X43X



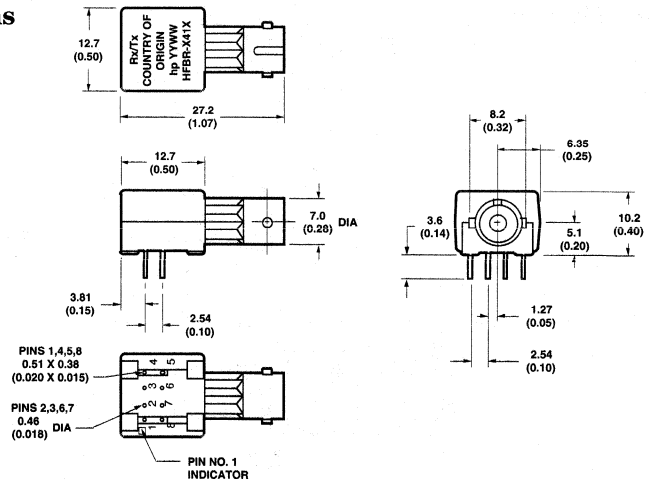
HFBR-X45X



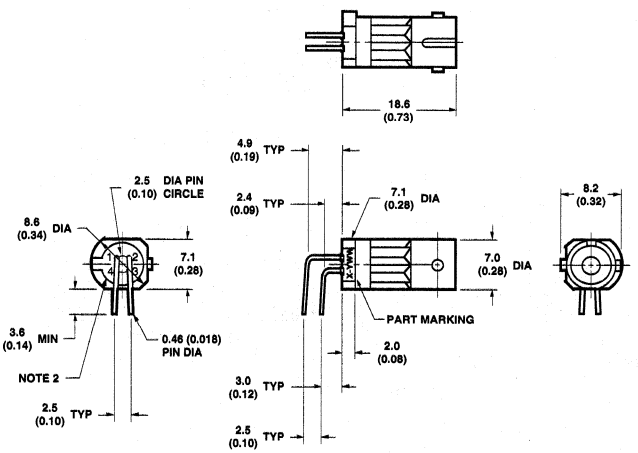
NOTE: ALL DIMENSIONS IN MILLIMETRES AND (INCHES).

Mechanical Dimensions
HFBR-0400 ST Series

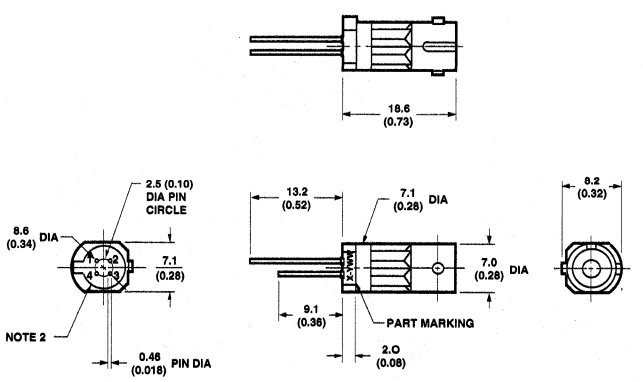
HFBR-X41X



HFBR-X44X



HFBR-X46X

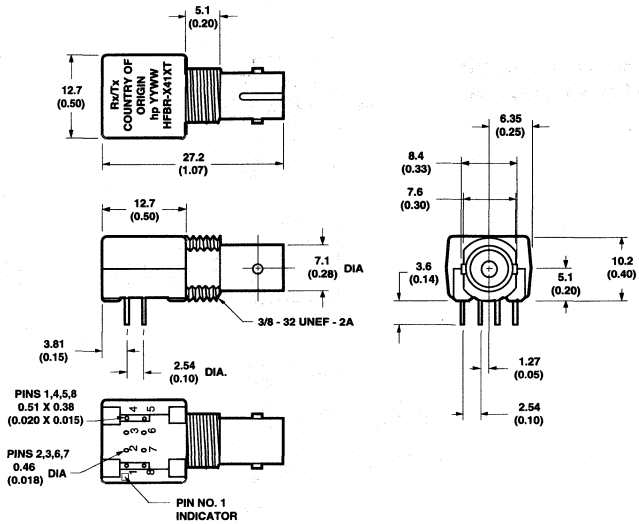


NOTE: ALL DIMENSIONS IN MILLIMETRES AND (INCHES).

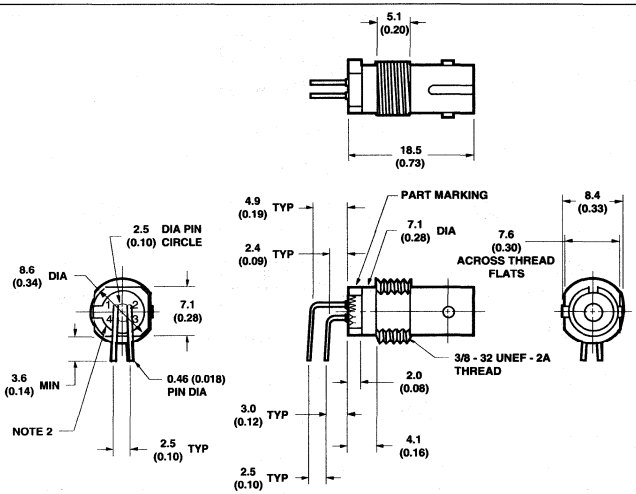
FIBER OPTICS

Mechanical Dimensions HFBR-0400T Threaded ST Series

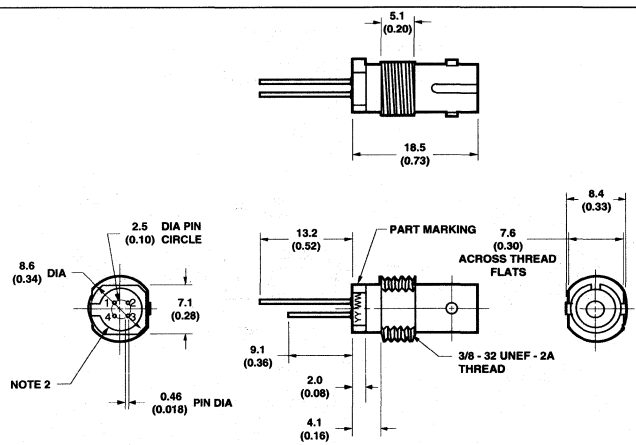
HFBR-X41XT



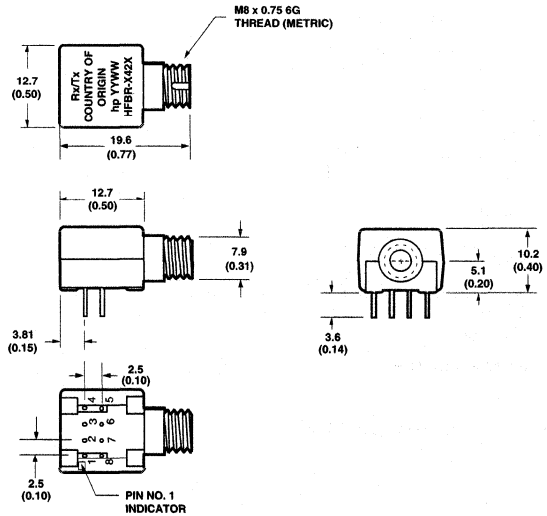
HFBR-X44XT



HFBR-X46XT

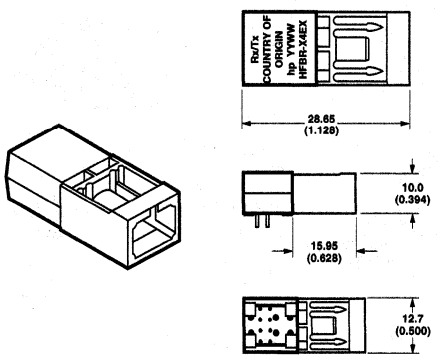


Mechanical Dimensions
HFBR-0400FC Series



Mechanical Dimensions
HFBR-0400 SC Series

HFBR-X4EX



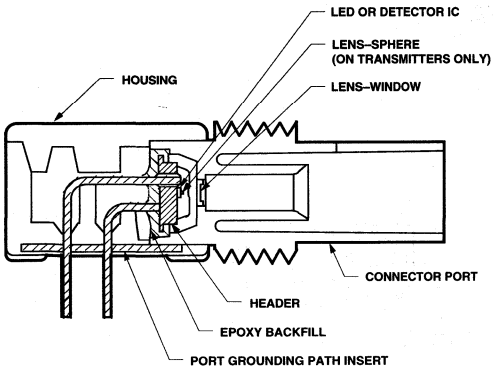
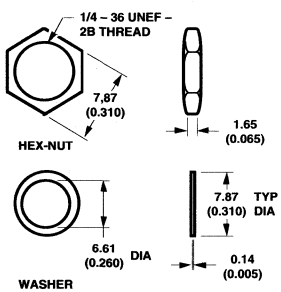


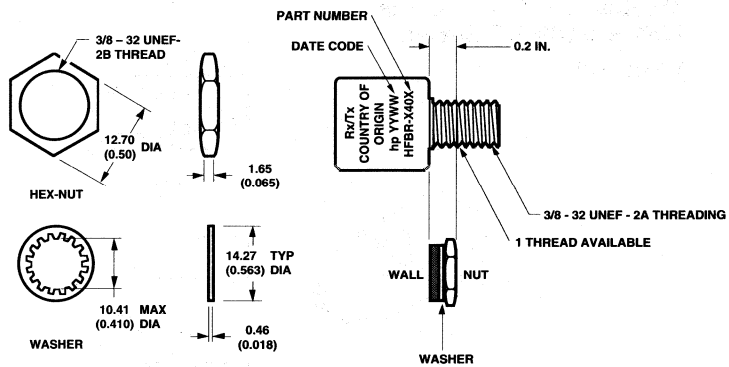
Figure 1. HFBR-0400 ST Series Cross-Sectional View.

Panel Mount Hardware

HFBR-4401: for SMA Ports



HFBR-4411: for ST Ports



(Each HFBR-4401 and HFBR-4411 kit consists of 100 nuts and 100 washers.)

Port Cap Hardware

HFBR-4402: 500 SMA Port Caps
HFBR-4120: 500 ST Port Plugs (120 psi)
HFBR-4412: 500 FC Port Caps
HFBR-4417: 500 SC Port Plugs

Options

In addition to the various port styles available for the HFBR-0400 series products, there are also several extra options that can be ordered. To order an option, simply place the corresponding option number at the end of the part number. For instance, a metal-port option SMA receiver would be HFBR-2406M. You can add any number of options in series at the end of a part number. Please contact your local sales office for further information or browse HP's fiber optics home page at http://www.hp.com/go/fiber

Option T (Threaded Port Option)

- Allows ST style port components to be panel mounted.
- Compatible with all current makes of ST multimode connectors
- Mechanical dimensions are compliant with MIL-STD-83522/13
- Maximum wall thickness when using nuts and washers from the HFBR-4411 hardware kit is 2.8 mm (0.11 inch)
- Available on all ST ports

Option C (Conductive Port Receiver Option)

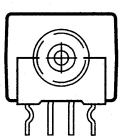
- Designed to withstand electrostatic discharge (ESD) of 25kV to the port
- Significantly reduces effect of electromagnetic interference (EMI) on receiver sensitivity
- Allows designer to separate the signal and conductive port grounds
- Recommended for use in noisy environments
- Available on SMA and threaded ST port style receivers only

Option M (Metal Port Option)

- Nickel plated aluminum connector receptacle
- Designed to withstand electrostatic discharge (ESD) of 15kV to the port
- Significantly reduces effect of electromagnetic interference (EMI) on receiver sensitivity
- Allows designer to separate the signal and metal port grounds
- Recommended for use in very noisy environments
- Available on SMA, FC, ST, and threaded ST ports

Option K (Kinked Lead Option)

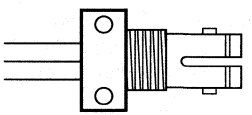
- Grounded outside 4 leads are "kinked"
- Allows components to stay anchored in the PCB during wave solder and aqueous wash processes



Options TA, TB, HA, HB (Active Device Mount Options)

(These options are unrelated to the threaded port option T.)

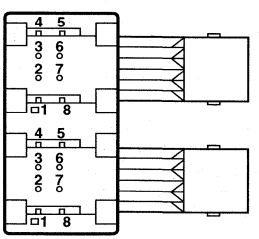
- All metal, panel mountable package with a 3 or 4 pin receptacle end
- Available for HFBR-14X4, 24X2 and 24X6 components
- Choose from diamond or square pinout, straight or bent leads ADM Picture



- TA = Square pinout/straight leads
  TB = Square pinout/bent leads
  HA = Diamond pinout/straight leads
  HB = Diamond pinout/bent leads

Duplex Option

In addition to the standard options, some HFBR-0400 series products come in a duplex configuration with the transmitter on the left and the receiver on the right. This option was designed for ergonomic and efficient manufacturing. The following part numbers are available in the duplex option:
HFBR-5414 (Duplex ST)
HFBR-5414T (Duplex Threaded ST)
HFBR-54E4 (Duplex SC)



Typical Link Data

HFBR-0400 Series

Description

The following technical data is taken from 4 popular links using the HFBR-0400 series: the 5 MBd link, Ethernet 20 MBd link, Token Ring 32 MBd link, and the 155 MBd link. The data given corresponds to transceiver solutions combining the HFBR-0400 series components and various recommended transceiver design circuits using off-the-shelf electrical components. This data is meant to be regarded as an example of typical link performance for a given design and does not call out any link limitations. Please refer to the appropriate application note given for each link to obtain more information.

5 MBd Link (HFBR-14XX/24X2)

Link Performance -40°C to +85°C unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions	Reference
Optical Power Budget with 50/125 µm fiber	OPB_{50}	4.2	9.6		dB	HFBR-14X4/24X2 NA = 0.2	Note 1
Optical Power Budget with 62.5/125 µm fiber	$OPB_{62.5}$	8.0	15		dB	HFBR-14X4/24X2 NA = 0.27	Note 1
Optical Power Budget with 100/140 µm fiber	OPB_{100}	8.0	15		dB	HFBR-14X2/24X2 NA = 0.30	Note 1
Optical Power Budget with 200 µm fiber	OPB_{200}	12	20		dB	HFBR-14X2/24X2 NA = 0.37	Note 1
Date Rate Synchronous		dc		5	MBd		Note 2
Asynchronous		dc		2.5	MBd		Note 3, Fig. 7
Propagation Delay LOW to HIGH	t_{PLH}		72		ns	T_A = 25°C, P_R = -21 dBm Peak	Figs. 6, 7, 8
Propagation Delay HIGH to LOW	t_{PHL}		46		ns		
System Pulse Width Distortion	t_{PLH}-t_{PHL}		26		ns	Fiber cable length = 1 m	
Bit Error Rate	BER			10^{-9}		Data Rate <5 Bd P_R > -24 dBm Peak	

Notes:

1. OPB at T_A = -40 to 85°C, V_{CC} = 5.0 V dc, $I_{F\,ON}$ = 60 mA. P_R = -24 dBm peak.
2. Synchronous data rate limit is based on these assumptions: a) 50% duty factor modulation, e.g., Manchester I or BiPhase Manchester II; b) continuous data; c) PLL Phase Lock Loop demodulation; d) TTL threshold.
3. Asynchronous data rate limit is based on these assumptions: a) NRZ data; b) arbitrary timing-no duty factor restriction; c) TTL threshold.

5 MBd Logic Link Design

If resistor R_1 in Figure 2 is 70.4 Ω, a forward current I_F of 48 mA is applied to the HFBR-14X4 LED transmitter. With I_F = 48 mA the HFBR-14X4/24X2 logic link is guaranteed to work with 62.5/125 µm fiber optic cable over the entire range of 0 to 1750 meters at a data rate of dc to 5 MBd, with arbitrary data format and pulse width distortion typically less than 25%. By setting R_1 = 115 Ω, the transmitter can be driven with I_F = 30 mA, if it is desired to economize on power or achieve lower pulse distortion.

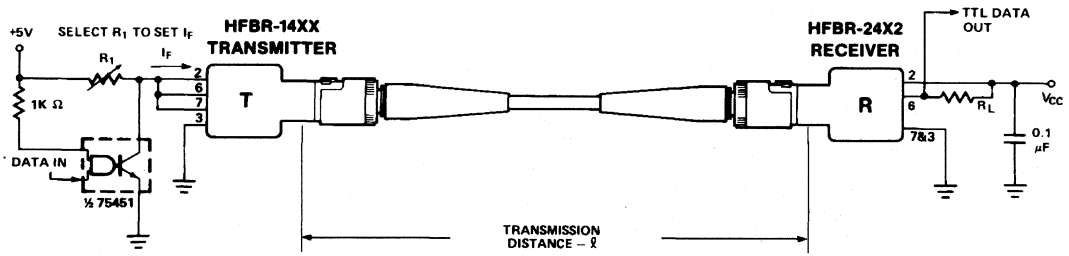
The following example will illustrate the technique for selecting the appropriate value of I_F and R_1.

Maximum distance required = 400 meters. From Figure 3 the drive current should be 15 mA. From the transmitter data V_F = 1.5 V (max.) at I_F = 15 mA as shown in Figure 9.

$$R_1 = \frac{V_{CC} - V_F}{I_F} = \frac{5\text{ V} - 1.5\text{ V}}{15\text{ mA}}$$

$$R_1 = 233\ \Omega$$

The curves in Figures 3, 4, and 5 are constructed assuming no in-line splice or any additional system loss. Should the link consists of any in-line splices, these curves can still be used to calculate link limits provided they are shifted by the additional system loss expressed in dB. For example, Figure 3 indicates that with 48 mA of transmitter drive current, a 1.75 km link distance is achievable with 62.5/125 µm fiber which has a maximum attenuation of 4 dB/km. With 2 dB of additional system loss, a 1.25 km link distance is still achievable.



NOTE:
IT IS ESSENTIAL THAT A BYPASS CAPACITOR (0.01 µF TO 0.1 µF CERAMIC) BE CONNECTED FROM PIN 2 TO PIN 7 OF THE RECEIVER. TOTAL LEAD LENGTH BETWEEN BOTH ENDS OF THE CAPACITOR AND THE PINS SHOULD NOT EXCEED 20 mm.

Figure 2. Typical Circuit Configuration.

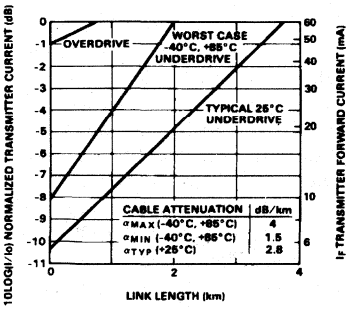


Figure 3. HFBR-1414/HFBR-2412 Link Design Limits with 62.5/125 µm Cable.

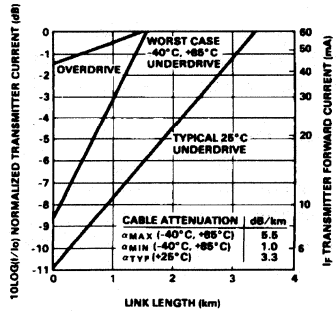


Figure 4. HFBR-14X2/HFBR-24X2 Link Design Limits with 100/140 µm Cable.

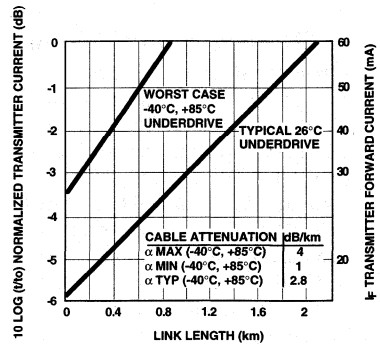


Figure 5. HFBR-14X4/HFBR-24X2 Link Design Limits with 50/125 µm Cable.

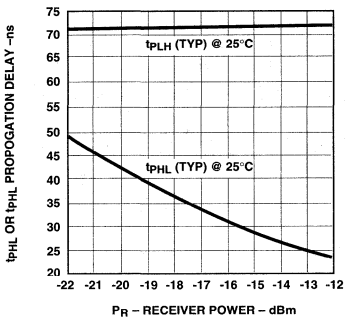


Figure 6. Propagation Delay through System with One Meter of Cable.

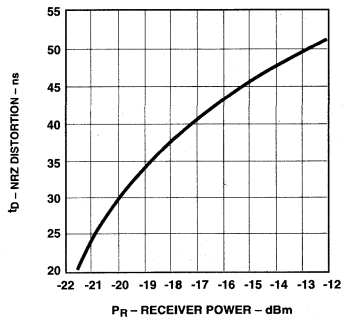


Figure 7. Typical Distortion of Pseudo Random Data at 5 Mb/s.

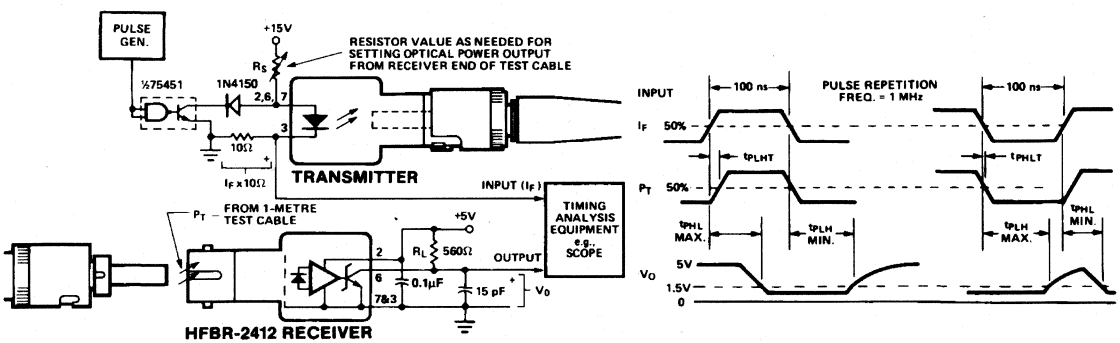


Figure 8. System Propagation Delay Test Circuit and Waveform Timing Definitions.

Ethernet 20 MBd Link (HFBR-14X4/24X6)

(refer to Application Note 1038 for details)

Typical Link Performance

Parameter	Symbol	Typ.[1,2]	Units	Conditions
Receiver Sensitivity		-34.4	dBm average	20 MBd D2D2 Hexadecimal Data 2 km 62.5/125 μm fiber
Link Jitter		7.56	ns pk-pk	ECL Out Receiver
		7.03	ns pk-pk	TTL Out Receiver
Transmitter Jitter		0.763	ns pk-pk	20 MBd D2D2 Hexadecimal Data
Optical Power	P_T	-15.2	dBm average	20 MBd D2D2 Hexadecimal Data Peak $I_{F,ON}$ = 60 mA
LED rise time	t_r	1.30	ns	1 MHz Square Wave Input
LED fall time	t_f	3.08	ns	
Mean difference	$\|t_r - t_f\|$	1.77	ns	
Bit Error Rate	BER	10^{-10}		
Output Eye Opening		36.7	ns	At AUI Receiver Output
Data Format 50% Duty Factor		20	MBd	

Notes:

1. Typical data at T_A = 25°C, V_{CC} = 5.0 V dc.
2. Typical performance of circuits shown in Figure 1 and Figure 3 of AN-1038 (see applications support section).

Token Ring 32 MBd Link (HFBR-14X4/24X6)

(refer to Application Note 1065 for details)

Typical Link Performance

Parameter	Symbol	Typ.[1,2]	Units	Conditions
Receiver Sensitivity		-34.1	dBm average	32 MBd D2D2 Hexadecimal Data 2 km 62.5/125 μm fiber
Link Jitter		6.91	ns pk-pk	ECL Out Receiver
		5.52	ns pk-pk	TTL Out Receiver
Transmitter Jitter		0.823	ns pk-pk	32 MBd D2D2 Hexadecimal Data
Optical Power Logic Level "0"	$P_{T\ ON}$	-12.2	dBm peak	Transmitter TTL in $I_{F\ ON}$ = 60 mA, $I_{F\ OFF}$ = 1 mA
Optical Power Logic Level "1"	$P_{T\ OFF}$	-82.2		
LED Rise Time	t_r	1.3	nsec	1 MHz Square Wave Input
LED Fall Time	t_f	3.08	nsec	
Mean Difference	$\|t_r - t_f\|$	1.77	nsec	
Bit Error Rate	BER	10^{-10}		
Data Format 50% Duty Factor		32	MBd	

Notes:

1. Typical data at T_A = 25°C, V_{CC} = 5.0 V dc.
2. Typical performance of circuits shown in Figure 1 and Figure 3 of AN-1065 (see applications support section)

155 MBd Link (HFBR-14X4/24X6)

(refer to Application Bulletin 78 for details)

Typical Link Performance

Parameter	Symbol	Typ.[1,2]	Units	Max.	Units	Conditions	Ref.
Optical Power Budget with 50/125 µm fiber	OPB_{50}	7.9	13.9		dB	NA = 0.2	Note 2
Optical Power Budget with 62.5/125 µm fiber	OPB_{62}	11.7	17.7		dB	NA = 0.27	
Optical Power Budget with 100/140 µm fiber	OPB_{100}	11.7	17.7		dB	NA = 0.30	
Optical Power Budget with 200 µm HCSfFiber	OPB_{200}	16.0	22.0		dB	NA = 0.35	
Data Format 20% to 80% Duty Factor		1		175	MBd		
System Pulse Width Distortion	$\lvert t_{PLH} - t_{PHL} \rvert$		1		ns	PR = -7 dBm Peak 1 meter 62.5/125 µm fiber	
Bit Error Rate	BER		10^{-9}			Data Rate < 100 MBaud PR >-31 dBm Peak	Note 2

Notes:

1. Typical data at T_A = 25°C, V_{CC} = 5.0 V dc, PECL serial interface.
2. Typical OPB was determined at a probability of error (BER) of 10^{-9}. Lower probabilities of error can be achieved with short fibers that have less optical loss.

HFBR-14X2/14X4 Low-Cost High-Speed Transmitters

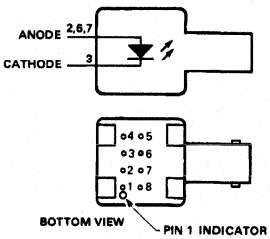
Description

The HFBR-14XX fiber optic transmitter contains an 820 nm AlGaAs emitter capable of efficiently launching optical power into four different optical fiber sizes: 50/125 µm, 62.5/125 µm, 100/140 µm, and 200 µm HCS®. This allows the designer flexibility in choosing the fiber size. The HFBR-14XX is designed to operate with the Hewlett-Packard HFBR-24XX fiber optic receivers.

The HFBR-14XX transmitter's high coupling efficiency allows the emitter to be driven at low current levels resulting in low power consumption and increased reliability of the transmitter. The HFBR-14X4 high power transmitter is optimized for small size fiber and typically can launch -15.8 dBm optical power at 60 mA into 50/125 µm fiber and -12 dBm into 62.5/125 µm fiber. The HFBR-14X2 standard transmitter typically can launch -12 dBm of optical power at 60 mA into 100/140 µm fiber cable. It is ideal for large size fiber such as 100/140 µm. The high launched optical power level is useful for systems where star couplers, taps, or inline connectors create large fixed losses.

Consistent coupling efficiency is assured by the double-lens optical system (Figure 1). Power coupled into any of the three fiber types varies less than 5 dB from part to part at a given drive current and temperature. Consistent coupling efficiency reduces receiver dynamic range requirements which allows for longer link lengths.

Housed Product



PIN	FUNCTION
1†	N.C.
2	ANODE
3*	CATHODE
4†	N.C.
5†	N.C.
6	ANODE
7*	ANODE
8†	N.C.

*PINS 2,6 AND 7 ARE ELECTRICALLY CONNECTED TO HEADER

†PINS 1, 4, 5, AND 8 ARE ELECTRICALLY CONNECTED

Unhoused Product

BOTTOM VIEW

PIN	FUNCTION
1	ANODE
2	CATHODE
3	ANODE
4	ANODE

FIBER OPTICS

Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Units	Reference
Storage Temperature		T_S	-55	+85	°C	
Operating Temperature		T_A	-40	+85	°C	
Lead Soldering Cycle	Temp.			+260	°C	
	Time			10	sec	
Forward Input Current	Peak	I_{FPK}		200	mA	Note 1
	dc	I_{Fdc}		100	mA	
Reverse Input Voltage		V_{BR}		1.8	V	

Electrical/Optical Specifications -40°C to +85°C unless otherwise specified.

Parameter	Symbol	Min.	Typ.[2]	Max.	Units	Conditions	Reference
Forward Voltage	V_F	1.48	1.70	2.09	V	I_F = 60 mA dc	Figure 9
			1.84			I_F = 100 mA dc	
Forward Voltage Temperature Coefficient	$\Delta V_F/\Delta T$		-0.22		mV/°C	I_F = 60 mA dc	Figure 9
			-0.18			I_F = 100 mA dc	
Reverse Input Voltage	V_{BR}	1.8	3.8		V	I_F = 100 µA dc	
Peak Emission Wavelength	λ_P	792	820	865	nm		
Diode Capacitance	C_T		55		pF	V = 0, f = 1 MHz	
Optical Power Temperature Coefficient	$\Delta P_T/\Delta T$		-0.006		dB/°C	I = 60 mA dc	
			-0.010			I = 100 mA dc	
Thermal Resistance	θ_{JA}		260		°C/W		Notes 3, 8
14X2 Numerical Aperture	NA		0.49				
14X4 Numerical Aperture	NA		0.31				
14X2 Optical Port Diameter	D		290		µm		Note 4
14X4 Optical Port Diameter	D		150		µm		Note 4

HFBR-14X2 Output Power Measured Out of 1 Meter of Cable

Parameter	Symbol	Min.	Typ.[2]	Max.	Unit	Conditions		Reference
50/125 µm Fiber Cable NA = 0.2	P_{T50}	-21.8	-18.8	-16.8	dBm peak	T_A = 25°C	I_F = 60 mA dc	Notes 5, 6, 9
		-22.8		-15.8				
		-20.3	-16.8	-14.4		T_A = 25°C	I_F = 100 mA dc	
		-21.9		-13.8				
62.5/125 µm Fiber Cable NA = 0.275	P_{T62}	-19.0	-16.0	-14.0	dBm peak	T_A = 25°C	I_F = 60 mA dc	
		-20.0		-13.0				
		-17.5	-14.0	-11.6		T_A = 25°C	I_F = 100 mA dc	
		-19.1		-11.0				
100/140 µm Fiber Cable NA = 0.3	P_{T100}	-15.0	-12.0	-10.0	dBm peak	T_A = 25°C	I_F = 60 mA dc	
		16.0		-9.0				
		-13.5	-10.0	-7.6		T_A = 25°C	I_F = 100 mA dc	
		-15.1		-7.0				
200 µm HCS Fiber Cable NA = 0.37	P_{T200}	-10.7	-7.1	-4.7	dBm peak	T_A = 25°C	I_F = 60 mA dc	
		-11.7		-3.7				
		-9.2	-5.2	-2.3		T_A = 25°C	I_F = 100 mA dc	
		-10.8		-1.7				

CAUTION: The small junction sizes inherent to the design of these components increase the components' susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of these components to prevent damage and/or degradation which may be induced by ESD.

HFBR-14X4 Output Power Measured Out of 1 Meter of Cable

Parameter	Symbol	Min.	Typ.[2]	Max.	Unit	Conditions		Reference
50/125 µm Fiber Cable NA = 0.2	PT50	-18.8	-15.8	-13.8	dBm peak	T_A = 25°C	I_F = 60 mA dc	Notes 5, 6, 9
		-19.8		-12.8				
		-17.3	-13.8	-11.4		T_A = 25°C	I_F = 100 mA dc	
		-18.9		-10.8				
62.5/125 µm Fiber Cable NA = 0.275	PT62	-15.0	-12.0	-10.0	dBm peak	T_A = 25°C	I_F = 60 mA dc	
		-16.0		-9.0				
		-13.5	-10.0	-7.6		T_A = 25°C	I_F = 100 mA dc	
		-15.1		-7.0				
100/140 µm Fiber Cable NA = 0.3	PT100	-9.5	-6.5	-4.5	dBm peak	T_A = 25°C	I_F = 60 mA dc	
		-10.5		-3.5				
		-8.0	-4.5	-2.1		T_A = 25°C	I_F = 100 mA dc	
		-9.6		-1.5				
200 µm HCS Fiber Cable NA = 0.37	PT200	-5.2	-3.7	+0.8	dBm peak	T_A = 25°C	I_F = 60 mA dc	
		-6.2		+1.8				
		-3.7	-1.7	+3.2		T_A = 25°C	I_F = 100 mA dc	
		-5.3		+3.8				

14X2/14X4 Dynamic Characteristics

Parameter	Symbol	Min.	Typ.[2]	Max.	Units	Conditions	Reference
Rise Time, Fall Time (10% to 90%)	t_r, t_f		4.0	6.5	nsec No Pre-bias	I_F = 60 mA Figure 12	Note 7,
Rise Time, Fall Time (10% to 90%)	t_r, t_f		3.0		nsec	I_F = 10 to 100 mA	Note 7, Figure 11
Pulse Width Distortion	PWD		0.5		nsec		Figure 11

Notes:
1. For I_{FPK} > 100 mA, the time duration should not exceed 2 ns.
2. Typical data at T_A = 25°C.
3. Thermal resistance is measured with the transmitter coupled to a connector assembly and mounted on a printed circuit board.
4. D is measured at the plane of the fiber face and defines a diameter where the optical power density is within 10 dB of the maximum.
5. P_T is measured with a large area detector at the end of 1 meter of mode stripped cable, with an ST® precision ceramic ferrule (MIL-STD-83522/13) for HFBR-1412/1414, and with an SMA 905 precision ceramic ferrule for HFBR-1402/1404.
6. When changing µW to dBm, the optical power is referenced to 1 mW (1000 µW). Optical Power P (dBm) = 10 log P (µW)/1000 µW.
7. Pre-bias is recommended if signal rate >10 MBd, see recommended drive circuit in Figure 11.
8. Pins 2, 6 and 7 are welded to the anode header connection to minimize the thermal resistance from junction to ambient. To further reduce the thermal resistance, the anode trace should be made as large as is consistent with good RF circuit design.
9. Fiber NA is measured at the end of 2 meters of mode stripped fiber, using the far-field pattern. NA is defined as the sine of the half angle,determined at 5% of the peak intensity point. When using other manufacturer's fiber cable, results will vary due to differing NA values and specification methods.

All HFBR-14XX LED transmitters are classified as IEC 825-1 Accessible Emission Limit (AEL) Class 1 based upon the current proposed draft scheduled to go in to effect on January 1, 1997. AEL Class 1 LED devices are considered eye safe. Contact your Hewlett-Packard sales representative for more information.

CAUTION: The small junction sizes inherent to the design of these components increase the components' susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of these components to prevent damage and/or degradation which may be induced by ESD.

Recommended Drive Circuits

The circuit used to supply current to the LED transmitter can significantly influence the optical switching characteristics of the LED. The optical rise/fall times and propagation delays can be improved by using the appropriate circuit techniques. The LED drive circuit shown in Figure 11 uses frequency compensation to reduce the typical rise/fall times of the LED and a small pre-bias voltage to minimize propagation delay differences that cause pulse-width distortion. The circuit will typically produce rise/fall times of 3 ns, and a total jitter including pulse-width distortion of less than 1 ns. This circuit is recommended for applications requiring low edge jitter or high-speed data transmission at signal rates of up to 155 MBd. Component values for this circuit can be calculated for different LED drive currents using the equations shown below. For additional details about LED drive circuits, the reader is encouraged to read Hewlett-Packard Application Bulletin 78 and Application Note 1038.

$$R_y = \frac{(V_{CC} - V_F) + 3.97\ (V_{CC} - V_F - 1.6\ V)}{I_{F\ ON}\ (A)}$$

$$R_{X1} = \frac{1}{2}\left(\frac{R_y}{3.97}\right)$$

$$R_{EQ2}(\Omega) = R_{X1} - 1$$

$$R_{X2} = R_{X3} = R_{X4} = 3(R_{EQ2})$$

$$C(pF) = \frac{2000(ps)}{R_{X1}(\Omega)}$$

Example for $I_{F\ ON}$ = 100 mA: V_F can be obtained from Figure 9 (= 1.84 V).

$$R_y = \frac{(5 - 1.84) + 3.97\ (5 - 1.84 - 1.6)}{0.100}$$

$$R_y = \frac{3.16 + 6.19}{0.100} = 93.5\ \Omega$$

$$R_{X1} = \frac{1}{2}\left(\frac{93.5}{3.97}\right) = 11.8\ \Omega$$

$$R_{EQ2} = 11.8 - 1 = 10.8\ \Omega$$

$$R_{X2} = R_{X3} = R_{X4} = 3(10.8) = 32.4\ \Omega$$

$$C = \frac{2000\ ps}{11.8\ \Omega} = 169\ pF$$

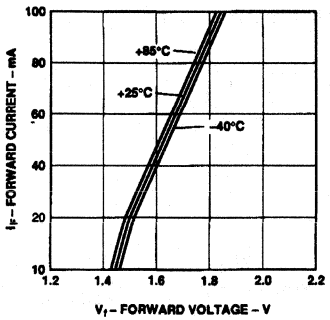


Figure 9. Forward Voltage and Current Characteristics.

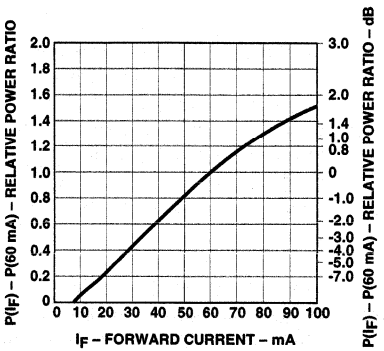


Figure 10. Normalized Transmitter Output vs. Forward Current.

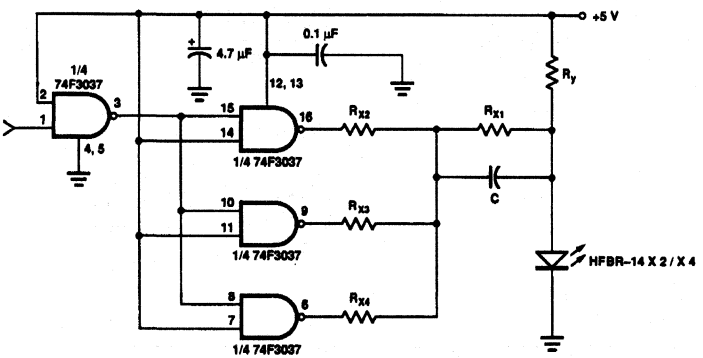


Figure 11. Recommended Drive Circuit.

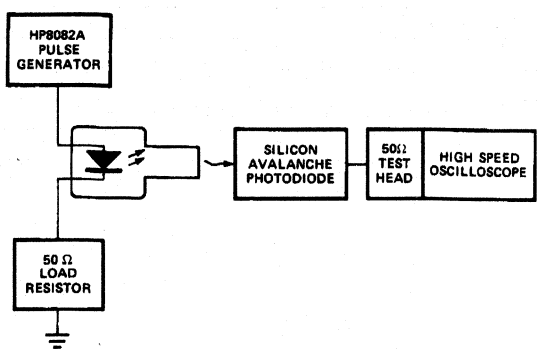


Figure 12. Test Circuit for Measuring t_r, t_f.

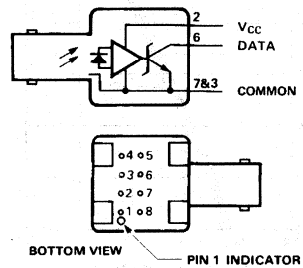
HFBR-24X2 Low-Cost 5MBd Receiver Description

The HFBR-24X2 fiber optic receiver is designed to operate with the Hewlett-Packard HFBR-14XX fiber optic transmitter and 50/125 µm, 62.5/125 µm, 100/140 µm, and 200 µm HCS® fiber optic cable. Consistent coupling into the receiver is assured by the lensed optical system (Figure 1). Response does not vary with fiber size ≤ 0.100 µm.

The HFBR-24X2 receiver incorporates an integrated photo IC containing a photodetector and dc amplifier driving an open-collector Schottky output transistor. The HFBR-24X2 is designed for direct interfacing to popular logic families. The absence of an internal pull-up resistor allows the open-collector output to be used with logic families such as CMOS requiring voltage excursions much higher than V_{CC}.

Both the open-collector "Data" output Pin 6 and V_{CC} Pin 2 are referenced to "Com" Pin 3, 7. The "Data" output allows busing, strobing and wired "OR" circuit configurations. The transmitter is designed to operate from a single +5 V supply. It is essential that a bypass capacitor (0.1 µF ceramic) be connected from Pin 2 (V_{CC}) to Pin 3 (circuit common) of the receiver.

Housed Product

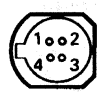


PIN	FUNCTION
1†	N.C.
2	V_{CC} (5 V)
3*	COMMON
4†	N.C.
5†	N.C.
6	DATA
7*	COMMON
8†	N.C.

*PINS 3 AND 7 ARE ELECTRICALLY CONNECTED TO HEADER

†PINS 1, 4, 5, AND 8 ARE ELECTRICALLY CONNECTED

Unhoused Product



BOTTOM VIEW

PIN	FUNCTION
1	V_{CC} (5 V)
2	COMMON
3	DATA
4	COMMON

Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Units	Reference
Storage Temperature		T_S	-55	+85	°C	
Operating Temperature		T_A	-40	+85	°C	
Lead Soldering Cycle	Temp.			+260	°C	Note 1
	Time			10	sec	
Supply Voltage		V_{CC}	-0.5	7.0	V	
Output Current		I_O		25	mA	
Output Voltage		V_O	-0.5	18.0	V	
Output Collector Power Dissipation		$P_{O\,AV}$		40	mW	
Fan Out (TTL)		N		5		Note 2

Electrical/Optical Characteristics -40°C to + 85°C unless otherwise specified

Fiber sizes with core diameter ≤ 100 µm and NA ≤ 0.35, 4.75 V ≤ V_{CC} ≤ 5.25 V

Parameter	Symbol	Min.	Typ.[3]	Max.	Units	Conditions	Reference
High Level Output Current	I_{OH}		5	250	µA	V_O = 18 P_R < -40 dBm	
Low Level Output Voltage	V_{OL}		0.4	0.5	V	I_O = 8 mA P_R > -24 dBm	
High Level Supply Current	I_{CCH}		3.5	6.3	mA	V_{CC} = 5.25 V P_R < -40 dBm	
Low Level Supply Current	I_{CCL}		6.2	10	mA	V_{CC} = 5.25 V P_R > -24 dBm	
Equivalent N.A.	NA		0.50				
Optical Port Diameter	D		400		µm		Note 4

Dynamic Characteristics

-40°C to +85°C unless otherwise specified; 4.75 V ≤ V_{CC} ≤ 5.25 V; BER ≤ 10^{-9}

Parameter	Symbol	Min.	Typ.[3]	Max.	Units	Conditions	Reference
Peak Optical Input Power Logic Level HIGH	P_{RH}			-40	dBm pk	λ_P = 820 nm	Note 5
				0.1	µW pk		
Peak Optical Input Power Logic Level LOW	P_{RL}	-25.4		-9.2	dBm pk	T_A = +25°C, I_{OL} = 8 mA	Note 5
		2.9		120	µW pk		
		-24.0		-10.0	dBm pk	I_{OL} = 8 mA	
		4.0		100	µW pk		
Propagation Delay LOW to HIGH	t_{PLHR}		65		ns	T_A = 25°C, P_R = -21 dBm, Data Rate = 5 MBd	Note 6
Propagation Delay HIGH to LOW	t_{PHLR}		49		ns		

Notes:

1. 2.0 mm from where leads enter case.
2. 8 mA load (5 x 1.6 mA), R_L = 560 Ω.
3. Typical data at T_A = 25°C, V_{CC} = 5.0 Vdc.
4. D is the effective diameter of the detector image on the plane of the fiber face. The numerical value is the product of the actual detector diameter and the lens magnification.
5. Measured at the end of 100/140 µm fiber optic cable with large area detector.
6. Propagation delay through the system is the result of several sequentially-occurring phenomena. Consequently it is a combination of data-rate-limiting effects and of transmission-time effects. Because of this, the data-rate limit of the system must be described in terms of time differentials between delays imposed on falling and rising edges.
7. As the cable length is increased, the propagation delays increase at 5 ns per meter of length. Data rate, as limited by pulse width distortion, is not affected by increasing cable length if the optical power level at the receiver is maintained.

CAUTION: The small junction sizes inherent to the design of these components increase the components' susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of these components to prevent damage and/or degradation which may be induced by ESD.

HFBR-24X6 Low-Cost 125 MHz Receiver Description

The HFBR-24X6 fiber optic receiver is designed to operate with the Hewlett-Packard HFBR-14XX fiber optic transmitters and 50/125 µm, 62.5/125 µm, 100/140 µm and 200 µm HCS® fiber optic cable. Consistent coupling into the receiver is assured by the lensed optical system (Figure 1). Response does not vary with fiber size for core diameters of 100 µm or less.

The receiver output is an analog signal which allows follow-on circuitry to be optimized for a variety of distance/data rate requirements. Low-cost external components can be used to convert the analog output to logic compatible signal levels for various data formats and data rates up to 175 MBd. This distance/data rate tradeoff results in increased optical power budget at lower data rates which can be used for additional distance or splices.

The HFBR-24X6 receiver contains a PIN photodiode and low noise transimpedance pre-amplifier integrated circuit. The HFBR-24X6 receives an optical signal and converts it to an analog voltage. The output is a buffered emitter-follower. Because the signal amplitude from the HFBR-24X6 receiver is much larger than from a simple PIN photodiode, it is less susceptible to EMI, especially at high signaling rates. For very noisy environments, the conductive or metal port option is recommended. A receiver dynamic range of 23 dB over temperature is achievable (assuming 10^{-9} BER).

The frequency response is typically dc to 125 MHz. Although the HFBR-24X6 is an analog receiver, it is compatible with digital systems. Please refer to Application Bulletin 78 for simple and inexpensive circuits that operate at 155 MBd or higher.

The recommended ac coupled receiver circuit is shown in Figure 12. It is essential that a 10 ohm resistor be connected between pin 6 and the power supply, and a 0.1 µF ceramic bypass capacitor be connected between the power supply and ground. In addition, pin 6 should be filtered to protect the receiver from noisy host systems. Refer to AN 1038, 1065, or AB 78 for details.

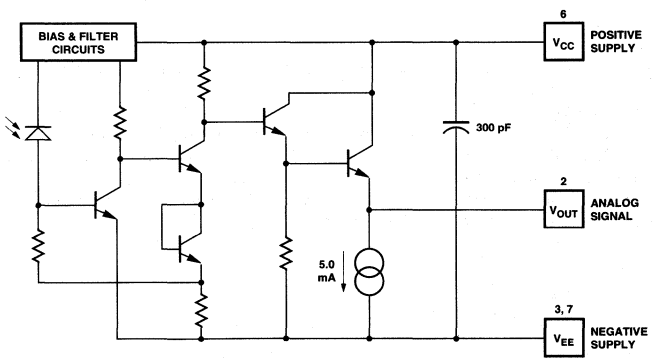
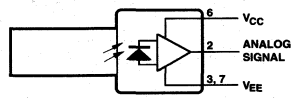
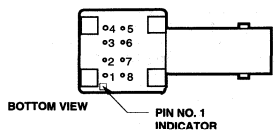


Figure 11. Simplified Schematic Diagram.

Housed Product





PIN	FUNCTION
1†	N.C.
2	SIGNAL
3*	V_{EE}
4†	N.C.
5†	N.C.
6	V_{CC}
7*	V_{EE}
8†	N.C.

* PINS 3 AND 7 ARE ELECTRICALLY CONNECTED TO THE HEADER.

† PINS 1, 4, 5, AND 8 ARE ISOLATED FROM THE INTERNAL CIRCUITRY, BUT ARE ELECTRICALLY CONNECTED TO EACH OTHER.

Unhoused Product

PIN	FUNCTION
1	SIGNAL
2*	V_{EE}
3	V_{CC}
4*	V_{EE}

CAUTION: The small junction sizes inherent to the design of these components increase the components' susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of these components to prevent damage and/or degradation which may be induced by ESD.

Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Units	Reference
Storage Temperature		T_S	-55	+85	°C	
Operating Temperature		T_A	-40	+85	°C	
Lead Soldering Cycle	Temp.			+260	°C	Note 1
	Time			10	s	
Supply Voltage		V_{CC}	-0.5	6.0	V	
Output Current		I_O		25	mA	
Signal Pin Voltage		V_{SIG}	-0.5	V_{CC}	V	

Electrical/Optical Characteristics -40°C to +85°C; 4.75 V ≤ Supply Voltage ≤ 5.25 V, R_{LOAD} = 511 Ω, Fiber sizes with core diameter ≤ 100 µm, and N.A. ≤ -0.35 unless otherwise specified

Parameter	Symbol	Min.	Typ.[2]	Max.	Units	Conditions	Reference
Responsivity	R_P	5.3	7	9.6	mV/µW	T_A= 25°C @ 820 nm, 50 MHz	Note 3, 4 Figure 16
		4.5		11.5	mV/µW	@ 820 nm, 50 MHz	
RMS Output Noise Voltage	V_{NO}		0.40	0.59	mV	Bandwidth Filtered @ 75 MHz P_R = 0 µW	Note 5
				0.70	mV	Unfiltered Bandwidth P_R = 0 µW	Figure 13
Equivalent Input Optical Noise Power (RMS)	P_N		-43.0	-41.4	dBm	Bandwidth Filtered @ 75 MHz	
			0.050	0.065	µW		
Optical Input Power (Overdrive)	P_R			-7.6	dBm pk	T_A = 25°C	Figure 14 Note 6
				175	µW pk		
				-8.2	dBm pk		
				150	µW pk		
Output Impedance	Z_o		30		Ω	Test Frequency = 50 MHz	
dc Output Voltage	$V_{o\ dc}$	-4.2	-3.1	-2.4	V	P_R = 0 µW	
Power Supply Current	I_{EE}		9	15	mA	R_{LOAD} = 510 Ω	
Equivalent N.A.	NA		0.35				
Equivalent Diameter	D		324		µm		Note 7

CAUTION: The small junction sizes inherent to the design of these components increase the components' susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of these components to prevent damage and/or degradation which may be induced by ESD.

Dynamic Characteristics -40°C to +85°C; 4.75 V ≤ Supply Voltage ≤ 5.25 V; R_{LOAD} = 511 Ω, C_{LOAD} = 5 pF unless otherwise specified

Parameter	Symbol	Min.	Typ.[2]	Max.	Units	Conditions	Reference
Rise/Fall Time 10% to 90%	t_r, t_f		3.3	6.3	ns	P_R = 100 µW peak	Figure 15
Pulse Width Distortion	PWD		0.4	2.5	ns	P_R = 150 µW peak	Note 8, Figure 14
Overshoot			2		%	P_R = 5 µW peak, t_r = 1.5 ns	Note 9
Bandwidth (Electrical)	BW		125		MHz	-3 dB Electrical	
Bandwidth - Rise Time Product			0.41		Hz • s		Note 10

Notes:

1. 2.0 mm from where leads enter case.
2. Typical specifications are for operation at T_A = 25°C and V_{CC} = +5 V dc.
3. For 200 µm HCS fibers, typical responsivity will be 6 mV/µW. Other parameters will change as well.
4. Pin #2 should be ac coupled to a load ≥ 510 ohm. Load capacitance must be less than 5 pF.
5. Measured with a 3 pole Bessel filter with a 75 MHz, -3 dB bandwidth. Recommended receiver filters for various bandwidths are provided in Application Bulletin 78.
6. Overdrive is defined at PWD = 2.5 ns.
7. D is the effective diameter of the detector image on the plane of the fiber face. The numerical value is the product of the actual detector diameter and the lens magnification.
8. Measured with a 10 ns pulse width, 50% duty cycle, at the 50% amplitude point of the waveform.
9. Percent overshoot is defined as:

$$\left(\frac{V_{PK} - V_{100\%}}{V_{100\%}}\right) \times 100\%$$

10. The conversion factor for the rise time to bandwidth is 0.41 since the HFBR-24X6 has a second order bandwidth limiting characteristic.

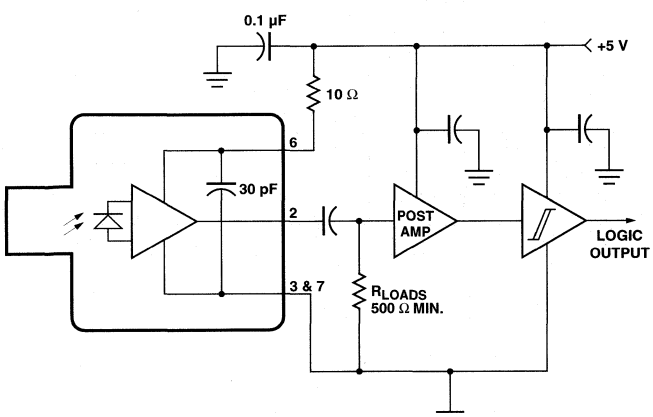


Figure 12. Recommended ac Coupled Receiver Circuit. (See AB 78 and AN 1038 for more information.)

CAUTION: The small junction sizes inherent to the design of these components increase the components' susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of these components to prevent damage and/or degradation which may be induced by ESD.

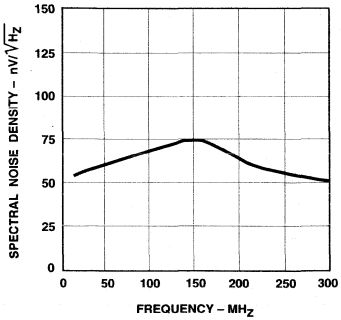


Figure 13. Typical Spectral Noise Distortion vs. Peak Input Power.

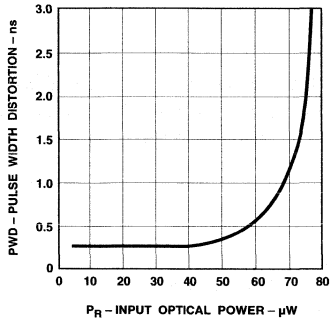


Figure 14. Typical Pulse Width Density vs. Frequency.

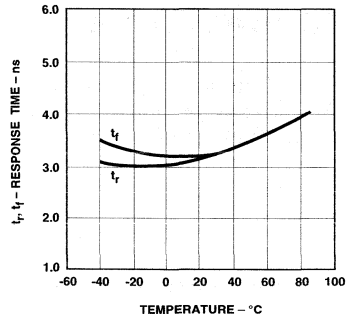


Figure 15. Typical Rise and Fall Times vs. Temperature.

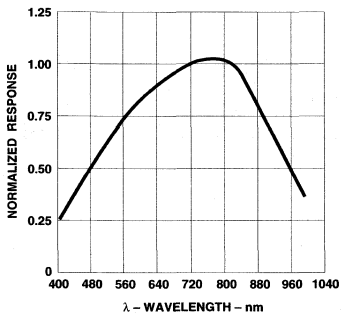


Figure 16. Receiver Spectral Response Normalized to 820 nm.

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Applications

The following application information is either published in this catalog or available from your local Hewlett-Packard sales office, authorized distributor or representative.

Application Notes

AB 78 – Low-Cost Fiber-Optic Links for Digital Applications up to 155 MBd 3-111

AN1035 – Versatile Link 3-135

AN 1038 – Complete Fiber-Optic Solutions for IEEE 802.3 FOIRL, 10Base-FB and 10 Base-FL 3-152

AN 1066 – Fiber-Optic Solutions for 125 MBd Data Communication Applications at Copper Wire Prices 3-168

AN1080 – DC to 10 MBd Versatile Link with Plastic Optical Fiber or Hard Clad Silica Fiber (HCS) for Factory Automation and Industrial Control Applications 3-184

Abstracts*

AN 1057 – Conductive Port Receiver 3-200

AN 1073 – HFBR-0319 Test Fixture for 1 x 9 Fiber-Optic Transceivers 3-200

*Complete Application Note is available from your HP sales office.

HEWLETT® PACKARD

Low Cost Fiber-Optic Links for Digital Applications up to 155 MBd

Application Bulletin 78

The HFBR-2406/16 High Performance Component

The HFBR-2406 and HFBR-2416 are high-speed, low-cost, linear, light-to-voltage converters with typical bandwidths of 125 MHz. These components can be used to make fiber-optic links for both analog and digital applications. Since the range of possible uses is so varied, this Application Bulletin concentrates on a specific digital application. The application is one of the most prevalent for the HFBR-24X6: the transmission of encoded digital signals, otherwise known as run-length limited* data.

The HFBR-0400 component family's inexpensive, one-piece plastic package allows engineers to construct low-cost high-performance fiber-optic links. All devices in the HFBR-0400 product family, including the HFBR-24X6, are available with optical ports that are compatible with the industry standard SMA and ST** fiber-optic connectors. Components that are compatible with the SMA connector are denoted by a "zero" in the third digit of their part numbers. If the ST connector is to be used, the component part number should contain a "one" in the third digit. For example, the equivalent of the high-performance HFBR-2406 SMA-compatible receiver with the ST connector option is the HFBR-2416.

The addition of the HFBR-24X6 receiver to the low-cost 0400 component family opens new avenues for designers. They can now develop fiber-optic links that meet tough cost and performance objectives. The wide bandwidth of the HFBR-24X6 allows high-speed, fiber-optic links to be built at lower prices than was formerly possible. Engineers can exploit the high performance of the HFBR-24X6 in other ways as well. For instance, the wide bandwidth of the linear light-to-voltage converter can be reduced by a low-pass filter to improve the sensitivity of the fiber-optic receiver in lower-speed applications. The HFBR-24X6 accommodates a larger optical signal than other HFBR-0400 fiber-optic receivers before it begins to overload. This improvement in the overload characteristics of the 24X6 was achieved with no significant reduction in the ultimate sensitivity when compared to the existing HFBR-24X4 receiver. The increased optical input power tolerated by the HFBR-24X6 allows it to function at short fiber lengths with large values of launched optical power. When the receiver can tolerate higher optical power, a longer cable is possible before attenuation reduces the light to the sensitivity limit of the receiver. The increased dynamic range of the HFBR-24X6 will thus permit greater optical link length for any given fiber attenuation.

Applications For 820 nm LED Based Fiber Optic Links

The 820-nm LED technology used in the HFBR-0400 family of components can be used in conjunction with the HFBR-24X6 receiver to construct digital fiber-optic links that transmit data at speeds up to 155 MBd. The length of the fiber cable that can be used with the HFBR-24X6 is restricted by the receiver sensitivity at low data rates. As the data rate is increased a phenomenon known as chromatic dispersion begins to limit the maximum distance. Chromatic dispersion results

* Run length limited means a limit on the number of consecutive symbols in the same state.

** ST is a trademark of AT&T Technologies.

from the interaction of the 60 nm-wide spectrum emitted by the LED and the propagation velocities of light in silica. Since the velocities of light at various wavelengths near 820 nm are different, the optical pulses sent by the LED are dispersed or spread out in time as they travel down the light guide. A chromatic dispersion null exists at a wavelength of 1300 nm in silica glass. If an LED were operated at the chromatic dispersion null the pulses would experience the minimum broadening as they traveled through the fiber. This is due to the nearly equal propagation velocity for all the wavelengths transmitted through the silica light guide by the long-wavelength emitter. Figure 1 illustrates the effect of the LED center wavelength and spectral width on the chromatic dispersion. An 820 nm LED with a 60 nm emission spectrum is shown to produce a larger change in the arrival time of the light pulses than a 1300 nm LED with a 100 nm spectral width. When selecting a fiber the designer should be aware of how the bandwidth-length product, expressed in MHz/km, was determined. The bandwidth of a fiber measured using a narrow spectrum emitter, such as a laser diode, is related to the various possible modes of light propagation that can exist in a fiber. This is referred to as the fiber's modal bandwidth. The modal bandwidth will be greater than the chromatic bandwidth which dominates when an LED is used. To determine the overall optical bandwidth of a fiber, the modal and chromatic bandwidths must be combined as an rms sum as shown in Equation 1. In LED-based systems the wavelength, spectral width and response time of the emitter used as the fiber-optic transmitter will affect the final system bandwidth. Thus, to understand how a fiber will work with an LED, one must know the type of optical source used to measure the manufacturer's stated bandwidth. HP HFBR-AWSyyy 100/140 µm fiber-optic cable has a typical optical bandwidth-length product of 40 MHz/km. This value represents the performance of the HP fiber with an 820 nm LED emitter that has a 60 nm spectral width. The 40 MHz/km typical bandwidth-length product of HP fiber results from the combination of the modal and chromatic bandwidths.

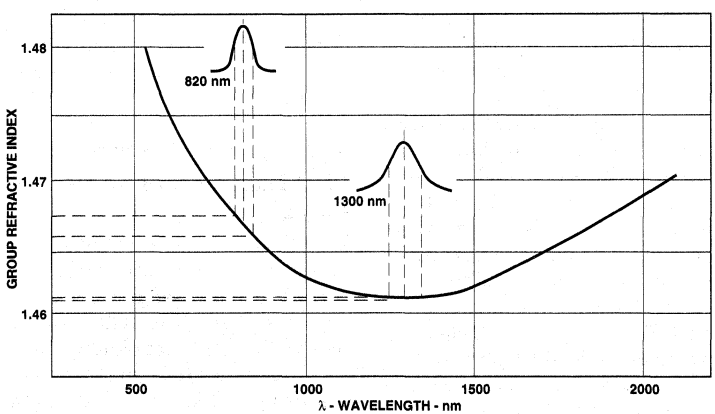


Figure 1. Group Delay vs. Wavelength.

$$B.W. = \left[\frac{1}{\left(\frac{1}{B.W.\ modal}\right)^2 + \left(\frac{1}{B.W.\ chromatic}\right)^2} \right]^{1/2}$$

Equation 1.

The typical distances and data rates possible with 820 nm LED emitters and the HFBR-2406/2416 receiver are shown in Figure 2. Note that the data rate versus distance for 100/140 and 62.5/125 µm graded-index fibers are both shown in the figure.[1, 2, 3, 4]

If greater distances or higher speeds are required, other options such as 1300 nm LEDs or laser diodes can meet these objectives. If the system requirements fall to the left of the curves shown in Figure 2 the design goals can be achieved using an 820 nm LED and the HFBR-24X6 for a substantially lower cost than possible with these other technologies. The inexpensive 820 nm LED technology offers the designer a cost-effective solution sufficient for many short-distance applications at data rates in excess of 100 megabaud.

Applications for 820 nm LED Based Systems Using HFBR-2406/2416 Include:

- CPU to disc interface.
- CPU to monitor interface
- CPU to peripheral interface
- Optical data bus applications.

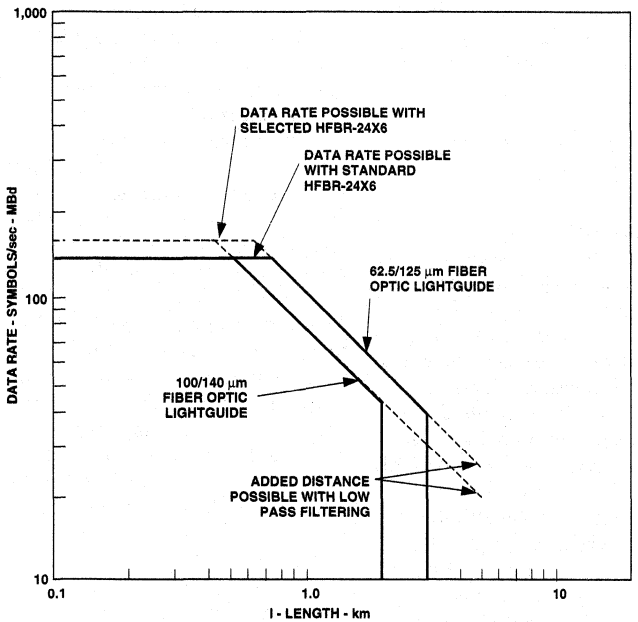


Figure 2. Typical Data Rate and Distance Possible with HFBR-2406/2416.

- Graphics workstation to host computer interface.
- Wide dynamic range, long distance, medium speed LAN applications.
- High-speed, point-to-point data links.
- Security, voltage isolation.

Advantages of Run Limited Code

Data is coded to prevent the digital information from remaining in one of the two possible logic states for an indefinite period of time. The coded data allows the fiber-optic receiver to be ac coupled. Without encoding, the fiber-optic receiver would have to detect dc levels to determine the proper logic state during long periods of inactivity, as when there is no change in the transmitted data. AC-coupled fiber-optic receivers tend to be lower in cost, are much easier to design, and contain fewer components than their dc-coupled counterparts.

Direct coupling decreases the sensitivity of a fiber-optic receiver since it allows the low-frequency flicker noise from the transistor amplifiers to be presented to the comparator input. Any undesired signals coupled to the comparator will reduce the signal-to-noise ratio at this critical point in the circuit, and reduce sensitivity of the fiber-optic receiver.

Another problem associated with direct-coupled receivers is minimizing the accumulation of dc offset. With direct coupling, the gain stages multiply the effects of undesirable amplifier offsets and voltage drifts due to temperature changes, and apply them to the comparator. Increases in the dc offset applied to the comparator result in reduced sensitivity of the fiber-optic receiver. The dc offset at the comparator can be referred to the optical input of the receiver by dividing by the receiver gain. This division refers the dc offset at the comparator to the receiver input where it appears as a change in optical power that must be exceeded before the receiver will switch states.

Another advantage of run-limited coding is related to timing recovery. If NRZ data were transmitted over a serial fiber-optic link the data could be in the logic "1" or logic "0" state for an indefinite period of time. When NRZ data remains in a particular state no transitions occur and the fundamental frequency of the data is dc. This lack of power at the fundamental frequency of the data eliminates the reference signal needed by the timing recovery circuits required to clock the received information. If an optical link is to transmit NRZ data, a clock signal must be sent on a separate fiber-optic link to synchronously detect the incoming serial data.

The particular run-length-limited code chosen must be considered carefully since it will affect the bandwidth required by the serial communication channel. A complete discussion of all run-limited codes is beyond the scope of this publication. If you desire additional information regarding various coding schemes, there are numerous technical papers devoted to this specific topic.[5] Without becoming too involved in the complexity of encoding selection, a quick comparison will now be made between two commonly recognized approaches to this problem.

One of the most familiar run-limited codes is Manchester. Manchester is very popular since it can be encoded and decoded

with relatively simple circuits. Manchester works well in ac-coupled systems since it has a 50% duty factor and two pulses or symbols for each bit transmitted. This simplifies the design and implementation of the timing recovery function since Manchester code has only two consecutive symbols without a transition, or a run limit of two. A drawback of Manchester is that two symbols must be sent for each data bit encoded, thus doubling the fundamental frequency that must pass through the information channel. Substitution codes have recently been made available in very large scale integrated (VLSI) circuits. These VLSI circuits function as a general purpose interface between the parallel architecture found in computer-based systems and the serial format required by fiber-optic communication links. The two different substitution codes available in the AMD TAXIchip™ parallel-to-serial encoder are 4B5B and 5B6B. These two codes have an efficiency of 4/5 and 5/6 respectively which compares to an efficiency of 1/2 for Manchester code. The significance of coding efficiency can be illustrated by an example. If an application calls for the transmission of 100 M bits/second, Manchester code requires that the information channel must pass 200 M symbols/second or 200 MBd. If the more efficient 4B5B code were used, 100 M bits/second could be sent at a speed of (5/4)(100 M bit/sec) = 125 MBd. Similarly, use of 5B6B would allow transmission of this data at a speed of (6/5)(100 M bit/sec) = 120 MBd.

Regardless of the particular coding scheme used there will always be two symbols per cycle. This is true because each half cycle of the maximum fundamental frequency that the communications channel must pass is equivalent to a symbol in a binary transmission system.

Designing With Fiber Optic Components

Transmitter Design

Now that the basic issues related to fiber-optic link design have been covered, some specifics related to the design of the optical transmitters and receivers will be discussed in greater detail. To achieve the wide bandwidth performance potential of the fiber-optic medium requires a fast LED and current modulator. The transmitter's pulse-width distortion and optical rise and fall times can be heavily influenced by the driver selected. Readily available off-the-shelf integrated circuit current drivers can be configured with the HFBR-14XX 820 nm LEDs to build high-performance fiber-optic transmitters with a typical pulse-width distortion of 800 psec.

To obtain the best performance from any LED and driver combination, two simple techniques known as prebias and drive current peaking should be employed. Prebias, as its name implies, is a small forward current applied to the LED in the "off" or "low" light state. The prebias current prevents the junction and parasitic capacitances from discharging completely when the LED is in the "off" state, thus reducing the amount of charge that the driver must transfer to turn the emitter back on. Peaking is a momentary increase in LED forward current that is provided by the driver during the rising and falling edges of the current pulses that are used to modulate the emitter. If the time constant of the peaking circuit is approximately equal to the minority carrier lifetime of the emitter, the momentary increase in LED current will transfer charge at a rate that improves the rise or fall time of the light output without causing excessive overshoot of the optical pulses. Problems that can result when excessive peaking is applied to the LED are illustrated in Figure 3. The narrow optical overshoot due to excessive peaking of the transmitter causes a narrow electrical output pulse from the fiber-optic receiver that must now be damped. Even if the receiver amplifiers were critically damped the electrical undershoot resulting from excessive peaking of the emitter can reduce the sensitivity of the fiber-optic link. This electrical undershoot can combine with noise from the amplifiers so that the sum of these two voltages exceeds the decision threshold of the comparator, which converts the low-level analog output of the fiber-optic receiver back to logic-compatible digital signals. Excessive peaking during the turn-off of the emitter can cause additional problems. Too much reverse current during the turn-off transition will reverse-bias the LED, seriously degrading the turn-on time.

A circuit with a low source impedance should be used to drive the LED. This is important because the light output of an LED is proportional to the number of electron hole pairs present in the LED's junction. If high speed operation of the transmitter is desired, a driver with a low source impedance should be used to provide the sudden changes in current required to quickly create and annihilate charge carriers in

the LED junction. LEDs are characteristically harder to turn off than to turn on. This difficulty manifests itself as a phenomenon commonly referred to as the long-tailed response. An example of long-tailed response is shown in Figure 4. The long-tailed response is most evident when a simple series switch is used to control the LED drive current as shown in Figure 5. A shunt drive configuration, which turns the LED off when the driver transistor saturates, significantly improves the performance of the LED transmitter. Shunt drive reduces pulse-width distortion and the magnitude of the slow tail by providing a low impedance path for charge stored in the LED junction. Without this low-impedance path the emitter would turn off slowly since the LED would continue to produce light until the diode junction discharges.

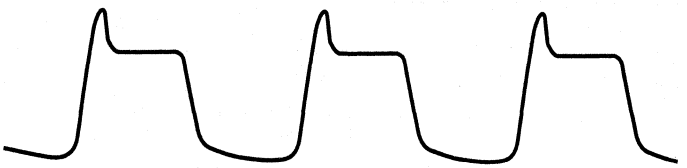


Figure 3a. Optical Overshoot Due to Excessive Peaking of the LED Drive Current.

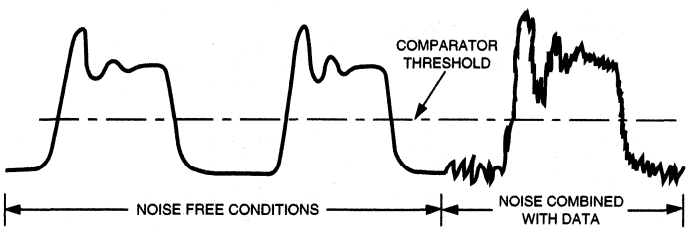


Figure 3b. Response of Optical Receiver to an Excessively Peaked LED Transmitter.

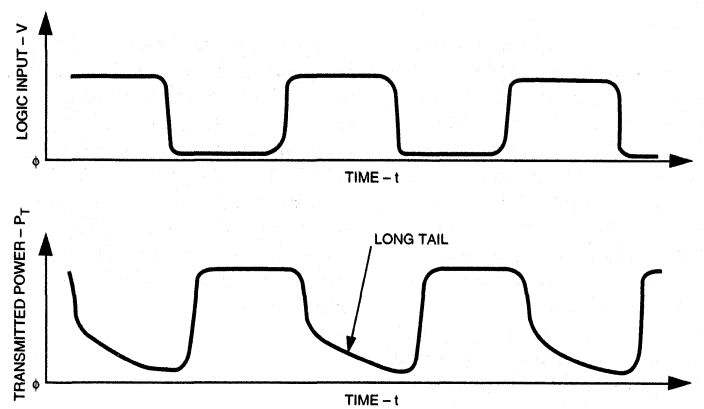


Figure 4. Example of Long-Tailed Response.

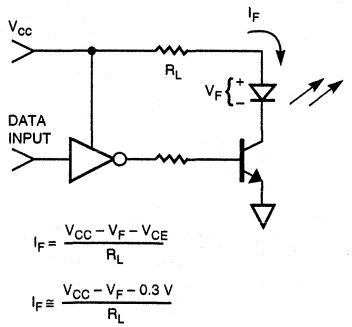


Figure 5. Series Switch LED Driver.

Readily available 74ACT logic gates can be used to implement a shunt drive configuration to current-modulate the LED. A current of 60 mA is typically required to drive the HFBR-14X2/4. Ordinary bipolar TTL gates generally do not have sufficient capability to sink and source 60 mA. A simple high-speed LED driver can be constructed by connecting the active output of 74ACT logic to the HFBR-14X2/4 as shown in Figure 6. In this configuration the pull-up transistor turns the LED off, and the pull-down transistor turns the LED on. The low impedance and high current rating of the MOSFET transistors used in 74ACT output stages allows these gates to quickly inject and remove charge from the LED. The ability of 74ACT gates to quickly move charge is very important as the LED turns off. The dynamic impedance of the LED increases rapidly as forward current decreases at turn off. The LED will continue to emit light as long as the junction contains minority charge carriers. The pull-up transistor of the 74ACT LED driver provides the low impedance discharge path needed to sweep charge from the junction and rapidly quench the light emitted by the LED. The low impedance of the pull-down

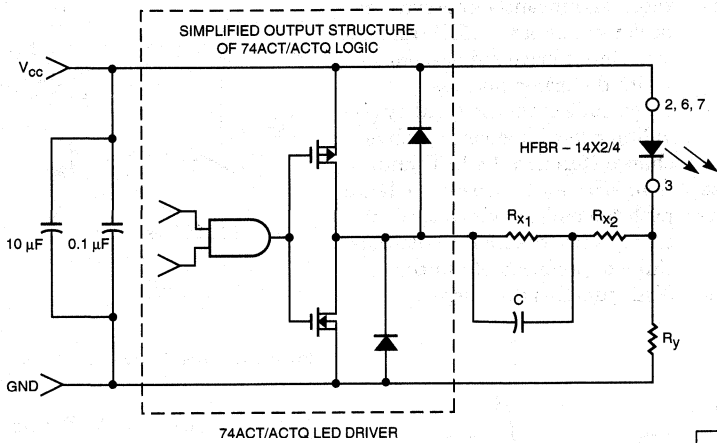


Figure 6. Simple High-Speed Transmitter Circuit.

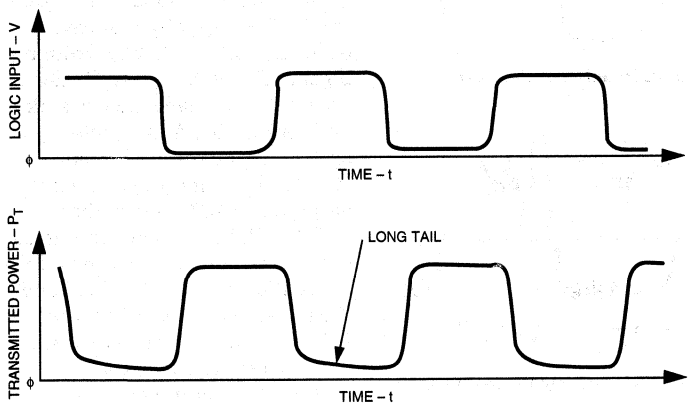


Figure 7. Improved Optical Output Waveform.

Equation 2.

N = The number of 74ACT gates connected in parallel.

B = Is an empirically determined constant which establishes an optimum relationship between prebias and LED forward current.

$$R_y = \frac{(V_{cc} - V_F)(1 + B)}{I_{F\ ON}}$$

$$R_{x_1} = \left(\frac{R_y}{2B}\right)$$

$$R_{x_2} = \left(\frac{R_y}{2B}\right) - \left(\frac{3}{N}\right)$$

$$C = \frac{2.5\ ns}{R_{x_1}}$$

transistor ensures that the LED turns on quickly by providing the current needed to rapidly charge the junction during the less difficult turn-on transition. When the 74ACT gate and LED are configured as shown by the schematic in Figure 6, the improvement in the optical output waveform is as shown in Figure 7. The high speed capability of 74ACT logic minimizes the difference between high-to-low and low-to-high propagation delays. The variance between t_{PHL} and t_{PLH} of the gate used to drive the LED will affect the pulse-width distortion present in the transmitter's optical waveform. When nand inverters from the same die are connected as shown in Figure 8 the distortion due to gate propagation delay differences is minimized. The transmitter circuit shown in Figure 8 typically has an optical jitter of 800 ps; this excellent transmitter performance can be achieved when an undistorted TTL signal is applied to the 74ACTQ00 quad nand gate used to current modulate the HFBR-14X2/4 LED.

The transmitter shown in Figure 8 is compatible with TTL logic and is suited for data with a maximum fundamental frequency of 78 MHz, which implies a symbol rate of 155 MBd. The design rules for the LED driver shown in Figure 8 are shown in Equation 2. This simple TTL-compatible fiber-optic transmitter has a typical rise/fall time of 3 ns.

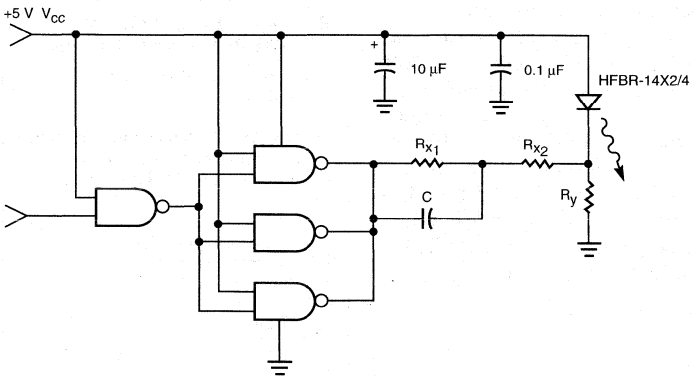


Figure 8. TTL Compatible LED Driver Implemented with 74ACT or 74ACTQ nand Logic.

Testing Fiber Optic Systems

Pseudo-random-bit-sequence (PRBS) generators are very useful for testing the performance of fiber-optic systems. The pseudo-random data pattern contains long periods of inactivity related to the length of the shift register used to build the PRBS generator. A PRBS generator made up of a 23-bit-long shift register could at any given clock time contain one of 8,388,610 possible data patterns. The number of data patterns possible can be calculated as 2^{23}-1 since the state where all shift register stages contain logic zeros is not allowed. These long periods of inactivity in the data pattern produced by the PRBS generator allow time for parasitic capacitances in the transmitter and receiver to charge. The time required to charge and discharge undesired capacitances in the transmitter and receiver result in pulse-width distortion related to the instantaneous duty factor of the data. This phenomenon is known as data dependent jitter or DDJ. If an oscilloscope is clock triggered on the PRBS generator it asynchronously samples the data due to the lack of correlation between the PRBS clock and the time base that generates the horizontal sweep of the scope. When triggered on the PRBS generator's clock the scope will display a signal known as the "eye pattern". The "eye pattern" can be very useful since the width and height of the opening between the data edges defines the time period during which the data is in a valid logic state.

TTL Transmitter Performance

The performance of the circuit shown in Figure 8 was tested using a 2^{23}-1 PRBS data pattern to demonstrate the typical performance of this TTL transmitter. Jitter in the data edges results due to the DDJ induced by the pseudo random bit sequence. The eye pattern shown in Figure 9 reveals that the HFBR-14X2/14X4 LED transmitter had a total data-dependent edge jitter of 800 ps when driven by the 74ACTQ00 gate at a rate of 155 MBd. This data was taken at an ambient temperature of 25°C and represents the typical performance possible with this simple fiber-optic transmitter. The total pulse-width distortion can be further reduced by using a limited-range potentiometer in place of fixed values of R_y for system applications that are extremely intolerant of symbol-width variations. But for most data communications applications, this transmitter performs adequately at speeds up to 155 MBd using fixed component values.

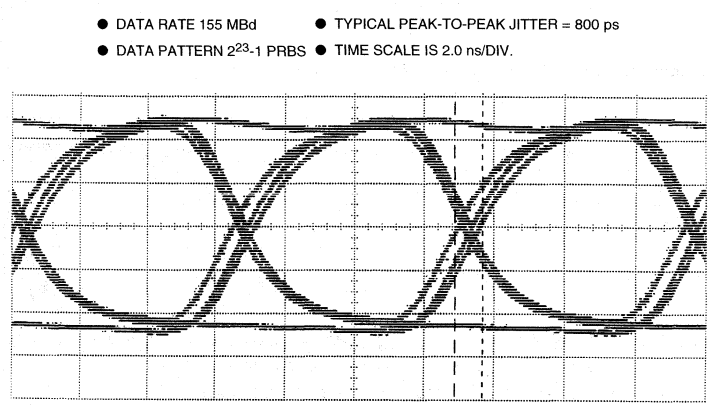


Figure 9. Optical Output of the TTL Transmitter.

ECL Transmitter Performance

If an ECL-compatible fiber-optic transmitter is needed it can be easily built using the circuit shown in Figure 10. The design rules for this high-performance fiber-optic transmitter are given in Equation 3. This particular transmitter uses a simple ECL to TTL converter and 74ACTQ nand logic in conjunction with the HFBR-14X2/X4 LED emitter. It is capable of typical optical rise/fall times of 3 nsec. The performance of the ECL transmitter was measured with a BCP Model 300 Optical Waveform Receiver. Figure 11 shows the optical "eye" pattern when a 155 MBd pseudo-random-bit-sequence of 2^{23}-1 is applied to the ECL transmitter.

Equation 3. Design Rules for 74ACTQ00 LED Driver Circuits.

N = Number of gates connected in parallel.

B = Empirically determined constant for optimum relationship between prebias and LED forward current.

$$R10 = \frac{(V_{CC} - V_F)(1 + B)}{I_{F\,ON}}$$

$$R8 = \frac{R10}{2B}$$

$$R9 = \frac{R10}{2B} - \frac{3}{N}$$

$$C4 = \frac{2.5 \times 10^{-9}}{R8}$$

Recommend B = 3.97

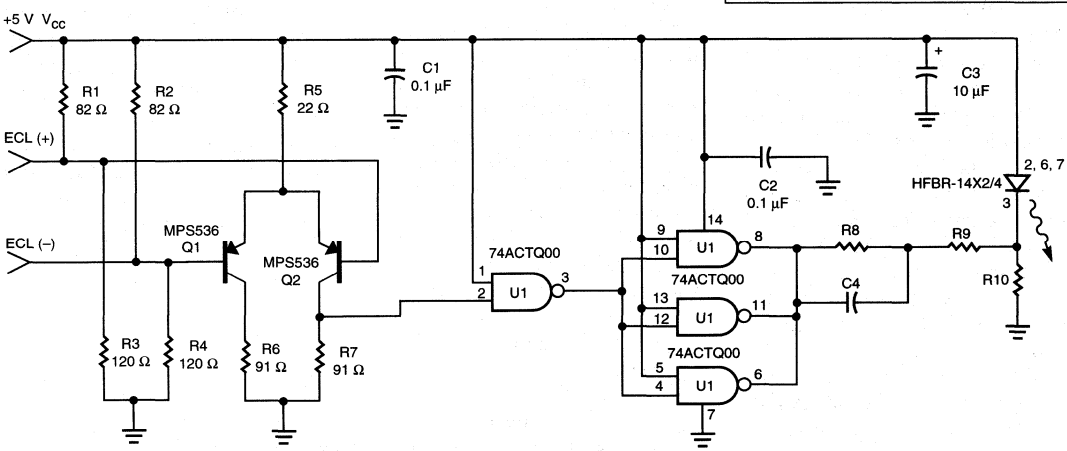


Figure 10. Transmitter with +5 V ECL Interface.

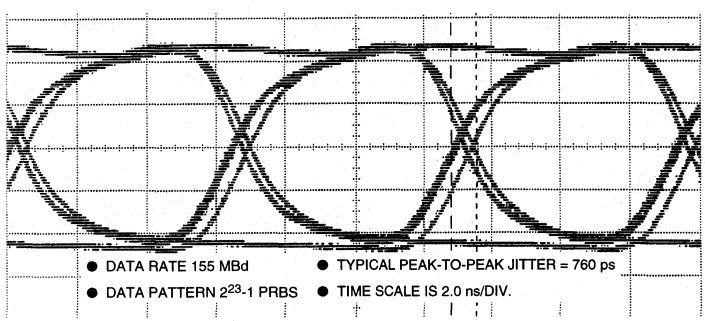


Figure 11. Optical Output of the +5 V ECL Transmitter.

Receiver Design

Now that the techniques required to build high-speed fiber-optic transmitters have been explained, emphasis must be placed on the methods necessary for design and construction of the fiber-optic receiver. Figure 12 shows the functional blocks required to interface the HFBR-24X6 light-to-voltage converter to digital logic. The HFBR-24X6 has a low-level analog output related to the incoming optical power by the 7 mV/μW conversion gain of the light-to-voltage transducer. The HFBR-24X6 needs additional external gain stages to increase the amplitude of its output before it can interface to any of the standard logics like TTL or ECL. The output voltage of the HFBR-24X6 is proportional to the received optical flux. Since the received optical power changes as a function of the fixed optical losses and as a function of fiber-optic link length, some provision must be made to accommodate the change in the output voltage of the light-to-voltage transducer. An amplifier with AGC or a limiting amplifier is needed to accommodate the wide range of output voltages that are possible under various fiber link operating conditions. In the following example, calculations show that the output voltage of the HFBR-24X6 could range from a minimum of 2.9 mV pp to a maximum of 1.74 V pp. This output voltage range is for worst-case conditions at a BER less than or equal to 1 x 10^{-9} when the component operates between -40 to +85°C.

Calculation of HFBR-24X6 Output Voltage Range

The peak-to-peak signal to rms noise ratio needed at the comparator input for a BER of 1 x 10^{-9} = 12:1.

This implies an extinction-to-peak (peak-to-peak) change in the received optical flux of (12) (rms noise) will be required. Thus, the peak-to-peak-to-rms-noise ratio required by the fiber-optic receiver for a BER of 1 x 10^{-9} becomes ($Signal_{pp}$) / ($noise_{rms}$) = 12:1.

The noise floor of the HFBR-24X6 is -43 dBm rms typical.

-43.0 dBm + [10 log (12/1)] = -43.0 dBm + 10.8 dB = -32.2 dBm pk. Thus -32.2 dBm pk is the minimum received optical power that will yield a BER better than or equal to 1 x 10^{-9}.

-32.2 dBm implies [antilog (-32.2/10)](1,000) = 0.603 μW minimum received optical power for BER better than or equal to 1 x 10^{-9}.

This minimum power of 0.603 μW implies a change in the receiver input from approximately 0 μW to 0.603 μW or a peak-to-peak change of approximately 0.603 μW pp. The minimum output of the HFBR-24X6 thus becomes (0.603 μW pp)(4.5 mV/μW) = 2.71 mV pp.

The HFBR-24X6 overloads at -8.2 dBm worst-case minimum. Overload is specified as P_r maximum on the data sheet. Overload is defined as the received optical power at which the output pulses from the HFBR-24X6 are distorted 2.5 ns due to saturation of the transimpedance amplifier that converts photo-current to voltage.

-8.2 dBm implies [antilog (-8.2/10)](1,000) = 151 μW. Thus the maximum allowed power of 151 μW implies a change in the receiver input from approximately 0 μW to 151 μW or a peak-to-peak change of approximately 151 μW pp. Thus a maximum received optical power of 151 μW implies a maximum output voltage of (151 μW pp) (11.5 mV/μW) = 1.74 V pp.

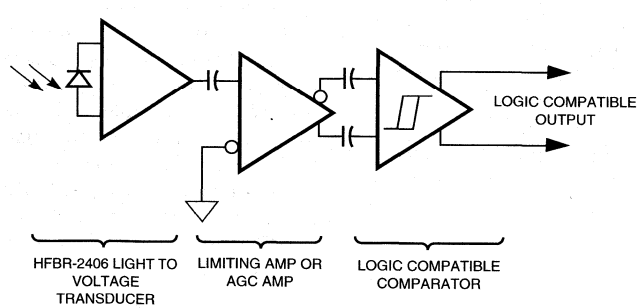


Figure 12. Fiber-Optic Receiver Block Diagram.

Error Rate Versus Signal-to-noise Ratio

The bit error rate (BER) possible with a fiber-optic link is a function of the difference between the peak-to-peak signal and the RMS noise voltages present at the comparator input. A linear relationship exists between optical power entering the HFBR-24X6 and the voltage output of the fiber-optic receiver, provided that interstage coupling and post amplifiers do not introduce significant distortion. This linear relationship implies that if a peak-to-peak signal voltage 12 times larger than the RMS noise voltage is needed at the comparator to ensure a BER of 1 x 10^{-9}, then the same ratio will be required at the receiver input. Thus the difference between the peak-to-peak optical input of light pulses applied to the HFBR-24X6 and the RMS equivalent noise power referred to the optical input must also be 12 to 1. Some confusion exists because changes in the emitter output from extinction to maximum power are often referred to as peak excursions of the transmitter launched power. This confusion results since the transmitter output is varying from zero light to a maximum or peak light output. The extinction-to-on excursion in the optical output of an emitter is actually a peak-to-peak change in intensity. Figure 13 is a graph of receiver signal-to-noise ratio versus BER. The relationship shown in Figure 13 was obtained from extensive reduction of statistical theory that relates the probability of an error to the receiver's signal-to-noise ratio.

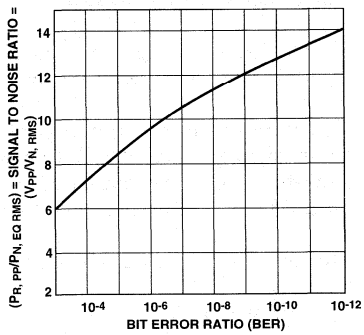


Figure 13. Signal-to-Noise Ratio vs. Probability of Error.

Advantages of Hysteresis

The use of hysteresis in the digitizer will not change the signal-to-noise ratio required at the comparator for a particular BER. Hysteresis will, however, introduce a discontinuous response in the receiver that alters the ratio between peak signal level and the RMS noise in stages prior to the comparator. When dual-threshold detection is used, the signal-to-noise ratio required at the decision circuit for a particular error rate is unaffected but the change in the received power level required to switch the state of the comparator is increased in proportion to the amount of the hysteresis. Dual-threshold receivers experience a reduction in sensitivity proportional to the amount of hysteresis used; however, this type of digitizer offers some interesting advantages. Hysteresis is used in all the receivers shown in this Application Bulletin. Use of hysteresis insures that the logic output of the fiber-optic receiver will not toggle in response to the rms output noise voltage of the HFBR-24X6 when no fiber is connected.

Low-pass Filtering to Enhance Receiver Sensitivity

The importance of filtering to eliminate unnecessary receiver bandwidth becomes apparent by studying Figure 14, which shows the relationship between frequency and the spectral noise density of the HFBR-2406/2416. If the fiber-optic link under consideration were intended for operation at 50 MBd (which implies a fundamental data frequency of 25 MHz) a substantial increase in receiver sensitivity can be realized. This increase in sensitivity is obtained by filtering out the noise peak that occurs in the HFBR-24X6 at higher frequencies than required for this application.

The selection of the low-pass filter corner frequency should be carefully considered since it is affected by the response of the transmitter, fiber, and receiver. To prevent problems that will cause interference between adjacent pulses of data transmitted over the fiber-optic communications channel, the bandwidth of the entire system from transmitter to receiver must be properly specified. A problem known as intersymbol

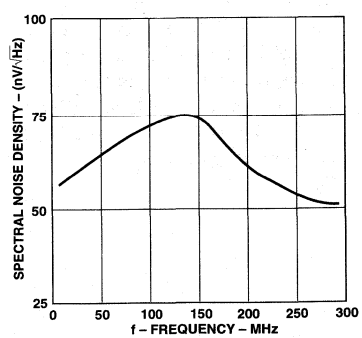
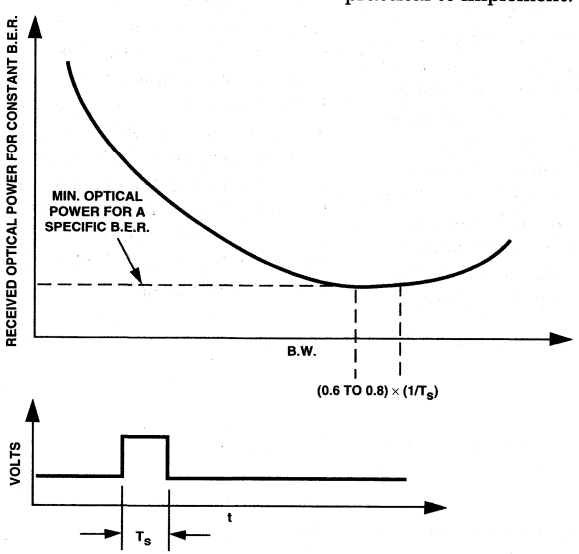


Figure 14. Frequency vs. Spectral Noise Density of the HFBR-2406/2416.

interference develops when the channel bandwidth is not correctly related to the minimum pulse width of the data that is to be transmitted over the communications system. Insufficient system bandwidth manifests itself as distortion in the receiver output signal at time intervals adjacent to the edges of each symbol. This distortion results in interference between adjacent pulses, which can combine with system noise to create errors. Noise is also directly related to bandwidth. Thus, fiber link performance and BER will degrade if system components are excessively fast. For optimum performance that minimizes the amount of optical power required at the receiver for a given BER, the system bandwidth should ideally be constrained to range between 0.6 to 0.8 times the signaling rate in baud, as shown in Figure 15a. If the bandwidth of the fiber-optic communications channel is excessive, a low-pass filter that restricts the system bandwidth to the amount shown in Figure 15a should be constructed in the fiber-optic receiver, at a point ahead of the decision circuit or comparator. For best results the low-pass filter chosen to limit the bandwidth should be a high-order, linear-phase type whenever practical. As the frequency increases, the cost and complexity of a linear-phase high-order filter may become excessive. These higher-speed applications will continue to benefit from a simple first-order or second-order RC low-pass filter that will still be practical to implement.



T_S IS THE MINIMUM PULSE WIDTH OF THE INFORMATION SENT OVER THE COMMUNICATION CHANNEL.

$B.W._{OPTIMUM}$ = [0.6 TO 0.8] (Hz/ baud) × [1/T_S] (SYMBOLS/sec)

$B.W._{OPTIMUM}$ = [0.6 TO 0.8] (Hz/ baud) × [1/T_S] (baud)

Figure 15a. Optimal Relationship Between Fiber-Optic Link Bandwidth and Maximum Receiver Sensitivity.

Compromises Associated With High Speed 820 nm Links

Systems with bandwidths less than (0.6 to 0.8) x (baud) will continue to function since catastrophic failure does not result if these recommendations are violated. Fiber-optic links with bandwidths less than (0.6 to 0.8) x (baud) will have a smaller optical power budget (OPB) than comparable optical links which operate in the flat portion of Figure 15b. This reduction in the OPB is sometimes called the chromatic dispersion power penalty. A decrease in the OPB due to chromatic dispersion is most apparent as an increase in the received power needed to assure a specific BER. The chromatic dispersion power penalty can be directly measured by testing the same transmitter and receiver with both long and short fibers. A fiber-optic link operated beyond the flat portion of Figure 15b requires more received optical power to offset the reduction in signal amplitude due to chromatic bandwidth limitations. Chromatic bandwidth limitations can be overcome if sufficient power is available at the receiver to provide the signal-to-noise ratio necessary for the BER required. The -32 dBm average sensitivity typically obtained when HFBR-24X6 is operated

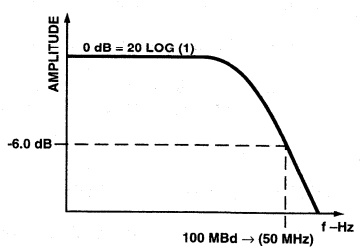


Figure 15b. Optical Link with Normalized Mid-Band Amplitude Response.

with short fibers will allow longer fiber-optic links to operate at frequencies beyond the flat portion of the system's amplitude response. Figure 15b is an example of an optical link whose mid-band amplitude response has been normalized to one. If this hypothetical link were operated at a frequency that reduced the total system output to 6 dB below mid-band amplitude, excess optical power margin (OPM) can still be shown to exist. This excess OPM, as calculated in Equation 4, is sufficient for low-error transmission of 100 MBd data over a 1 km length of 62.5/125 graded index fiber. The HFBR-24X6 receiver has typically demonstrated a BER less than or equal to 1 x 10^{-9} at received optical powers of -32 dBm average (-29 dBm peak) at 100 MBd with a short 1 m length of fiber. In this somewhat pessimistic example, the link sensitivity was assumed to decrease by 6 dB, due to chromatic dispersion of a 1 km length of 62.5/125 μm fiber. The following calculation shows that an ample 3.25 dB OPM remains to assure that the BER is better than 1 x 10^{-9} when 100 MBd data is transmitted over a 1 km length of 62.5/125 μm fiber.

High-frequency Circuit Design

The HFBR-24X6 and each of the amplifiers used in the 10H116 are stable gain blocks that have no tendency to oscillate. Although each of these components is individually stable, the combined phase shift and gain that results when they are cascaded might produce oscillation unless proper circuit construction techniques are used. The effect of all the amplifier poles that accumulate as the signal is amplified and digitized by the various gain blocks in the receiver results in a very steep high-order roll-off for the overall input-to-output open-loop receiver gain. In essence, the fiber-optic receiver relies on the fact that it is an open-loop system. It has sufficient gain and phase shift to meet the criteria for oscillation if the loop were to be closed. To assure stability the loop gain must be kept to less than unity; to prevent oscillation the attenuation of parasitic and conductive feedback paths must be greater than the gain of the receiver. Parasitic feedback from the high-level logic-compatible output must be kept to a minimum by layouts that physically separate the receiver inputs and outputs. Filtering must be used to ensure that power supply busses do not provide a metallic feedback path that will degrade the stability of the receiver, and a ground plane is recommended to minimize the inductance of supply commons.

When good layout practices are employed, fiber-optic receivers with 155 MBd data rates can be easily constructed using commonly available breadboarding techniques. A sound breadboard technique suitable for prototyping the HFBR-2406/2416 can be implemented using perforated PC boards with holes on tenth-inch centers and a copper-clad ground plane on one side only. Use a small hand-held twist drill holder (pin vise) and a number 32 drill to clear copper away from holes through which the component leads will pass. Do not clear all the copper away between these holes. This copper provides ground connections between each IC lead, thus reducing ground-loop size and increasing circuit performance. Install the components on the copper foil side using the component leads for point-to-point wiring interconnections on the insulated side of the board. Production fiber-optic systems can

Equation 4.

OPM (dB) = Optical power margin.

P_R (dBm) = Optical power required at HFBR-24X6 receiver for BER ≤ 1 x 10^{-9}.

P_T (dBm) = Transmitter launched power

CDP (dB) = The chromatic dispersion power penalty due to fiber bandwidth, response time of the transmitter, and response time of the receiver.

α_o (l) (dB) = fiber loss.

$OPM = -(P_R) + P_T - \alpha_o(l) + CDP$

OPM = - (-29 dBM) + (-16 dBm) - (3.75 dB/km) (1 km) - 6 dB

OPM = 3.25 dB

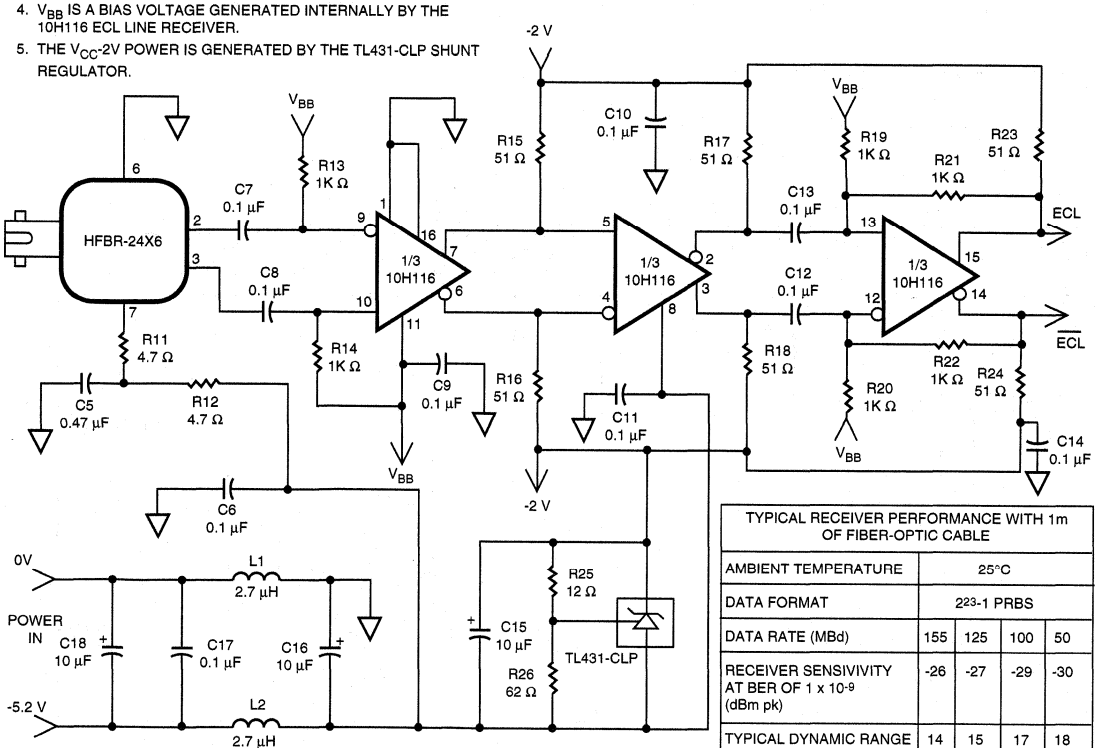
be implemented on ordinary double-sided G-10 printed circuit material or multi-layer boards as long as the layout practices discussed here are observed.

The importance of good construction and layout practices cannot be over-stressed: poor circuit design will seriously degrade system performance. Circuit designs that result in excessive amounts of parasitic inductance or capacitance will degrade the stability and bandwidth of the fiber-optic receiver. Any unintended reduction in the bandwidth or stability of the receiver will result in loss of receiver sensitivity or, in the case where received optical power is held constant, could degrade the BER. It is generally acknowledged that the receiver is the most critical portion of the fiber-optic link electronics. Despite this tendency to focus on the receiver, careful attention must be paid to the transmitter. Care should be taken to keep traces short in the transmitter to minimize inductance of conductors that must carry fast current pulses which can reach momentary peak values as large as 140 mA.

EMI Issues

If a fiber-optic transceiver is to be constructed, additional attention must be paid to minimize crosstalk between a transmitter that is switching hundreds of milliamps and a receiver whose optical detector will have photocurrents as small as hundreds of nanoamps. Individual ground

NOTES:
1. ALL RESISTORS ARE ±5% TOLERANCE.
2. ALL ELECTROLYTIC CAPACITORS ARE ±20% TOLERANCE. ALL OTHER CAPACITORS SHOULD BE RADIAL LEAD MONOLITHIC CERAMIC TYPES WITH ±10% TOLERANCE.
3. L1 AND L2 SHOULD HAVE A ±10% TOLERANCE, SERIES RESISTANCE OF ROUGHLY 0.5 Ω, AND A SELF RESONANT FREQUENCY ≥ 100 MHz.
4. V_{BB} IS A BIAS VOLTAGE GENERATED INTERNALLY BY THE 10H116 ECL LINE RECEIVER.
5. THE V_{CC}-2V POWER IS GENERATED BY THE TL431-CLP SHUNT REGULATOR.



TYPICAL RECEIVER PERFORMANCE WITH 1m OF FIBER-OPTIC CABLE				
AMBIENT TEMPERATURE	25°C			
DATA FORMAT	2^{23}-1 PRBS			
DATA RATE (MBd)	155	125	100	50
RECEIVER SENSIVIVITY AT BER OF 1 x 10^{-9} (dBm pk)	-26	-27	-29	-30
TYPICAL DYNAMIC RANGE WITH 62.5/125 µm CABLE	14	15	17	18

Figure 16a. 155 MBd Fiber-Optic Receiver for -5.2 V ECL Interface.

planes are recommended for the transmitter and the receiver if they are to be laid out next to one another as is typically done in transceivers. The receiver designs shown in Figures 16a, 17a & 18a use a balanced power supply filter that eliminates noise conducted by both the power and common sides of the voltage source used to power the circuit. This filter should be located between the fiber-optic receiver and the noisy voltage source that powers the digital logic to which the fiber-optic receiver must interface. The fiber-optic transmitter can be directly connected to the noisy logic power supply. The transmitter is a large signal device that is not particularly sensitive to digital system noise. Note that when using the balanced power filter a differential interface between the receiver's digital output and the host systems is required.

Another factor that could degrade the performance of a fiber-optic receiver is environmental noise. The HFBR-2406/2416 combines the PIN diode optical detector and the current-to-voltage converter in a small hybrid package. This miniature hybrid package reduces the size of the antenna at the high-impedance input of the transimpedance amplifier that converts the photo-current to a voltage. The small geometry of this hybrid circuit allows the light-to-voltage converter to achieve excellent electro-magnetic interference immunity. Caution must be exercised, however, to ensure that the metal ferrule of the fiber-optic connector does not act as an EMI source by contacting electrically noisy parts of the system in which it is used. Electrostatic shielding should be applied to the receiver if the system using the fiber-optic link is extremely noisy. For noisy system applications the HFBR-2406C or HFBR-2416TC receivers should be specified. The HFBR-2406C and HFBR-2416TC utilize a conductive plastic housing which provides the shielding needed for electrically noisy environments. The conductive plastic receivers can be used in systems that have EMI fields as large as 10 volts/meter (see AN-1057). Another method that improves the EMI

TYPICAL PEAK POWER COUPLED INTO A 1m LENGTH OF FIBER-OPTIC CABLE I_F = 60 mA T_A = 25°C			
FIBER CABLE	NA	HFBR-14X2	HFBR-14X4
100/140 µm	0.3	-12.0	-6.5
62.5/125 µm	0.275	-16.0	-12.0
50/125 µm	0.20	-18.8	-15.8

NOTES:
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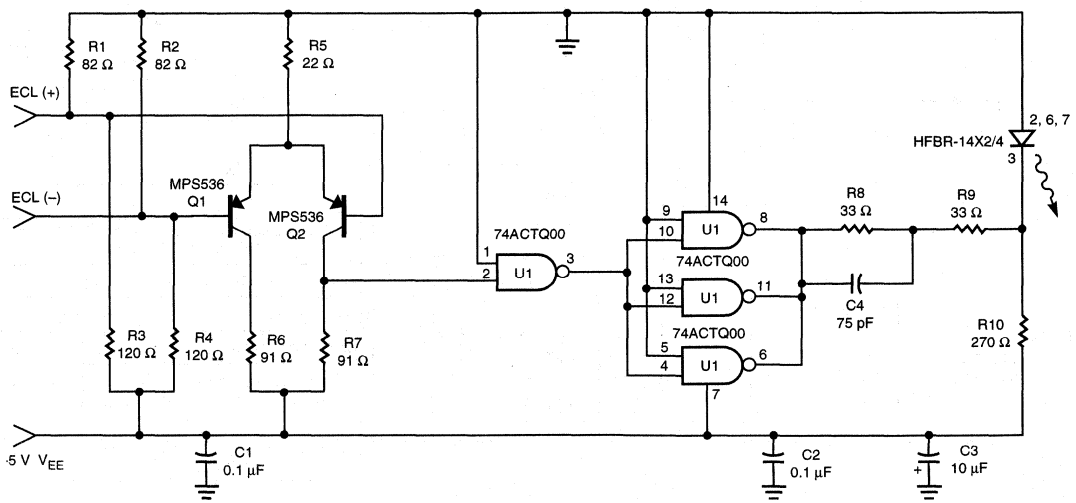

Figure 16b. 155 MBd Fiber-Optic Transmitter for -5.2 V ECL Interface.

TYPICAL RECEIVER PERFORMANCE WITH 1m OF FIBER-OPTIC CABLE				
AMBIENT TEMPERATURE	25°C			
DATA FORMAT	2^{23}-1 PRBS			
DATA RATE (MBd)	155	125	100	50
RECEIVER SENSIVIVITY AT BER OF 1 x 10^{-9} (dBm pk)	-26	-27	-29	-30
TYPICAL DYNAMIC RANGE WITH 62.5/125 µm CABLE	14	15	17	18

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3. L1 AND L2 SHOULD HAVE A ±10% TOLERANCE, SERIES RESISTANCE OF ROUGHLY 0.5 Ω, AND A SELF RESONANT FREQUENCY ≥ 100 MHz.
4. V_{BB} IS A BIAS VOLTAGE GENERATED INTERNALLY BY THE 10H116 ECL LINE RECEIVER.
5. THE V_{CC}-2V POWER IS GENERATED BY THE TL431-CLP SHUNT REGULATOR.

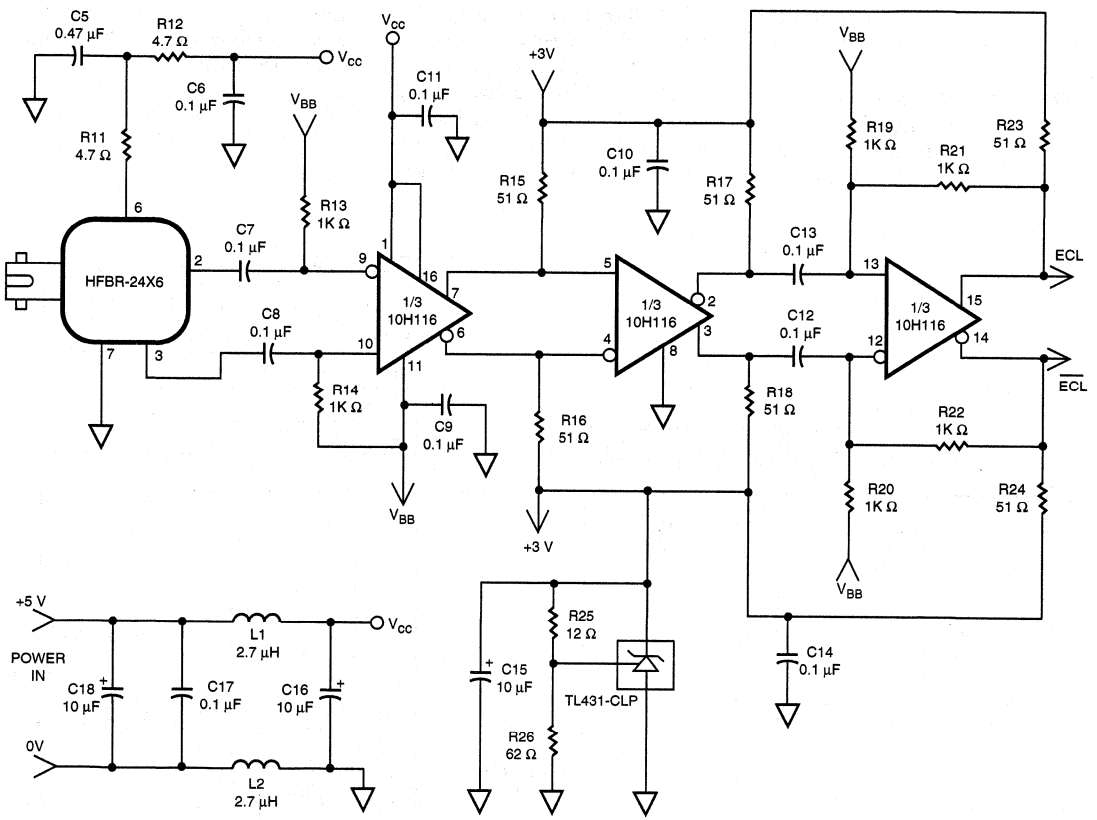

Figure 17a. 155 MBd Fiber-Optic Receiver for +5 V ECL Interface to Am 7969.

immunity of the receiver is to use a connector with a non-conductive plastic or ceramic ferrule. In extremely noisy applications the fiber-optic receiver can be enclosed in a metal box. This box eliminates noise that would otherwise be coupled into the fiber-optic receiver from the system in which it is installed. Systems that require metal shielding have proved to be unusual. Thus, in the majority of applications, the inherent noise immunity of the components combined with the shielding provided by the receiver ground plane have provided sufficient noise immunity.

Applications Support

Some complete designs that allow the use of HFBR-2406/2416 for run-length-limited data applications will now be discussed. Various transceivers have been designed which permit the HFBR-2406/2416 to be interfaced with:

(1) ECL logic operating on -5.2V. (Figure 16)
(2) The AMD TAXIchip™ +5V 100K ECL interface. (Figure 17)
(3) TTL logic operated on +5V. (Figure 18)

At an ambient temperature of 25°C all three interface circuits provided a typical receiver sensitivity of -29 dBm average with a BER of 1 x 10^{-9} at a data rate of 155 MBd. Sensitivity at 125 MBd is typically -30 dBm average at a BER of 1 x 10^{-9}. Figure 19 shows the typical performance of the ECL transmitter/receiver at 25°C. Note that in this test a 2^{23}-1 PRBS pattern at 155 MBd was transmitted over 500 m of 62.5/125 µm graded-index fiber at a BER less than 1 x 10^{-9}. If the low-cost, high-performance fiber-optic links possible with the HFBR-2406/2416 interest you, contact your local HP Field Sales Engineer for additional assistance. Your local HP sales representative can simplify your prototyping task by providing complete artwork for the fiber-optic transmitters and receivers discussed in this Application Bulletin.

*TAXIchip is a registered trademark of Advanced Micro Devices Inc.

TYPICAL PEAK POWER COUPLED INTO A 1m LENGTH OF FIBER-OPTIC CABLE
I_F = 60 mA T_A = 25°C

FIBER CABLE	NA	HFBR-14X2	HFBR-14X4
100/140 µm	0.3	-12.0	-6.5
62.5/125 µm	0.275	-16.0	-12.0
50/125 µm	0.20	-18.8	-15.8

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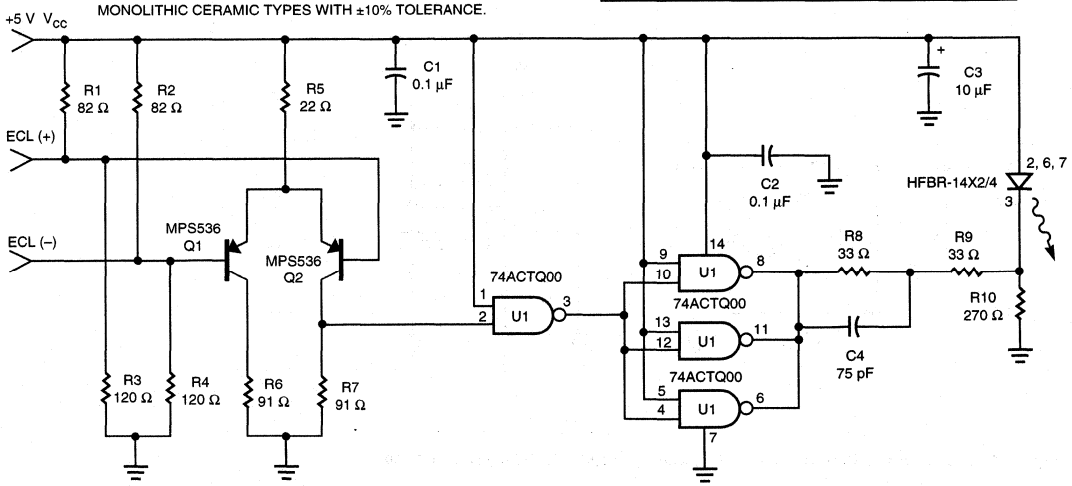
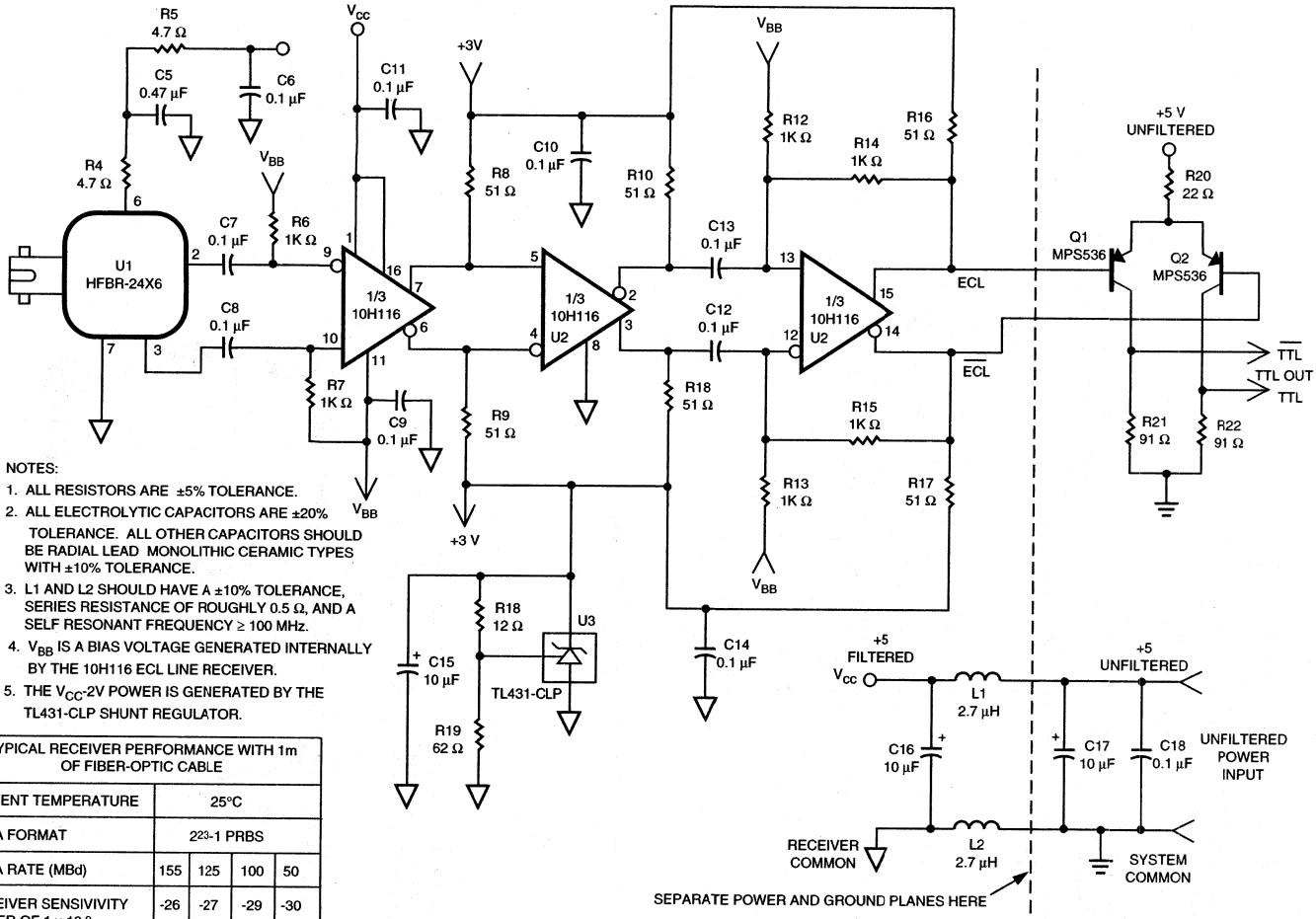


Figure 17b. 155 MBd Transmitter for +5 V ECL Interface to Am 7968.



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3. L1 AND L2 SHOULD HAVE A ±10% TOLERANCE, SERIES RESISTANCE OF ROUGHLY 0.5 Ω, AND A SELF RESONANT FREQUENCY ≥ 100 MHz.
4. V_{BB} IS A BIAS VOLTAGE GENERATED INTERNALLY BY THE 10H116 ECL LINE RECEIVER.
5. THE V_{CC}-2V POWER IS GENERATED BY THE TL431-CLP SHUNT REGULATOR.

TYPICAL RECEIVER PERFORMANCE WITH 1m OF FIBER-OPTIC CABLE				
AMBIENT TEMPERATURE	25°C			
DATA FORMAT	2^{23}-1 PRBS			
DATA RATE (MBd)	155	125	100	50
RECEIVER SENSIVIVITY AT BER OF 1 x 10^{-9} (dBm pk)	-26	-27	-29	-30
TYPICAL DYNAMIC RANGE WITH 62.5/125 µm CABLE	14	15	17	18

Figure 18a. 155 MBd Fiber-Optic Receiver for TTL Interface.

TYPICAL PEAK POWER COUPLED INTO A 1m LENGTH OF FIBER-OPTIC CABLE I_F = 60 mA T_A = 25°C			
FIBER CABLE	NA	HFBR-14X2	HFBR-14X4
100/140 µm	0.3	-12.0	-6.5
62.5/125 µm	0.275	-16.0	-12.0
50/125 µm	0.20	-18.8	-15.8

NOTES:
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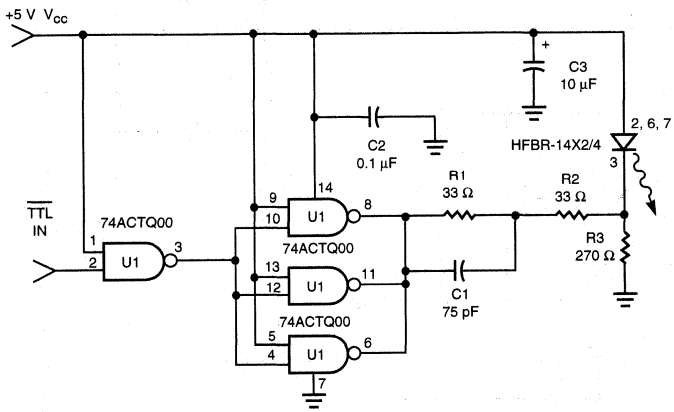


Figure 18b. 155 MBd Fiber-Optic Transmitter for TTL Interface.

- DATA RATE 155 MBd
- DATA PATTERN 2^{23}-1 PRBS
- FIBER TYPE SIECOR 62.5/125 µm
- FIBER LENGTH 500 m
- TYPICAL PEAK-TO-PEAK JITTER = 760 ps
- TIME SCALE IS 2.0 ns/DIV.

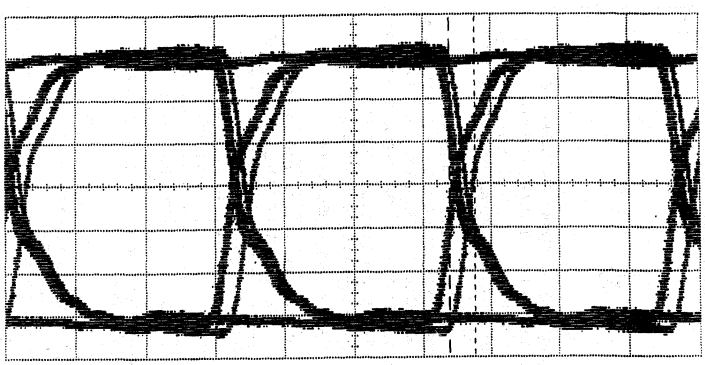


Figure 19. ECL Output of the Transceiver Shown in Figures 17a and 17b.

Complete Transceiver Solution

Figure 21 shows the schematic for a complete fiber-optic transceiver. This transceiver is constructed on a printed circuit, which is 1" wide by 1.78" long, using surface mount components. The transceiver in Figure 21 has an industry standard +5 V ECL (PECL) electrical interface. The transceiver shown in Figure 21 can be populated with HP's HFBR-14X4/24X6 820 nm components or HP's HFBR-1312T/2316T pin compatible 1300 nm components. When the transceiver shown in Figure 21 is populated with 820 nm components, and tested at a data rate of 155.5 MBd, using a 500 m length of 62.5/125 μm fiber, it provides a typical eye opening of 5.2 ns at a BER of 1 x 10-9, as shown in Figure 20.

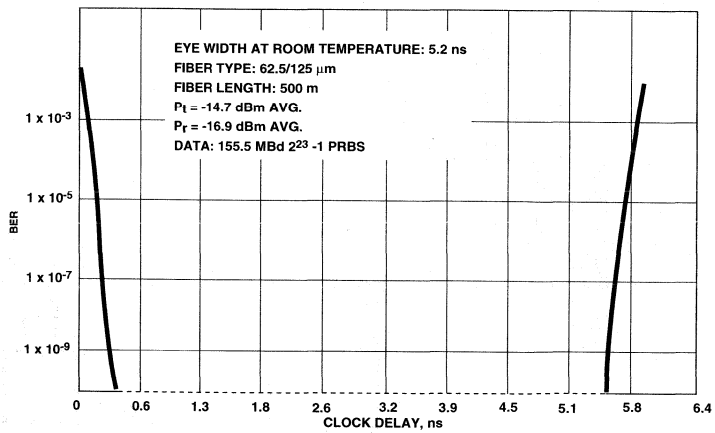


Figure 20. Typical BER vs. Clock Delay at 155.5 MBd.

The power supply filter and ECL terminations shown in Figure 22 are recommended for use with the transceiver shown in Figure 21. The printed circuit artwork for the surface mount transceiver is shown in Figure 23. A complete parts list for the 820 nm transceiver is shown in Table 1, and a complete parts list for the 1300 nm transceiver is shown in Table 2.

Designers interested in inexpensive solutions are encouraged to embed the complete fiber-optic transceiver described in this Application Note into the next generation of their new data communication products. All of the information needed to imbed the transceiver shown in Figure 21 can be obtained by calling the electronic bulletin board at 408-435-6733. Just call the bulletin board, then download the file named FURBALL.EXE to obtain electronic copies of the transceiver's artwork, schematic, and material list. If time to market is critical, the product development cycle can be shortened by ordering a fully assembled HFBR-0416 transceiver demo board from your local HP Field Sales Engineer.

References

[1] Hewlett-Packard Optoelectronics Designer's Catalog 1988, HFBR-AWSyyy data sheet.

[2] James J. Refi, "LED Bandwidth of Multimode Fibers as a Function of Laser Bandwidth and LED Spectral Characteristics", Journal of Lightwave Technology, Volume LT-4 No. 3, March 1986.

[3] Delon C. Hanson and Jerry Hutchison, "LED Source and Fiber Specification Issues for the FDDI Network", COMPCON Spring '87, IEEE Computer Society, (San Francisco, CA), February 24-26, 1987.

[4] Delon C. Hanson, "Fiber Optic Sub-System for Local Area Networks", OFC '88, (New Orleans, LA), January 24-28, 1988.

[5] Hans O. Sorensen, "Use of Standard Modulation Codes for Fiber Optic Link Optimization", FOC 1984.

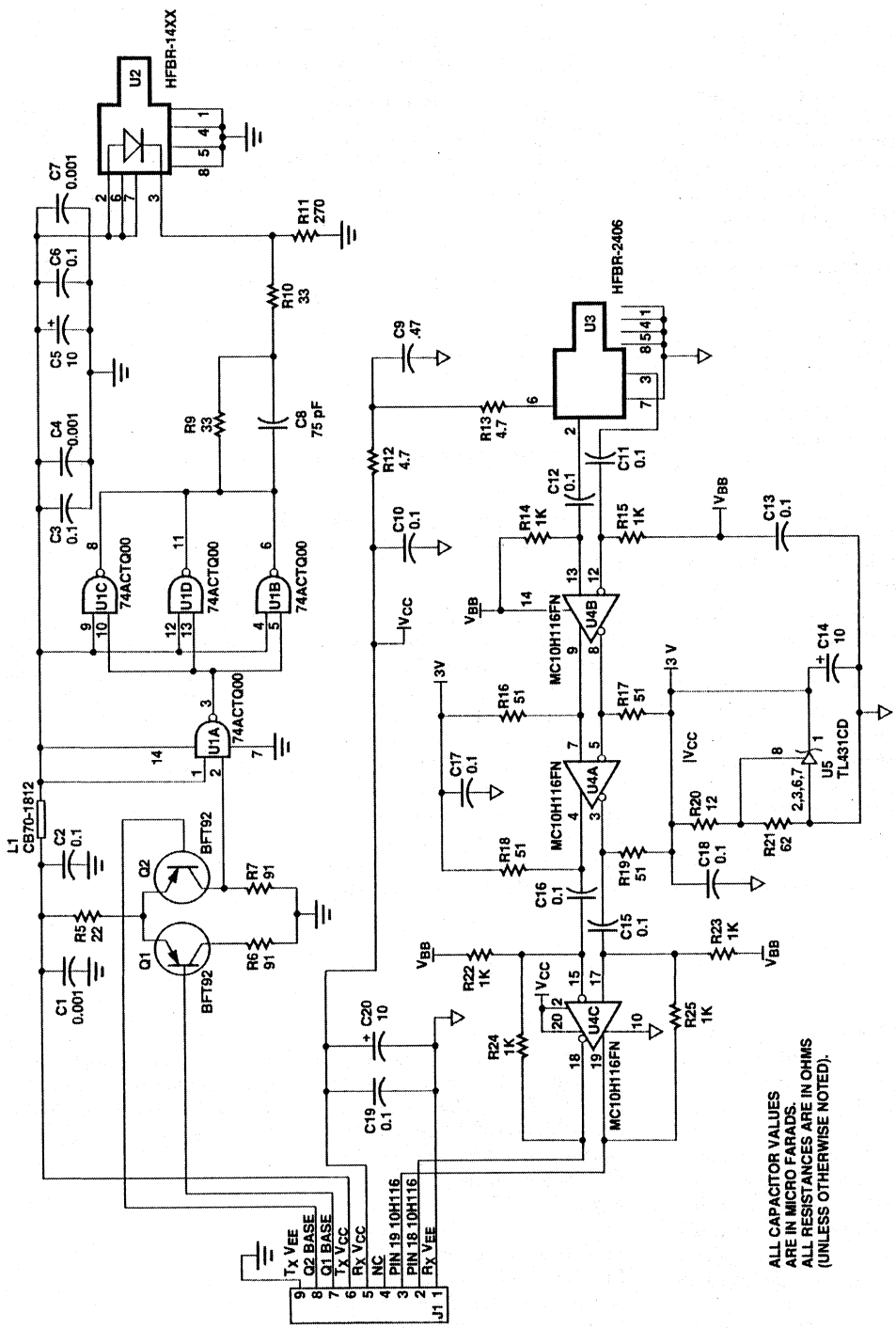


Figure 21. 155 MBd 1x9 Transceiver Schematic

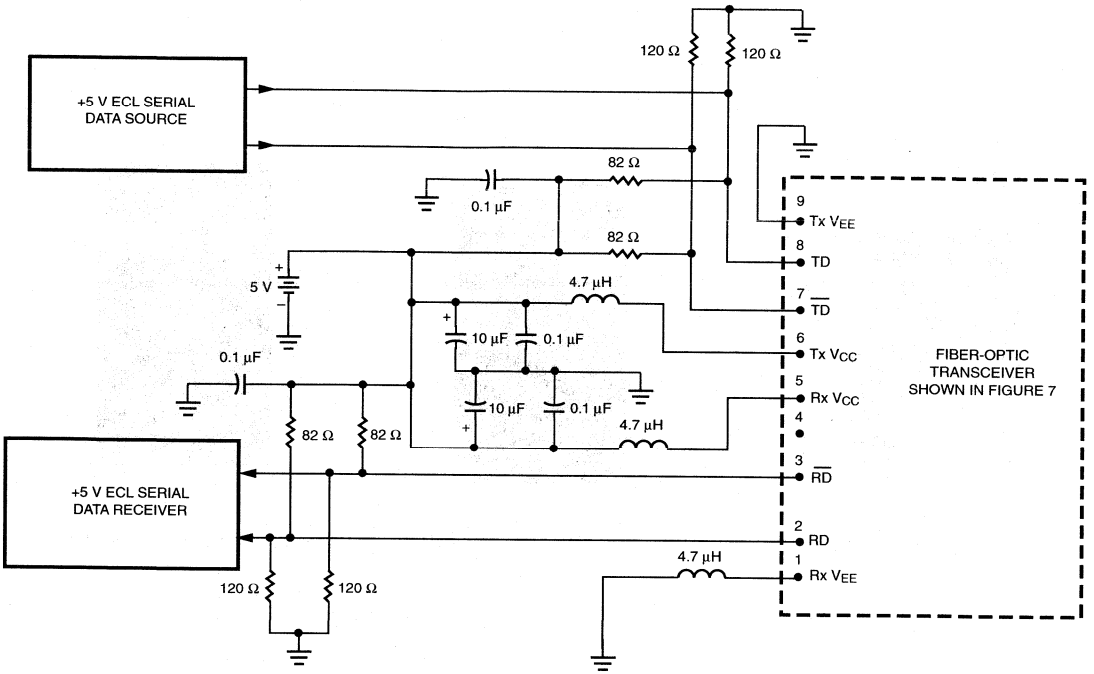


Figure 22. Recommended Power Supply Filter and +5 V ECL Signal Terminations

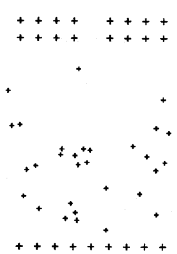


Figure 23a. Drill Drawing

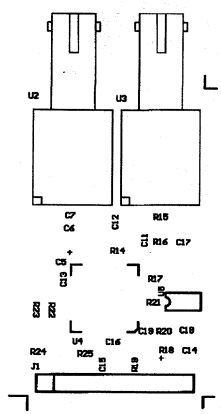


Figure 23b. Top Silkscreen

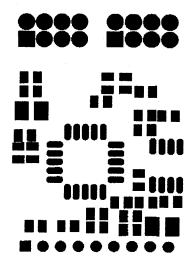


Figure 23c. Top Side Solder Mask

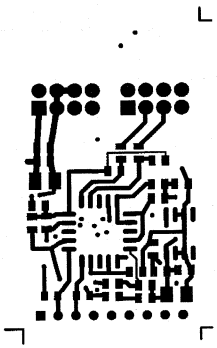


Figure 23d. Top Layer Copper

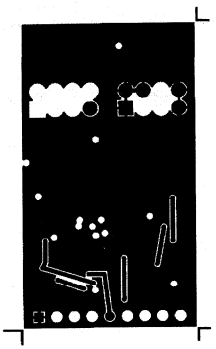


Figure 23e. Mid Layer (2) Rx GND

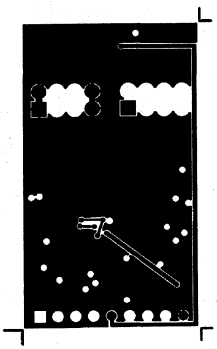


Figure 23f. Mid Layer (3) Ts GND

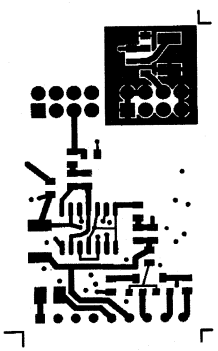


Figure 23g. Bottom Copper

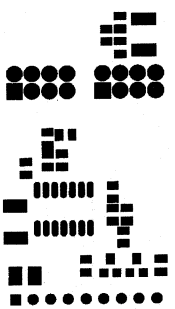


Figure 23h. Bottom Side Solder Mask

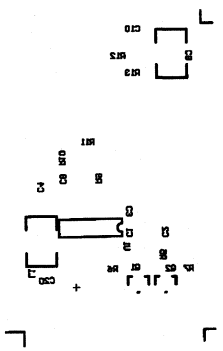


Figure 23i. Bottom Silkscreen

Table 1. Bill of Materials for Multi-Mode 820 nm Fiber-Optic Transceiver

Designator	Part Type	Description	Footprint	Material	Part Number	Quantity	Vendor 1
C1	0.001	Capacitor	805	NPO/COG	C0805NPO500102JNE	3	Venkel
C4	0.001	Capacitor					
C7	0.001	Capacitor					
C10	0.1	Capacitor	805	X7R or better	C0805X7R500104KNE	12	Venkel
C 11	0.1	Capacitor					
C 12	0.1	Capacitor					
C 13	0.1	Capacitor					
C 15	0.1	Capacitor					
C 16	0.1	Capacitor					
C17	0.1	Capacitor					
C 18	0.1	Capacitor					
C 19	0.1	Capacitor					
C2	0.1	Capacitor					
C3	0.1	Capacitor					
C6	0 1	Capacitor					
C9	0.47	Capacitor	1812	X7R or better	C 1812X7R500474KNE	1	Venkel
C14	10	Capacitor	B	Tantalum, 10v	TA010TCM106MBN	3	Venkel
C20	10	Capacitor					
C5	10	Capacitor					
C8	75 pF	Capacitor	805	NPO/COG	C0805COG500750JNE	1	Venkel
U1	I.C.	Nand Gate	S08		74ACTQ00	1	National
U2	Fioer-Optic	Transmitter			HFBR-1414	1	HP
U3	Fiber-Optic	Receiver			HFBR-2416	1	HP
U4	MC10H116FN	IC, ECL line receiver	PLCC20		MC10H116FN	1	Motorola
U5	TL431CD	IC, Voltage Regulator	SO-8		TL431CD	1	T.I.
L1	CB70-1812	Inductor	1812		HF30ACB453215	1	TDK
R12	4.7	Resistor	805	5%	CR080510W4R7JT	2	Venkel
R 13	4.7	Resistor					
R20	12	Resistor	805	5%	CR080510W120JT	1	Venkel
R9	33	Resistor	805	5%	CR080510W330JT	1	Venkel
R10	33	Resistor	805	5%	CR080510W330JT	1	Venkel
R11	270	Resistor	805	5%	CR080510W271JT	1	Venkel
R5	22	Resistor	805	5%	CR080510W220JT	1	Venkel
R16	51	Resistor	805	5%	CR080510W510JT	4	Venkel
R17	51	Resistor					
R18	51	Resistor					
R19	51	Resistor					
R21	62	Resistor	805	5%	CR080510W620JT	1	Venkel
R6	91	Resistor	805	5%	CR080510W910JT	2	Venkel
R7	91	Resistor					
R14	1K	Resistor	805	5%	CR080510W102JT	6	Venkel
R15	1 K	Resistor					
R22	1 K	Resistor					
R23	1 K	Resistor					
R24	1 K	Resistor					
R25	1 K	Resistor					
Q1	BFT92	Transistor	SOT-23		BFT92	2	Philips
Q2	BFT92	Transistor					
J1		Pins			343B	9	McKenzie

Table 2. Bill of Materials for Multi-Mode 1300 nm Fiber-Optic Transceiver

Designator	Part Type	Description	Footprint	Material	Part Number	Quantity	Vendor 1
C1	0.001	Capacitor	805	NPO/COG	C0805NPO500102JNE	3	Venkel
C4	0.001	Capacitor					
C7	0.001	Capacitor					
C10	0.1	Capacitor	805	X7R or better	C0805X7R500104KNE	12	Venkel
C 11	0.1	Capacitor					
C 12	0.1	Capacitor					
C 13	0.1	Capacitor					
C 15	0.1	Capacitor					
C 16	0.1	Capacitor					
C17	0.1	Capacitor					
C 18	0.1	Capacitor					
C 19	0.1	Capacitor					
C2	0.1	Capacitor					
C3	0.1	Capacitor					
C6	0 1	Capacitor					
C9	0.47	Capacitor	1812	X7R or better	C 1812X7R500474KNE	1	Venkel
C14	10	Capacitor	B	Tantalum, 10v	TA010TCM106MBN	3	Venkel
C20	10	Capacitor					
C5	10	Capacitor					
C8	150 pF	Capacitor	805	NPO/COG	C0805COG500151JNE	1	Venkel
U1	I.C.	Nand Gate	S08		74ACTQ00	1	National
U2	Fioer-Optic	Transmitter			HFBR-1312T	1	HP
U3	Fiber-Optic	Receiver			HFBR-2316T	1	HP
U4	MC10H116FN	IC, ECL line receiver	PLCC20		MC10H116FN	1	Motorola
U5	TL431CD	IC, Voltage Regulator	SO-8		TL431CD	1	T.I.
L1	CB70-1812	Inductor	1812		HF30ACB453215	1	TDK
R12	4.7	Resistor	805	5%	CR08051OW4R7JT	2	Venkel
R 13	4.7	Resistor					
R20	12	Resistor	805	5%	CR080510W120JT	1	Venkel
R9	22	Resistor	805	5%	CR080510W220JT	1	Venkel
R10	27	Resistor	805	5%	CR080510W270JT	1	Venkel
R5	22	Resistor	805	5%	CR080510W220JT	1	Venkel
R16	51	Resistor	805	5%	CR080510W510JT	4	Venkel
R17	51	Resistor					
R18	51	Resistor					
R19	51	Resistor					
R21	62	Resistor	805	5%	CR08051OW620JT	1	Venkel
R6	91	Resistor	805	5%	CR080510W91OJT	2	Venkel
R7	91	Resistor					
R14	1 K	Resistor	805	5%	CR080510W102JT	6	Venkel
R15	1 K	Resistor					
R22	1 K	Resistor					
R23	1 K	Resistor					
R24	1 K	Resistor					
R25	1 K	Resistor					
Q1	BFT92	Transistor	SOT-23		BFT92	2	Philips
Q2	BFT92	Transistor					
J1		Pins			343B	9	McKenzie

HEWLETT® PACKARD

Versatile Link

Application Note 1035

Introduction

This application note describes how fiber optics can be used to solve many different types of application problems, introduces Hewlett-Packard's Versatile Link plastic fiber optics, and shows how to design a fiber-optic link using the Versatile Link. Below is an outline of this application note.

I. Introduction
II. Example Applications
III. Versatile Link Description
IV. System Specifications and Link Design
V. Pulse-Width Distortion
VI. Additional Circuit Recommendations
VII. Appendix

Optical fiber is typically made from either plastic or glass. Because both plastic and glass are electrical insulators, there is no direct electrical connection between the transmitter and the receiver of a fiber-optic link. This helps to alleviate ground-loop and common-mode noise problems, as well as to isolate large common-mode voltages. Another useful property of optical fiber is that it does not emit radiation and is not susceptible to electromagnetic interference (EMI). This prevents an optical fiber from interfering with neighboring wires and also gives it inherent immunity to induced or coupled noise from adjacent wires.

Fiber optics can protect equipment from excessive voltages, reduce EMI, increase safety by eliminating the hazard of generating sparks, and ensure data integrity in environments with large amounts of noise or with high common-mode voltages.

Example Applications

Different applications have different requirements and, therefore, different reasons for using fiber optics. The following paragraphs discuss some examples of common fiber-optic applications and why fiber optics are used in those applications.

The first type of application utilizes the EMI immunity of fiber-optics for data transmission in electrically noisy environments. A good example is data transmission between a programmable logic controller (PLC) and the computer that is directing it, illustrated in Figure 1a. The two computers might be in a factory containing machinery that generates large amounts of electrical noise. Data transmission lines commonly run alongside lines that supply power to the machinery. There may be large amounts of electrical noise present on the power lines caused by the machinery. This noise can couple electromagnetically into any adjacent lines. If one of those adjacent lines is a twisted-pair or coax line carrying data, the coupled electrical noise may significantly interfere with the data transmission. The noise may cause only periodic errors, or it might completely corrupt all of the data being sent. Because optical fiber is not susceptible to EMI, it can eliminate the undesirable coupling of noise from the power lines onto the data lines and ensure error-free data transmission.

Figures 1b, 1c and 1d illustrate other applications which utilize the EMI immunity of fiber optics. Figure 1b shows how fiber can connect a robot controller with the cell controller and the robot. The fiber eliminates the large amounts of noise generated by the motors, solenoids, etc. that are part of the robot. Figure 1c illustrates how fiber is used to network point-of-sales terminals (cash registers) in a retail store. Fiber optics ensures that sales information is not corrupted or lost due to noise generated inside the building. Figure 1d shows fiber optics connecting two HPIB (IEEE-488) data buses. The HPIB data bus

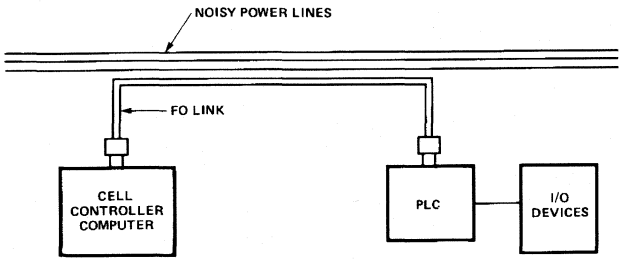


Figure 1a. Programmable Logic Controller.

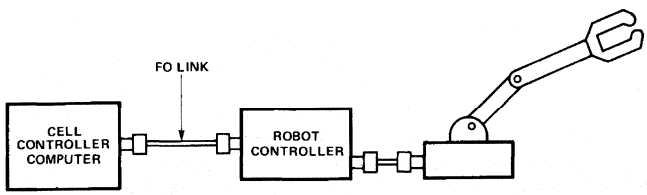


Figure 1b. Robot Controller.

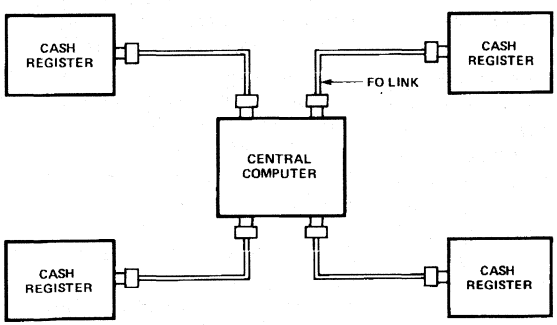


Figure 1c. Point of Sales Terminals

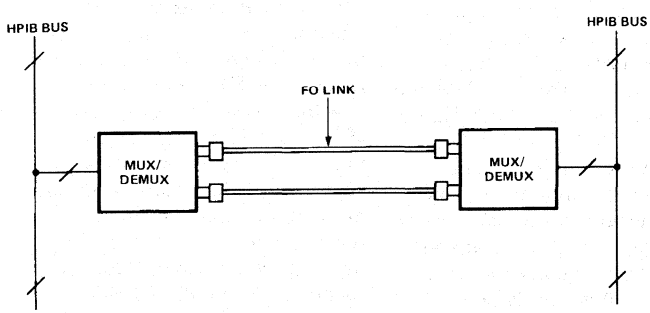


Figure 1d. HPIB (IEEE-488) Bus Extender.

is commonly used to connect test instruments in manufacturing automated test systems. Again, fiber optics eliminates the noise that is commonly present in a factory and ensures that correct test data is transferred to the test system controller.

The second type of application uses fiber-optics for voltage isolation. A digital voltmeter, illustrated in Figure 2a, is a good example. There is typically some circuitry at the input of the voltmeter that converts the analog voltage across the input terminals into a digital signal; this circuitry is called an analog-to-digital converter (ADC). The output of the ADC is then sent to processing circuitry that displays the information on the front panel or, perhaps, sends the information to an external computer. A problem arises, however, when the signal to be measured has a very high common-mode voltage component. An example of this is measuring the difference between two very high voltages. The ADC will also be at the same common-mode voltage, causing a problem in safely sending information from the ADC to the digital control circuitry at ground potential. Because of its insulating properties, an optical fiber is not affected by such high voltages and does not conduct any current that might interfere with or damage the circuitry to which it is connected. Fiber optics allow data to be transmitted and still maintain a high degree of voltage isolation.

Figures 2b, 2c and 2d also illustrate the use of fiber in voltage-isolation applications. Figure 2b is a simple block diagram of an electrocardiograph, which is

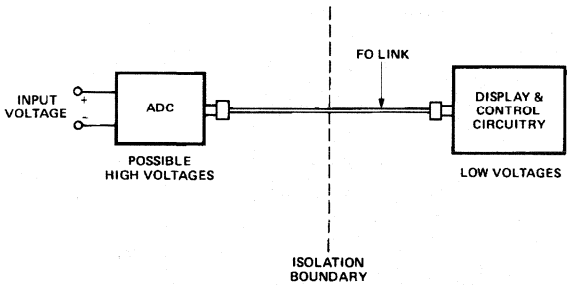


Figure 2a. Digital Voltmeter.

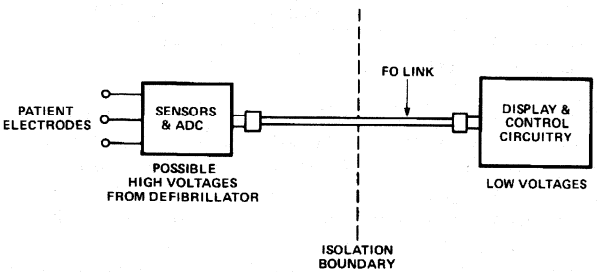


Figure 2b. Medical Equipment – Heart Monitor.

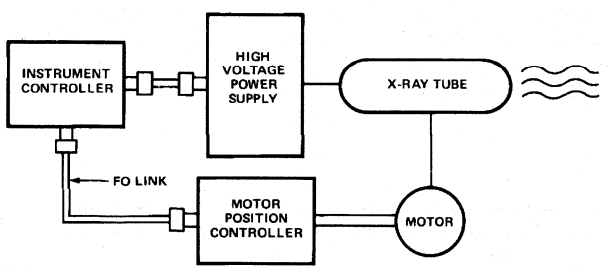


Figure 2c. X-Ray Machine.

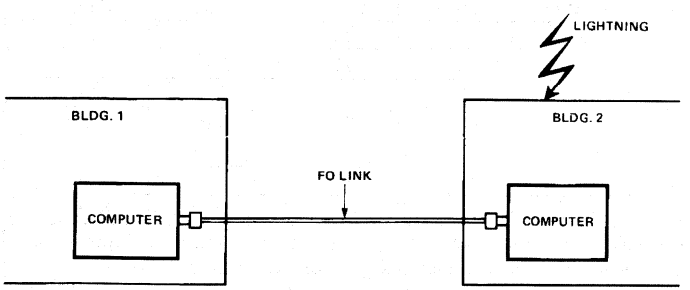


Figure 2d. Lightning Protection.

used to monitor a patient's heart. If the heart were to stop beating, a defibrillator might be used to restart it. The fiber protects the electrocardiograph from the very high voltages that are generated by the defibrillator. Figure 2c shows the use of fiber in a clinical X-ray machine. The fiber isolates the high voltages used to power the X-ray tube and provides EMI immunity from the noise generated by switching high voltages and currents. Figure 2d illustrates how fiber can protect electronic equipment from the high voltages generated by nearby lightning strikes.

Another type of application reduces the amount of unwanted electromagnetic radiation emitted by a transmission line. This type of application is the converse of the first type; the idea is to minimize the amount of EMI that is radiated from the transmission line itself, rather than being concerned with the susceptibility of the transmission line to external interference. An example is high speed video transmission from a workstation computer to a high resolution video monitor, shown in Figure 3a. As the resolution of a video monitor increases, the number of pixels (dots) on the screen also increases. If the computer is updating the screen with the same number of frames per second, the computer must send more pixels per second as the resolution increases. Therefore, the bandwidth of the video transmission link must increase as well. If a coaxial cable is used to transmit the video information, it becomes more and more difficult (and expensive) to shield the cable and reduce unwanted radiation as the frequency of the transmitted information

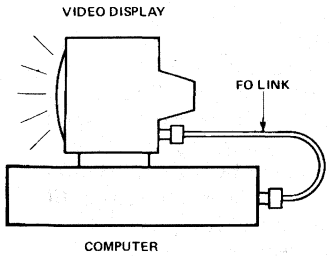


Figure 3a. High Speed Video Transmission.

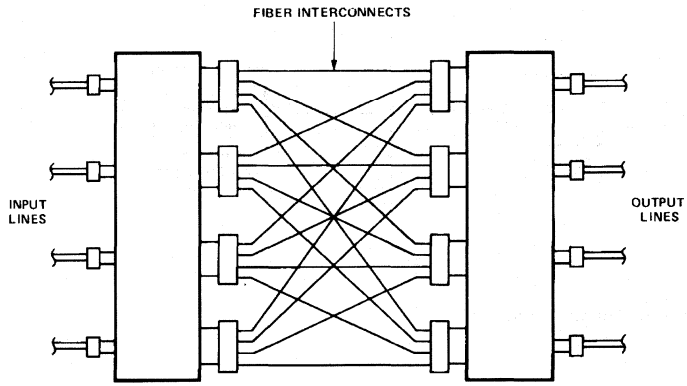


Figure 3b. Telephone Switching Network.

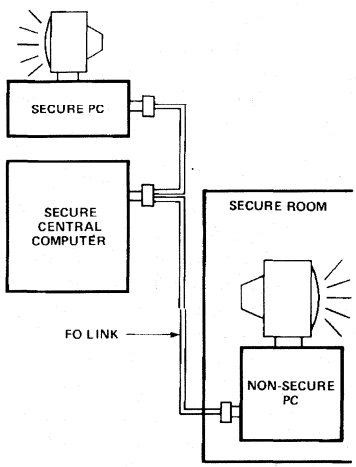


Figure 3c. Tempest Applications.

increases. Because an optical fiber does not emit radiation, it can significantly reduce the amount of EMI generated in transmitting information at very high data rates or when there are many transmission lines.

Figures 3b and 3c show two additional applications that use fiber optics to reduce the amount of unwanted emissions. Figure 3b illustrates the use of fiber in the telephone switching network of a central office switch. Fiber helps to minimize the amount of unwanted radiation generated by the large number of interconnects in the network. Figure 3c illustrates how fiber might be used in Tempest applications. Tempest is a federal government specification that restricts the amount of radiation that can be emitted by "secure" electronic equipment. Because fiber does not emit any radiation, it is well suited for Tempest applications. Figure 3c shows how fiber is used to connect a secure personal

Table 1. Distance and Data Rate Summary

Versatile Link		Guaranteed Minimum Link Length Metres				Typical Link Length Metres	
		0°C - 70°C		25°C		25°C	
		Standard Cable	Improved Cable	Standard Cable	Improved Cable	Standard Cable	Improved Cable
High Performance	5 MBd	12	17	17	24	35	40
High Performance	1 MBd	24	34	30	41	50	65
Low Current Link	40 kBd	8	11	-	-	30	35
Extended Distance Link	40 kBd	60	82	65	90	100	125
Standard	1 MBd	5	7	11	15	30	40
Photo Interrupter	500 kHz	N.A.	N.A.	N.A.	N.A.	N.A.	N.A.
Evaluation Kit	1 MBd (Standard)	Contents: Horizontal transmitter, horizontal receiver packages; 5 metres of simplex cable with simplex and simplex latching connectors installed; individual connectors: simplex, duplex, simplex latching, bulkhead adapter; polishing tool, abrasive paper, literature.					

computer (i.e., a computer constructed to limit the amount of emissions) with a secure central computer. The fiber also connects the secure central computer with a non-secure personal computer, located inside of a secure room (i.e., a room specifically designed to limit unwanted emissions).

The above examples illustrate how the features of fiber optics can be used to solve problems found in many different types of applications.

Versatile Link Description

The Hewlett-Packard HFBR-0501 series low-cost fiber-optic system, the Versatile Link, was designed for ease of use, versatility, and reliability. Table 1 summarizes the data rate and distance capabilities of the Versatile Link family. Typical distances at room temperature are also shown. The maximum data rates for Versatile Link components range from 40 kBd to 5 MBd, with even higher data rates available in the future.

Hewlett-Packard guarantees minimum and maximum specifications of its components both at room temperature and over the full operating temperature range (0 to 70°C). These guaranteed specifications were obtained from extensive characterizations of the Versatile Link components and cover the full range of manufacturing process variations. This ensures reliable circuit operation and allows HP to guarantee minimum link distances.

The Versatile Link family, shown in Figure 4, is intended

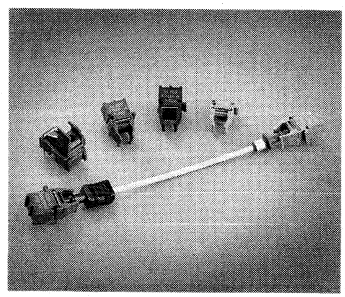


Figure 4. Versatile Link Family.

for use with 1 mm plastic optical fiber. No optical design is required because the specifications include any connector losses at the transmitter and at the receiver. The compact, low-profile package is color coded to distinguish transmitters from receivers; connectors are also color coded. Both horizontal and vertical package styles are available with standard 8-pin DIP pinouts. The packages can also be interlocked or stacked ("n-plexed") to decrease the required amount of PC-board space.

Figure 5 shows an exploded view of the Versatile Link horizontal style package. The package was designed for improved performance and ease of manufacturing. The active components are attached to a lead frame which is then transfer molded with clear plastic to form the insert. A precision lens is molded into the insert to optimize the optical coupling from the package to the fiber. The insert is held in the main part of the housing by a snap-on cap on the back of the package.

The Versatile Link package uses an active optical alignment system to ensure proper coupling between the connector and the package. Figure 6 illustrates

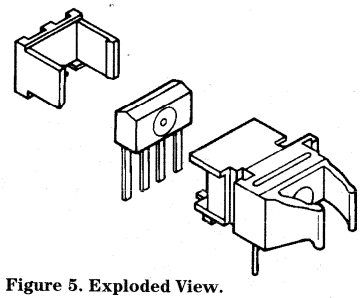


Figure 5. Exploded View.

how the alignment system operates. The precision-molded lens on the insert is located at the bottom of a depression in the shape of a truncated cone. When the connector is inserted into the package, the jaws of the housing force the beveled end of the connector into the cone-shaped depression. This accurately centers the fiber directly above the molded lens on the insert and ensures reliable and repeatable connections.

The gray transmitter modules contain 660 nm large-area LEDs that can be easily interfaced to all standard logic families. The blue receiver modules contain monolithic integrated optical detectors with TTL/CMOS-compatible outputs.

Four connector options are available for use with the Versatile Link:

1. Simplex connector, which is compatible with our previous Snap-In Link family,
2. Latching simplex connector, for applications that require increased connector pullout force,
3. Duplex connector, which incorporates a lockout feature that ensures correct orientation of the connector when used with interlocked packages,
4. Latching duplex connector.

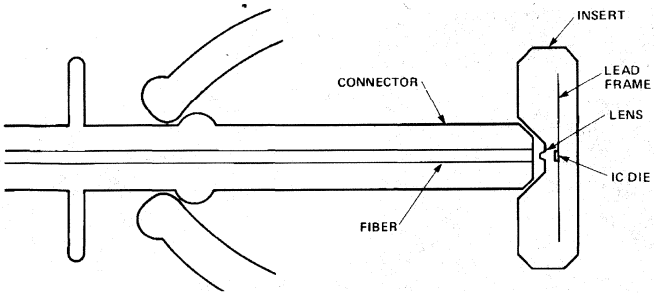


Figure 6. Connector Alignment.

Hewlett-Packard offers simplex and duplex cables with two grades of attenuation, standard and improved. Cable with connectors is offered in one meter increments of length; unconnectored cable is available in lengths of 25, 100, and 500 meters. These cables are UL-recognized and pass UL VW-1 flame-retardancy specifications.

An evaluation kit is available which contains a standard 1 MBd transmitter and receiver, 5 m of connectored cable, individual simplex, simplex latching, and duplex connectors, a bulkhead adapter, polishing tools and literature.

The data sheet for the Versatile Link family contains complete guaranteed specifications for entire links and individual components, electrical pinouts, interface circuits, connectoring information, mechanical dimensions, part number and ordering information.

Reliability Data Sheets are available which provide complete reliability information for all Versatile Link components.

System Specifications and Link Design

To obtain optimum performance under a variety of different conditions, it is helpful to understand some of the basic specifications of the Versatile Link and how to use them in designing a fiber optic link. This section will first discuss how Hewlett-Packard specifies its transmitters, receivers, and plastic fiber-optic cable, then explain how to use those specifications in determining proper operating conditions. This section will also explain what a link operating diagram is and how to use it to quickly determine transmitter drive current or link length.

A basic fiber-optic system is very simple: an LED transmitter couples light into a fiber, the light travels down the fiber to an optical detector, and the detector converts the light into a digital output signal. The important specifications of the fiber-optic data link are:

1. How much light is coupled into the fiber by the transmitter,

2. How much light the receiver needs to function properly,

3. How much light is lost on the way to the receiver.

For a brief explanation of how optical power is specified in "dB" and "dBm", see the Appendix.

Transmitter Specifications

The primary transmitter specification is P_T, the amount of optical power coupled into the fiber at a specified LED drive current. P_T specifies how much power is actually coupled into the fiber; this eliminates the need to calculate the loss in coupling light from the LED to the fiber. Due to normal process variations, HP specifies a range of coupled power for each type of transmitter. Figure 7 shows the coupled power specifications for each of the Versatile Link transmitters. Guaranteed specifications over the full operating range are shown in Figure 7 because these values typically are used in "worst-case" designs and are also used in our examples.

The amount of coupled power can be easily adjusted by changing the LED forward drive current, I_F, as indicated in Figure 8. Notice that the coupled power is normalized to the value at

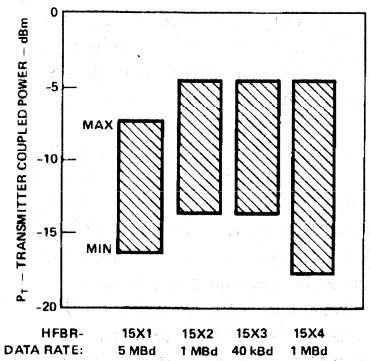


Figure 7. Transmitter Specifications.

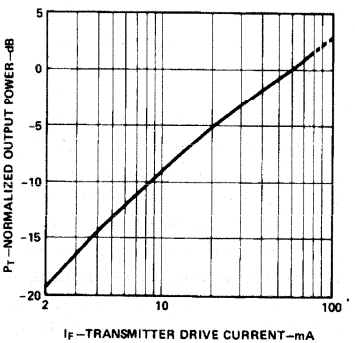


Figure 8. Normalized Typical Output Power vs. Drive Current.

I_F= 60 mA. The graph, therefore, represents the CHANGE in output power for different drive currents. For example, operating the transmitter at a drive current of 20 mA will drop the output power by about 5 dB. There is an approximately linear relationship between drive current and output power; therefore, the output power will drop approximately in half (i.e., about 3 dB) when the drive current is cut in half.

Figure 9 shows thc recommended transmitter drive circuits. You should note that for the 5 MBd and 40 kBd drive circuits, an input-high level turns the LED on; for the 1 MBd circuit, an input-high level turns the LED off. The capacitor in the 1 MBd circuit slows the falling edge of the optical waveform and allows the receiver to operate up to the maximum output power of the 1 MBd transmitter. The value of R1 can be determined from the equations in the figure. Typical values for the forward voltage of thc LED, V_F, and the output low voltage of the gate, V_{OL}, are 1.6 V and 0.25 V respectively.

Additional transmitter drive circuits will be covered later in the application note.

Receiver Specifications

The Versatile Link receivers function somewhat as optical inverters: high input power causes a low output voltage, and low input power causes a high output voltage.

There are two primary receiver specifications:

1. $P_{R(L)}$ specifies the input power required for a LOW output voltage,

2. $P_{R(H)}$ specifies the input power required for a HIGH output voltage.

Figure 10 shows the ranges of $P_{R(L)}$ and $P_{R(H)}$ for each of the receivers over the full operating temperature range.

Typically, both a minimum and a maximum are specified for $P_{R(L)}$. For proper operation, the received optical power must be between the minimum and the maximum $P_{R(L)}$. If no maximum is specified, the corresponding transmitter (i.e., the HFBR-15X2 transmitter for the HFBR-25X2 receiver) is not capable of overdriving the receiver for drive currents up to the recommended maximum value of 60 mA, and

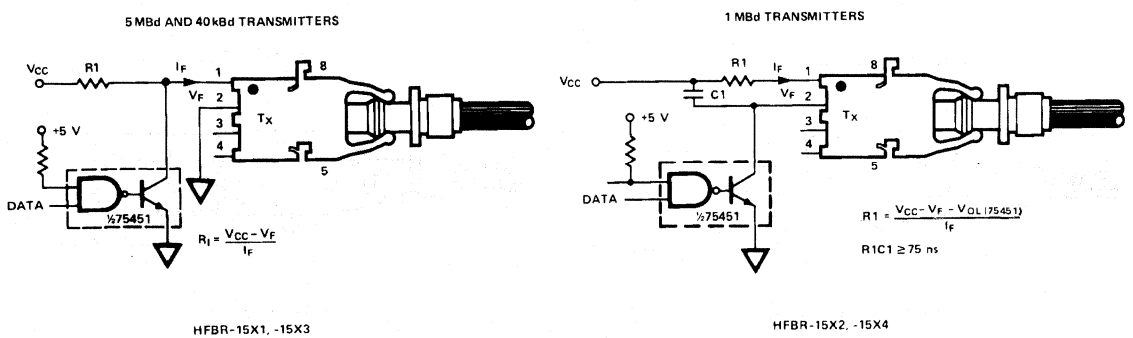


Figure 9. Transmitter Drive Circuits.

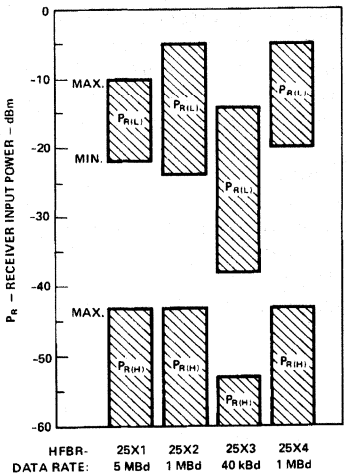


Figure 10. Receiver Specifications.

you need ensure only that the input power is greater than the minimum $P_{R(L)}$. If the maximum $P_{R(L)}$ is exceeded, the receiver may exhibit excessive pulse-width distortion (discussed later) or multiple edge transitions.

Only a maximum $P_{R(H)}$ is specified for each receiver. When the transmitter LED is in the off state, the received optical power must be less than the maximum $P_{R(H)}$ for proper receiver operation.

The minimum $P_{R(L)}$ is called the sensitivity of the receiver. A receiver with good sensitivity (lower minimum $P_{R(L)}$) will allow longer link lengths or lower transmitter drive current. The difference between the minimum and maximum $P_{R(L)}$ is called the dynamic range of the receiver. A receiver with a large dynamic range can handle a wider variation in received power and therefore more variation in the length of the link. Note that the 40 kBd receiver has very good sensitivity and a large dynamic range. The 40 kBd link can therefore handle long link lengths and large variations in the length of the link. Also note that the maximum $P_{R(L)}$ for the 1 MBd receivers is determined by the maximum coupled power of the 1 MBd transmitters.

Because the receiver switching threshold is between the minimum $P_{R(L)}$ and the maximum $P_{R(H)}$, the receiver input power should be within this region only very briefly during signal transitions. Very slow rise or fall times of the input optical waveform may cause multiple transitions on the output of the receiver.

Figure 11 shows how simple the receiver interface circuits are, requiring only one or two external components. The 0.1 µF bypass capacitor is mandatory and must be located close to the receiver; the total lead length between the ends of the capacitor and the receiver power supply pins should not exceed 20 mm. The external pull-up resistor is optional. The 1 MBd and 5 MBd receivers have an internal 1K ohm pull-up resistor, and the 40 kBd receiver has an internal 150 µA pull-up current source. All data sheet specifications for propagation delay and rise/fall time use an external pull-up resistor, a 560 ohm resistor for the 1 MBd and 5 MBd receivers, and a 3.3K ohm resistor for the 40 kBd receiver.

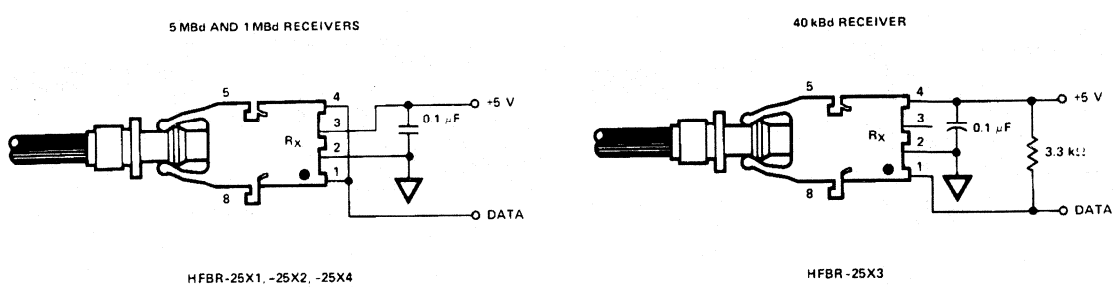


Figure 11. Receiver Interface Circuits.

Optical Losses

There are two primary causes of optical loss in a fiber-optic link: losses due to cable attenuation and connector coupling efficiency.

Attenuation is defined as loss per unit length of fiber, expressed in dB/m. To obtain the optical loss in a fiber, simply multiply the length of the fiber by the attenuation. Figure 12 shows the range of attenuation for the two grades of fiber, standard and improved, that Hewlett-Packard offers.

For a given length and type of fiber, there will be a range of optical loss due to the range of attenuation of the fiber. For our standard fiber, Figure 13 illustrates how the range of loss, as well as the magnitude of the loss, increases as the length of the fiber increases. You can see that for a 40 m length of fiber, the losses due to attenuation will be between 7.6 dB and 17.2 dB, a range of almost 10 dB. A fiber optic receiver must be able to handle the range of loss as well as the magnitude of the loss. Therefore, receivers with both large dynamic range and good sensitivity are required for long link lengths.

Connector losses at the transmitter and receiver are already included in the transmitter and receiver specifications. However, connector losses due to connections through bulkhead adaptors need to be determined. There should be a minimum and a maximum loss specified for the bulkhead connection. Hewlett-Packard specifies the loss of a bulkhead connection as a minimum of 0.7 dB and a maximum of 2.8 dB. As you increase the number of bulkhead connections, the range of loss increases as does the magnitude of the losses.

It is important to remember that the range of loss is just as important as the magnitude of the loss.

The total loss in a system is the sum of the individual losses due to attenuation and connectors. It is important to calculate both the minimum and the maximum losses of the system due to attenuation and connectors. A wide range of losses results in a wide range of input power at the receiver. This places greater requirements on the dynamic range of the receiver.

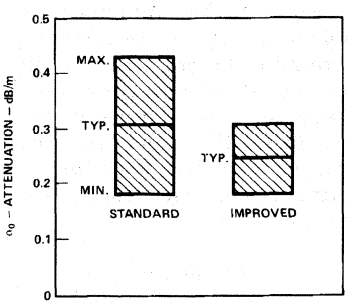


Figure 12. Cable Attenuation.

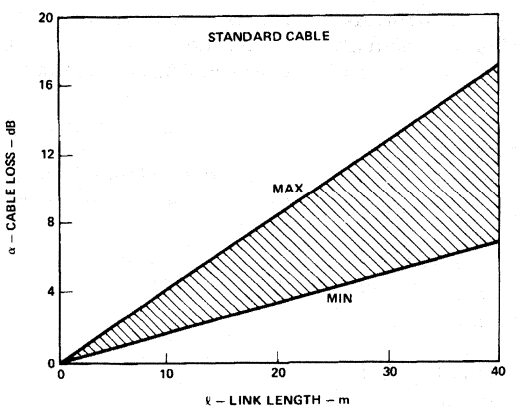


Figure 13. Possible Range of Cable Loss vs. Cable Length.

Table 2. Example Loss Calculation

Attenuation Loss - dB		
	min.	max.
loss/meter	0.19	0.43
total	0.95	2.15
Bulkhead Connection Loss - dB		
	min.	max.
loss/bulkhead	0.7	2.8
total	1.4	5.6
System Loss - dB		
	min.	max.
total	2.35	7.75
	$=\alpha_{min}$	$=\alpha_{max}$

Table 2 shows the results of calculating the minimum and maximum losses for a 5 m link of standard cable with two bulkhead connections.

You can see that even for this relatively short link, there is over 5 dB difference between the minimum and maximum losses.

Link Design

The fundamental requirement in the design of a fiber-optic link is to ensure that the receiver gets the proper amount of light. As mentioned earlier, this actually places three requirements on the design:

For a high output voltage,

1. input power must be LESS than the maximum $P_{R(H)}$.

For a low output voltage,

2. input power must be GREATER than the minimum $P_{R(L)}$,

3. input power must be LESS than the maximum $P_{R(L)}$.

The first requirement is usually easy to meet: just ensure that the LED drive current is below about 20 μA, or that the forward voltage drop of the LED is less than about 1.0 V.

The second requirement defines the underdrive, or sensitivity, limit of the receiver. You must ensure that the receiver has enough input power. This requires that the minimum transmitter coupled power minus the maximum system losses be GREATER than the minimum $P_{R(L)}$. In equation form:

$$P_{Tmin} - \alpha_{max} > P_{R(L)min}.$$

You should start your design with the transmitter drive current at the maximum recommended current of 60 mA, and decrease it later on in the design if required. Remember to use the maximum link length when calculating the maximum system losses.

Another way of looking at the same requirement is in terms of an optical power budget (OPB). The optical power budget is how much optical power you can "spend" on losses in your system; it is defined as the difference between the minimum transmitted power and the minimum $P_{R(L)}$:

$$OPB = P_{Tmin} - P_{R(L)min}$$

Your total system losses must then be less than the optical power budget:

$$\alpha_{max} < OPB.$$

You may want to include a safety or power margin (PM) in your design. This margin is included to account for any decreases in the received optical power over the lifetime of the link. The received power may decrease over time due to increases in attenuation of the fiber, due to optical contamination of the connectors or active components, or due to a drop in the output power of the transmitter. If you include a power margin in your calculations, your system losses plus the power margin must be less than the optical power budget:

$$\alpha_{max} + PM < OPB.$$

A typical power margin is around 3 dB; choose a larger margin for harsh environments and a smaller margin for more benign environments. For example, if your maximum system losses are 12 dB and you want a power margin of 3 dB, then you must have an optical power budget of greater than 15 dB. As another example, if you have an optical power budget of 10 dB and you want a power margin of 3 dB, then your maximum system losses must be less than 7 dB.

To calculate the minimum allowable transmitter drive current, determine if there is any budget left over after subtracting system losses and the power margin. This is the amount that you can decrease the transmitter output power by decreasing the drive current:

$$\text{Remaining budget} = OPB - (\alpha_{max} + PM).$$

As an example, let's assume we have a 40 kBd 5 m link with standard cable, 2 bulkhead connections, and a power margin of 3 dB. We have already calculated the maximum losses for this system:

Maximum system losses:
α_{max} = 7.75 dB.

With a power margin of 3 dB, the optical power budget, OPB, must be greater than 7.75 dB + 3 dB = 10.75 dB, or

10.75 dB < OPB.

The 40 kBd transmitter can couple a minimum power of -13.6 dBm over temperature at 60 mA, and the receiver has a minimum $P_{R(L)}$ of -39 dBm. Therefore the optical power budget is given by:

OPB = -13.6 dBm - (-39 dBm) = 25.4 dB.

There is plenty of power budget to cover the system losses and power margin. To determine the minimum transmitter drive current, determine the remaining budget:

Remaining budget = 25.4 dB - (7.75 dB + 3 dB) = 14.65 dB.

This is how much we can decrease the transmitter output power and still guarantee that we will not underdrive the receiver. According to Figure 8, decreasing the drive current to about 4 mA will drop the output power by about the right amount. You can see why we call the 40 kBd link a "low-current" link!

So far, we've covered the first two requirements for designing a fiber-optic link. The third requirement defines the overdrive limit of the receiver; you must ensure that the receiver does not get too much power. In other words, the maximum possible received optical power, which equals the maximum transmitter power minus the minimum system losses, must be LESS than the maximum $P_{R(L)}$. In equation form:

$P_{Tmax} - \alpha_{min} < P_{R(L)max}$

Remember to use the shortest link length for calculating the minimum system losses.

If the received optical power is too high, then the transmitter coupled power must be decreased by decreasing the drive current. To calculate the maximum allowable transmitter drive current, first determine how far above $P_{R(L)max}$ the received power is, and then decrease the transmitter output power by that much:

Amount of decrease =
$(P_{Tmax} - \alpha_{min}) - P_{R(L)max}$

Let's use our previous example to illustrate. We have already calculated the minimum system losses:

Minimum system losses:
α_{min} = 2.35 dB.

The 40 kBd transmitter can couple a maximum power of -4.5 dBm at 60 mA, and the receivcr has a maximum $P_{R(L)}$ of -13.7 dBm. First determine the maximum possible received power:

-4.5 dBm - 2.35 dB = -6.85 dBm.

This is above the overdrive limit, $P_{R(L)max}$, of -13.7 dBm. Therefore, we must decrease the transmitter drive current to decrease the transmitter coupled power:

Amount of decrease =
-6.85 dBm - (13.7 dBm)
= 6.85 dB.

According to Figure 8, decreasing the transmitter drive current to about 14 mA will ensure that the receiver is not overdriven. For the example link discussed above, the minimum transmitter drive current is about 4 mA, and the maximum current is about 14 mA. Choosing a current between the minimum and maximum currents will provide additional safety or power margin.

After you have determined the minimum transmitter drive current from underdrive considerations and the maximum current from overdrive considerations, it might turn out that the maximum is less than the minimum (this did not happen, however, in the above examples). This occurs when the maximum possible range, or variation, of received power is greater than the dynamic range of the receiver. If this does occur, you can reduce the possible range of received power by doing any or all of the following:

1. Use improved cable. Improved cable has a smaller range of attenuation than standard cable and will therefore reduce the possible range of loss in the link.

2. Reduce the maximum link length.

3. Restrict the allowable variation in the length of the link. A link that is designed to operate from 0 m to 10 m will have

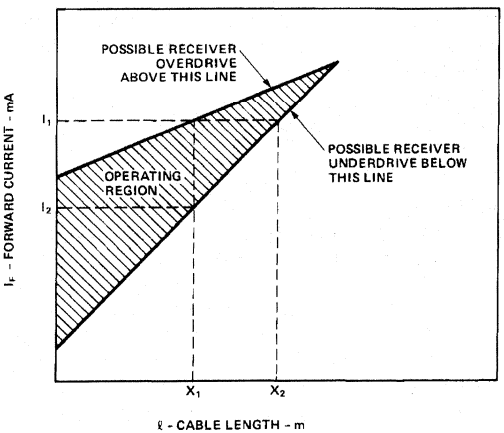


Figure 14. Link Operating Diagram.

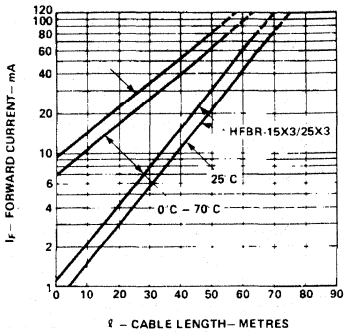


Figure 15. 40 kBd Link Operating Diagram.

more possible variation in the received power than a link designed to operate from 8 m to 10 m (the above examples dealt with a fixed link length of 5 m).

4. Reduce the number of bulkhead connections. There is a possible connection loss variation of (2.8 dB - 0.7dB) = 2.1 dB per bulkhead connection.

Link Operating Diagram

A link operating diagram, shown in Figure 14, can simplify the design of a simple point-to-point fiber-optic link, defined as a link with no bulkhead connections and a single length of fiber between the transmitter and the receiver. It illustrates the allowable combinations of link length and transmitter drive current.

The two primary features of the diagram are the overdrive and underdrive lines. If you operate a link in the region above the overdrive line (i.e., a combination of transmitter drive current and link length that lies above the overdrive line), then it is possible that you might overdrive the receiver. Conversely, if you operate the link below the underdrive line, then it is possible that you might underdrive the receiver. Therefore, the region between the two lines defines the valid operating region.

As shown in Figure 14, operating the transmitter at a fixed drive current of I_1 allows link lengths from X_1 to X_2. For a fixed link length of X_1, a drive current of between I_1 and I_2 is required for proper operation.

As an example, Figure 15 shows the link operating diagram for the 40 kBd link with standard cable. Operating the transmitter at 40 mA allows link lengths from about 40 m to 55 m. Or, for a fixed link length of 20 m, a transmitter drive current between about 4 mA and 17 mA is required.

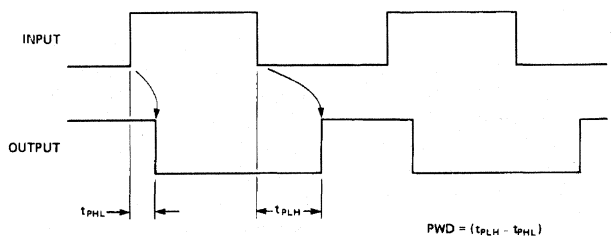


Figure 16. Pulse-Width Distortion.

Pulse-Width Distortion

Pulse-width distortion (PWD) is often the limiting factor that determines the maximum data rate of a fiber-optic link. Pulse-width distortion is caused by unequal propagation delays and is defined as the difference between the propagation delays, as shown in Figure 16:

$$PWD = t_{PLH} - t_{PHL}$$

The term t_{PHL} refers to the propagation delay from the input to the high-to-low transition of the OUTPUT, as shown in Figure 16. Pulse-width distortion lengthens or shortens the duration of transmitted pulses, depending on the polarity of the pulse.

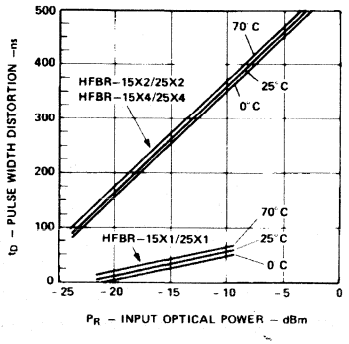


Figure 17. Typical Pulse-Width Distortion vs. Input Power of 5 MBd and 1 MBd Receivers.

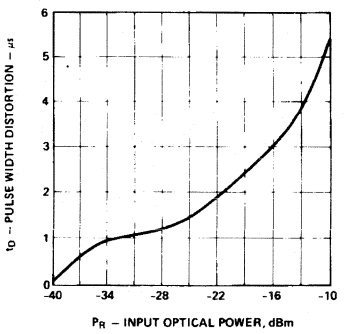


Figure 18. Typical Pulse-Width Distortion vs. Input Power of 40 kBd Receiver.

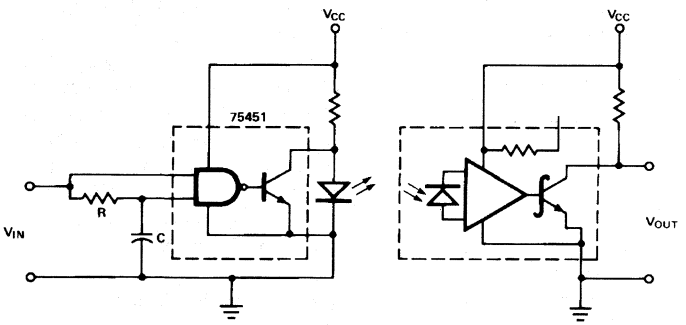


Figure 19. Pre-Correction of PWD.

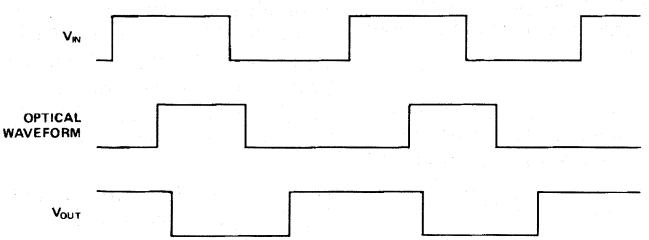


Figure 20. Pre-Correction Timing Diagrams.

Figure 17 shows the pulse-width distortion specifications for the 1 MBd and 5 MBd Versatile Links. Note that the 5 MBd link has significantly less distortion than the 1 MBd link and much less variation in distortion over the full input optical power range. Figure 18 shows the distortion for the 40 kBd link. Notice that the PWD is always positive for all three receiver types (i.e., t_{PLH} is always longer than t_{PHL}). We can utilize this fact to correct or compensate for the PWD by selectively delaying one of the transmitted edges.

Figure 19 illustrates how to implement a "pre-correction" circuit, which corrects for distortion at the transmitter. The circuit is almost the same as our recommended 5 Mbd transmitter circuit, except for the RC network at the input of the gate. The RC network delays the turn-on of the LED, but not the turn-off. Both inputs must be high for the LED to turn on; the RC network delays one of the inputs and, therefore, delays the turn-on of the LED. However, only one of the inputs needs to go low for the LED to turn off. Figure 20 is a timing diagram which illustrates the operation of the correction circuit. Note how the turn-on of the LED is delayed and how the distortion is reduced. It is possible to calculate the required values for R and C to achieve the desired amount of correction; however, it is usually just as easy to experimentally determine their values. For the 5 MBd link, start with R = 100 ohms and C = 390 pF and adjust the values to obtain the desired amount of correction.

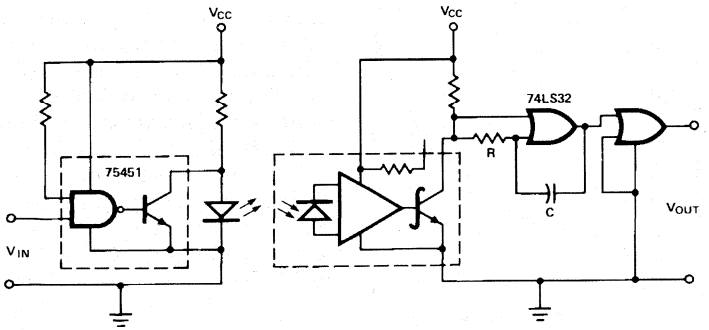


Figure 21. Post-Correction of PWD.

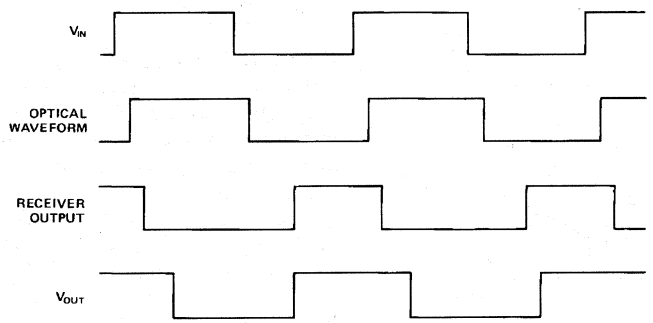


Figure 22. Post-Correction Timing Diagrams.

It is also possible to correct the distortion at the receiver using "post-correction". Figure 21 shows a post-correction circuit. It works on the same principle of delaying one of the edges. Again, it is similar to the recommended circuit, except for the addition of a delay circuit on the output of the receiver. The RC network delays the falling edge of the receiver output. Both of the inputs to the OR gate must go low for the output to go low; the RC network delays one of the inputs and, therefore, delays the falling edge. Connecting the capacitor to the output provides positive feedback to ensure rapid switching of the output. Only one of the OR gate inputs needs to go high for the output to go high; therefore, there is no delay of the rising edge.

Figure 22 is a timing diagram illustrating the operation of the circuit. Notice the distortion of the receiver output and how the post-correction circuit delays the falling edge to reduce the amount of distortion. Again, it is easiest to experimentally determine the values of R and C to achieve the desired amount of correction. For the 5 MBd link, start with R = 330 ohms and C = 39 pF and adjust the values to get the desired amount of correction.

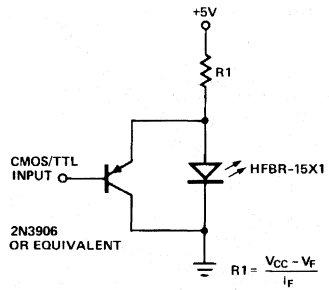


Figure 23. Simple 5 MBd PNP Transmitter Circuit.

Although it is possible to use pre-correction and post-correction in the same link, there is no need to incorporate both, and we recommend using only one type of correction. The choice of which circuit to use depends on external system constraints, such as a limit on the total number of system components, or other constraints on the transmitter or receiver circuitry.

Additional Circuit Recommendations

This section presents several additional circuits that can be used with the Versatile Link. The transmitter circuits discussed below should be used only with the 5 MBd and 40 kBd links; the 1 MBd link requires the transmitter circuit shown in Figure 9 for proper operation.

The first circuit, shown in Figure 23, is a simple PNP transmitter circuit. The primary feature of the circuit is its simplicity: only two components are required other than the transmitter. It uses an inexpensive PNP transistor in a shunt drive configuration; when the input (i.e. the base of the transistor) is high, the transistor is cut off and the LED is on.

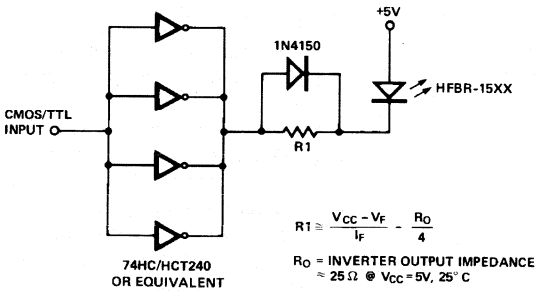


Figure 24. Low-Current CMOS Transmitter Circuit.

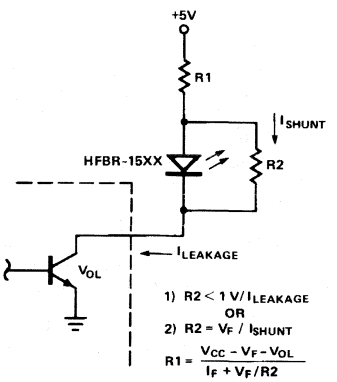


Figure 25. LED Shunt Resistor for Open Collector Drive.

When the input is low, the transistor turns on and shunts current away from the LED, turning the LED off.

Thc circuit is very fast for several reasons. The transistor allernates between the cutoff and active regions of operation and, therefore, never saturates. The circuit presents a very low impedance during turn-off of the LED, which helps to turn off the LED more rapidly. And finally, the emitter base junction voltage of the transistor "pre-charges" the junction capacitance of the LED to about 700 mV, which helps to turn on the LED more rapidly. The "pre-charge" eliminates the time that would otherwise be required to charge the LED capacitance from 0 V to the pre-charge voltage of 700 mV during turn-on of the LED.

The circuit has a high input impedance because the input source need supply only the base current of the transistor; the large LED drive current is handled by the transistor. This allows the circuit to be driven directly from low-current outputs, such as CMOS. Choose the value of R1 according to the equation in Figure 23.

Figure 24 is the schematic of a low-current CMOS-compatible transmitter circuit. The circuit operation is straightforward. The outputs of four CMOS buffers are arranged in parallel to ensure adequate drive capability for large LED currents. For smaller LED currents, fewer buffers can be used. The circuit has a very high input impedance, is CMOS compatible, and draws essentially no quiescent current when the LED is off. The diode helps to speed up the circuit. The capacitance of the diode provides additional current during the turn-on transition to help turn on the LED more rapidly. It also provides a low impedance during turn-off, which helps to turn the LED off more quickly. Choose the value of R1 according to the equation in Figure 24. If fewer buffers are used, divide R_O by the number of buffers in the circuit, instead of the four shown in the figure.

If an open-collector output is used to drive the LED, a shunt resistor in parallel with the LED, shown in Figure 25, can improve the performance of the transmitter. The shunt resistor R2 serves two purposes:

1. It shunts any output leakage current around the LED, ensuring that the LED is off when it is supposed to be off. The leakage current will cause a voltage drop across R2; as long as the voltage drop is less than about 1 V, the LED will not turn on. Equation No. 1 in the figure can be used to determine the value of R2 in this case.

2. It also helps turn the LED off more quickly by discharging the stored charge in the junction of the LED. Smaller resistors will shunt more current and will turn the LED off more rapidly, at the expense of more overall drive current. Equation No. 2 in the figure can be used to determine the value of R2 in this case.

In either case, select R1 according to the equation in Figure 25.

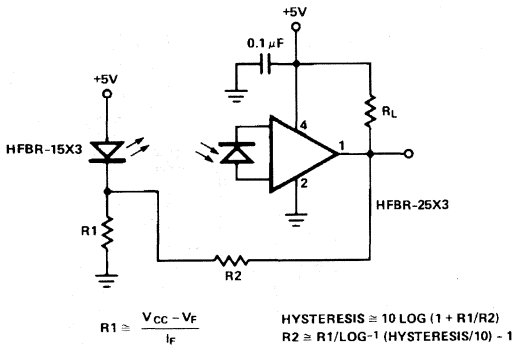


Figure 26. Photo Interrupter Hysteresis Circuit.

The final application circuit is used in photo-interrupter applications. A photo-interrupter is comprised of a transmitter and a receiver connected by two lengths of fiber. The ends of the fibers are not connected directly together, but have a small separation between them. This allows small objects to pass between them and interrupt the light from the transmitter. The Versatile Link data sheet discusses how to use Versatile Link components in photo-interrupter applications. The circuit shown in Figure 26 illustrates how to add hysteresis to the recommended photo-interrupter circuit shown in the data sheet. Hysteresis may be required because it is possible that the received optical power may occasionally be at the threshold of the receiver. This could cause multiple transitions on the output and lead to improper circuit operation. It is common in this application for the transmitter and the receiver to be located next to each other. This allows a small amount of positive feedback to be applied from the receiver to the transmitter, resulting in hysteresis.

The hysteresis will rapidly switch the output and eliminate the problem mentioned above. The amount of hysteresis is determined by the values of R1 and R2. Choose R1 to achieve the desired drive current according to the equation in Figure 26. The amount of hysteresis, expressed in dB, is given approximately by the following equation:

Hysteresis = 10 log (1 + R1/R2).

Solving for the value of R2 yields:

R2 = R1/ [log-1 (Hysteresis/10)-1]

Values of hysteresis from 0.25 to 1 dB should be sufficient for most applications. As an example, for hysteresis of 0.25 dB, R2 should be about 17 times the value of R1.

For additional information regarding the photo-interrupter application, please refer to the Versatile Link data sheet.

Summary

The Versatile Link low-cost fiber optic components were designed and specified for easy design. Guaranterd electrical and optical parameters ensure reliable system performance. The wide variety of package configurations and connector types allow maximum flexibility to meet application requirements. The Hewlett-Packard HFBR-0501 series of fiber optic components offer guaranteed performance, quality, and reliability.

For more information, please call your local Hewlett-Packard Components Sales Office or authorized HP Components Distributor.

Appendix

We quantify the amount of light by measuring its power. Optical power is measured in watts or, more commonly in fiber optics, in microwatts (μW). Optical power is also commonly expressed in dBm. dBm is a logarithmic measure of power relative to 1 milliwatt (mW), as explained below.

The ratio of two powers, P1 and P2, can be expressed in dB as follows:

dB = 10 log (P1/P2).

A positive number indicates that P1 is greater than P2, and a negative number indicates that P1 is less than P2. Remember, dB is a relative measure of two powers.

The ratio of a power, P1, to 1 mW is expressed in dBm as follows:

dBm = 10 log (P1/1 mW) or
10 log (P1/1000 μW).

Negative numbers do not indicate negative power, only power less than 1 mW. Remember, dBm is an absolute measure of power because it references the measured power to 1 mW.

To convert from dBm to mW or μW, use the following equations:

$mW = \log^{-1}(dBm/10)$, or ,
$\mu W = 1000 \log^{-1}(dBm/10)$.

As an example, to convert 150 μW to dBm:

$$dBm = 10 \log^{-1}(150\ \mu W / 1000\ \mu W) = -8.24.$$

To convert -24 dBm to μW:

$$\mu W = 1000 \log^{-1}(-24/10) = 3.98.$$

If optical power is lost in the fiber, the loss can be expressed in dB as the ratio of output power to input power as follows:

$loss\ (dB) = 10 \log (P_{out} P_{in})$.

Expressing power loss in dB allows the different losses in a system to be added together to determine the total loss. Therefore, the output power can be determined simply by subtracting the total system losses, expressed in dB, from the input power, expressed in dBm:

$P_{out}\ (dBm) = P_{in}\ (dBm)$ - losses (dB).

As an example, if the input power to the system is -10 dBm and the total system losses are 12 dB, then the output power is:

$$P_{out}\ (dBm) = -10\ dBm - 12\ dB = -22\ dBm.$$

HEWLETT® PACKARD

Complete Fiber-Optic Solutions for IEEE 802.3 FOIRL, 10Base-FB, and 10Base-FL

Application Note 1038

Introduction

Hewlett-Packard's HFBR-0400 fiber-optic components are widely used in Ethernet LAN systems. These 820 nm wavelength components were first used in 802.3 FOIRL applications. The same low-cost HFBR-0400 components have subsequently been used in systems which comply with the IEEE 802.3 10Base-FB, and 10Base-FL standards. Several integrated circuits are now available which make it easier to use HFBR-0400 components in fiber-optic Ethernet applications. This Application Note shows how easy it is to build high-performance Ethernet transceivers using inexpensive, off-the-shelf, integrated circuits and HP's low-cost HFBR-14X4 and HFBR-24X6 short-wavelength fiber-optic components.

Two categories of fiber-optic Ethernet applications will be discussed in this Application Note. The first category addresses fiber-optic transmitters and receivers suited for use in LAN equipment such as hubs, bridges, routers, and repeaters. The second category addresses Medium Attachment Unit (MAU) applications that convert standard Attachment Unit Interface (AUI) Ethernet connections to optical fiber. The MAU circuits recommended in this Application Note use the HFBR-4663 transceiver IC with low-cost HFBR-0400 fiber-optic components. The HFBR-4663 allows fiber-optic MAU transceivers which meet IEEE standards to be implemented with a single integrated circuit.

IEEE 802.3 System Specifications

Tables 1 and 2 provide a brief listing of some key parameters specified in the 802.3 FOIRL, 10Base-FB, and 10Base-FL standards.

Capabilities of HFBR-0400 Components

The transmitter and receiver circuits recommended in this Application Note characteristically exceed the limits called for in IEEE 802.3 by a comfortable margin. The optical power launched into 62.5/125 μm fiber by the HFBR-14X4 LED is typically -12 dBm peak at a dc forward current of 60 mA. When Manchester encoded data with a 50% duty factor is applied to the LED transmitter the HFBR-14X4 LED can typically launch -15 dBm average into the core of a 1m length of 62.5/125 μm fiber with a numerical-aperture of 0.275. This 3 dB difference between peak and average power is due to the 50% duty factor of Manchester data and the averaging response of most optical-power meters. The HFBR-24X6 is a simple hybrid component that contains a silicon PIN detector and a transimpedance amplifier. The HFBR-24X6 can be combined with simple inexpensive integrated circuits to build digital receivers that have an optical dynamic range and sensitivity greater than called for in the IEEE 802.3 specifications.

Recommended Transmitters for Hub, Bridge, Router, and Repeater Applications.

Two different techniques have commonly been used to drive the HFBR-1414 LED in Ethernet applications. Both of the LED drivers recommended in this Application Note will address the requirements called out in the IEEE 802.3 LAN specifications. The HFBR-14X4 LED has typical rise/fall times of less than 4 ns when used in the circuits recommended in Figure 1 or Figure 2. Transmitter jitter and

Table 1. Key IEEE 802.3 LED Transmitter Specifications

Parameter	Symbol	802.3 FOIRL Limits	802.3 10Base-FB Limits	802.3 10Base-FL Limits	Units
Launched Optical Power Over Life	P_T on	-12 to -20	-12 to -20	-12 to -20	dBm avg
Extinction	P_T off	13 dB less than P_T on	13 dB less than P_T on	13 dB less than P_T on	–
Maximum Optical Rise Time	t_r	10	10	10	ns
Maximum Optical Fall Time	t_f	10	10	10	ns
Maximum Difference Between Optical Rise & Fall Times	$\lvert t_r - t_f \rvert$	3	3	3	ns
Maximum Jitter at Optical Output	–	±2	±2	±4	ns
Maximum Duty Cycle Distortion	–	Not Specified	±2.5	±2.5	ns
Min. Eye Opening	–	46	41	37	ns

Table 2. Key IEEE 802.3 Fiber-Optic Link Specifications

Receiver Input Conditions			Required Link Performance		
IEEE 802.3 STANDARD	**Maximum Rise/Fall Time of Received Optical Pulse (ns)**	**Received Optical Power (dBm avg)**	**802.3 FOIRL Maximum Jitter (ns)**	**802.3 10Base-FB Maximum Jitter (ns)**	**802.3 10Base-FL Maximum Jitter (ns)**
FOIRL 10Base-FB 10Base-FL	10 with 1 m of 62.5/125 µm fiber	-12 max.	±6	±6.5	±15
10Base-FB 10Base-FL	31.5 with 2 km of 62.5/125 µm fiber	-32.5 min.	–	±6.5	±15
FOIRL	Not Specified	-30.0 min.	±6	–	–
IEEE 802.3 STANDARD	**Maximum Rise/Fall Time of Received Optical Pulse (ns)**	**Received Optical Power (dBm avg)**	**802.3 FOIRL Minimum Eye Opening (ns)**	**802.3 10Base-FB Minimum Eye Opening (ns)**	**802.3 10Base-FL Minimum Eye Opening (ns)**
FOIRL 10Base-FB 10Base-FL	10 with 1m of 62.5/125 µm fiber	-12 max.	38	37	20
10Base-FB 10Base-FL	31.5 with 2 km of 62.5/125 µm fiber	-32.5 min.	–	37	20
FOIRL	Not Specified	-30.0 min.	38	–	–

duty-cycle distortion are normally less than 1 ns when using either of the recommended LED drivers. The cost complexity and performance tradeoffs associated with these two different LED drivers will now be discussed in greater detail.

The LED forward current (I_F) supplied by the simple voltage-source driver shown in Figure 1 will change with variations in V_{CC} and LED forward voltage (V_F). The tolerance of resistors R7, R8, and R9 will also effect the magnitude of I_F. Deviations in I_F due to the 74ACT11000 nand-gate voltage-source are insignificant. The typical output impedance of the three parallel connected nand gates is only 1 ohm and the external resistors R7 and R8 which limit the LED current total to 66 ohms. This large difference between the source-impedance of the nand-gate voltage-source and the sum of R7 and R8 makes it improbable that changes in LED I_F will result due to process variations in the 74ACT11000.

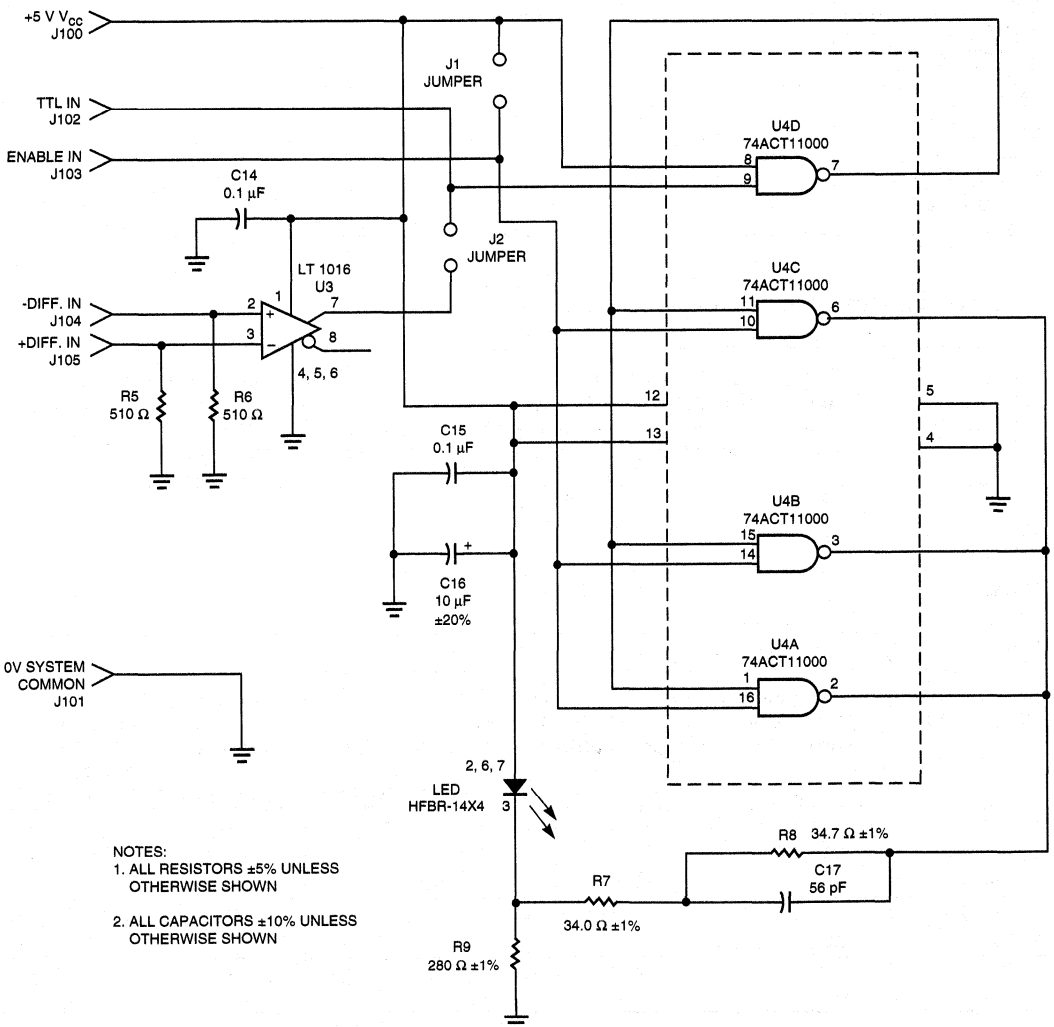


Figure 1. Voltage Source Transmitter for Hub, Bridge, Router, and Repeater Applications.

A voltage-source drive-circuit suited for 802.3 applications is shown in Figure 1. This simple drive-circuit has an LED forward current (I_F) that varies from the nominal 60 mA peak value desired for fiber-optic Ethernet applications. This variation in I_F causes a small decrease in the power coupled into 62.5/125 µm fiber. When using the circuit shown in Figure 1, the launched power will be 1 dB less than specified in the HFBR-14X4 data sheet, under worst-case conditions. The worst-case occurs when V_{CC} is low and LED forward voltage (V_F) and resistor tolerance are high. The HFBR-1414 data sheet specifies launched power at I_F = 60 mA, and assumes that LED forward current is constant. Normal tolerances of the voltage-source LED driver will cause variations in LED I_F that lower the minimum power launched into the fiber. This reduction in launched power relative to the P_{t62} specification given in the HFBR-14X4 data sheet is expected. Voltage-source drive-circuit tolerances will lower LED forward current and the amount of light coupled into the fiber-optic cable is directly proportional to I_F.

For applications that require tighter control over LED I_F, and less variation in launched optical power, the current-source transmitter shown in Figure 2 is recommended. Figure 2 shows an LED drive-circuit which provides a forward current that is independent of V_{CC} and LED forward voltage. The LED current provided by this driver is primarily determined by the tolerance of the bandgap reference U3, and the tolerance of resistors R5 and R6. The -2 mV/°C temperature coefficient of the base-emitter junction of Q3 or Q4 increases the voltage applied to R5 and R6 as ambient temperature rises. The temperature coefficient of NPN transistor base-emitter voltage is thus used to increase the magnitude of the current applied to the LED as temperature rises. This technique prevents LED light output from decreasing as temperature rises by compensating for changes in the LED quantum efficiency.

Either of the LED drivers shown in this Application Note will address the requirements called out in the IEEE 802.3 specifications. The design rules for the LED driver shown in Figure 1 are given in Equation 1 and the design rules for the LED driver shown in Figure 2 are provided in Equation 2.

When choosing the driver the designer should consider the fol-

Equation 1
Design rules for voltage source LED driver circuits.

N = Number of gates connected in parallel.
B = Empirically determined constant for optimum relationship between prebias and LED forward current.

$$R9 = \frac{(V_{CC} - V_F)(1 + B)}{I_{F_{ON}}}$$

$$R8 = \frac{R9}{2B}$$

$$R7 = \frac{R9}{2B} - \frac{3}{N}$$

$$C = \frac{2.0 \times 10^{-9}}{R8}$$

Recommend B = 3.97

Equation 2
Design rules for temperature compensated current source LED driver circuit.

$$I_F = \frac{\Delta V_{U3} - V_{BE_{Q3}}}{R5} + \frac{\Delta V_{U3} - V_{BE_{Q4}}}{R6}$$

$$I_F = \frac{1.24 - 0.7}{R5} + \frac{1.24 - 0.7}{R6}$$

$$I_F = (1.24 - 0.7)\left(\frac{1}{R5} + \frac{1}{R6}\right)$$

$$R3 = \frac{V_{OH} - V_{OL}}{I_F} = \frac{5V}{I_F}$$

$$C4 = \frac{2.0\ ns}{R3}$$

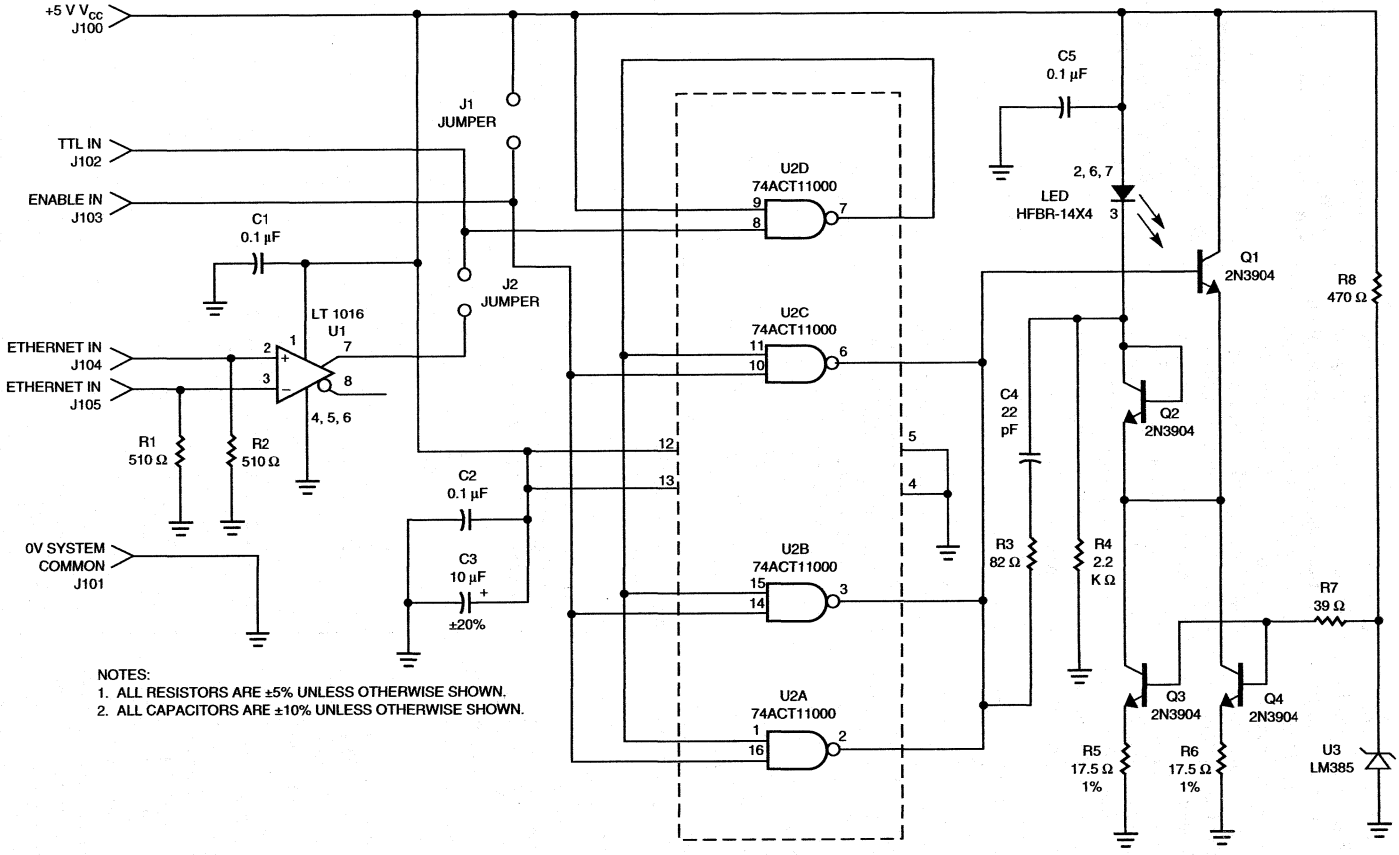


Figure 2. Current Source Transmitter for Hub, Bridge, Router, and Repeater Applications.

lowing factors. The LED driver shown in Figure 1 is simple but has a larger variation in the power coupled from the LED to the fiber. The circuit shown in Figure 2 is more complex, but offers tighter control over variations in launched optical power. System designers are encouraged to choose the LED driver which best meets their requirements. If cost and board space are of greater concern than variations in launched optical power then the voltage-source transmitter circuit shown in Figure 1 makes the most sense. If the designer desires to maximize the optical power budget of the fiber-optic link then the transmitter circuit shown in Figure 2 is a better choice.

Recommended Receiver for Hub, Bridge, Router, and Repeater Applications.

A simple receiver which complies with IEEE 802.3 specifications is shown in Figure 3. The post-amplifier comparator function used to convert the analog output of the HFBR-24X6 to digital data is generally referred to as a quantizer. The ML-4622 quantizer shown in Figure 3 also contains a link-monitor which inhibits the data output when the optical power drops below the minimum level needed to ensure that the receiver's output is error free.

The receiver recommended in Figure 3 has a typical sensitivity of -36 dBm average at a Bit-Error-Rate (BER) of $1x10^{-10}$ when receiving 20 MBd Manchester encoded data. This receiver performance was measured using 2 km of 62.5/125 µm fiber with the BER tester's clock centered in the middle of the received 20 MBd Manchester symbols. The link-monitor function must be disabled by grounding pin 15 of the ML-4622 quantizer in order to measure the ultimate sensitivity of the receiver. In normal operating mode the ML-4622's link monitor disables the data output of the fiber-optic receiver before the probability of an error exceeds 1 in 10^{10} bits.

When receiving a repetitive 20 MBd D2D2 hexadecimal word the total peak-to-peak jitter at the data output of the circuit shown in Figure 3 is typically

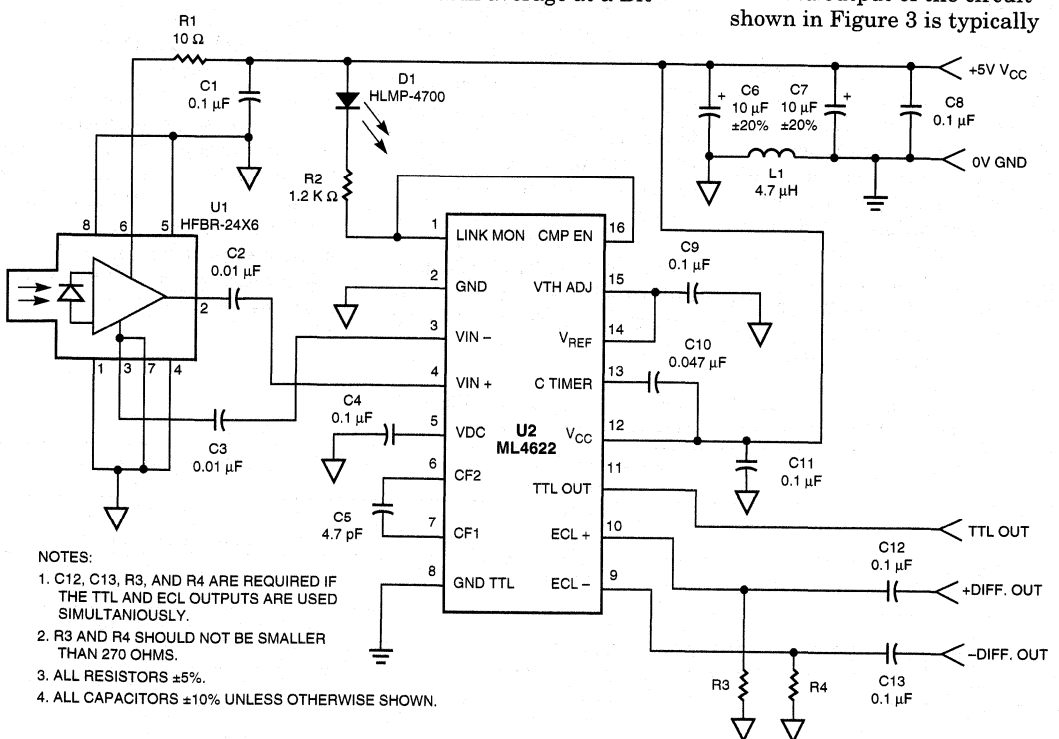


Figure 3. Receiver for Hub, Bridge, Router, and Repeater Applications.

less than 10 ns. A D2D2 Hexadecimal pattern was used to test the complete fiber-optic link because it emulates the worst stress possible with Manchester encoding. The excellent performance of the circuits recommended in this Application Note allows low jitter to be achieved when data is transmitted over a 2 km segment of 62.5/125 µm fiber with a received optical power of -32.5 dBm average. The low jitter attained at the receiver's output corresponds to a 40 ns clear eye-opening between the edges of the data symbols. A wide eye-opening is desirable because this minimizes the accumulation of jitter when active star hubs are cascaded.

Demo Kit For Fiber-Ethernet

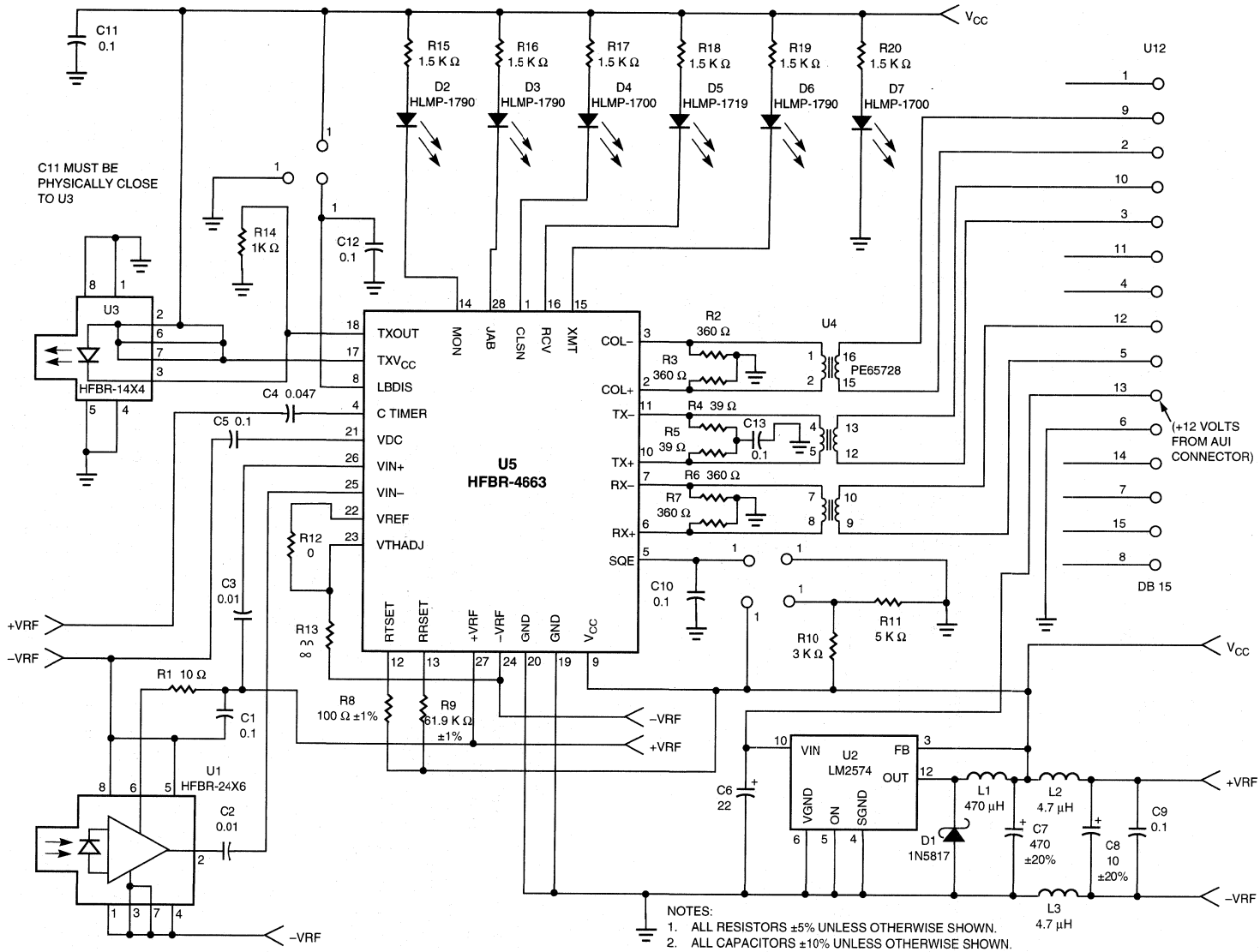
The transceiver circuits shown in Figures 1, 2, and 3 are suited for use in fiber-optic hubs, bridges, routers, and repeaters. This recommended transceiver can easily be compared to the IEEE specifications listed in Tables 1 and 2 by ordering the HFBR-0414 demo kit. The HFBR-0414 kit contains a small 2 3/4 by 1 3/4 inch through-hole printed circuit board and all of the active devices needed to build the circuits shown in Figures 1 and 3. This inexpensive kit can be completed using readily-available passive components such as radial-lead monolithic ceramic capacitors, radial-lead epoxy-dipped tantalum capacitors, and axial-lead 1/4 W resistors. The passive components needed to assemble this fiber-optic demo are available in most engineering stock rooms. The HFBR-0414 demo kit minimizes the engineering cost of building the fiber-optic transceiver recommended in this Application Note, reduces time-to-market by minimizing the effort required to construct working prototypes, and enables designers to quickly determine that Hewlett-Packard's HFBR-0400 fiber-optic components can meet Ethernet LAN requirements. The measured performance of the circuits used in the HFBR-0414 demo can be found in Tables 3 and 4. Table 3 shows the measured performance of the transmitter recommended in Figure 1. Table 4 shows the measured performance of an entire fiber-optic link which uses the circuits recommended in Figures 1 and 3.

Recommended Circuit for Ethernet Fiber-Optic MAU Applications

Circuits recommended for use in Medium-Attachment-Unit (MAU) applications will now be discussed. Figure 4 shows a MAU transceiver using the HFBR-4663 single-chip transceiver IC. The HFBR-4663 provides all of the circuit elements needed to build a complete fiber-optic transmitter and receiver which complies with the 802.3 10Base-FL standards. The HFBR-4663 provides every function needed to make HFBR-0400 fiber-optic components compatible with a standard Ethernet AU interface. This single IC also provides all necessary network and status indicators needed by a fiber-optic MAU. The HFBR-4663 replaces two-chip solutions that were formerly needed to construct fiber-optic MAUs. A highly efficient switching power-supply that allows the MAU transceiver to operate from the +12 V power available at the AUI is also included in Figure 4. The measured performance of the transmitter portion of the MAU is shown in Table 5.

Table 3. Measured Performance of the Transmitter shown in Figure 1
Mean Performance of Five Transmitters Tested at Room Temperature

Parameter	Measured Typical Performance	Test Conditions
P_t On	-12.2 dBm pk.	Logic "0" at Transmitter TTL Input, I_f dc = 60 mA
P_t Off	-82.2 dBm pk.	Logic "1" at Transmitter TTL In
LED t_r	1.30 ns	1 MHz Square Wave Input
LED t_f	3.08 ns	1 MHz Square Wave Input
$\lvert t_r - t_f \rvert$	1.77 ns	1 MHz Square Wave Input
Tx jitter	0.763 ns pp	20 MBd D2D2 Hexadecimal Input



NOTES:
1. ALL RESISTORS ±5% UNLESS OTHERWISE SHOWN.
2. ALL CAPACITORS ±10% UNLESS OTHERWISE SHOWN.
3. THE HFBR-4663 DATA SHEET (PUBLICATION #5091-7391E 4/93) CONTAINS ERRORS THAT HAVE SUBSEQUENTLY BEEN CORRECTED IN THIS SCHEMATIC.
4. ALL CAPACITORS ARE IN µF.

Figure 4. Ethernet Fiber-Optic MAU Transceiver.

Table 4. Measured Performance of the Transceiver Shown in Figures 1 and 3

Mean Jitter of 5 Transceivers at Maximum Received Optical Power at Room Temperature

Parameter	Measured Typical Performance	Test Conditions
1 m Link Jitter at Rx ECL Output	3.07 ns pp	P_r = -11.4 dBm avg. with 20 MBd D2D2 Hexadecimal Data
1 m Link Jitter at Rx TTL Output	2.73 ns pp	P_r = -11.7 dBm avg. with 20 MBd D2D2 Hexadecimal Data

Mean Performance of 5 Receivers with 1 m of 62.5/125 mm fiber at Room Temperature

Parameter	Measured Typical Performance	Test Conditions
Mid Bit Rx Sensitivity	-36.5 dBm avg. at BER of $1x10^{-10}$	20 MBd D2D2 Hexadecimal Data
Link Monitor Assert Threshold	-35.4 dBm avg.	20 MBd D2D2 Hexadecimal Data

Mean Performance of 5 Links with 2 km of 62.5/125 mm Fiber at Room Temperature

Parameter	Measured Typical Performance	Test Conditions
Mid Bit Rx Sensitivity	-34.4 dBm avg. at BER of $1x10^{-10}$	20 MBd D2D2 Hexadecimal Data
Link Jitter at Rx ECL out	7.56 ns pp	P_r = -32.5 dBm avg. with 20 MBd D2D2 Hexadecimal Data
Link Jitter at Rx TTL out	7.03 ns pp	P_r = -32.5 dBm avg. with 20 MBd D2D2 Hexadecimal Data

The complete performance of a fiber-optic link which uses the HFBR-4663 is shown in Table 6. A long length of 62.5/125 µm fiber was used to slow the response time of the light pulses applied to the receiver. The test results shown in Table 6 were obtained by adjusting the length of the optical cable until the 90% to 10% fall-time of the light pulses exiting the fiber slowed to 31 ns. The 10% to 90% optical rise-time at the end of the 2.5 km fiber was 28 ns. The dispersion in the 2.5 km test fiber approaches the maximum 31.5 ns exit response time limit given in the IEEE 802.3 specifications. Table 6 shows how well the MAU transceiver recommended in this Application Note functions as fiber dispersion approaches the maximum limits allowed in the 10Base-FB and 10Base-FL specifications.

Table 7 shows how to select the functions listed in the HFBR-4663 data sheet. The MAU implemented with the HFBR-4663 can be connected directly to data terminal equipment (DTE) through an Ethernet adapter card with an AUI connection. The SQEN, JABD, LBDIS, and COLL functions should be enabled when the MAU shown in Figure 4 is connected to DTE. When the fiber-optic MAU is connected to an Ethernet hub the SQEN, LBDIS, and COLL functions should be disabled.

The HFBR-4663 data sheet can be used in conjunction with Table 7 to determine if functions should be enabled or disabled when evaluating fiber-optic MAU performance. When measuring the performance of the MAU it is usually necessary to disable JABD so that the fiber-optic transmitter will remain active for more than the 1024 byte limit allowed by Ethernet protocol. When JABD is disabled the rise/fall time, jitter, and launched power of the fiber-optic transmitter can easily be measured.

The JABD function should also be disabled when determining the bit error rate (BER) versus receiver sensitivity of MAUs constructed with the HFBR-4663. A D2D2 hexadecimal test pattern should be used to measure the BER of fiber-optic transceivers used in Ethernet

Table 5. Measured Performance of the MAU Transceiver Shown in Figure 4

Mean Performance of 14 Transmitters. All Tests done at Room Temperature.

Parameter	Measured Typical Performance	Test Conditions
P_t avg	-17.1 dBm avg.	5 MHz Square Wave Input I_f pk = 56 mA
LED t_r	2.88 ns	5 MHz Square Wave Input
LED t_f	3.34 ns	5 MHz Square Wave Input
$\lvert t_r - t_f \rvert$	0.46 ns	5 MHz Square Wave Input
Tx jitter	1.64 ns pp	20 MBd D2D2 Hexadecimal Input

Table 6. Typical Performance of a Complete Fiber-Optic Link Which Uses the MAU Transceiver Shown in Figure 4

**All results measured at a received power of -32.5 dBm avg. with fiber dispersion ≅ to max. limits called out in the IEEE 802.3 Specifications.

Eye Opening at the AUI output of the Receiver	V_{CC}	Temperature
32.8 ns	4.75 V	0°C
36.9 ns	5.00 V	0°C
32.2 ns	5.25 V	0°C
33.7 ns	4.75 V	25°C
36.7 ns	5.00 V	25°C
33.5 ns	5.25 V	25°C
37.2 ns	4.75 V	70°C
36.7 ns	5.00 V	70°C
36.7 ns	5.25 V	70°C

**Measured Results for a Solitary MAU Transceiver.

Table 6. HFBR-4663 Functions vs. Input Conditions

Input Conditions		Status of HFBR-4663 Functions			
HFBR-4663 Pin #	Voltage at Pin	SQEN	JABD	LBDIS	COLL
5	+5V	EN	EN	–	–
5	V_{CC}-2	DIS	DIS	–	–
5	0V GND	DIS	EN	–	–
8	+5V	–	–	DIS	DIS
8	0V GND	–	–	EN	EN

Notes:
1. DIS = Disabled
2. EN = Enabled

applications. The D2D2 test pattern is equivalent to the worst data induced stress that will occur when sending Manchester encoded data. The JABD function must be disabled when measuring BER because this test is certain to exceed the 1024 byte limit allowed for normal Ethernet traffic.

Printed Circuit Layout Techniques

The circuits given in this Application Note are recommended for use in any system which addresses the requirements specified in the IEEE 802.3 draft standard. HP encourages customers that want to use HFBR-0400 components in fiber-optic Ethernet applications to utilize these circuits in their products. The performance of the fiber-optic transceivers shown in this publication is partially dependent on the layout of the printed circuit board on which these recommended circuits are constructed.

The following simple rules should be followed if you desire to lay out a unique printed circuit (PC) board for the fiber-optic transceivers recommended in this publication.

1) Design the PC board with a ground plane. Use a ground and a power plane if possible. This minimizes the inductance of the ground and power leads connected to the transceiver.

2) Minimize the size of cuts or openings in the ground and power planes. This minimizes the parasitic inductance and improves the dampening of both the transmitter and receiver circuits.

3) The two circuit traces connected between the HFBR-24X6 and the differential input of the receiver's quantizer should be of equal length, and the components in both traces should be placed to achieve symmetry. This minimizes the cross-talk between the fiber-optic transmitter and receiver and improves the receiver's immunity to environmental noise.

4) Connections between the drive circuit and the LED should be of minimum length. This minimizes the noise emitted by the transmitter and improves the optical rise/fall time of the LED.

5) A large 10 µF electrolytic capacitor and a 0.1 µF monolithic-ceramic capacitor should be located as close to the signal source which drives (current-modulates) the LED. This minimizes the noise emitted by the transmitter and improves the optical response time of the LED.

6) The low-pass filters shown on the recommended schematics must be used to protect the fiber-optic receiver from noise that is present in the V_{CC} power supply.

7) If an inductor is used in series with the receiver's V_{CC} and V_{ee} connections the receiver should be referenced to V_{CC} and V_{ee} islands that are isolated from the remainder of the transceiver's power planes. A differential interface at the receiver's output is required if inductors are used in series with V_{CC} and V_{ee}. This dual-inductor filter is recommended if the receiver is connected to an AUI interface or operated in a noisy environment.

Printed Circuit Artwork

Variations in transceiver performance due to circuit layout can be avoided by using the artwork shown in Figures 5 through 7. Designers that would like to use the artwork provided by HP are encouraged to embed the PC artwork shown in this Application Note into their systems. The PC art shown here is available from an electronic bulletin board that can be down loaded using a 2.4 kBd telephone modem. If you desire an electronic copy of this PC art call 408-435-6733 in the continental USA and Canada. The Orcad file for the through-hole transceiver shown in Figures 1 and 3 is 802KITP.EXE. The through-hole transceiver is also available as a Gerber file under the file name 802KITG.EXE. The file name for the current-source LED driver shown in Figure 2 is IDRIVE.EXE. The artwork for the surface-mount MAU transceiver shown in Figure 4 is available in the file called 802MAU.EXE.

Designers should note that printed circuits for the fiber-optic solutions recommended in this Application Note are not difficult to create. If your product requires a unique printed circuit this can easily be accomplished by following the 7 layout rules previously discussed. The printed circuit art provided in this Application Note was developed in one design cycle using these PC design rules.

System designers that want to quickly evaluate the transceiver recommended for hub, bridge, router, and repeater applications should order the HFBR-0414 demo kit. The HFBR-0414 contains a printed circuit board and

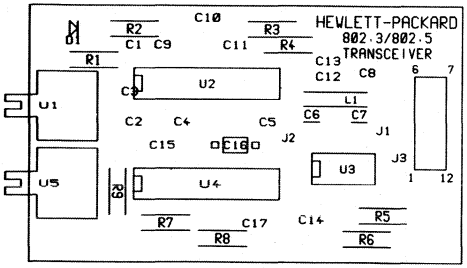


Figure 5a. Silkscreen artwork for the HFBR-0414 Demo Kit. Transmitter per Figure 1. Receiver per Figure 3.

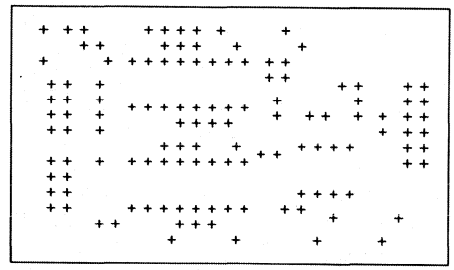


Figure 5b. Drill.

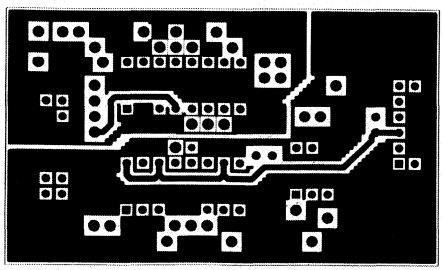


Figure 5c. Layer 1 Component Side.

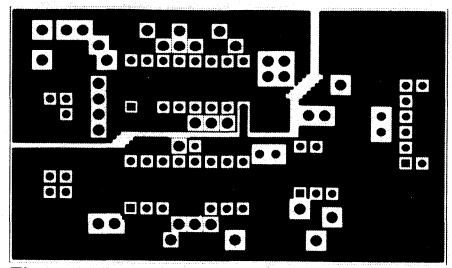


Figure 5d. Layer 2.

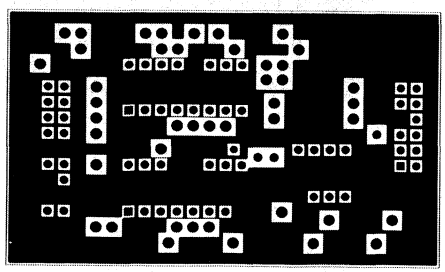


Figure 5e. Layer 3.

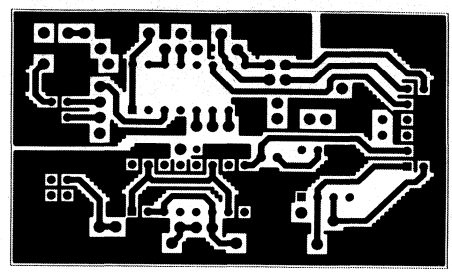


Figure 5f. Layer 4.

WARNING: DO NOT USE PHOTOCOPIES OR FAX COPIES OF THIS ARTWORK TO FABRICATE PRINTED CIRCUITS.

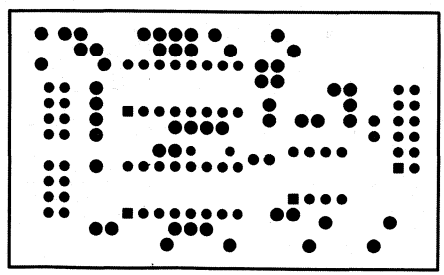


Figure 5g. Solder Mask.

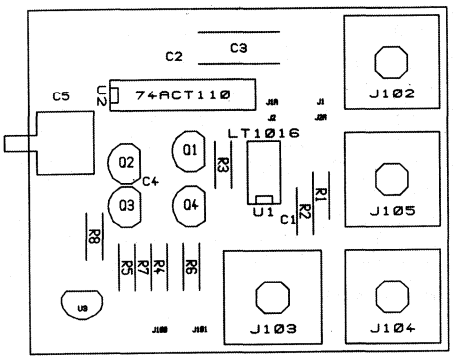


Figure 6a. Silkscreen artwork for the Constant Current Transmitter per Figure 2.

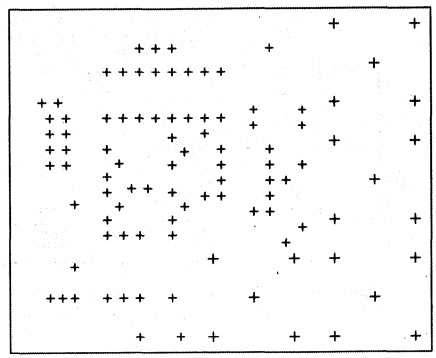


Figure 6b. Drill.

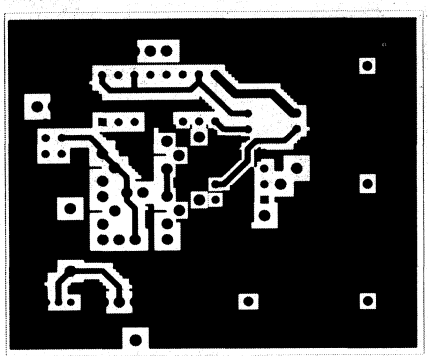


Figure 6c. Layer 1 Component Side.

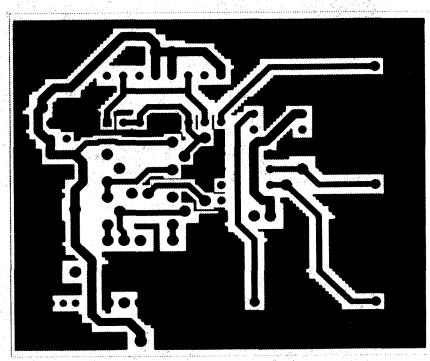


Figure 6d. Layer 2.

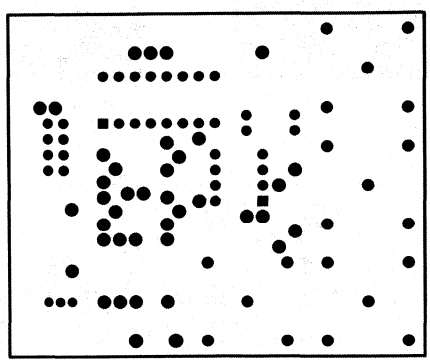


Figure 6e. Solder Mask.

WARNING: DO NOT USE PHOTOCOPIES OR FAX COPIES OF THIS ARTWORK TO FABRICATE PRINTED CIRCUITS.

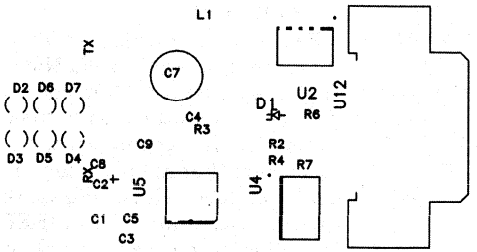


Figure 7a. Top side silkscreen artwork for the Fiber-Optic MAU Transceiver.

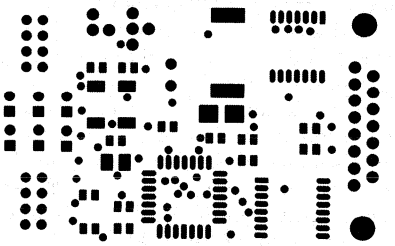


Figure 7b. Top Side Solder Mask.

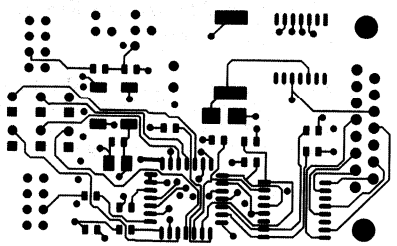


Figure 7c. Top Layer.

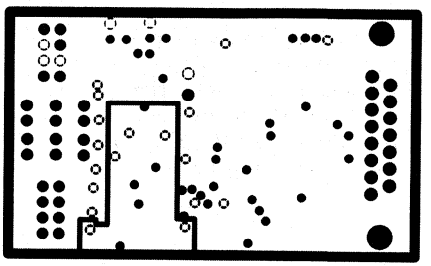


Figure 7d. Layer 2.

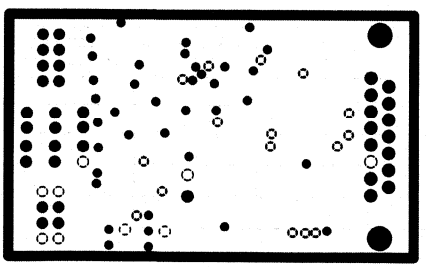


Figure 7e. Layer 3.

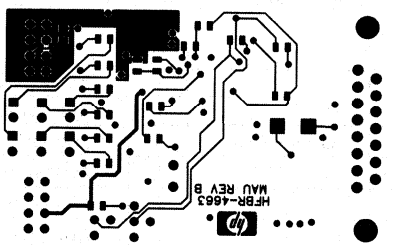


Figure 7f. Bottom Layer.

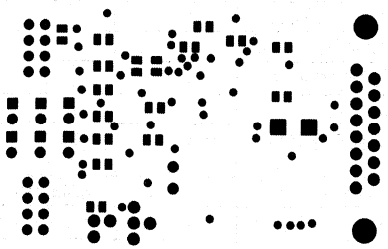


Figure 7g. Bottom Side Solder Mask.

WARNING:
DO NOT USE PHOTOCOPIES OR FAX COPIES OF THIS ARTWORK TO FABRICATE PRINTED CIRCUITS.

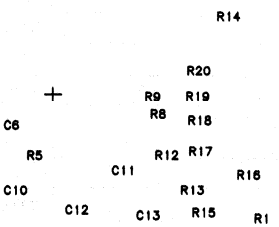


Figure 7h. Bottom Side Silkscreen.

all of the active devices needed to build the transceiver shown in Figures 1 and 3 of this Application Note. A list of the components needed to construct the transceiver shown in Figures 1 and 3 is shown in Table 8. Designers can also quickly determine how well the HFBR-4663 works with HFBR-0400 components in fiber-optic MAU applications by ordering the HFBR-0463. The HFBR-0463 is a fully assembled surface-mount fiber-optic MAU that is implemented using the circuit shown in Figure 4 of this Application Note. A list of the components needed to construct the MAU in Figure 4 is shown in Table 9.

The HFBR-0414 and HFBR-0463 evaluation kits minimize the design effort needed to implement fiber-optic systems that comply with IEEE 802.3 standards and reduce the time needed to bring these new Ethernet LAN products to the market.

Conclusion

The transmitters and receivers shown in this Application Note are an excellent starting point for engineers interested in fiber-optic Ethernet applications. Designers that are planning to build products which address the specifications called for in IEEE 802.3 are encouraged to evaluate these recommendations and determine how well HP's HFBR-0400 fiber-optic components can address their Ethernet LAN application.

Note: The data sheet for the HFBR-4663 (Publication #5091-7391E 4/93) contains errors that have subsequently been corrected in Figure 4 of this Application Note.

Table 8. Bill of Materials for Circuits in Figures 1 and 3.

Item #	Ref. Desig.	Qty. Each	Description	Vendor	Vendor Part Number
1	R1	1	Axial lead resistor 10 Ω ±5% 1/8W		
2	R2	1	Axial lead resistor 1.2K Ω ±5% 1/8W		
3	R3, R4, R5, R6	4	Axial lead resistor 510 Ω ±5% 1/8W		
4	R7	1	Axial lead resistor 34.0 Ω ±1% 1/8W		
5	R8	1	Axial lead resistor 34.7 Ω ±1% 1/8W		
6	R9	1	Axial lead resistor 280 Ω ±1% 1/8W		
7	C1, C4, C8, C9, C11 C12, C13, C14, C15	9	Monolithic ceramic radial lead capacitor 0.1μF ±10% 50V X7R		
8	C2, C3	2	Monolithic ceramic radial lead capacitor 0.01μF ±10% 50V X7R		
9	C5	1	Monolithic ceramic radial lead capacitor 4.7pF ±10% 50V COG		
10	C10	1	Monolithic ceramic radial lead capacitor 0.047μF ±10% 50V X7R		
11	C17	1	Monolithic ceramic radial lead capacitor 56pF ±10% 50V COG		
12	C6, C7, C16	3	Tantalum radial lead capacitor 10μF ±20% 10V		
13	L1	1	Axial lead molded inductor 4.7μH ±10%, Resonant Freq. 75MHz, 1.2 Ω DC res.	Delevan	1025-36K
14	U1	1	125 MHz low cost miniature fiber-optic PIN-amplifier receiver	HP	HFBR-2416
15	U2	1	Integrated post amplifier/comparator (quantizer)	Micro Linear	ML-4622
16	U3	1	Comparator	Linear Tech.	LT-1016
17	U4	1	Quad two input NAND gate NI barrier, SN or SN/PB plated	Texas Instr.	74ACT11000
18	U5	1	820 nm LED transmitter	HP	HFBR-1414
19	D1	1	Low current LED lamp	HP	HLMP-4700

Table 9. Bill of Materials for the Circuit in Figure 4

Item #	Ref. Desig.	Qty. Each	Description	Vendor	Vendor Part Number
1	R1	1	Res, 0805 10 Ω ±5% ni barrier, sn or sn/pb plated	Venkel	CR0805-10W-100JT
2	R2, R3, R6, R7	4	Res, 0805 360 Ω ±5% ni barrier, sn or sn/pb plated	Venkel	CR0805-10W-361JT
3	R4, R5	2	Res, 0805 39.2 Ω ±1% ni barrier, sn or sn/pb plated	Venkel	CR0805-10W-390FT
4	R8	1	Res, 0805 100 Ω ±1% ni barrier, sn or sn/pb plated	Venkel	CR0805-10W-1000FT
5	R9	1	Res, 0805 61.9K Ω ±1% ni barrier, sn or sn/pb plated	Venkel	CR0805-10W-6192FT
6	R10	1	Res, 0805 3K Ω ±5% ni barrier, sn or sn/pb plated	Venkel	CR0805-10W-302JT
7	R11	1	Res, 0805 5K Ω ±5% ni barrier, sn or sn/pb plated	Venkel	CR0805-10W-202JT
8	R12	1	Res, 0805 0 Ω ±5% ni barrier, sn or sn/pb plated	Venkel	CR0805-10W-000JT
9	R13	1	Res, 0805 select Ω ±5% ni barrier, sn or sn/pb plated	Venkel	CR0805-10W-XXXJT
10	R14	1	Res, 0805 1K Ω ±5% ni barrier, sn or sn/pb plated	Venkel	CR0805-10W-102JT
11	R15, R16, R17 R18, R19, R20	6	Res, 0805 1.5K Ω ±5% ni barrier, sn or sn/pb plated	Venkel	CR0805-10W-152JT
12	C1, C5, C9 C10, C11, C12	6	Cap 0805, .1µF, Z5U, 25V, +80/-20% ni barrier, sn or sn/pb plated	Venkel	C0805Z5U250-104ZNE
13	C2, C3	2	Cap, 0805, .01µF,X7R, 25V, ±20% ni barrier, sn or sn/pb plated	Venkel	C0805X7R250-103MNE
14	C4	1	Cap 0805, .047µF, Z5U,25V, ±20% ni barrier, sn or sn/pb plated	Venkel	C0805Z5U250-473MNE
15	C6	1	Cap case size C (.236" x .126"), 22µF, tant, 16V, ±20% ni barrier, sn or sn/pb plated	AVX	TAJC226M016R
16	C7	1	Cap aluminum, radial lead, 470µF (.315" dia x .450" long), 10V +-20%	Sprague	515D477M010BB6A
17	C8	1	Cap case size B (.138" x .110"),10µF, tant, 10V, ±20% ni barrier, sn or sn/pb plated	AVX	TAJB106M010R
18	L1	1	Inductor, DT series, (.510" x .365"), 560 µH ±20% molybdenum/ manganese base metal, sn or sn/pb plated	Coilcraft	DT3316-554XM3C
19	L2, L3	2	Inductor, DT series, (.260" x .175"), 4.7 µH ±20% molybdenum/ manganese base metal, sn or sn/pb plated	Coilcraft	DT1608-472XMBC
20	D1	1	Schottky power rectifier, surface mount MBRS120T3, case 403A-01, (.213" x .140")	Motorola	MBRS120T3
21	U1	1	125 MHz low cost miniature fiber optic PIN-amplifier Receiver	HP	HFBR-2416(ST)
22	U2	1	Simple switcher, 0.5A step-down voltage regulator LM2574, 14 lead surface, (.354" x .406")	National	LM2574M-5.0
23	U3	1	125 MHz low cost miniature fiber optic transmitter	HP	HFBR-1414(ST)
24	U4	1	10base-t transformer, 16 pin, (.500" x .370")	Pulse	PE-65728
25	U5	1	Ethernet transceiver, package: Q28, 28 pin molded leaded PCC, .490"sq	HP	HFBR-4663
26	D2, D3, D6	3	LED green T1	HP	HLMP-1790
27	D4, D7	2	LED red T1	HP	HLMP-1700
28	D5	1	LED yellow T1	HP	HLMP-1719
30	N/A		Solder paste, SN63		
31	N/A		SN63 RMA core solder		
32	U12		15 pin right-angle posted D connector, 318 mount	AMP	747841-4

HEWLETT® PACKARD

Fiber-Optic Solutions for 125 MBd Data Communication Applications at Copper Wire Prices

Application Note 1066

Introduction

Fiber-optic cables have historically been used when the distance is too long, or the data rate is too high, for the limited bandwidth of wire. Optical communication links are also favored when the environment through which the data will pass is elec-trically noisy, or when electro-magnetic radiation from wire cables is a concern. Optical fibers have numerous technical advantages over conventional wire alternatives, but the cost of fiber-optic solutions has always been higher until now.

The Inherent Disadvantages Of Wire

Systems which must communicate are often connected to different reference potentials which are not necessarily zero volts, or in other situations ground references that are thought to be 0 V are electrically noisy. Metallic connections between systems with different ground potentials can be implemented by using the proper isolation and grounding techniques, but if these techniques are not strictly adhered to conductive cables will introduce conflicts between systems operating at different ground potentials. Data communication system designers must exercise caution to ensure that conductive cables do not exceed radiated noise limits established by the FCC, and cable installers need to route wire cables away from other power conductors that might couple electrical noise into the data by magnetic induction. Conventional wire transmission lines must also be terminated using a load resistor equal to the characteristic impedance of the metallic cable. This termination resistor must always be connect-ed to the receiving end of every wire cable to ensure that pulses are not reflected back toward the data source causing interference with the transmitted data.

Fundamental Advantages Of Optical Communication

Non-conductive optical cables have none of the traditional problems associated with wire. When using a fiber-optic solution, system designers do not need to be concerned about environmental noise coupling into cables, or worry about whether there is a termination resistor at the end of the cable. Conflicts between systems with different reference potentials do not happen when using insulating fiber-optic media because optical cables do not have conductors or shields that can be improperly grounded when the cables are installed or maintained. The fiber-optic receiver is the only portion of the optical link which is sensitive to noise, and it can easily be protected because it is contained within the host system which is receiving the data. A simple power supply filter is usually sufficient to protect the fiber-optic receiver from the host system's electrical noise. Electrostatic shielding can be applied to the receiver if the host system is particularly noisy, but electrostatic shields are not needed in most applications if the circuit techniques recommended in this application note are used.

A Fiber-Optic Solution At Wire Prices

The traditional argument for using copper wire has always been that fiber-optic solutions cost more, but Hewlett-Packard's Versatile Link components now enable system designers to overcome cost barriers that have historically prevented the use of fiber-optic cables in short distance applications. The HFBR-15X7 LED transmitter, and the HFBR-25X6 receiver, can be used with large diameter 1 mm plastic, or 200 μm Hard Clad Silica

(HCS™) step index fibers to build unusually low cost data communication equipment. The fiber-optic solution described in this application note can transmit data at rates up to 125 MBd for the same price as shielded twisted pair wire, but this unusually low cost optical data link has none of the disadvantages that are inherent to wire cables.

Distances and Data Rate Capabilities of HFBR-15X7/25X6

Various distances and data rates are possible when the HFBR-15X7 and HFBR-25X6 components are used with large core step index fibers. At low data rates, the distances achievable are determined by the sensitivity of the receiver, cable attenuation, and the amount of light which the LED can launch into the fiber core. As data rate increases, fiber bandwidth will begin to influence how long the optical data link can be, and how fast the data can be transmitted. A plastic fiber with a 1 mm core diameter will couple more light from the LED than a composite fiber with a 200 μm diameter silica glass core and plastic cladding, but greater distances are achievable with the composite fiber since it has significantly lower attenuation than possible with an all-plastic fiber.

The distance data rate curves shown in Figures 1 and 2 are provided to allow designers to quickly determine if HFBR-15X7 and HFBR-25X6 can be used with large core optical fibers to meet their system requirements. Figure 1 shows the distances and data rates that can be achieved with HP's 1 mm plastic fibers and Figure 2 shows what can be accomplished when using HP's 200 μm hard clad silica fibers. If designers utilize the

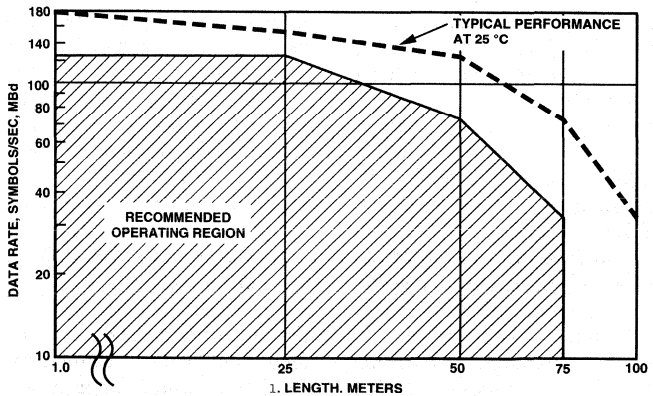


Figure 1. Distances and Data Rates Possible with 1 mm Plastic Fiber.

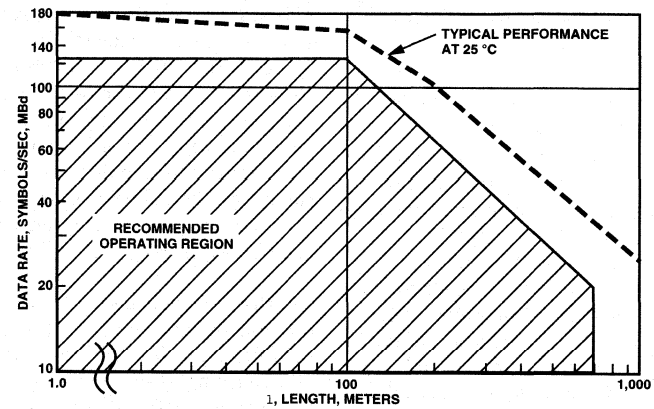


Figure 2. Distances and Data Rates Possible with 200 HCS Fiber.

circuits recommended in this application note, digital fiber-optic links can normally be implemented at distances and data rates within the shaded portions of Figure 1 and Figure 2 . The fiber-optic transceiver shown in this publication was optimized for operation at 125 MBd. Greater distances can be achieved at data rates less than 125 MBd by optimizing the transmitter and receiver circuits for operation at lower speeds.

Figure 1 shows the performance possible with 1 mm diameter plastic fiber. The HFBR-15X7/25X6 components can be used with standard 1 mm plastic cables to build 20 meter links which are capable of transmitting data at a rate of 125 MBd. When low loss plastic fiber is used, distances of 25 meters are possible at 125 MBd. As data rate decreases, the distance achievable with 1 mm fiber increases. Figure 1 shows that a distance of 100 meters is typically possible at rates as low as 33 MBd when using low loss 1 mm plastic fiber.

Composite fiber with a silica glass core and plastic cladding can achieve greater distances than possible with an all plastic fiber. Figure 2 shows what can be ac-

complished when HFBR-15X7 and HFBR-25X6 components are used with 200 μm diameter hard clad silica (HCS) fiber. Substantial increases in cable length are possible when using 200 μm HCS™ fiber since it has a much lower optical attenuation than 1 mm plastic fiber. Figure 2 indicates that 125 MBd data rates are typically possible with 125 meter lengths of 200 μm HCS™ fiber when using the transceiver recommended in this publication. Distances of 1 km can typically be achieved at data rates as low as 20 MBd due to the much lower optical losses of 200 μm HCS™ cable.

Advantages of Encoded Run Limited Data

Fiber-optic transceivers are commonly used in systems that use some form of encoding. When data is encoded the original data bits are replaced with a different group of bits known as a symbol. Data is encoded to prevent the digital information from remaining in one of the two possible logic states for an indefinite period of time. When data is encoded, a characteristic known as the "run limit" is established. If data is not changing, the run limit defines how much time may pass before the encoder inserts a transition from one logic state to another. The run length, or run limit of the encoder, is the number of symbol periods that are allowed to pass before the encoder changes logic state. Encoders also force the encoded data to have a 50 % duty factor, or they restrict the duty factor to a limited range, such as 40 to 60%. When data is encoded, the fiber-optic receiver can be ac coupled as shown in Figure 3.

Without encoding, the fiber-optic receiver would need to detect dc levels to determine the proper logic state during long periods of inactivity, as when there is no change in the transmitted data. AC-coupled fiber-optic receivers tend to be lower in cost, are much easier to design, and contain fewer components than their dc-coupled counterparts.

The output of the HFBR-25X6 should not be direct coupled to the amplifier and comparator shown in Figure 3. Direct coupling decreases the sensitivity of a digital fiber-optic receiver, since it allows low-frequency flicker noise from transistor amplifiers to be presented to the receiver's comparator input. Any undesired signals coupled to the comparator will reduce the signal-to-noise ratio at this critical point in the circuit, and reduce the sensitivity of the fiber-optic receiver.

Another problem associated with direct-coupled receivers is the accumulation of dc offset. With direct coupling, the receiver's gain stages amplify the effects of undesirable offsets and voltage drifts due to temperature changes. These amplified dc offsets will eventually be applied to the comparator and result in reduced sensitivity of the fiber-optic receiver. The dc offset at the comparator can be referred to the optical input of the receiver by dividing by the receiver gain. This division refers the dc offset at the comparator to the receiver input where it appears as a change in optical power that must be exceeded before the receiver will switch logic states. Problems with dc drift can be avoided by constructing the receiver as shown in Figure 3.

Encoding has other advantages. Encoding merges the data and clock signals in a manner that allows a timing-recovery circuit to reconstruct the clock at the receiver end of the digital data link. This is essential because fiber-optic links can send data at such high rates that asynchronous timing-recovery techniques, such as over-sampling, are not very practical. Without encoding, the clock signal required to synchronously

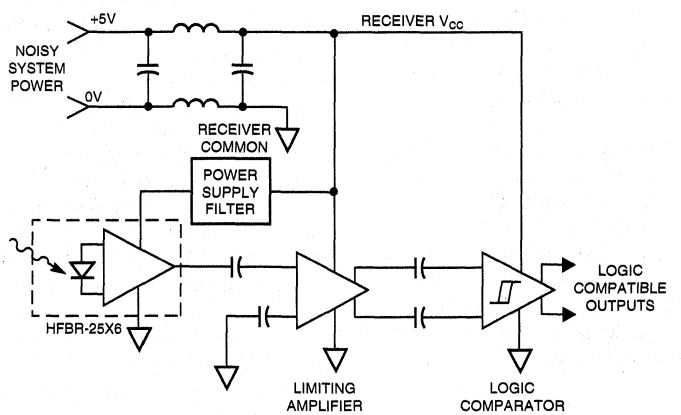


Figure 3. Fiber-Optic Receiver Block Diagram.

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detect the data would need to be sent via a second fiber-optic link. Separate transmission channels for data and clock signals are usually avoided due to cost, but problems with time skew between the data and clock can also arise if separate fibers are used to transmit these signals.

Characteristics of Encoders

A Manchester encoder replaces each bit with two symbols, for instance, a logic "1" is replaced by a ("1","0") symbol, and a logic "0" is replaced by a ("0", "1") symbol. Manchester code is not very efficient since it doubles the fundamental frequency of the data by substituting 2 symbols for each bit transmitted. Block substitution codes such as 4B5B replace 4 bit groups of data with a 5 bit symbol. Another popular block substitution code is 5B6B, which replaces each group of 5 bits with a 6 bit symbol. Substitution codes encode the data more efficiently. If a Manchester code is used to transmit data at 100 Mbits/second the fiber-optic channel must be capable of passing 200 M symbols/second. Baud (Bd) is expressed in units of symbols/second, thus the Manchester encoder in this example requires a serial data link that can work at 200 MBd. If the Manchester encoder is replaced by a 4B5B encoder, the 100 M bit/second data can be sent at a signaling rate of 125 MBd. In binary transmission systems the maximum fundamental frequency of the data is half the symbol rate expressed in Bd. When a Manchester encoder is used to send 100 M bit/second data, at a symbol rate of 200 MBd, the maximum fundamental frequency of the data is 100 MHz. By using a 4B5B encoder, the same 100 M bit/second data can be transmitted at 125 MBd, at a maximum fundamental frequency of 62.5 MHz.

The minimum fundamental frequency that the fiber-optic link must pass is determined by the encoding rule chosen. The run limit of the encoder determines the maximum number of symbol periods that the encoder will allow before it forces a transition, thus the encoder's run limit determines the minimum fundamental frequency of the encoded data. Manchester code will allow only two symbol periods to pass without a transition. As many as 3 symbol times without a transition will be allowed by the 4B5B encoder used in the AMD TAXIchip™.

Figure 4 illustrates the attributes of various encoding techniques. Figure 4 shows that as encoder efficiency improves the bandwidth needed in the fiber-optic communication channel is reduced, or conversely, for a fixed communication channel bandwidth the number of bits/second that can be transmitted will go up as encoder efficiency improves.

Total Solution Cost

125 Mbd Link Costs

The cost of a 125 MBd link consists of the cost of the data transceiver, and the cost of the media (cable and connectors). For the recommended +ECL transceiver discussed in this application note, the material costs in low volume are approximately $28.

The total material cost for a logic-to-light transceiver is under $30 in moderate volume, which compares favorably with the cost of a wire transceiver solution capable of 125 MBd performance over 100 meter spans, but the big advantage of this low cost fiber-optic technology is its ability to provide better data integrity than comparably priced wire alternatives.

Cable costs

The price per meter of HCS cable from HP and SpecTran is comparable to the cost of shielded twisted pair wire in similar volumes. Connectors cost approximately a dollar, similar to typical twisted pair RJ jack connectors for data communications. Connec-

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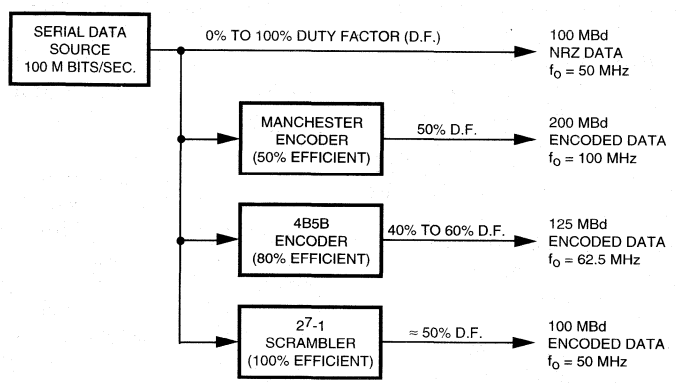
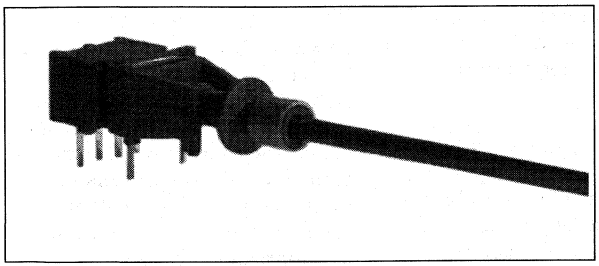
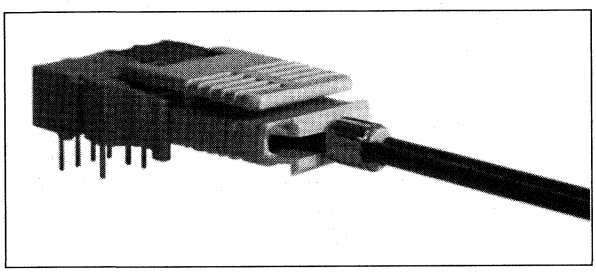


Figure 4. Attributes of Encoding.



Versatile Link Receiver with Simplex Connector for HCS® fiber attached.



Stacked Versatile Link Transmitter/Receiver pair with Latching Duplex Connector for plastic fiber attached.

tor installation requires no epoxy or polishing, and can be completed in less than a minute per connector. Therefore the installed cost of HCS cable is similar to the installed cost of wire links of comparable performance.

For shorter distance links, pre-connectored plastic fiber cable assemblies are available from Hewlett-Packard Distributors at attractive prices. For example, a 1 meter, duplex, pre-connectored plastic fiber cable has a suggested list price of approximately $13 for a quantity of more than 50 units. Again, these costs compare favorably with the cost of data grade wire cable assemblies at similar volumes.

The costs of the 125 MBd Versatile Link electronics, cable, and connectors are all competitive with wire solutions. However, wire solutions frequently incur additional costs in use due to unanticipated trouble-shooting of electrical interference due to poor terminations or adjacent sources of electrical noise. The inherent electrical isolation of optical fiber results in a more robust solution and lower cost to the end user.

Circuits Recommended for use with HFBR-15X7 and HFBR-25X6

The HFBR-15X7/25X6 components can be used in a diverse range of applications. Not all applications can be addressed with the circuits shown in this publication, however, the transceiver recommendation which follows is useful in a wide range of systems which transmit encoded data at rates up to 125 MBd. If the design suggestions given in this publication do not meet your needs, please feel free to contact your Hewlett-Packard Components representative for more information.

Recommended Transmitter

The transmitter shown in Figure 5 is recommended for use with 1 mm plastic fiber. The transmitter in Figure 5 applies a forward current of 20 mA to the HFBR-15X7 LED. If 200 μm HCS™ fiber is to be used the LED forward current must be increased to 60 mA and the drive circuit shown in Figure 6 is recommended. The forward current applied to the HFBR-15X7 was chosen so that the LED will couple the maximum amount of light into the core of the fiber without overdriving the HFBR-25X6 receiver when short optical cables are used.

The transmitters shown in Figures 5 and 6 use the following techniques to improve LED performance. When the output of U1 is a logic "1", resistor R11 applies a small residual prebias current to the LED. This small prebias current minimizes the propagation delay distortion of the LED. Prebias also improves LED linearity sufficiently to permit the use of a frequency compensation circuit, which reduces the optical rise/fall time of the fiber-optic transmitter.

This frequency compensation technique is often called drive current peaking, because it adds brief current spikes to the LED drive current pulses. When prebiased, the HFBR-15X7 LED has an amplitude versus frequency response which is

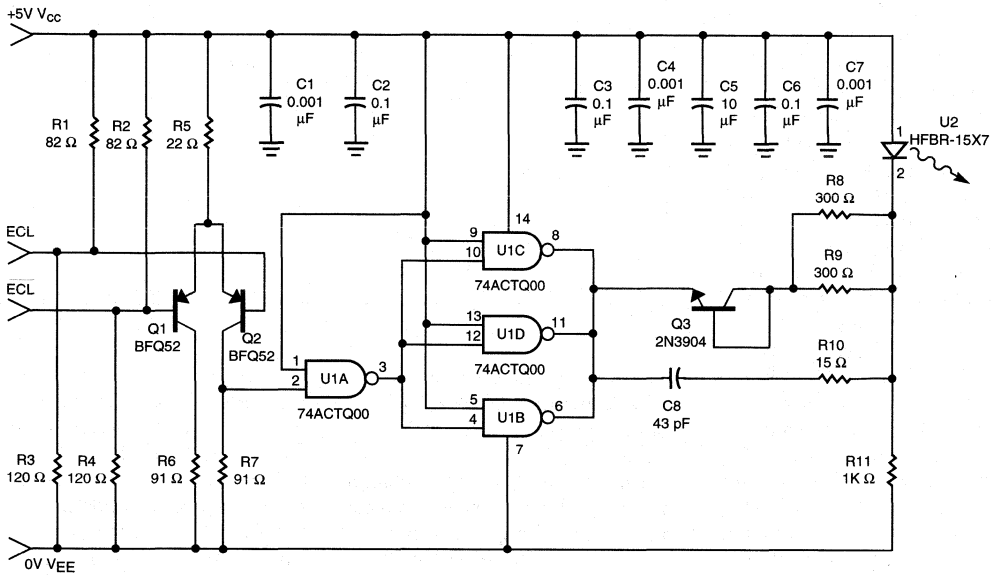


Figure 5. +5 V ECL Through Hole Transmitter for 1 mm Plastic Optical Fiber (POF).

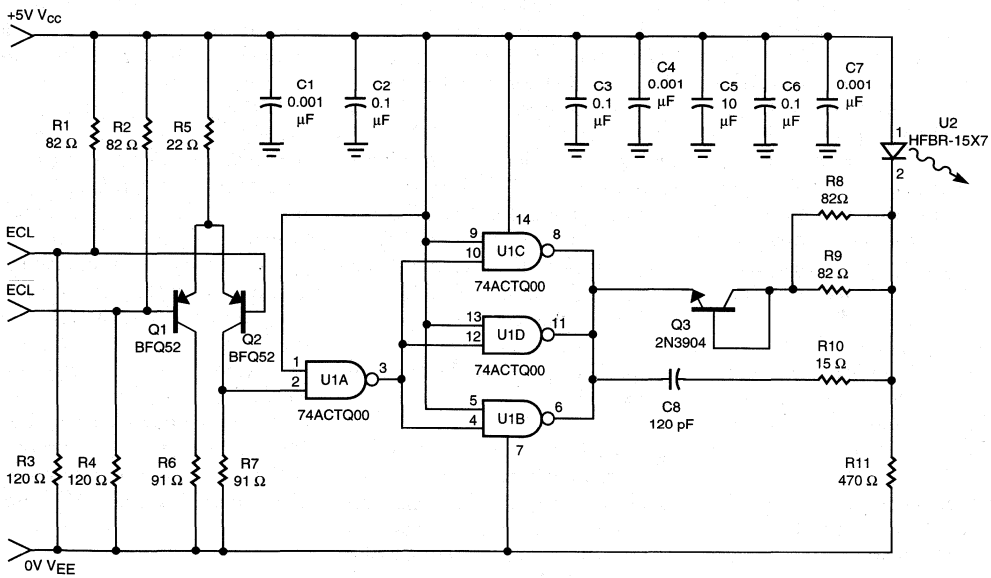


Figure 6. +5 V ECL Through Hole Transmitter for 200 µm HCS™ Fiber.

roughly equivalent to a first order low pass filter. Without prebias and peaking, the HFBR-15X7 LED has a typical 10% to 90% optical rise time of 12 ns. When prebias is provided by R11, and frequency compensation (peaking) is provided by R10, and C8, the 10% to 90% optical rise time of the HFBR-15X7 LED decreases to a typical value of 3 ns, when using 1 mm plastic fiber. Optical rise times of 3.5 ns are typical when the peaked LED driver is used with 200HCS fiber. The LED's on-state current is primarily determined by the values of resistors R8 and R9, but Equation 1 shows that some on-state current is also provided by R11. Transistor Q3 is connected to form a low cost high speed diode. This diode allows LED prebias current to be set independent of the resistance chosen for R8 and R9. The LED's prebias current can be calculated as shown in Equation 2. Capacitance between the emitter and collector of Q3 changes as a function of the diode connected transistor's forward current. Current dependent changes in the capacitance of Q3 ensure that the current peak which turns the LED off will have a larger amplitude than the current peak applied when the LED is switched on. LEDs are characteristically harder to turn off than on. The difference between the amplitude of the peak current applied at turn on, and turn off, helps to reduce the optical pulse width distortion of the fiber-optic transmitter. One of the best features of this recommended LED driver circuit is that all of the active and passive components needed to build 10,000 of the transmitters shown in Figures 5 or 6 can be purchased for about $10.00 per circuit.

Equation 1:

$$I_{F_{ON}} = \frac{(V_{cc} - V_{F_{ON}})}{R11} + \frac{[V_{cc} - (V_{F_{ON}} + V_{CE_{Q3}} + V_{OL_{U1}})]}{[(R8)(R9)/(R8 + R9)]}$$

Equation 2:

$$I_{F_{OFF}} = \frac{(V_{cc} - V_{F_{OFF}})}{R11}$$

Recommended Receiver

The recommended receiver is shown in Figure 7. The HFBR-25X6 component used in this receiver linearly converts changes in received optical power to a corresponding change in voltage. The output of the HFBR-25X6 is an analog signal which can easily be converted to logic by a post amplifier and comparator. This post amplifier comparator function is often called a quantizer. A very inexpensive quantizer can be implemented using an MC10H116 ECL line receiver. The MC10H116 provides three low cost differential amplifiers in a single package. The MC10H116 can accommodate a large range of input voltages. *The large dynamic range of the MC10H116 is very important!* The quantizer must have a large dynamic range because the output of the HFBR-25X6 can change from a few millivolts to hundreds of millivolts when fiber length and attenuation are varied.

Several subtle techniques are used to maximize the receiver's sensitivity to optical pulses, while minimizing the receiver susceptibility to electromagnetic interference (EMI). In most systems, the same +5 V dc supply which powers the fiber-optic receiver is also used to power micro processors and digital logic. *The receiver must be isolated from noisy dc power supplies!* This isolation is provided by low pass filters that prevent noise injection into the HFBR-25X6, and quantizer, through the +5 V power connections. The HFBR-25X6 is a miniature hybrid circuit that, due to its small physical size, is relatively immune to environmental noise. In most applications, the HFBR-25X6 has sufficient noise immunity to operate without any additional electrostatic shielding, but the connection between the HFBR-25X6 and the non-inverting input of the MC10H116 forms a loop antenna with sufficient area to receive significant amounts of EMI. The receiver's susceptibility to EMI is minimized by connecting a second loop antenna with equal area to the inverting input of the MC10H116 quantizer. When connections to the quantizer's input are symmetric, and have equal loop areas, the common mode rejection of the MC10H116's difference amplifiers will assure that the fiber-optic receiver provides good EMI immunity.

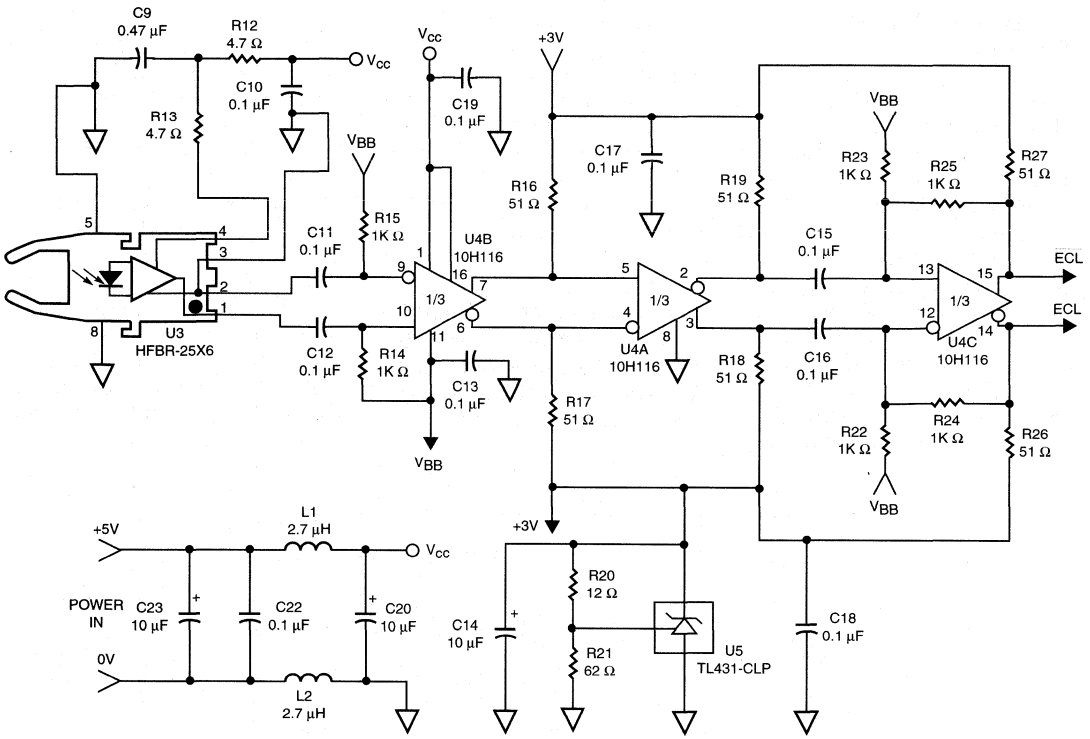


Figure 7. +5 V ECL Receiver with Through Hole Pin Out.

Design techniques which improve the EMI immunity of the receiver help to minimize crosstalk between the transmitter and the receiver. Crosstalk will also be reduced when the printed circuit for the fiber optic transceiver is designed so that pin 4 of the HFBR-15X7 LED transmitter is next to pin 1 of the HFBR-25X6 receiver. This arrangement maximizes the distance between pin 2 of the HFBR-15X7 LED and the power supply lead (pin 4) of the HFBR-25X6. When the distance between pin 4 of the HFBR-25X6 and pin 2 of the LED is maximized, the crosstalk between the LED transmitter and the HFBR-25X6 receiver's power pin is reduced. The typical transmitter to receiver crosstalk which occurs when using the printed circuit shown in this application note is equivalent to a 0.5 dB reduction in receiver sensitivity. The effect of transceiver crosstalk has already been factored into the recommended distances and data rates shown in Figures 1 and 2.

The 125 MBd receiver shown in Figure 7 typically provides a sensitivity of -28 dBm average modulated when used with 1 mm plastic fibers. The same receiver can be used with 200 µm HCS™ fibers and will provide a typical sensitivity of -29 dBm average modulated at a data rate of 125 MBd. Overload characteristics of the receiver are not influenced by characteristics of the MC10H116 quantizer. The maximum power which can be applied to the receiver shown in Figure 7 is determined by the saturation characteristics of the transimpedance amplifier used in the HFBR-25X6. The HFBR-25X6 is guaranteed to provide pulse width distortion which is less than 2 ns when received optical power is less than -9.4 dBm peak. Many features have been incorporated into the receiver recommended in this publication, but one of the most prominent characteristics of the circuit shown in Figure 7 is that all of the active and passive components needed to build 10,000 fiber-optic receivers can be purchased for about $15.00 per circuit.

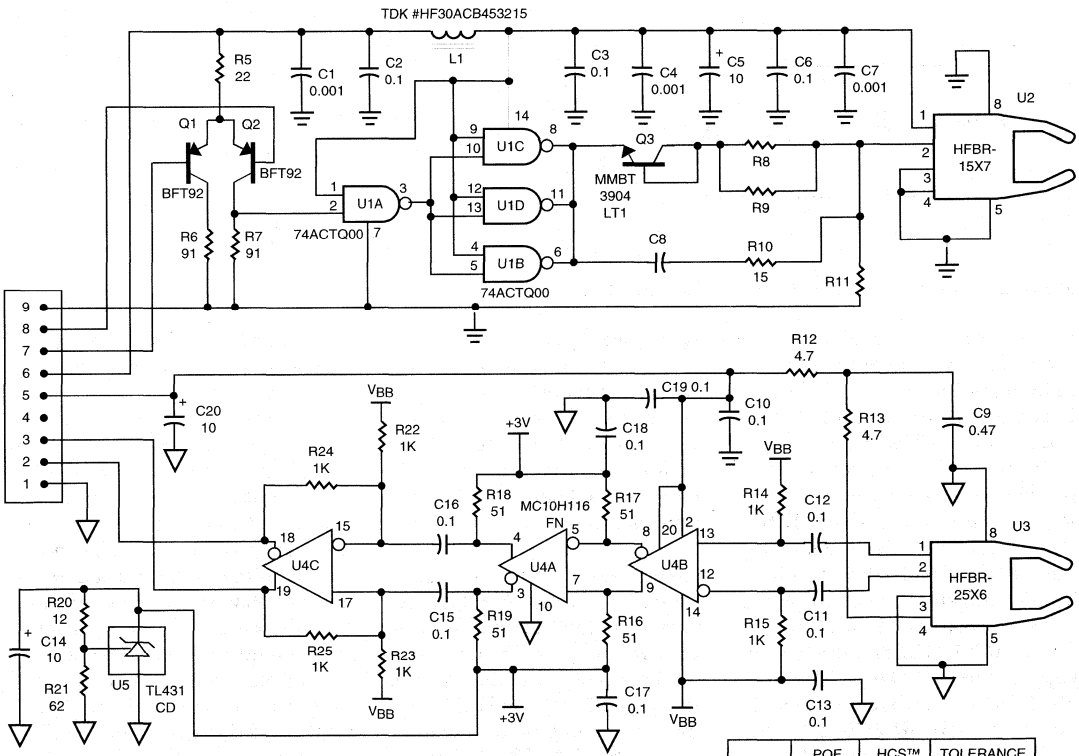
A Complete Fiber-Optic Transceiver Solution

Figure 8 shows the schematic for a complete fiber-optic transceiver. This transceiver is constructed on a printed circuit, which is 1" wide by 1.6" long, using surface mount components. When the transceiver shown in Figure 8 is tested at a data rate of 125 MBd, using 100 m of 200 µm HCS™ fiber, it provides a typical eye opening of 5.4 ns at a BER of $1x10^{-9}$. The power supply filter and ECL terminations shown in Figure 9 are recommended for use with the transceiver shown in Figure 8.

The artwork for the surface mount transceiver is shown in Figure 10, and a complete parts list is shown in Table 1. Designers interested in inexpensive solutions are encouraged to embed the complete fiber-optic transceiver described in this Application Note into the next generation of new data communication products.

Local Area Network Links

High speed LANs such as FDDI and ATM have adopted a common footprint +5 V ECL transceiver, often referred to as a "1X9 transceiver". The circuit in Figure 8 matches the electrical functions of these industry standard transceivers, with the exception that there is no signal detect function in the Figure 8 circuit (pin 4 is nonfunctional). Therefore, the recommended circuit can be directly inserted into boards designed for 1X9 transceivers and used as a lower-cost alternative to the industry standard 1300 nm transceivers. If the MC10H116 comparator is replaced with a Signetics NE5224 IC, the signal detect function can



NOTES:

(1) ALL CAPACITORS ARE IN µF WITH ±10% TOLERANCE UNLESS OTHER WISE NOTED.

(2) ALL RESISTORS ARE IN OHMS WITH ±5% TOLERANCE UNLESS OTHER WISE NOTED.

	POF	HCS™	TOLERANCE
R8	301 Ω	82.5 Ω	1%
R9	301 Ω	82.5 Ω	1%
R11	1K Ω	475 Ω	1%
C8	43 pF	120 pF	5%

Figure 8. Fiber-Optic Transceiver Using Surface Mount Components.

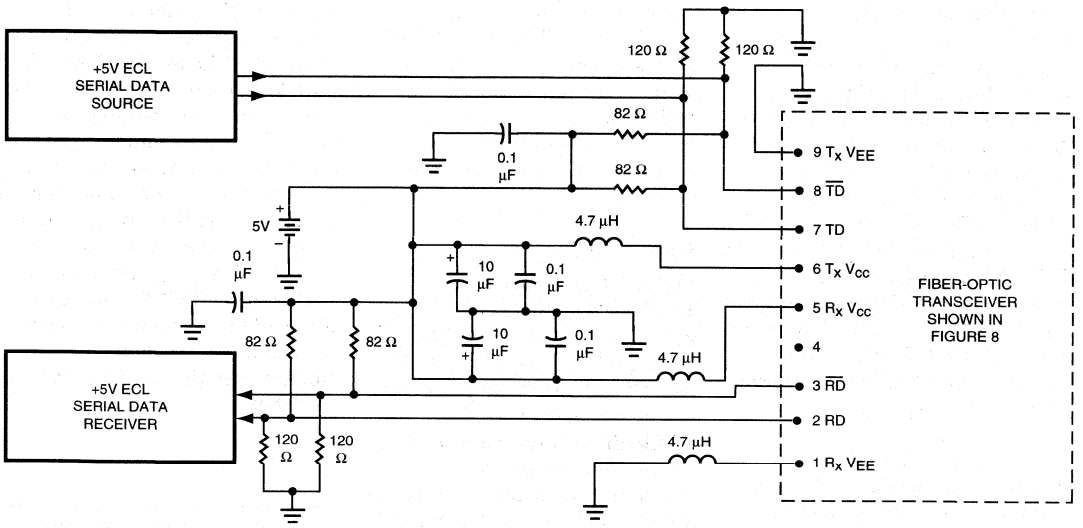


Figure 9. Recommended Power Supply Filter and +5 V ECL Signal Terminations.

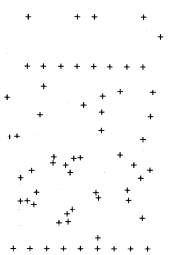


Figure 10a. Drill Drawing

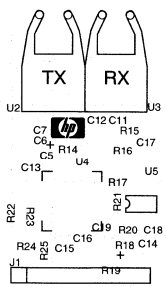


Figure 10b. Top Silkscreen

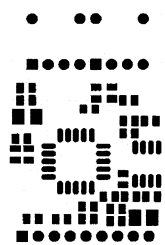


Figure 10c. Top Side Solder Mask

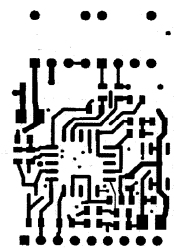


Figure 10d. Top Layer

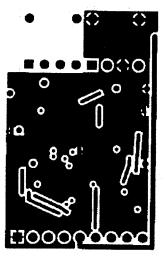


Figure 10e. Second Layer

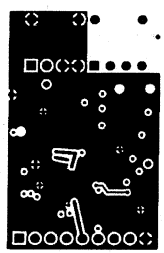


Figure 10f. Third Layer

Figure 10g. Bottom Layer

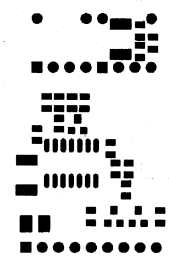


Figure 10h. Bottom Side Solder Mask

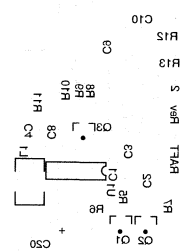


Figure 10i. Bottom Silkscreen

WARNING: DO NOT USE PHOTOCOPIES OR FAX COPIES OF THIS ARTWORK TO FABRICATE PRINTED CIRCUITS.

also be implemented, at a total transceiver cost that is slightly higher than the MC10H116 circuit, but still significantly less than half the cost of an integrated 1300 nm 1X9 transceiver. Lower speed LANs such as Ethernet and Token Ring typically use TTL ICs. The circuit of Figure 8 can easily be modified for TTL I/O for such networks. Also note that the HFBR-25X6 receiver will work well with the Micro Linear ML4622/4624 quantizer ICs designed specifically for Ethernet and Token Ring.

The fiber-optic data links described in this note will not be interoperable with the available industry standard transceivers, and do not conform to the specifications of IEEE or ANSI LAN standards as currently defined. However, these fiber-optic links can be used in proprietary systems where a lower-cost, fiber-optic solution is desired.

Byte-to-Light Data Communication

The fiber-optic transceiver shown in Figure 8 has a +5 V ECL interface that is compatible with the AMD TAXIchip. This transceiver can be combined with the TAXIchip to build complete data communication systems that bridge the gap between the serial architecture of optical fibers and the parallel architecture used in computing, peripheral, and telecom systems. TAXIchip provides all of the MUX, DEMUX, encode, decode, and timing recovery functions needed to interface a serial fiber-optic communication channel to a parallel processor. The transceiver shown in Figure 8 provides all of the circuitry needed to interface the HFBR-15X7 and HFBR-25X6 components to the Am7968/Am7969 TAXIchips. Figure 11 shows how the fiber-optic transceiver should be connected to the Am7968 and Am7969.

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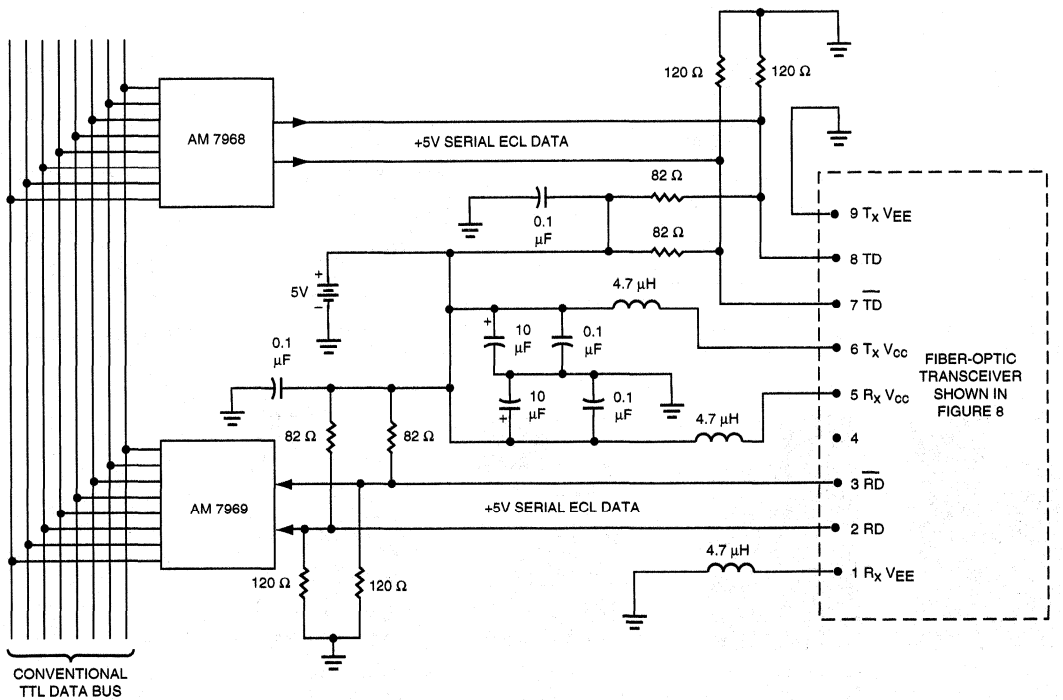

Figure 11. Byte-to-Light Transceiver.

Testing Digital Fiber-Optic Links

The overall performance of a complete digital fiber-optic link can be determined by stimulating the transmitter with a pseudo random bit sequence (PRBS) data source while observing the response at the receiver's output. A PRBS data source is a shift register where data bits from two or more shift register stages are combined using an exclusive-or gate. When a clock signal is applied to the CLK input of the shift register, and the output of the exclusive-or gate is applied to the D_S input of the shift register, the PRBS generator produces a serial bit stream which appears to be random, but is actually periodic and reproducible. If the PRBS generator is constructed using a 23 bit long shift register, the exclusive-or feedback can be configured so that the shift register will be in one of 2^{23}-1 possible states at any given clock time. The 2^{23}-1 PRBS data generator appears to be a source of random serial data, but it is actually the output of a shift register which is in one of 8,388,610 precisely repeatable states. PRBS generators send an exactly repeating serial data pattern that can be checked bit-by-bit to determine if the fiber-optic link made errors while transporting the data. A bit-error-ratio test set is an instrument which contains a PRBS generator, a bit-by-bit error detector, and an error counter. Bit-error-ratio test sets measure the probability that the fiber-optic link will make an error. Probability of error is commonly expressed as a bit-error-ratio or BER. The BER is simply the number of errors which occurred divided by the number of bits transmitted through the fiber-optic link in some arbitrary time interval.

The +5 V ECL interface of the transceiver shown in Figure 8 is convenient for use with off-the-shelf VLSI chips like the TAXIchip, but it is not compatible with the majority of the test equipment used to measure the performance of fiber-optic links. Most bit error rate (BER) test sets have conventional -5 V ECL inputs and outputs. The test fixture shown in Figure 12 provides a convenient way to convert +5 V ECL to -5 V ECL. This test fixture allows the transceiver in Figure 8 to be used with any BER test set (BER machine) with a conventional -5V ECL interface. The test fixture in Figure 12 was used to collect the performance data shown in this application note.

The waveforms shown in Figures 13 and 14 are known as eye diagrams. These eye diagrams were measured by connecting a Digitizing Oscilloscope, with a 1 GHz bandwidth, to the receiver's +5 V ECL output. The HP 54100A oscilloscope used for these measurements was triggered from the PRBS generator's clock. The lack of correlation between the oscilloscope's time base, and the PRBS generator's clock, assures that the oscilloscope will randomly sample the PRBS data. The infinite persistence mode of the HP 54100A Digitizing Oscilloscope was used, and the electrical output of the receiver was measured for roughly 1 hour, to determine the eye opening. As eye opening, or eye width, increases, the probability that the fiber-optic link will make an error decreases. A wide eye opening makes it easier to extract the clock signal which is normally encoded with the data passing through the serial communication channel. Fiber-optic links are less likely to make errors when the eye is wide open, because there is more time for the clock to synchronously detect the data while it is stable and unchanging.

The results measured in Figure 13 were obtained at room temperature when 125 MBd PRBS data was transmitted through a plastic fiber-optic link. Figure 13 shows that the eye opening is typically 5.52 ns when the recommended transceiver in Figure 8 is used with 20 meters of 1 mm plastic fiber. Excellent performance can also be achieved by using the transceiver in Figure 8 with HP's 200 µm HCS™ fiber. Figure 14 indicates that the eye opening is typically 5.56 ns wide when 125 MBd data is transmitted through 100 meters of 200 µm HCS™ fiber.

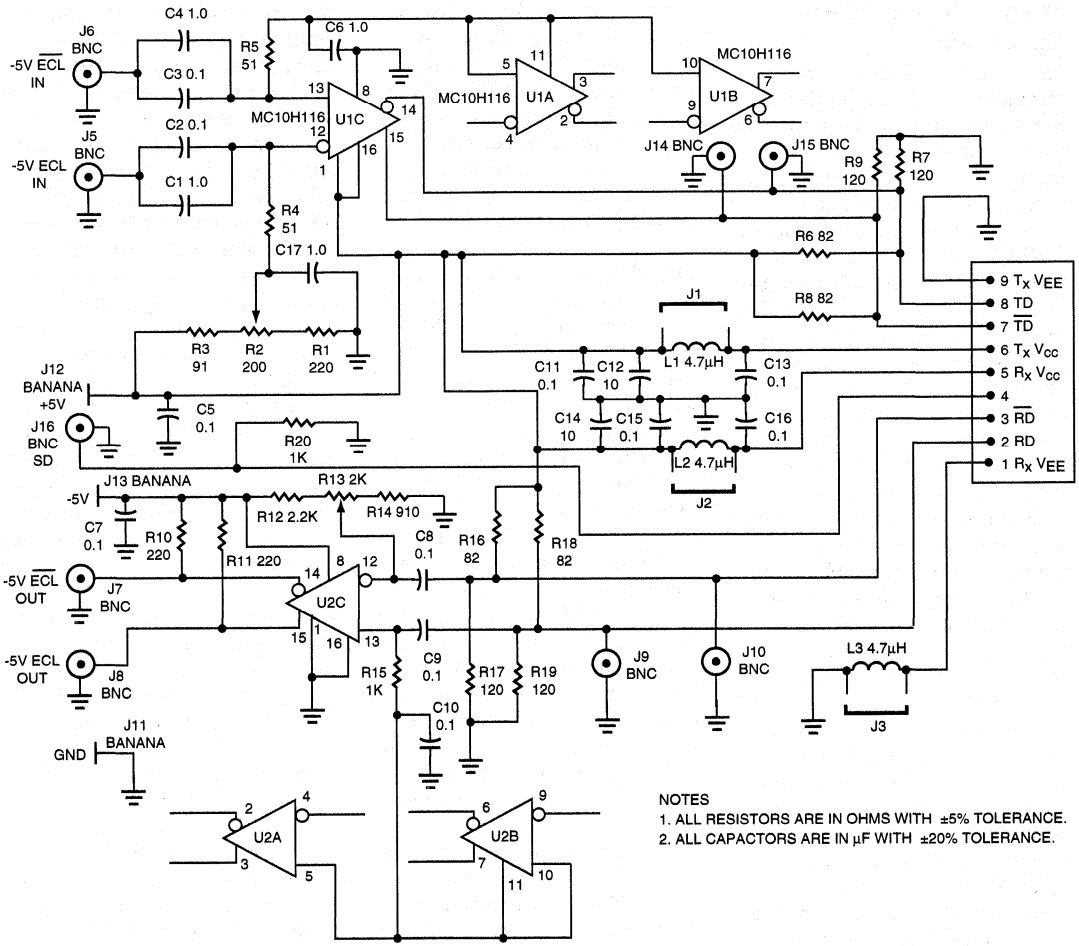

Figure 12. Fiber-Optic Transceiver Test Fixture.

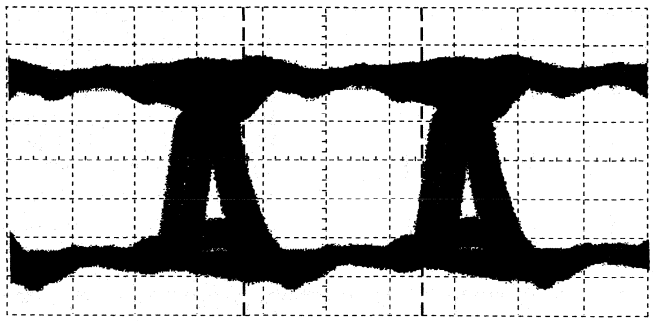

Figure 13. Typical Eye Opening with 25 m of Low Loss 1 mm Plastic Optical Fiber (POF).

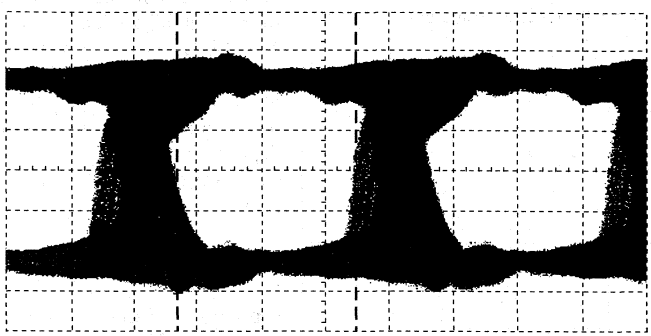

Figure 14. Typical Eye Opening with 100 m of 200 μm HCS™ Fiber.

A better method for measuring the performance of a complete optical data link is to use a computer controlled delay line and a BER test set. This technique uses a computer to adjust the delay of the BER test set's clock relative to the PRBS data. At a data rate of 125 MBd the clock delay was changed in 100 ps increments. The test system then measures and stores the probability of error at each 100 ps delay step until the clock has been swept through the entire 8.0 ns period of every 125 MBd symbol transmitted through the fiber-optic link. The results in Figure 15 were obtained when the BER test set applied 2^{23}-1 PRBS data to the transmitter portion of the transceiver under evaluation. Figure 15 shows that when using the transceiver recommended in Figure 8 BER is typically $\leq 1 \times 10^{-10}$ for 5.8 ns of each pseudo random symbol transmitted through a 20 m length of 1 mm plastic fiber. The optical power applied to the receiver was Pr = -16.4 dBm average for the measured results shown in Figure 15. Figure 16 shows the performance that can be achieved at 125 MBd with 200 μm HCS™ fiber. Figure 16 shows that when using the transceiver recommended in Figure 8, BER will be typically $\leq 1 \times 10^{-10}$ for 5.3 ns of each pseudo random symbol transmitted through a 100 m length of 200 μm HCS™ fiber. The optical power applied to the receiver was Pr = -18.0 dBm average for the measured results shown in Figure 16.

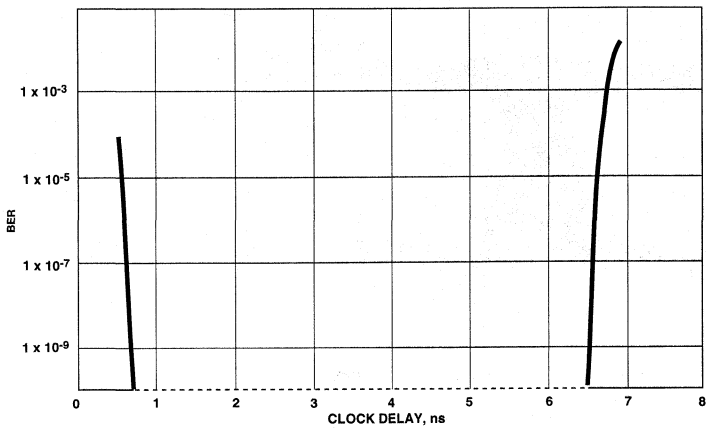

Figure 15. Typical BER vs. Clock Delay at 125 MBd with 20 m of 1 mm Plastic Fiber.

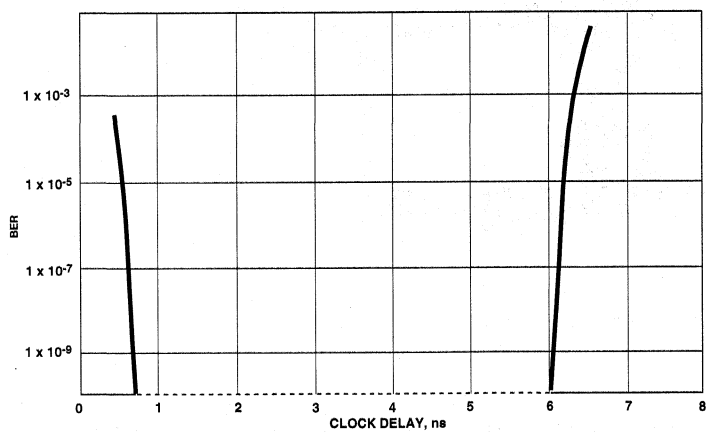

Figure 16. Typical BER vs. Clock Delay at 125 MBd with 100 m of 200 µm HCS™ Fiber.

Applications Support

Variations in performance due to circuit layout can be avoided by using the artwork shown in Figure 10. Designers that would like to use the printed circuit layout developed by HP are encouraged to embed the PC artwork shown in this Application Note into their systems. The PC art shown here is available from an electronic bulletin board that can be down loaded using a 2.4 kBd telephone modem. If you desire an electronic copy of this PC art call your Hewlett-Packard Components representative.

System designers can quickly determine if the HFBR-15X7 and HFBR-25X6 will meet their needs by ordering the HFBR-0527. The HFBR-0527 is a completely assembled demo board for the transceiver shown in Figure 8. When using plastic fiber order the HFBR-0527P, and when using 200 µm HCS™ fibers specify the HFBR-0527H. The test fixture in Figure 12 is also available as the HFBR-0319. The HFBR-0319 is a fully assembled test fixture. This test fixture adapts any fiber-optic transceiver with a 1x9 footprint to test equipment with -5 V ECL inputs and outputs. The HFBR-0527 and the HFBR-0319 minimize the effort needed to design new products which use fiber-optic data links. The HFBR-0527 and the HFBR-0319 provide a high level of technical support. This high level of technical assistance drastically reduces the time needed to develop and market new products which utilize the fundamental advantages of optically isolated data communication.

Conclusion

The HFBR-15X7 and HFBR-25X6 components can be used with large core fibers and inexpensive optical connectors to build exceptionally low cost digital fiber-optic links. When these Versatile Link components are used with 1 mm plastic, or 200 µm HCS™ fibers, digital data links that are comparable with the cost of shielded twisted pair wire can easily be implemented. The HFBR-15X7 and HFBR-25X6 provide designers with a short haul data communication solution that costs the same as shielded twisted pair wire, but this low cost fiber-optic solution has none of the grounding and electromagnetic compatibility problems inherent in metallic cables.

Table 1. Parts List for Circuit Shown in Figure 8.

Designator	Part Type	Description	Footprint	Material	Part Number	Quantity	Vendor 1
C1	0.001	Capacitor	805	NPO/COG	C0805NPO500102JNE	3	Venkel
C4	0.001	Capacitor					
C7	0.001	Capacitor					
C10	0.1	Capacitor	805	X7R or better	C0805X7R500104KNE	12	Venkel
C11	0.1	Capacitor					
C12	0.1	Capacitor					
C13	0.1	Capacitor					
C15	0.1	Capacitor					
C16	0.1	Capacitor					
C17	0.1	Capacitor					
C18	0.1	Capacitor					
C19	0.1	Capacitor					
C2	0.1	Capacitor					
C3	0.1	Capacitor					
C6	0.1	Capacitor					
C9	0.47	Capacitor	1812	X7R or better	C1812X7R500474KNE	1	Venkel
C14	10	Capacitor	B	Tantalum, 10v	TA016TCM106KBN	3	Venkel
C20	10	Capacitor					
C5	10	Capacitor					
C8 1mm Plastic	43 pF	Capacitor	805	NPO/COG	C0805COG500470JNE	1	Venkel
C8 200HCS	120 pF	Capacitor	805	NPO/COG	C0805COG500121JNE	1	Venkel
U4	MC10H116FN	IC, ECL line receiver	PLCC20		MC10H116FN	1	Motorola
U5	TL431CD	IC, Voltage Regulator	SO-8		TL431CD	1	T.I.
L1	CB70-1812	Inductor	1812		HF30ACB453215	1	TDK
R12	4.7	Resistor	805	5%	CR080510W4R7JT	2	Venkel
R13	4.7	Resistor					
R20	12	Resistor	805	5%	CR080510W120JT	1	Venkel
R10	15	Resistor	805	5%	CR080510W150JT	1	Venkel
R5	22	Resistor	805	5%	CR080510W220JT	1	Venkel
R16	51	Resistor	805	5%	CR080510W510JT	4	Venkel
R17	51	Resistor					
R18	51	Resistor					
R19	51	Resistor					
R21	62	Resistor	805	5%	CR080510W620JT	1	Venkel
R8 1mm Plastic	301	Resistor	805	1%	CR080510W3010FT	2	Venkel
R9 1mm Plastic	301	Resistor					
R8 200HCS	82.5	Resistor	805	1%	CR080510W82R5FT	2	Venkel
R9 200HCS	82.5	Resistor					
R6	91	Resistor	805	5%	CR080510W910JT	2	Venkel
R7	91	Resistor					
R11 1mm Plastic	1K	Resistor	805	1%	CR080510W1001FT	1	Venkel
R11 200HCS	475	Resistor	805	1%	CR080510W4750FT	1	Venkel
R14	1K	Resistor	805	5%	CR080510W102JT	6	Venkel
R15	1K	Resistor					
R22	1K	Resistor					
R23	1K	Resistor					
R24	1K	Resistor					
R25	1K	Resistor					
Q1	BFT92	Transistor	SOT-23		BFT92	2	Philips
Q2	BFT92	Transistor					
Q3	MMBT3904LT1	Transistor	SOT-23		MMBT3904LT1	1	Motorola
U1	74ACTQ00	IC			74ACTQ00	1	National
U2	HFBR-1527	Transmitter			HFBR-1527	1	HP
U3	HFBR-2526	Receiver			HFBR-2526	1	HP

HEWLETT® PACKARD

DC to 10 MBd Versatile Link with Plastic Optical Fiber or Hard Clad Silica Fiber (HCS®) for Factory Automation and Industrial Control Applications

Application Note 1080

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HCS® is a registered trademark of SpecTran Corporation

I. Introduction

This application note discusses the functions and features of the **New 10 MBd HFBR-0508 Fiber Optic Versatile Link**, which is designed for a variety of industrial applications. These include serial data interfaces in robots, machine tools, assembly and printing machines, and gate-drive circuits in frequency inverters. Circuit design hints and other subjects not found in the product data sheet will also be presented. The reader can use this information to design reliable fiber-optic links based on plastic optical fibers (POF) for distances below 50 m and hard clad silica (HCS®) fibers for distances up to 500 m.

Further information about fiber-optic link design can be found in Application Briefs AB 73 and AB 78, and Application Notes AN 1035 and AN 1066, which are listed in appendix VII. Hewlett-Packard applications engineers or your local certified distribution application engineers are available for further design assistance.

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1. Interconnects without Crosstalk

Fiber-optic technology is completely changing data communications, particularly in industrial environments, where data must be transferred between machines more quickly than ever before. HP believes that fiber optics is replacing copper cabling in many of these applications because of the wide range of advantages inherent to fiber cable. Glass and plastic fibers, being dielectric materials, are completely immune to stray electromagnetic fields, which are common in industrial applications that use motors and power switches. These fibers can be placed in a duct alongside high-voltage metal cables without being susceptible to crosstalk. This feature simplifies system installation. Twisted-pair copper cables require a minimum distance from power lines to guarantee error-free data transfer.

2. International EMC Regulations

Due to increasingly stricter international control over electromagnetic compatibility of electronic equipment, manufacturers often cannot legally sell their products in many countries unless specific immunity and emission limits are met. These limits are based on standards such as FCC, VCCI, EN, CISPR, IEC, VDE, and so forth. For example, beginning January 1, 1996, all equipment and systems that will be sold into the European Union have to meet European EMC standards, otherwise they can be excluded from the market. The generic standards for the industrial field are EN 50081-2 (emission) and EN 50082-2 (immunity). In many applications design engineers do not have a cost-effective alternative to fiber optics if their systems must meet the national or international regulations for electromagnetic compatibility.

3. Fiber Optic Connectors vs. Electrical Connectors

In the past, many design engineers were reluctant to design with fiber optics. Terminating fiber cable was more time consuming than connecting twisted-pair wire because fibers required epoxy and their ends needed to be polished. Large-core polymer optical fiber [POF] and the new crimp and cleave technology for the Versatile Link Snap-in connector (V-System) allow fiber optic cables to be terminated more easily than shielded twisted-pair cables, while offering an electromagnetic-compatible communication link. This is a very strong reason for using fiber optic cables, a reason that the installation and service divisions of a company should also accept.

4. Galvanic Insulation

Ground-loop currents due to different ground potentials are a common problem in industrial communication networks. Ground loops and their associated noise problems are totally eliminated by the insulation characteristics of fiber, allowing a straightforward and fast system integration. In addition, the insulating property of glass and plastic fibers is ideal for many monitor and control functions needed in high-voltage applications. For intrinsically safe applications, which are

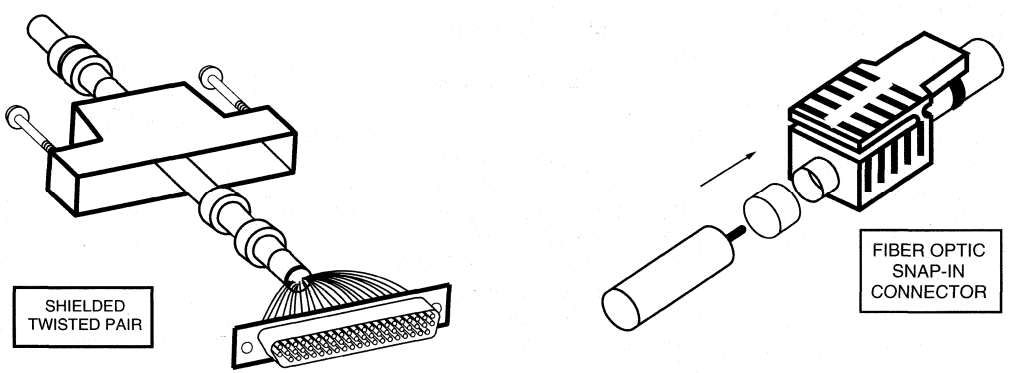


Figure 1. Comparison of Shielded Twisted Pair vs. Fiber Optic Snap-in Connector.

common in the chemical industry, fiber optics is easy to qualify and is also the best medium for connecting one electrical device to another through an isolation barrier.

II. Product Description

1. Housing and optical port
The Versatile Link family has been used successfully in many different industrial applications based on plastic fibers. Users have the benefit of a reliable system that is easy to install in the field. The compact package is made of a flame retardant (UL V-0) material in a standard, six-pin DIP. Transmitters or receivers can be stacked together, creating duplex optical ports that save printed circuit board space and avoid fault connections. The conductive housing of the HFBR-2528 receiver provides an excellent EMI shield. The color-coded packages eliminate confusion between transmitters and receivers. A plug protects the optical port during auto-insertion and soldering.

The Versatile Link package uses an active alignment system to ensure proper coupling between the fiber and the optoelectronic converter. Figure 3 illustrates how the alignment system operates. The precision-molded lens on the insert is located at the bottom of a depression in the shape of a truncated cone. The connector is inserted into the package; the jaws of the housing force the bevelled end of the connector into the cone-shaped depression. This accurately centers the fiber directly above the molded lens on the insert and ensures efficient, reliable and repeatable connections.

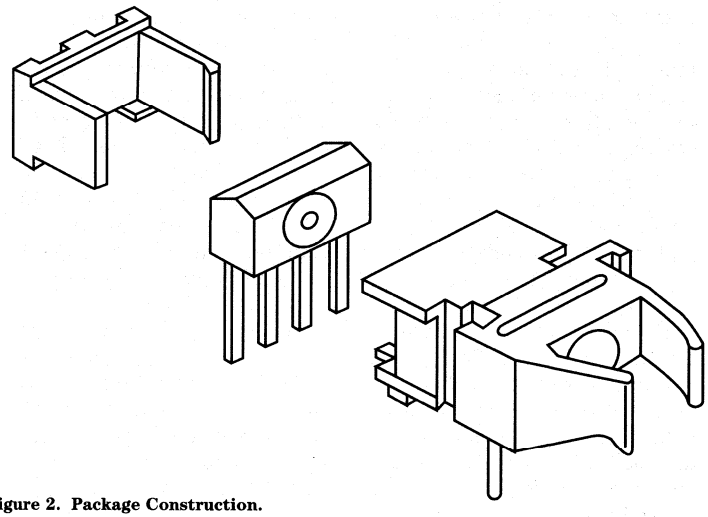


Figure 2. Package Construction.

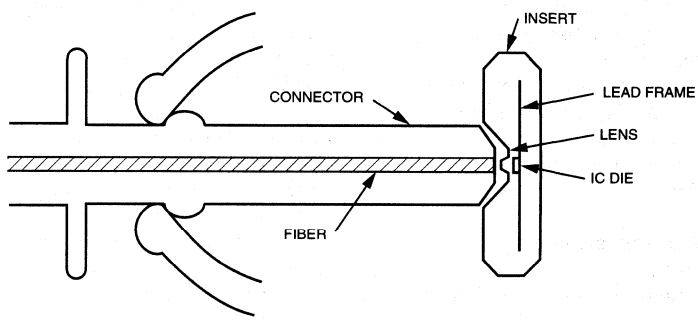


Figure 3. Connector Alignment to Transmitter LED or Receiver IC.

2. Transmitter Technology
The new HFBR-1528 transmitter uses a high quantum efficiency LED based on a new HP AlInGaP technology. At a 60 mA drive current, the coupled power into a 1 mm POF is typically -3 dBm, a 6 dB improvement over previously used transmitters. With a center wavelength of 650 nm at room temperature, the transmitter is in the minimum attenuation window of the POF. Typical link distances of 100 m with low-cost plastic fibers are now a reality. When using the

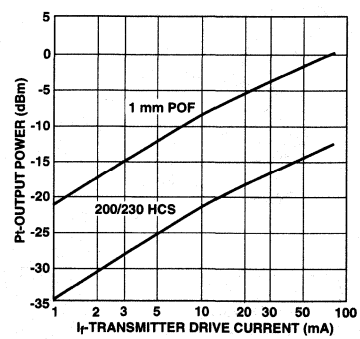


Figure 4. Typical Transmitter Output Power vs. Drive Current.

200 μm HCS fiber link, 500 m distances are possible. In addition to the higher coupled power, the optical rise and fall times have become much faster, allowing much simpler LED drive circuits without the need for peaking and pre-biasing for data rates of 10 MBd.

3. Receiver Technology
The new HFBR-2528 receiver with its TTL/CMOS-compatible output is specified for data rates from dc to 10 MBd NRZ (non-return to zero). It has a sensitivity of -21 dBm peak with 1 mm POF, or a sensitivity of -23 dBm peak with 200 HCS® fiber. Propagation delay times t_{PLH} (output low to high) and t_{PHL} (output high to low) are equally distributed to achieve pulse-width distortion (PWD) of less than ±30 ns over a large input power range. As a result, LED drive current adjustments for different link lengths and fiber types are unnecessary.

A patented first-bit PWD correction circuit makes the HFBR-2528 the ideal product for arbitrary duty-cycle links or for the use in frequency inverters such as gate-drive applications. Other products on the market with similar optical and electrical specifications require the transmission of overhead bits prior to the data because of heavily distorted first bits. Therefore, the user has to add additional circuitry to transmit a preamble prior to the data bits, making the transmit and receive circuit more complex and costly. For better electromagnetic compatability, a conductive housing material has been chosen for shielding the receiver in electromagnetically polluted industrial environments.

4. Types of Fiber Optic Cables
Historically, glass fibers have been used in long-haul telecommunication links and local-area networks because of low attenuation and large bandwidth. Ethernet and FDDI (Fiber Distributed Data Inter-face) standards, for example, have specified multimode 62.5/125 μm glass fibers. These small-core fibers need high-precision connectors to minimize the coupling loss. For industrial application, fibers with lower-cost connectors, which are easier to install and less sensitive to dirty environments, are required. For these applications, 1 mm POF (Polymer Optical Fibers) and 200 μm HCS (Hard Clad Silica) fibers are the best media.

While there are many types of fiber-optic cables (a cable is composed of a fiber and a jacket), only two types, 1 mm POF and 200 HCS, are specified for use with Versatile Link POF and HCS Snap-In Connectors. These step-index fibers are made from silica (HCS) or a polymer (POF) in which the core has a higher refractive index than the cladding. A 2.2 mm jacket around the fiber protects against mechanical or thermal damage and increases the strength of the cable.

4.1. Polymer Optical Fiber (POF)
The large-core diameter (980/1000 μm) and numerical aperture of the POF (Polymer Optical Fiber) are well matched to the large effective diameter and numerical aperture of the optical ports, allowing the power launched into the core to be as high as 0 dBm with the HFBR-1528 transmitter. The POF also offers comparably low-cost termination, which can be done

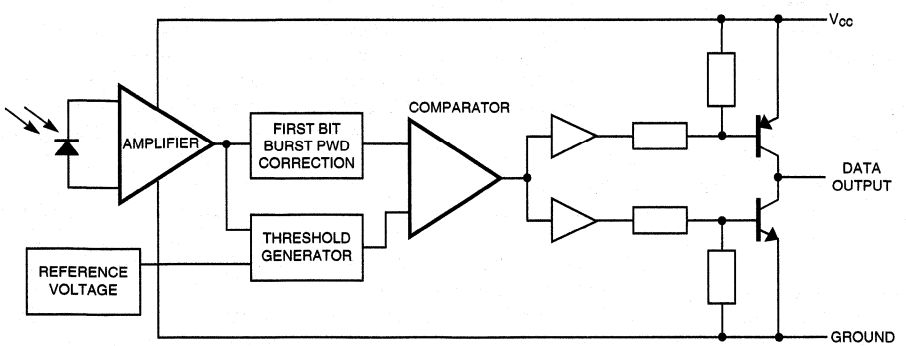
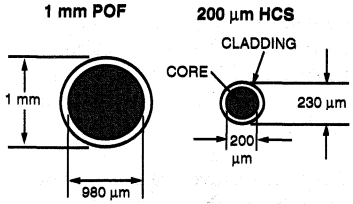


Figure 5. Receiver Block Diagram.



PARAMETER	POF 1 mm	HCS 200/230 µm
TENSION (60 min) TENSION (10 YEAR)	50N 1N	100N 25N
BEND RADIUS (1H)	25 mm	10 mm
FLEX	1,000 X	50,000 X
ATTENUATION (660 nm)	200 dB/km	6 dB/km
NA	0.47	0.37
INSTALLATION TEMPERATURE	-20°C TO +70°C	-20°C TO +85°C
FLAMMABILITY	VW1	RISER PLENUM LSZH

Figure 6. Polymer vs. Hard Clad Silica Cables.

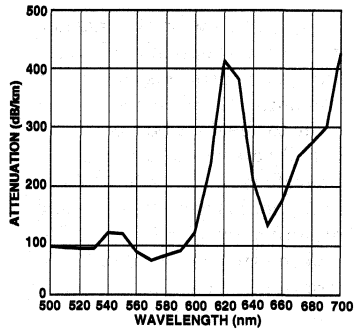


Figure 7. Attenuation vs. Wavelength for POF.

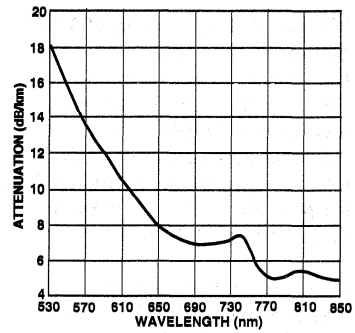


Figure 8. Typical Attenuation vs. Wavelength of HCS Fibers.

"in the field" in less than a minute using a simple and inexpensive crimping and cutting procedure. The attenuation minimum is at 650 nm and is typically about 0.2 dB/m. It should be noted that the spectrum of the new transmitter has a center wavelength at 650 nm at the minimum attenuation of the POF.

4.2. Hard Clad Silica Fiber (HCS)
Step-index silica fibers, such as PCS (Plastic Clad Silica) or HCS® (Hard Clad Silica) fibers with a large-core (200 µm diameter compared to glass fibers with 62.5 µm core diameter) permit the use of low-cost transmitter/receiver lensing systems. Because of the high attenuation in the visible red wavelength range, PCS fibers are commonly used in a lower attenuation window with higher-cost infrared LEDs. The fiber with the lowest attenuation in the visible red wavelength range is the HCS fiber. At 650 nm the attenuation is typically 8 dB/km.

The core of the HCS fiber is silica and the cladding is a proprietary hard polymer that also acts as a strength enhancer and makes it impervious to moisture and impurities. High temperature specifications for extended industrial temperature ranges, and UL ratings for plenum and riser applications are also available.

The snap-in V-System connectors can be crimped directly onto the HCS fiber because the proprietary hard cladding bonds to the silica core material, thus eliminating the need for messy epoxies. A patented cleaving tool cuts the excess fiber protruding from the connector end. Due to the simplicity of the termination process, the Versatile Link Snap-In connector can be mounted in less than 45 seconds.

III. Fiber Optic Link Design

The HFBR-0508 family is designed and characterized for data rates from dc to 10 MBd; Hewlett-Packard specifies link length for 1 mm POF fibers (0 to 60 m) and 200 µm HCS fibers (0 to 500 m). Power supply variations, connector coupling loss and temperature drift effects are part of the guaranteed data sheet specifications. In addition, a 3 dB margin takes aging into account. HP specifies the link performance using the transmitter and receiver interface circuits described in the product data sheet, which gives HP customers the maximum available design security. The following considerations will help the design engineer to become more familiar with low-cost, fiber-optic link design and gives guidelines to optimize the link performance for particular applications.

1. Link Length Considerations
A fiber-optic system basically consists of an LED, a length of fiber, and an optical detector. The LED transmitter, modulated by the electrical input signal, couples light into the fiber. The light travels along the fiber to an optical detector, which converts the light into an electrical signal again. The important specifications for fiber-optic links are how much light is coupled into the fiber, how much light the

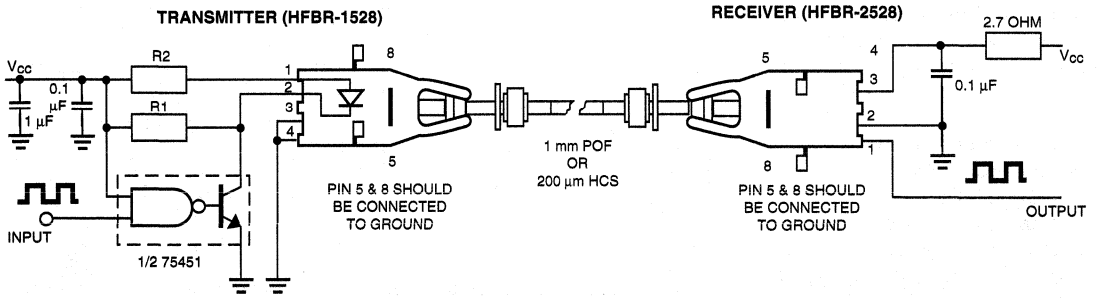


Figure 9. Versatile Link Set-Up.

receiver needs to function properly, and how much light is lost in the fiber between the transmitter and the receiver.

Depending upon the fiber length and wavelength of the signal source, if data rates are very high (125 MBd or greater), the optical signal is distorted. This effect, called dispersion[3], limits the bandwidth of the fiber-optic system. Fortunately, in most industrial communication systems the data rate is less than 10 MBd and the dispersion effect contributes only if the link length exceeds 100 m with POF or 1000 m with HCS Fibers. Below these values the links are limited by attenuation, so a straightforward optical power budget calculation is the only consideration.

1.1 Optical Power Budgeting Computation

The optical power budget is the difference between the output power of the transmitter and the sensitivity of the receiver. The maximum length of the optical fiber is determined by the attenuation of the fiber, additional losses due to feed-through connections and a "safety factor" called optical power margin (see

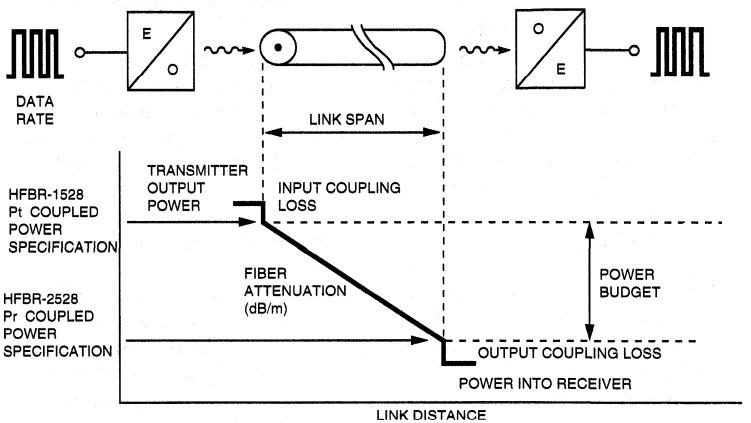


Figure 10. Fiber Optic Link Main Parameters.

chapter III/1.4). Formula III/1 gives the maximum link length for worst-case conditions:

Equation III/1:

$$l(\max) = \frac{P_T(min) - P_{RL,\,min} - IL - OPM}{\alpha(\max)} \quad (m)$$

$P_T(min)$:	Minimum coupled power of transmitter (dBm)
$P_{RL,\,min}$:	Sensitivity of the receiver (dBm)
IL:	Sum of insertion loss of feed-throughs (dB)
OPM :	Optical power margin, which accounts for LED degradation, supply voltage variation, etc. (dB)
$\alpha(max)$:	Maximum attenuation of fiber (dB/m)

Versatile Link transmitter and receiver specifications account for coupling losses to and from 1 mm POF or 200 µm HCS fiber.

1.2. Dynamic Range

An important link design consideration is the receiver's optical dynamic range, the difference between sensitivity ($P_{RL,\,min}$) and overdrive conditions ($P_{RL,\,max}$) : in other words, the dynamic range specifies the minimum-to-maximum link length. Exceeding the dynamic range of the receiver may lead to an increase in PWD. The maximum allowed power level of the receiver specifies the minimum link length needed to avoid overdrive condition. The maximum optical power that the HFBR-1528 can launch, however, is well matched to the HFBR-2528 receiver's overdrive characteristics. If the LED drive circuit recommended in the HFBR-1528 data sheet is used, the transmitter cannot over-drive the HFBR-2528 receiver even when the length of the fiber-optic cable is virtually zero meters.

Equation III/2:

$$l(\text{min}) = \frac{P_T(\text{max}) - P_{RL,\,max}}{\alpha(\text{min})} \quad (\text{in m})$$

$P_T(\text{max})$: Maximum coupled power of transmitter (dBm)

$P_{RL,\,(\text{max})}$: Maximum optical power level of receiver (dBm)

$\alpha(\text{min})$: Minimum attenuation of fiber (dB/m)

The extremely large dynamic range of the HFBR-2528 receiver typically allows room-temperature distances from 0 to 100 meters when using 1 mm plastic fibers. Typically, LED current adjustments are not needed as the length of the plastic fiber can vary from 0 to 100 meters at room temperature, and the maximum adjustment-free distances possible over the temperature range are specified in the HFBR-0508 series data sheet.

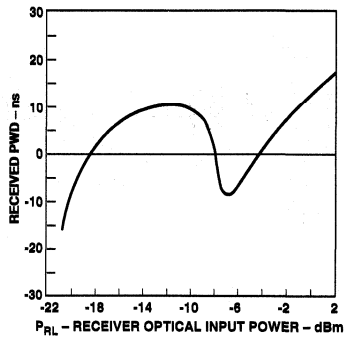


Figure 11. Typical Receiver Pulse-Width Distortion vs. Optical Input Power at 10 MBd.

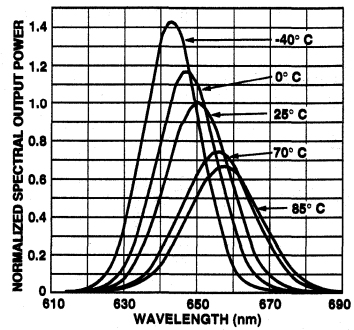


Figure 12. Typical Normalized Optical Spectra to Peak at 25°C.

1.3 Temperature Drift Considerations

The data sheet includes the transmitter output power range for ambient temperatures at T_A = 25°C, T_A = 0 to +70°C, and T_A = -20°C to +85°C, in addition to the guaranteed link length specifications. But by knowing and understanding all different temperature drift effects that the link depends on, the design engineer will be able to optimize the link performance, particularly, the maximum fiber length.

The output power of the transmitter is inversely proportional to the junction temperature, resulting in a lower output power at high temperatures ($\Delta P_T/\Delta T$).

Equation III/3:

$$P_T\,(T) = P_T\,(25) - \frac{\Delta P_T}{\Delta T} \bullet (T - 25)$$

$P_T(T)$: Output power at desired temperature (dBm)

$P_T(25)$: Output power at room temperature specified in the data sheet (dBm)

$\Delta P_T/\Delta T$: Output power temperature coefficient (dB/°C)

The forward voltage ($\Delta V_F/\Delta T$) of the LED will drop with an increase in temperature, causing an increase of drive current, which partially compensates for the decreasing output power.

Equation III/4:

$V_F(T)$: Forward Voltage at desired temperature (V)

$V_F(25)$: Forward Voltage at room temperature, specified in the data sheet (V)

$\Delta P_T/\Delta T$: Forward Voltage temperature coefficient ($\Delta V/\Delta$°C)

The center wavelength of the LED transmitter, typically 650 nm at room temperature, changes wavelength as the temperature changes. In the POF data sheet, attenuation is specified at 660 nm

because of compatibility with the older type, lower output power 660 nm GaAsP transmitters. At room temperature the center wavelength of the new AlInGaP transmitter is exactly in the minimum attenuation window of the POF. Therefore, the optical power budget allows a longer link distance at 25°C than specified in the data sheet. Attenuation at 650 nm is about 0.05 dB/m less than at 660 nm, which permits a 65 m link . (Please see note 3 in the HFBR-0508 Series data sheet. [5])

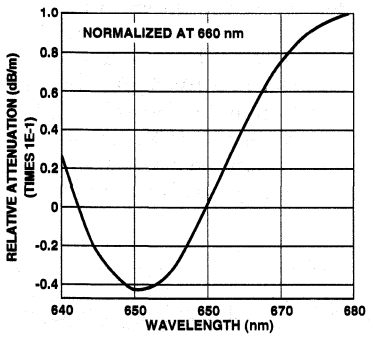


Figure 13. Typical Normalized Spectral Attenuation of 1 mm POF.

Because of the complexity of the receiver circuit IC, a detailed discussion about sensitivity temperature drift is beyond the scope of this application note. Drift effects are specified in the product data sheet and one should not be concerned about them.

1.4. Reliability Considerations

The service lifetime of the fiber-optic link is, however, quite often a concern. One can separate link reliability into transmitter, receiver, connector and fiber reliability. HCS fibers are known to be very stable under harsh ambient conditions and have been qualified for 30-year lifetimes. POFs are estimated for up to 20-year lifetimes. Short-term and long-term bend radius, tensile load, flexing, as well as the mechanical properties of the connectors are specified in the cable data sheet [8]. A detailed discussion about fiber [11,12] and connector [8] reliability is beyond the scope of this application note.

More of a concern is the useful lifetime of short-wavelength LED transmitters, which must be taken into account in power budget calculations. It can be assumed that the receiver sensitivity will not change over time. The transmitter light output reduction is a function of junction temperature, drive current, and endurance time. The useful lifetime of the LED transmitter is typically defined when the initial light output is reduced by 3 dB. Reliability tests of the HFBR-1528 transmitter project a median useful life of 9 years at -3dB, 85°C, 50 % duty cycle, and forward current equal to 60 mA. Therefore, the optical power budget must be decreased by the expected reduction in light output at the end-of-life specification. More detailed information can be found in the reliability data sheet [6].

Table III/1: Projected useful life for various temperatures, where end of life is defined as a 50% drop (-3dB) in light output.

I_F [mA] 50% DC	T_A [°C]	Median Useful Life [y]	90% Survival Life [y]
60	85	9	4
60	70	17	8
60	55	33	15
60	40	68	32

1.5. Connector Loss

Connector coupling losses at the transmitter and receiver are already included in the data sheet specifications. Connector coupling losses due to connections through bulkhead adapters need to be determined. The following table shows the minimum and maximum insertion loss specifications for HP's 1 mm POF bulkhead connections. As the number of bulkhead connections increases, the range of losses increases, as does the magnitude of the losses. Coupling loss characterization of special bulkhead connectors for the 200 µm HCS fiber was not completed when this application note was printed.

Table III/2. Feed Through Loss Specifications.

Part No.	Fiber Size	Min. Loss	Typ. Loss	Max. Loss
HFBR-45X5	1 mm POF	0.7 dB	1.5 dB	2.8 dB

1.6. Coupling Loss

If light from a larger-core fiber is coupled into a smaller-core fiber, a significant loss of optical power can be measured. The loss is a function of the difference in area (d) and the numerical aperture (NA), and is expressed by the following formula:

Equation III/5:

$$IL(dB) = 20 \bullet \log \frac{d1}{d2} + 20 \bullet \log \frac{NA1}{NA2}$$

d1: Emitting fiber diameter
d2: Receiving fiber diameter
NA1: Numerical Aperture emitting fiber
NA2: Numerical Aperture receiving fiber

Light from a smaller core fiber will be coupled into a larger core fiber without area and NA losses.

2. Transmitter Drive Circuits

LED-based transmitters are easy and simple to drive because the current through the LED is proportional to the optical output power. The current can be amplitude modulated using only a switching transistor and a single resistor in series with the LED. Because of the simplicity of the drive circuit, the design engineer has many options to realize this function. As mentioned previously, the HFBR-0508 link performance is guaranteed when using the drive circuit in the data sheet (see also 2.2), as it meets most application requirements. The pros and cons of a few other approaches that will help design engineers to optimize their link performance for specific applications are discussed in the following section.

2.1. Pros and Cons of Parallel and Series Transmitter Drive Circuits

Basically, two methods exist for driving LEDs. One uses a series driver (Figure 9), the other is based on a parallel driving scheme (Figure 14). Series driving circuits consume only half the power but generate higher transient noise in the power supply line when the LED current is switching. The parallel driver uses a constant current from the power supply rail, thus minimizing power supply noise, which could couple into the receiver and degrade sensitivity. The parallel drive circuit also presents a very low impedance to the LED junction during turn off. This low impedance rapidly discharges the junction and quickly extinguishes the optical output of the LED.

One should keep in mind that the transmitter drive circuit topology contributes to the overall pulse-width distortion (PWD) of the fiber optic link. Therefore, it is important that the optical rise and fall times are fast compared to the symbol time. The transmitter propagation delay times, t_{PLH} and t_{PHL}, should also be equally balanced for the PWD of the entire link to be low. Fortunately, the HFBR-1528 transmitter has rise and fall times that are fast enough to be switched without peaking and prebias[3] for data rates as high as 10 MBd. This keeps the drive circuit as simple as possible. Drive circuits for rise and fall times on the order of 3 ns are discussed in AN1066[3].

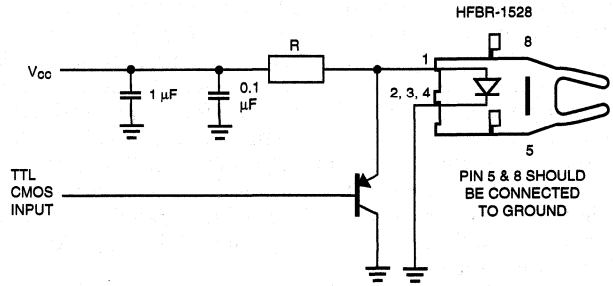


Figure 14. PNP Shunt Drive Circuit.

2.2. Series Driver Circuit using Standard TTL Buffer ICs

Data sheet Drive Circuit

The driver circuit, Figure 9, is designed in such a way that the LED is in series with the open-collector output of the driving gate. Resistor R2 sets the drive current through the LED, and resistor R1 provides a discharge path when the LED forward current is turned off.

Equation III/2:

$$R1 = \frac{Vcc\text{-}Vce\text{-}V_F}{I_F}$$

The low-impedance path R1 quickly discharges the LED, decreasing the optical fall time. A 2 kOhm resistor was empirically found to be an optimum value for best PWD. It is important to note that capacitors C1 and C2 near the LED anode filter the noise in the power supply line during switching periods.

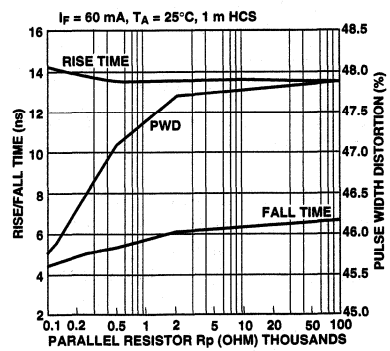


Figure 15: Typical Optical Switching Speed vs. Parallel Resistor R1.

Figure 16 shows how LED forward current deviates from the intended or nominal room temperature design value when using a series drive circuit, due to the following factors:

a. part-to-part variations in LED forward voltage,

b. current-limiting resistor tolerance,
c. power supply tolerance, and
d. variations in the Vce saturation potential of the 75451 peripheral driver.

Figure 16 also shows that as Vcc increases, the total variation in LED forward current, due to other circuit tolerances, is minimized.

The recommended LED driver shown in Figure 9 takes advantage of the negative temperature coefficient of the HFBR-1528 LED forward voltage. When temperature rises, the forward voltage of the LED decreases and a greater percentage of the supply potential must be dropped across resistor R2. As temperature increases and LED forward voltage declines, the potential difference across R2 increases and Ohm's law dictates that the current through R2 and the HFBR-1528 will increase. This increase in the drive current partially equalizes the reduced light output due to the negative output-power temperature coefficient.

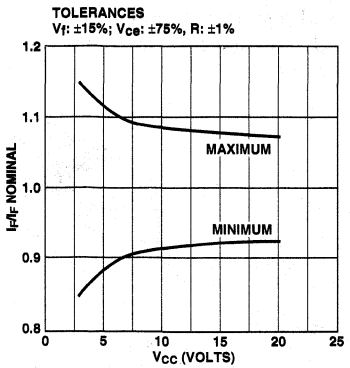


Figure 16. Output Power Variation vs. Supply Voltage and Components Tolerances.

The coupled power into 1 mm POF and 200 µm HCS is specified for minimum and maximum values versus the temperature range for 20 mA and 60 mA. Intermediate power levels can be calculated based on Figure 2 in the HFBR-1528 data sheet. At drive currents less than specified in the data sheet, the part-to-part variation of the output power increases.

2.3. The Simplest LED Transmitter Shunt Drive Circuit

The circuit shown in Figure 14 is a simple-shunt drive transmitter circuit that uses a pnp transistor. The primary feature is its simplicity: only two components are required and the circuit can be interfaced to TTL or CMOS gates without additional components. The circuit is also fast for several reasons:

- the transistor never saturates,
- it presents a very low impedance during turn off of the LED, and
- the emitter base junction voltage "prebiases" the LED junction resulting in a faster optical rise time

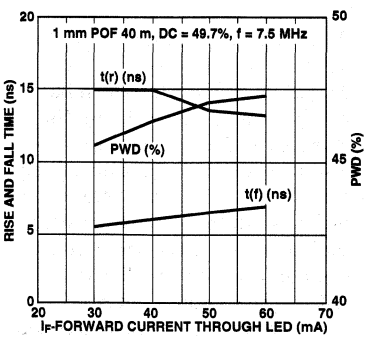


Figure 17. Switching Speed vs. Drive Current.

In addition, the pnp drive circuit generates low power-supply ripple because of the constant load during LED switching. The drawback is increased power consumption due to the constant current flow through the bias resistor.

3. Receiver Interface Circuit Design

The HFBR-2528 receiver has a push/pull digital output. It is capable of sourcing and sinking current as high as ±6 mA (receivers HFBR-25X1,2,3,4 need pull-up resistors) and can drive CMOS and TTL logic families without external resistors. HP recommends that an RC first-order, low-pass filter (see Figure 9) be used to minimize the power-supply noise between the ground and power supply terminals of the receiver. This arrangement will meet the power-supply rejection specification. The bypass capacitor should be connected as close as possible to the power supply terminals of the HFBR-2528 receiver. A ground plane underneath the conductive receiver housing and connected to pins 5 and 8 provides an excellent shield against electric fields as high as 8 kV/m, which could otherwise interfere with the receiver IC.

3.1. Sensitivity

DC-coupled receivers, such as the HFBR-2528, are specified for sensitivity at different conditions than ac-coupled receivers[3] in which the bit-error ratio (BER) is an important criterion. For the HFBR-2528, sensitivity is the minimum optical power level for a PWD of less than |30| ns, measured with a 50 percent duty cycle, square-wave signal.

3.2. Off-State-Limit

HP recommends that no light be coupled to the receiver when it should remain in the logic-high state. In some instances, it might not be possible to turn the transmitter totally off. But the power delivered to the receiver should be always less than -42 dBm for 1 mm POF or -44 dBm for 200 µm HCS fibers to ensure that the output does not randomly change state.

3.3. Overdrive Limit

The overdrive limit is specified where the PWD exceeds | 30 | ns. For example, at low temperatures, power levels can be above $P_{RL,max} > +1$ dBm and PWD may exceed 30 ns, when using a driver circuit topology other than specified in the data sheet. The transmitter application circuit, recommended in the product data sheet, decreases the LED drive current at low temperatures because of the higher voltage drop across the LED transmitter.

IV. Manufacturing Consideration

1. Handling and Assembly Guidelines

Non-stacked Versatile Link parts do not require special handling during assembly onto printed circuit boards. HP advises, however, that normal static precautions be taken in handling and assembly of these components to prevent damage and/or degradation, which may be induced by electrostatic discharge (ESD).

HFBR-1528	Class 3
HFBR-2528	Class 1

ESD Human Body Model
Mil. Std. 883 Method 3015

All transmitters and receivers are delivered to customers in standard tubes for dual in-line packaged components and can be easily picked and placed with auto-insertion machines. During soldering, an optical port plug is recommended to prevent contamination of the port. Solderability is specified under Mil. Std. 883 Method 2003. Please follow the maximum time and temperature guidelines given in the product and reliability data sheet. Water-soluble fluxes, not rosin-based fluxes, are recommended.

2. Connectoring Guidelines

2.1. Plastic Fiber

Plastic optical cables can be terminated in less than 30 seconds by using Versatile Link Snap-in connectors and standard tools[27]. After cutting the cable to the desired length, 7 mm of the fiber jacket should be removed with a 16-gauge wire stripper. The crimp ring and connector are positioned then crimped over the end of the cable. Any excess fiber protruding from the connector end may be cut off. For better light coupling the fiber end must be polished by using 600-grit abrasive paper. See the detailed connecting instruction in the appendix of the fiber-optic cable data sheet [8].

2.2. 200 µm HCS Crimp and Cleave Termination

The 200 µm HCS fiber can be easily terminated by using the Snap-in V-System connector and the HFBR-4584 termination kit [28], which contains one fiber buffer strip tool, one cable strip tool, one pair of scissors and a diamond cleaving tool. The entire process does not need either epoxy or polishing and so can be completed in less than a minute. The following is an abstract from the detailed Crimp and Cleave Connectoring manual:

1. Remove cable jacket
2. Remove fiber buffer
3. Apply first crimp ring to fiber buffer
4. Crimp connector to jacket
5. Cleave the fiber end

2.3. Optical Port Protection

During equipment manufacture HP recommends using the optical port plug inserted into the transmitter and receiver when delivered to prevent contamination of the port. During the operational life of the communication equipment the port plug may be misplaced or lost. Therefore, a very simple "optical short circuit" between the transmitter and receiver can be constructed of a short length of 1 mm POF and a duplex connector (Figure 18). A small ring and chain can be fed through the cable opening and screwed to the front or back panel of the system so that the port plug can always be located.

Whenever the connector is inserted the station will receive its own signal and the function of the optical serial interface can be tested. In addition, a warning message telling the user that the serial port is not connected might be displayed on a system monitor.

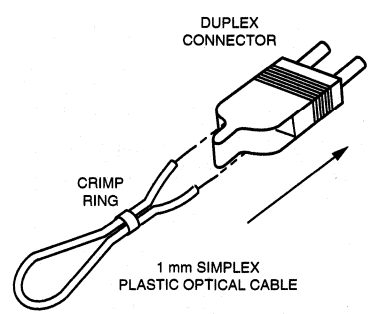


Figure 18. In use Optical Port Protection Connector.

V. Application Examples

1. Introduction to Industrial Communication Networks

Compared to 10 years ago, today's industrial control equipment has changed dramatically. No longer are many single twisted-paired lines from sensors and actuators bundled into one huge and heavy cable and connected to a programmable logic controller. Today, the intelligence is distributed in the network; the actuators and sensors are connected via a bus, star or ring topology to a master unit. Standards committees and user groups have defined serial data rates from several kBd to more than 2 MBd for twisted pair and fiber-optic media interfaces. But these open-system standards do not always meet the application requirements because of speed, noise immunity, and distance specifications. Proprietary networks for critical, real-time applications, for example, must have faster response times than today's standards are specified for. These applications need serial noiseless communication channels with data rates as high as 10 MBd to achieve the desired performance of the control system. At these conditions, it is worth considering the de-facto industry standard HFBR-0508, fiber-optic link for isolated and reliable optical interconnects.

1.1. Interface to RS 422 and RS 485

Many networks are based on an RS-485/422 physical media interface, which are based on a bus topology. Different ground potentials and noise sources may not allow a non-isolated bus structure. Therefore, active star couplers with fiber-optic ports are preferred. Quite often, a mixed topology consisting of fiber cable and twisted-pair wire is desired. In this case, the Versatile Link family is the most cost-effective line of products for fiber-optic inter-repeater links. The Versatile Link's small package allows HP's parts to be assembled into an adapter housing for an electrical-optical converter. One side of the housing holds the electrical subminiture connector to interface with the twisted-pair bus, the opposite side has the duplex, snap-in, fiber-optic connection. Standard "off-the-shelf" line drivers and receivers for RS- 422 and RS-485 [15,16,20] interface between the twisted-pair bus and the TTL receiver output and transmitter input.

While the majority of industrial communication applications are specified for data rates of 2 MBd and below (much lower than the speed of the HFBR-0508 link), the large dynamic range of the HFBR-2528 receiver allows a fiber-optic link to be designed without transmitter optical output power adjustment. This factor makes the installation instruction much simpler and avoids trouble-shooting exercises due to receiver overdrive conditions. Whether the link is anywhere from zero meters up to the maximum length specified in the data sheet or whether the fiber is HCS or POF, the link will work reliably the moment that the power is turned on.

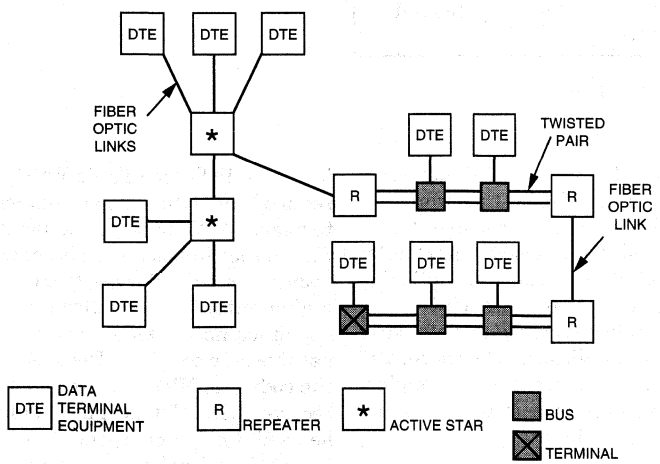


Figure 19. Network Overview with RS 485 TP Bus and Fiber Optic Active Star

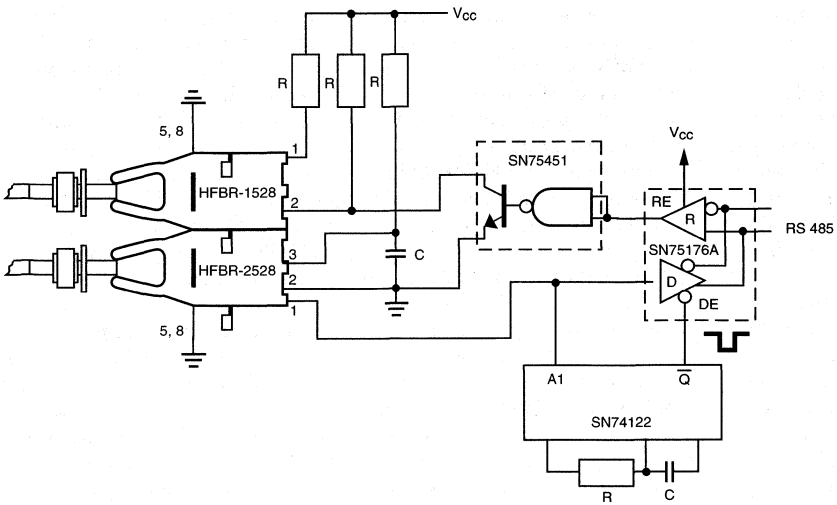


Figure 20. Basic RS 485 Fiber Optic Interface Adapter to Data Terminal.

Table V/1. Link Length Overview of HFBR-0508 for POF and HCS Fibers.

Fiber Type	Guaranteed Link Distance	Temperature Range	Conditions
1 mm POF	0.1 to 50 m 0.1 to 40 m 0.1 to 30 m	T_A = 25°C 0°C< T_A<+70°C -20°C< T_A<+85°C	I_F = 60 mA, 10 MBd
200 HCS	0.1 to 500 m 0.1 to 300 m 0.1 to 100 m	T_A = 25°C 0°C< T_A<+70°C -20°C< T_A<+85°C	I_F = 60 mA, 10 MBd

For more details please see product data sheet!

1.2. Controller Area Network (CAN)

A special controller-area network (CAN), which meets the stringent reliability requirements of automobile manufacturers, has been developed for low-cost, real-time applications in cars. CAN can be found in field buses because of its open-system interface and high noise immunity. Semiconductor manufacturers [18,19,21] offer integrated circuits for ISO layer 1 (Physical) and 2 (Data Link). When using fiber optics the best network configuration is a passive star coupler. The passive star coupler [23, 24, 25 ,29] divides the optical signal from one source into multiple optical signals of nearly equal amplitude. Therefore, all devices connected to the coupler receive the transmitted data at the same time.

In the past, the high insertion loss of the passive star couplers for 1 mm POF (see Table V/2) reduced the optical power budget to nearly 0 dB, making the use of fiber optics impossible. The new transmitter technology, with 6 dB-higher output power, allows expanded networks based on passive star couplers. Because the coding is NRZ, a dc-coupled receiver with TTL output should be used. Design engineers have two choices for the receiver interface. For data rates of 125 kBit/s

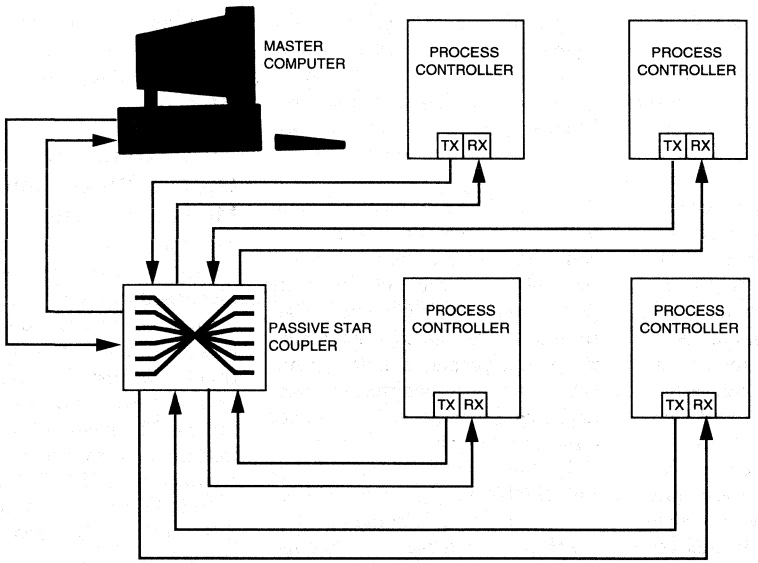


Figure 21. CAN with Passive Star Coupler.

(ISO/DIS 11519-1), they can use the HFBR-25X2 receiver. If the serial bit rate is 1 MBit/s (ISO/DIS 11898), they should consider the HFBR-2528 receiver because of its lower pulse-width distortion (PWD) specification and large dynamic range. The large dynamic range will compensate for the spread of insertion loss by the coupler.

Table V/2: Typical Insertion Loss at 660 nm for 1 mm POF Star coupler.

Ports	Insertion Loss
2•2	4 dB
3•3	7 dB
4•4	7 dB
5•5	10 dB
7•7	11 dB

For detailed specifications, please contact suppliers [23 ,24, 25].

The following equation (V/2) should be used to calculate the maximum possible link length.

The maximum link length is the sum of the distance from the transmitter to the bulkhead connector and from the bulkhead connector to the receiver.

Equation V/2:

$$l = \frac{P_T(\min) - P_{RL,\,min} - IL(\max) - OPM}{\alpha(max)}$$

$P_T(min)$: Minimum coupled power of transmitter in (dBm)

$P_{RL,\,(min)}$: Sensitivity of the receiver [coupled power] (dBm)

IL: Insertion loss measured from input port to output port (dB) of the passive star coupler

OPM: Optical power margin in (dB)

$\alpha(max)$: Maximum attenuation of fiber in (dB/m)

The maximum data rate is also a function of the maximum distance between two nodes, because the propagation delay time must be less than half the bit time. The propagation delay constant for optical signals is 4.8 ns/m in fiber-optic links because the signal speed is equal to the speed of light divided by the refractive index. The propagation delay of the transmitter and receiver are listed in Table V/3. Transmitter and receiver delays must be added to the propagation delay of the fiber to determine the total delay of the fiber-optic link.

2. Gate Driving Using Fiber-Optic Interfaces

With the improvements in the development of power switches such as GTOs and IGBTs, frequency inverters can be operated at higher speed and higher power levels. On one hand, the circuit needed to drive the gates of IGBTs and GTOs has to be fast.

On the other hand, the gate-drives must reliably reject the higher and faster switching transient voltages caused by the large variations in current in the power rails.

Traditional techniques based on transformers for galvanic isolation and shielded cables require very experienced engineers to design a "trouble free" interface. Even so, minimum distance requirements between the signal lines and power units and good ground contacts can make the system larger and more costly than it would be if the features inherent to fiber optics are taken advantage of. In these applications, transformers will become redundant because of the dielectric property of the fiber and the fact that it will easily meet any regulatory requirements of IEC, UL, CSA, CENELEC, VDE, etc. In addition, the fiber is immune to any kind of electromagnetic fields and can be placed alongside power lines without affecting the transmission quality. The result is a simplified design with higher reliability and less sensitivity to system failures during installation and maintenance.

The following aspects should be considered when taking advantage of the many features the new Versatile Link offers for gate-drive applications. These include shielded housing, high-temperature HCS fiber, low PWD, and the fact that the receiver can accept arbitrary duty-cycle. HP recommends one of the transmitter drive circuits from chapter III because the switching speed is a major design issue. Because the link distance is very short in such applications, the drive current can be set to a value as low as 20 mA. The output power at 20 mA is specified in the data sheet and the power budget calculation from chapter III should be followed. The receiver and its conductive housing should be grounded and a good power-supply filter should be used because the isolated power supply is known to be very noisy.

The dead-time specification is one of the most important design parameters. A worst-case propagation delay from the controller to the gate of the power switch has to be computed. For the fiber-optic link, the overall propagation delay time is the sum of transmitter, receiver and fiber delay times. Typical fiber optic link delay times are listed in Table V/3. The PWD is specified in the HFBR-2528 data sheet. Since the speed of light is limited to about 2.99E-8 m/s in a vacuum, photons will travel at a lower speed in dense media such as glass or plastic fibers.

Equation V/2:

$$vp = \frac{c}{n} \quad \text{in m/s}$$

c: Speed of light in vacuum
c = 2.99E-8 m/s
n: Refractive index of the media n =1.5 for PMMA

Table V/3: Typical Propagation Delay Times at 25°C for HFBR-0508 Link with 1m POF

Parameters	Tx(in) to Rx(out) with 1 mm POF	Units
tp LH	140	ns
tp HL	158	ns

To avoid fault connections, which can cause shoot-through conditions in a half bridge, HP recommends that the transmitters for a single half bridge be latched in pairs. Duplex connectors have a key function and will fit into the latched pair in only one position. Therefore, human error, such as mixing the cables, can cause only a fail function and will not destroy the power switches.

VI. Introduction to Optical Power and Loss Measurements

The theoretical methods used to specify optical parameters were discussed in chapter III. Theoretical values must be verified, however, not only by empirical functional tests but also by optical power and loss measurements. The relevant standard for loss measurements on cables and connectors is IEC 874-1. A detailed discussion of all the different methods described in the standard is beyond the scope of this application note. Only the most important methods will be briefly described. The recommendations in this application note for measurement equipment and accessories will help the newcomer to fiber optics, even one with financial constraints, to quickly implement a system.

1. Recommended Equipment and Accessories

The following items are needed: connectors, several meters of cable, transmitters and receivers, and tools to terminate the plastic or HCS cable. The lowest-cost approach is the POF termination kit [27]. For details, please see fiber-optic cable data sheet [8]. One of the Versatile Link transmitters can be used as an optical reference source. Power meters with a large-area Si detector, LED sources for 1 mm POF and 200 µm HCS, and adapter accessories are available from several manufacturers listed in the appendix [26].

1.1. Transmitter Output Measurement

A reference cable of 50 cm should be terminated with a carefully polished connector on each end. The cable is connected to the transmitter and the optical power meter. The coupled power into a 1 mm POF can be read in the display in power (mW) or reference power (dBm).

Equation VI/1:

$$P\ (dBm) = 10 \bullet \log \frac{P(mW)}{1mW}$$

P(mW): Power in mW
P(dBm): Power in decibels referenced to 1 mW

If the detector area is larger than the fiber's cross-sectional area, the coupling loss between connector and detector can be neglected. HP also recommends repeating the measurement with the connections reversed. A different power-level reading will indicate coupling loss variation.

It is also possible to measure the output power of a pulsed transmitter. A 50% duty-cycle pulse gives an average power-level (Pavg) reading. The actual peak amplitude (Ppk) is twice as high (3 dB in referenced power) as the average.

Example: Pavg = -21 dBm
Ppk = -18 dBm

1.2. Receiver Sensitivity Measurement

The transmitter and receiver are linked by a fiber-optic cable and pulsed with the desired data rate at a 50% duty cycle. An optical attenuator or different fiber length is used to lower the power at the receiver while monitoring the pulse-width distortion (PWD). Using a simple vise, one can also construct a gap attenuator by increasing the Z-axis spacing of the two fibers. When the PWD is 30 ns, the fiber is disconnected from the receiver and inserted into the optical power meter. The optical power meter shows the average received power. To calculate the receiver peak-power sensitivity, $P_{RL,min}$, add 3 dB to the reading.

1.3. Cable Attenuation Measurement

First the reference cable is connected to the transmitter and the power meter is set to zero (0 dB). Then the attenuation of the fiber being tested is measured. The power meter displays the incremental change in attenuation. This value is divided by the length of the fiber to calculate the optical loss per meter in dB/m. Typically, longer cables are measured; and so, the attenuation of the reference cable (about 0.1 dB to 0.2 dB) can be neglected. HP recommends repeating the measurement with the connections reversed. A different power reading will indicate coupling loss variation due to connector-port dimension tolerances and/or uneven polished fiber surfaces.

VII. Appendix

1. Literature Reference

[1] Application Bulletin 73; Low Cost Fiber Optic Transmitter and Receiver Interface Circuits
[2] Application Bulletin 78; Low Cost Fiber Optic Links for Digital Applications up to 155 MBd
[3] Application Note 1066; Fiber Optic Solutions for 125 MBd Communication Applications at Copper Wire Prices
[4] Application Note 1035; Versatile Link
[5] Data sheet HFBR-0508 Series; 10 MBd Versatile Link Fiber Optic Transmitter and Receiver for 1 mm POF and 200 µm HCS
[6] Reliability Data sheet HFBR-1527/8
[7] Reliability Data sheet HFBR-2528
[8] Data sheet; Plastic Optical Fiber and HCS Fiber Cable and Connectors for Versatile Link
[9] Fiber Optic Handbook, Hewlett-Packard, Christian Hentschel
[10] IEC 874-1
[11] POF Data book, MRC Techno Research
[12] High Strength, Reliable, Hard Clad Silica HCS® Fibers, Ensign-Bickford Industries
[13] Elektronik Plus, Automatisierungstechnik 1,
[14] EMV Störfestigkeitsprüfung, Fischer,Balzer,Lutz, Franzis Verlag

2. Supplier Reference

[15] Texas Instruments
[16] Motorola
[17] SGS Thomson
[18] Siemens
[19] Philips
[20] Maxim
[21] Intel
[22] Spectran
[23] Kabelwerke Rheinshagen GmbH
[24] MicroParts
[25] Nichimen
[26] a. RIFOCS "V-Kit Measurement Instruments" 557B Power Meter, 253B LED Source; b. Photodyne, Model 18XTA; c. Mitsubishi, Rayon, EMT 100-205
[27] Plastic Fiber Termination Accessories, HFBR -4593 Polishing Kit, HFBR-4597 Plastic Fiber Crimping Tool
[28] HCS Termination Kit, HFBR-4584

Applications

The following abstracts represent application notes that are not published in this catalog. These application notes can be obtained from your local Hewlett-Packard sales office or authorized HP distributor or representative (see section 5).

In the US/Canada, technical literature is available from the Hewlett-Packard Components Group fax-back service at: 1-800-450-9455, or from the Components Sales Response Center at 1-800-235-0312.

AN 1057
Conductive Port Receiver
This application note compares the performance of fiber-optic receivers with conductive ports to fiber-optic receivers with nonconductive ports. It explains how conductive port receivers solve specific problems encountered in some applications and how they help to improve the electromagnetic immunity of part number HFBR-24X6XC, required by such standards as MIL 461 and IEC 801-3. This application note also presents test data that shows why HP's low-resistance conductive port has an advantage over the higher-resistance conductive ports of other manufacturers. Test methods are also included.

Publication No. 5091-6001E

AN1073
HFBR-0319 Test Fixture for 1x9 Fiber-optic Transceivers
This application note focuses on testing fiber-optic transceivers with a 1x9 footprint, and how HP's HFBR-0319 evaluation kit test fixture makes it easy. Attributes of the HFBR-0319 test fixture are discussed including calibration procedures. An example test system circuit diagram for 1x9 fiber-optic transceivers is presented along with PCB artwork, recommended component values, and example results.

Publication No. 5963-2202E
Document ID #11086*

*Application Notes referencing document ID number are available from Fax-Back service.

HEWLETT® PACKARD

Bar Code Components

- **Digital Wands and Slot Readers**
- **Sensors and Sapphire Tips**
- **Intelligent Wands**
- **Digitizer and Decoder ICs**

Data Sheet Index 4-3
Product Selection Guide 4-4
Applications 4-81

HEWLETT® PACKARD

Bar Code Components

Bar Codes are used in a wide range of data entry applications where the combination of speed, simple operation and accuracy are critical.

HP's family of bar code products is designed for ease of use, flexibility, integrity of design, and ruggedness.

HP offers a wide range of products for both OEMs and end users, ranging from optical reflective sensors, tips and encoder ICs, to slot readers, digital wands, and intelligent scanners.

HEWLETT® PACKARD

Bar Code Components Data Sheet Index

- Optical Reflective Sensors 4-7
- High Resolution Optical Reflective Sensor 4-15
- Optical Reflective Sensors 4-22
- Bar Code Reader Tips and Optical Nest Assembly 4-30
- Low Current Bar Code Digitizer IC 4-33
- Single Chip Bar Code Decode IC 4-37
- Programmable Bar Code Decode IC 4-47
- KeyWand Bar Code Reader 4-62
- SmartWand Bar Code Reader 4-66
- Low Current Digital Bar Code Wand 4-71
- Industrial Digital Bar Code Slot Reader 4-75

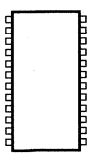
Optical Reflective Sensors

Part	Part Number	Resolution	Wave-length	LED Fwd Current	DC Mode	Pulsed Mode	Comments	Page No.
	HBCC-1570	0.330 mm (0.013 in.)	655 nm	125 mA Peak		•	• Focused emitter and detector in a TO-5 sealed metal package • Photodiode output	4-7
	HBCC-1580	0.185 mm (0.007 in.)	655 nm	100 mA Peak		•		
	HBCC-1590	0.130 mm (0.005 in.)	820 nm	40 mA Peak		•		
	HBCS-1100	0.190 mm (0.0075 in.)	700 nm	50 mA Avg	•			4-15
	HEDS-1300	0.190 mm (0.0075 in.)	700 nm	50 mA Avg	•			4-22

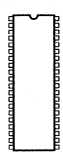
Tips

Part	Part Number	ESD Isolation	Overall Length	Thread Engagement	Poly-carbonate Enclosure	Metal Enclosure	Comments	Page No.
	HBCS-A998	15 kV	18.4 mm (0.725 in.)	2.5 mm (0.098 in.)	•		• Compatible with HP Bar Code Sensors • HBCS-T998 for HBCS-T5XX only.	4-30
	HBCS-A999	15 kV	18.3 mm (0.721 in.)	4.4 mm (0.172 in.)	•			
	HBCS-2999	N/A	15.9 mm (0.625 in.)	2.5 mm (0.098 in.)		•		
	HBCS-4999	N/A	15.7 mm (0.620 in.)	4.4 mm (0.172 in.)		•		
	HBCS-T998	N/A	14.6 mm (0.576 in.)	3.8 mm (0.151 in.)		•		
	HBCS-T999	N/A	14.6 mm (0.576 in.)	3.8 mm (0.151 in.)		•		

Digitizer IC

Part	Part Number	Current Draw	Package	Comments	Page No.
	**HBCC-0500**	4.0 mA w/Sensor	SOIC 24	• Compatible with HP Bar Code Sensors HBCC-15XX Series. • Used in all HP Bar Code Wands	4-33

Decode ICs

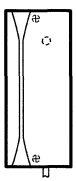
Part	Part Number	Supply Voltage (V)	Supply Current (mA)	Package			Input		Page No.
				40 Pin DIP	44 Pin PLCC	44 Pin QFP	Laser Scanner	Wand/Slot Reader	
	HBCR-1610 Series	4.5-5.5	18 (max) @ 11 MHz 24 (Max) @ 16 MHz	1610	1611	1612		•	4-37
	HBCR-2210 Series	4.0-6.0	18 (Max) @ 5.0 V	2210	2211			•	4-37

Bold Type = New Product

Digital Wands

Part	Part Numbers for Medium Resolution	Case	Switched	Connector		Replacement Parts	Comments	Page No.
				5-Pin DIN	9-Pin D-Sub	Case/Tip		
	HBCS-A300	Polycarbonate		•		HBCS-A991	• Medium Resolution: 0.15 mm (0.006 in.) • LED Wavelength: 655 nm • High and Low Resolution and Strip and Tin also available as built to order product.	4-71
	HBCS-A308	Polycarbonate			•	HBCS-A991		
	HBCS-A200	Polycarbonate	•	•		HBCS-A992		

Slot Readers

Part	Part Numbers	Infrared	Connector		Comments	Page No.
			5-Pin DIN	9-Pin D-Sub		
	HBCS-7100	880 nm	•		• Resolution: 0.19 mm (0.0075 in.) • Case: Metal (Environmentally Sealed) • HBCS-7X50 is the module only • Strip and Tin also available as built to order	4-75
	HBCS-7108	880 nm		•		
	HBCS-7150	880 nm	•			

Smart Wands

Part	Part Numbers for Medium Resolution	Case	Replacement Parts		Comments	Page No.
			Tip	Case/Tip		
	HBSW-8200	Polycarbonate		HBSW-8991	• Medium Resolution: 0.19 mm (0.0075 in.); LED Wavelength: 655 nm • High and Low Resolutions are also available as built to order product • Kit Includes: Wand, User's Manual, and Black Wand Holder • SmartWand Accessory Part Numbers: User's Manual: HBSW-8997 Wand Holder: HBCS-2998	4-66
	HBSW-8205 (Kit)	Polycarbonate		HBSW-8991		
	HBSW-8300	Metal	HBCS-4999			
	HBSW-8305 (Kit)	Metal	HBCS-4999			

Keywands

Part	Part Numbers for Medium Resolution	Connector		Replacement Tip/Case	Comments	Page No.
		5 Pin DIN	6 Pin Mini Din			
	HBKW-1210	•		HBKW-8991	• Medium Resolution: 0.19 mm (0.0075 in.); LED Wavelength: 655 nm • High and Low Resolutions available as built to order product • Kit Includes: Wand, User's Manual, Wand Holder, Interface Adapters, and Quick Start Instructions • KeyWand Accessory Part Numbers: User's Guide: HBKW-1910 Wand Holder: HBKW-1920 Interface Adapters: HBKW-1925	4-62
	HBKW-1220		•	HBKW-1991		
	HBKW-1240 (Kit)	•	•	HBKW-1991		

HEWLETT® PACKARD

Optical Reflective Sensors

Technical Data

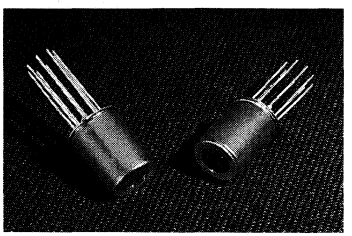
HBCC-1570
HBCC-1580
HBCC-1590

Features

- **Focused Emitter and Detector in a Single Package**
- **TO-5 Miniature Sealed Package**
- **Photodiode Output**
- **Choice of Resolutions (0.13 mm, 0.178 mm, 0.33 mm)**
- **Two Wavelengths Available; 655 nm, 820 nm (see selection guide)**

Description

The HBCC-15XX series sensors are fully integrated modules designed for applications requiring optical reflective sensing. The modules contain a 655 nm (or 820 nm) LED emitter and a photodiode. A bifurcated aspheric lens is used to image the active areas of the emitter and detector to a single spot 4.27 mm (0.168 in.) in front of the package. The output signal is a current generated by the photodiode.



Applications

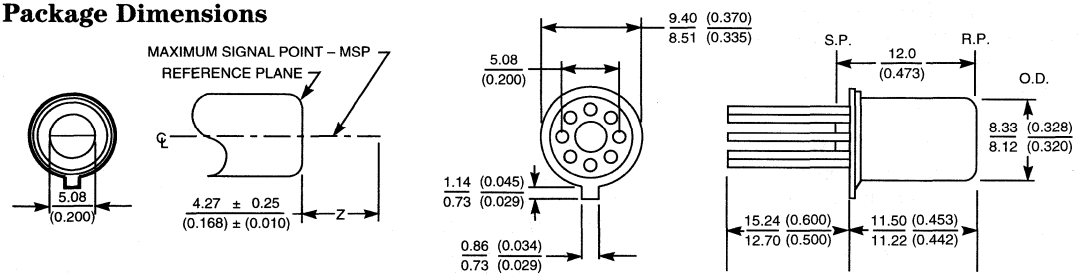
The HBCC-15XX sensors are intended for use with the Hewlett-Packard HBCC-0500 and HBCC-0600 low current digitizer ICs, or

BAR CODE

Selection Guide

Sensor Part Number	HBCC-1570	HBCC-1580	HBCC-1590
LED Resolution	0.33 mm (0.013 in.)	0.185 mm (0.007 in.)	0.13 mm (0.005 in.)
LED Wavelength	655 nm	655 nm	820 nm

Package Dimensions



NOTES:

A. ALL DIMENSIONS IN MILLIMETERS AND (INCHES).
B. ALL UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.
C. THE REFERENCE PLANE (R.P.) IS THE TOP SURFACE OF THE PACKAGE.
D. NICKEL CAN AND GOLD PLATED LEADS.
E. S.P. = SEATING PLANE.
F. THE LEAD DIAMETER IS 0.45 mm (0.018 in.) TYP.
G. O.D. = OUTSIDE DIAMETER OF CAN MEASURED IN REGION ABOVE WELD FLANGE TO MIDWAY OF CAN LENGTH.

with suitable PCB assemblies provided by HP for use with these sensors. The HBCC-15XX sensors have been characterized for use only with Hewlett-Packard's digitizer IC technology. Use of these sensors in designs or applications other than those stated is at the customer's risk.

Mechanical Considerations

The HBCC-15XX series are packaged in a high profile 8 pin TO-5 metal can with a glass window. The LED and photodiode are mounted on a header at the base of the package. Positioned above these active elements is a bifurcated aspheric acrylic lens that focuses them to the same point.

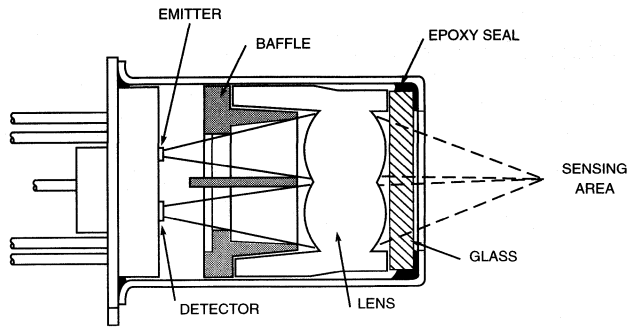
The sensor can be rigidly secured by commercially available TO-5 style heat sinks or 8 pin 0.200 inch diameter pin circle sockets. These fixtures provide a stable reference platform for affixing the HBCC-15XX sensors to a circuit board.

In applications requiring contact scanning (such as bar code reading), protective focusing tips are available. Focusing tips are available in either metal or polycarbonate packages using a sapphire ball as the contact surface. The Hewlett-Packard part numbers are HBCS-2999, HBCS-4999, HBCS-A998, and HBCS-A999.

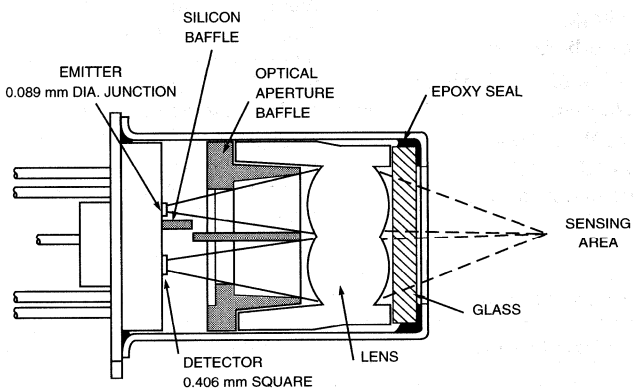
Electrical Operation

The sensor detector is a pn photodiode. The LED cathode is physically and electrically connected to the case-substrate of the sensor.

HBCC-1570, 1580 Optical System



HBCC-1590 Optical System



The HBCC-15XX sensors are characterized for use with Hewlett-Packard's low current digitizer ICs. The digitizer IC part numbers are HBCC-0500 and HBCC-0600. Data Sheets including circuit diagrams are available.

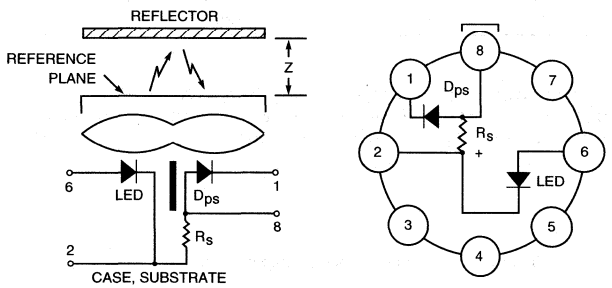
Absolute Maximum Ratings

T_A = 25°C unless specified otherwise (unless specified separately, data applies to all sensors)

Parameter	Symbol	Min.	Max.	Units	Notes
Storage Temperature	T_S	-40	+75	°C	
Operating Temperature	T_A	-20	+75	°C	
Lead Soldering Temperature (1.6 mm from Seating Plane)			260 (for 10 seconds)	°C	1
Average LED Forward Current	I_f				2
Peak LED Forward Current	I_{fp}		125 100 40	mA mA mA	3 (HBCC-1570) 3 (HBCC-1580) 4 (HBCC-1590)
Reverse LED Input Voltage	V_r		5.0 2.5	V V	 HBCC-1590 Only
Photodiode Bias	V_d	-0.3	6.0	V	5

Notes:

1. CAUTION: The thermal constraints of the acrylic lens will not permit conventional wave soldering procedures. The typical preheat and post-soldering cleaning procedures and dwell times can subject lens to thermal stresses beyond the absolute maximum ratings and can cause it to defocus.
2. These sensors are specified for use with the drive conditions provided by the HBCC-0500 and HBCC-0600 Digitizer IC ONLY.
3. When used with HBCC-0500 or HBCC-0600 digitizer ICs.
4. At all combinations of pulse width and duty cycle.
5. Voltage differential between Pin 1 and Pin 8 with Pin 8 taken as reference. Exceeding maximum conditions may cause permanent damage to photodiode or to chip metallization.



R_S = CHARACTERISTIC NOT DEFINED

PIN#	FUNCTION
1	PHOTODIODE CATHODE
2	HEADER GROUND
6	LED ANODE
8	PHOTODIODE ANODE

BAR CODE

HBCC-1570 and HBCC-1580: Electrical and Optical Characteristics

$T_A = 25°C$

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions	Note	Figure
Reflected Photocurrent	I_{pr}	(see Bin Table)			nA	I_f = 70 mA peak	6,7	1,2A, 4A, 4B, 5
Quality Factor	<Q>	0.82	0.95	1.0	–	I_f = 70 mA peak	6,8	
Maximum Signal Point (MSP)	Z	4.11 (0.162)	4.27 (0.168)	4.42 (0.174)	mm (in.)	I_f = 70 mA peak	6,9	1, 4A, 4B
LED Forward Voltage	V_f	1.5	1.75	2.0	V	I_f = 70 mA		3
LED Reverse Breakdown Voltage	BVR	5.0	–	–	V	I_r = 100 µA		
Photodiode Dark Current	I_d	–	60	1000	pA	V_d = 5 V		
Photodiode Capacitance	C_d	–	100 60	– –	pF pF	V_d = 0 V V_d = 1 V		
LED Peak Wavelength	λ	–	650	670	nm	I_f = 35 mA DC		6A
Ipr Temperature Coefficient	K_e	–	-0.006	–	1/°C	I_f = 35 mA DC	10	
System Optical Step Response (OSR) HBCC-1570	d	–	0.268 (0.0106)	–	mm (in.)	4.27 mm (Target from sensor)	11	7A
(OSR) HBCC-1580	d	–	0.154 (0.0061)	–	mm (in.)	4.27 mm (Target from sensor)	11	7B

Notes:

6. Measured from a reflector coated with 99% diffuse reflective white paint (Kodak 6080) positioned 4.27 mm (0.168 in.) from the reference plane. Measured physically is the total photocurrent, Ipt, which consists of a signal (reflected from target) component, Ipr, and a component induced by reflections internal to the sensor (stray), Ips. Ipt = Ipr + Ips. Specified is the reflected signal component, Ipr.
7. See Bin Table
8. <Q> = Ipr/Ipt
9. Measured from reference plane (R.P.) of sensor.
10. Photocurrent variation with temperature varies with LED output which follows a natural exponential law: $I_p(T) = I_p(T_o)*\exp[K_e(T-T_o)]$
11. OSR is defined as the distance for a 10%-90% "step" response of Ipr as the sensor moves over an abrupt black-white edge, or from opaque white to free space (no reflection).

HBCC-1590: Electrical and Optical Characteristics

T_A = 25°C

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions	Note	Figure
Reflected Photocurrent	I_{pr}	(see Bin Table)			nA	I_f = 30 mA peak	6,7	1,2B, 4C, 5
Quality Factor	<Q>	0.82	0.95	1.0	–	I_f = 30 mA peak	6,8	
Maximum Signal Point (MSP)	Z	4.01 (0.158)	4.27 (0.168)	4.62 (0.182)	mm (in.)	I_f = 30 mA peak	6,9	1, 4C
LED Forward Voltage	V_f	1.3	1.45	1.8	V	I_f = 30 mA		3
LED Reverse Breakdown Voltage	BVR	2.5	–	–	V	I_r = 100 µA		
Photodiode Dark Current	I_d	–	60	1000	pA	V_d = 5 V		
Photodiode Capacitance	C_d	–	100 60	–	pF pF	V_d = 0 V V_d = 1 V		
LED Peak Wavelength	λ	805	820	835	nm	I_f = 35 mA DC		6B
Ipr Temperature Coefficient	K_e	–	-0.005	–	1/°C	I_f = 35 mA DC	10	
System Optical Step Response (OSR)	d	– –	0.140 (0.0055)	– –	mm (in.)	4.27 mm (Target from sensor)	11	7C

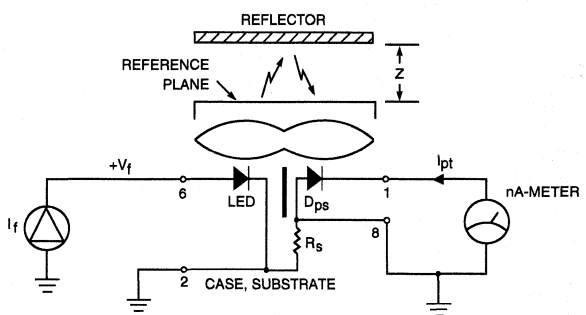


Figure 1. Photocurrent Test Circuit.

Bin Table

Bin#	Ipr Limits (nA)	
	Min.	Max.
1	160	225
2	215	270
3	255	313
4	300	375
5	360	440
6	430	555

Product Marking

The photocurrent binning of the sensor is incorporated as part of the product marking format. The Bin # is represented as the last number (N) on the last line of marking.

HP
HBCC-15XX
XXXXXXXN

N = bin number

Bin Availability

The entire available distribution of parts, appropriately marked, will be shipped. Requests for individual bin selections cannot be honored.

Binning and Temperature Effects

Test algorithm bins units to the lower bin number if a unit is in the bin overlap region. Such units can cross bin boundaries as temperature changes. (Ambient temperature affects LED efficiency slightly and may cause several percentage changes in Ipr.) Bin numbers are for "reference only" and do not constitute an absolute guarantee. The output of all LEDs degrades with time, depending on drive conditions and temperature. LED degradation is minimized by the drive conditions generated by both the HBCC-0500 and HBCC-0600, (when used as specified).

Warranty and Service

HP Optical Reflective Sensors are warranted for a period of one year after purchase covering defects in material and workmanship. Hewlett-Packard will repair or, at its option, replace products that prove to be defective in material or workmanship under proper use during the warranty period.

NO OTHER WARRANTIES ARE EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANT ABILITY AND FITNESS FOR A PARTICULAR PURPOSE. HEWLETT-PACKARD IS NOT LIABLE FOR CONSEQUENTIAL DAMAGES.

For additional warranty or service information please contact your local Hewlett-Packard sales representative or authorized distributor.

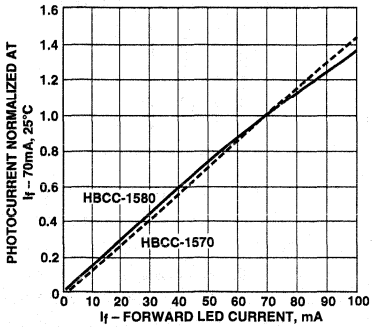


Figure 2A. Typical Reflected Photocurrent.

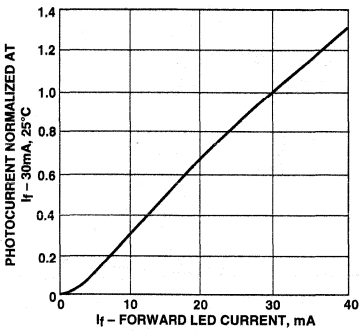


Figure 2B. Typical HBCC-1590 Reflected Photocurrent.

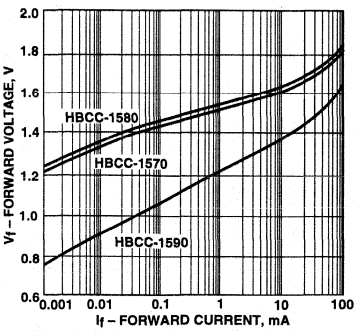


Figure 3. Typical LED Forward Voltage vs. Forward Current.

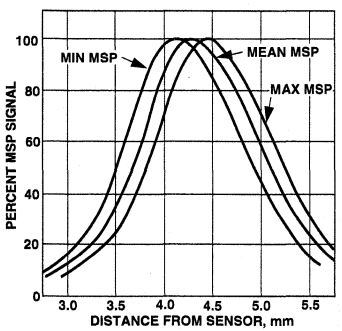


Figure 4A. HBCC-1570 Signal vs. Distance from Sensor.

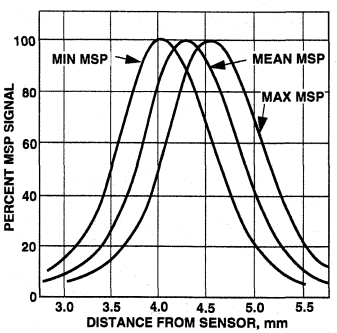


Figure 4B. HBCC-1580 Signal vs. Distance from Sensor.

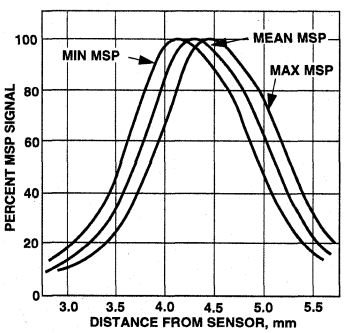


Figure 4C. HBCC-1590 Signal vs. Distance from Sensor.

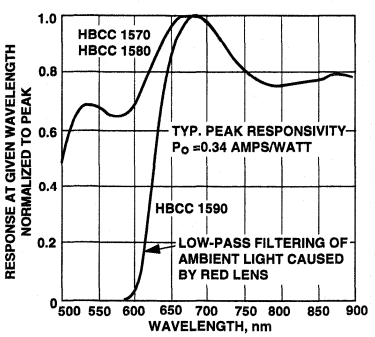


Figure 5. Relative Spectral Response of Sensors.

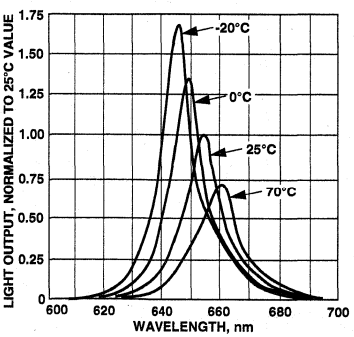


Figure 6A. Typical Spectral Distribution of 655 nm LED.

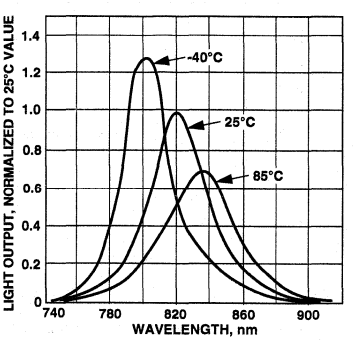


Figure 6B. Typical Spectral Distribution of 820 nm LED.

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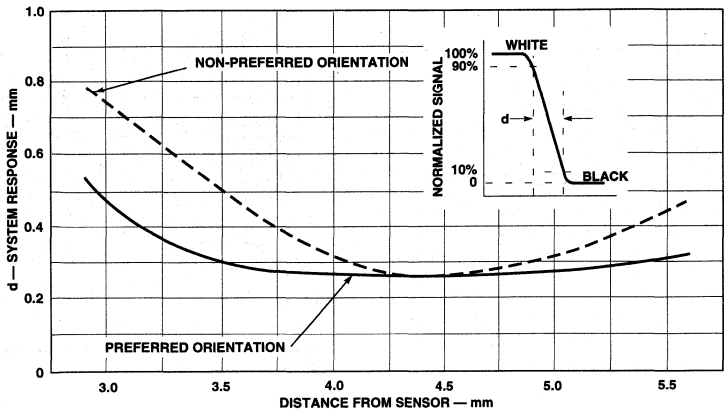


Figure 7A. HBCC-1570, System Optical Step Response Variation with Distance.

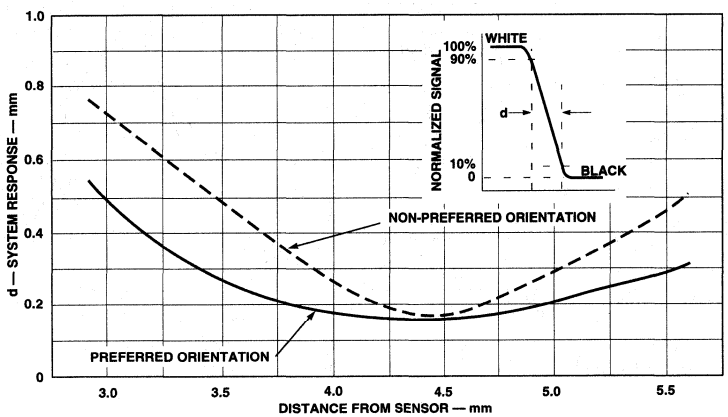


Figure 7B. HBCC-1580, System Optical Step Response Variation with Distance.

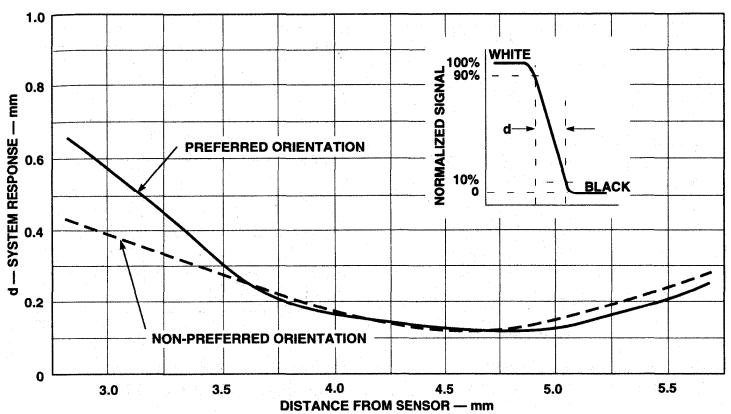
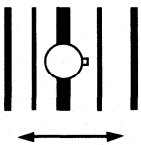


Figure 7C. HBCC-1590, System Optical Step Response Variation with Distance.

Preferred Orientation



At maximum signal point (MSP) when the sensor is in focus, the orientation of the sensor is unimportant. However, as one moves away from MSP (either by distance or angle), the preferred orientation indicated above is recommended to maintain a higher resolution spot size.

HEWLETT® PACKARD

High Resolution Optical Reflective Sensor

Technical Data

HBCS-1100

Features

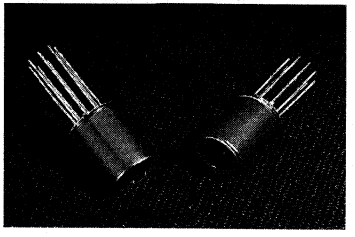
- **Focused Emitter and Detector in a Single Package**
- **High Resolution–0.190 mm Spot Size**
- **700 nm Visible Emitter**
- **Lens Filtered to Reject Ambient Light**
- **TO-5 Miniature Sealed Package**
- **Photodiode and Transistor Output**
- **Solid State Reliability**

Description

The HBCS-1100 is a fully integrated module designed for optical reflective sensing. The module contains a 0.178 mm (0.007 in.) diameter 700 nm visible LED emitter and a matched I.C. photodetector. A bifurcated aspheric lens is used to image the active areas of the emitter and the detector to a single spot 4.27 mm (0.168 in.) in front of the package. The reflected signal can be sensed directly from the photodiode or through an internal transistor that can be configured as a high gain amplifier.

Applications

Applications include pattern recognition and verification, object sizing, optical limit switching, tachometry, textile thread counting and defect detection, dimensional monitoring, line locating, mark, and bar code scanning, and paper edge detection.



Mechanical Considerations

The HBCS-1100 is packaged in a high profile 8 pin TO-5 metal can with a glass window. The emitter and photodetector chips are mounted on the header at the base of the package. Positioned above these active elements is a bifurcated aspheric acrylic lens that focuses them to the same point.

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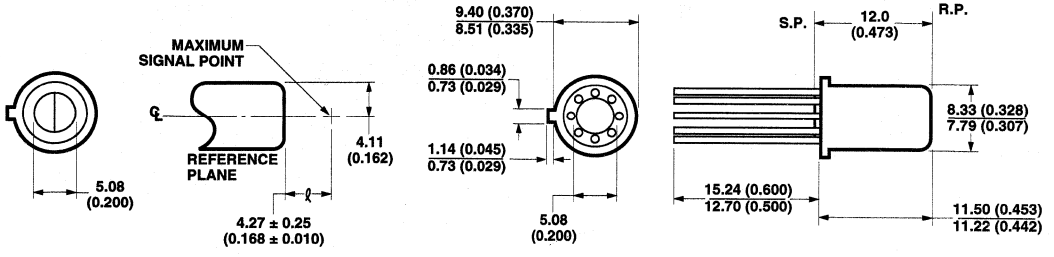
Package Dimensions



NOTES:
1. ALL DIMENSIONS IN MILLIMETERS AND (INCHES).
2. ALL UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.
3. THE REFERENCE PLANE IS THE TOP SURFACE OF THE PACKAGE.
4. NICKEL CAN AND GOLD PLATED LEADS.
5. S.P. SEATING PLANE.
6. THE LEAD DIAMETER IS 0.45 mm (0.018 IN.) TYP.

The sensor can be rigidly secured by commercially available two piece TO-5 style heat sinks, such as Thermalloy 2205, or Aavid Engineering 3215. These fixtures provide a stable reference platform and their tapped mounting holes allow for ease of affixing this assembly to the circuit board.

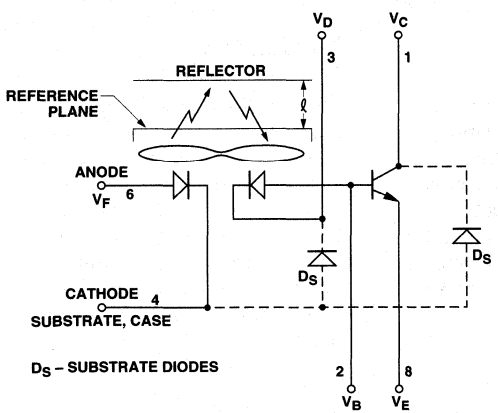
Electrical Operation

The detector section of the sensor can be connected as a single photodiode or as a photodiode transistor amplifier. When photodiode operation is desired, it is recommended that the substrate diodes be defeated by connecting the collector of the transistor to the positive potential of the power supply and shorting the base-emitter junction of the transistor. Figure 15 shows photocurrent being supplied from the anode of the photodiode to an inverting input of the operational amplifier. The circuit is recommended to improve the reflected photocurrent to stray photocurrent ratio by keeping the substrate diodes from acting as photodiodes.

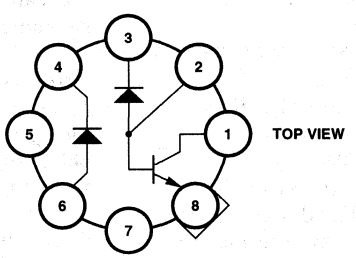
The cathode of the 700 nm emitter is physically and electrically connected to the case-substrate of the device. Applications that require modulation or switching of the LED should be designed to have the cathode connected to the electrical ground of the system. This insures minimum capacitive coupling of the switching transients through the substrate diodes to the detector amplifier section.

The HBCS-1100 detector also includes an NPN transistor which can be used to increase the output current of the sensor. A current feedback amplifier as shown in Figure 6 provides moderate current gain and bias point stability.

Schematic Diagram



Connection Diagram



PIN	FUNCTION
1	TRANSISTOR COLLECTOR
2	TRANSISTOR BASE, PHOTODIODE ANODE
3	PHOTODIODE CATHODE
4	LED CATHODE, SUBSTRATE, CASE
5	NC
6	LED ANODE
7	NC
8	TRANSISTOR EMITTER

CAUTION: The small junction sizes inherent to the design of this bipolar component increase the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be introduced by ESD.

Absolute Maximum Ratings at T_A = 25°C

Parameter	Symbol	Min.	Max.	Units	Fig.	Notes
Storage Temperature	T_S	-40	+75	°C		
Operating Temperature	T_A	-20	+70	°C		
Lead Soldering Temperature 1.6 mm from Seating Plane			260 for 10 sec.	°C		11
Average LED Forward Current	I_F		50	mA		2
Peak LED Forward Current	I_{FPK}		75	mA	1	1
Reverse LED Input Voltage	V_R		5	V		
Package Power Dissipation	P_P		120	mW		3
Collector Output Current	I_O		8	mA		
Supply and Output Voltage	V_D, V_C, V_E	-0.5	20	V		10
Transistor Base Current	I_B		5	mA		
Transistor Emitter Base Voltage	V_{EB}		0.5	V		

System Electrical/Optical Characteristics at T_A = 25°C

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions	Fig.	Note
Total Photocurrent (I_{PR} + I_{PS})	I_P			575	nA	T_A = 20°C; I_F = 35 mA, V_D = V_C = 5 V	2, 3	4
		150	250	375		T_A = 25°C; V_D = V_C = 5 V	15	
		80				T_A = 70°C; V_D = V_C = 5 V		
Reflected Photocurrent (I_{PR}) to Internal Stray Photocurrent (I_{PS})	$\frac{I_{PR}}{I_{PS}}$	4	8.5			I_F = 35 mA, V_C = V_D = 5 V	3	
Transistor DC Static Current Transfer Ratio	h_{FE}	50				T_A = 20°C; V_{CE} = 5 V, I_C = 10 µA	4, 5	
		100	200			T_A = 25°C; V_{CE} = 5 V, I_C = 10 µA		
Slew Rate			0.08		V/µs	R_L = 100 K, I_{PK} = 50 mA, R_F = 10 M, t_{ON} = 100 µs, Rate = 1 kHz	6	
Image Diameter	d		0.17		mm	I_F = 35 mA, ℓ = 4.27 mm (0.168 in.)	8, 10	8, 9
Maximum Signal Point	ℓ	4.01	4.27	4.52	mm	Measured from Reference Plane	9	
50% Modulation Transfer Function	MTF		2.5		$I_{npr/mm}$	I_F = 35 mA, ℓ =4.27 mm	10, 11	5, 7
Depth of Focus	$\Delta\ell$ FWHM		1.2		mm	50% of I_P at ℓ = 4.27 mm	9	5
Effective Numerical Aperture	N.A.		0.3					
Image Location	D		0.51		mm	Diameter Reference to Centerline ℓ = 4.27 mm		6
Thermal Resistance	Θ_{JC}		85		°C/W			

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Detector Electrical/Optical Characteristics at T_A = 25°C

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions		Fig.	Note
Dark Current	I_{PD}		5	200	pA	T_A = 25°C	I_F = 0, V_D = 5 V; Reflection = 0%		
				10	nA	T_A = 70°C			
Capacitance	C_D		45		pF	V_D = 0 V, I_P = 0, f = 1 MHz			
Flux Responsivity	$R\phi$		0.22		A/W	λ = 700 nm, V_D = 5 V		12	
Detector Area	A_D		0.160		mm^2	Square, with Length = 0.4 mm/Side			

Emitter Electrical/Optical Characteristics at T_A = 25°C

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions	Fig.	Note
Forward Voltage	V_F		1.6	1.8	V	I_F = 35 mA	13	
Reverse Breakdown Voltage	BV_R	5			V	I_R = 100 µA		
Radiant Flux	ϕ_E	5	9.0		µW	I_F = 35 mA, λ = 700 nm	14	
Peak Wavelength	λ_p	680	700	720	nm	I_F = 35 mA	14	
Thermal Resistance	Θ_{JC}		150		°C/W			
Temperature Coefficient of V_F	$\Delta V_F/\Delta T$		-1.2		mV/°C	I_F = 35 mA		

Transistor Electrical Characteristics at T_A = 25°C

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions	Fig.	Note
Collector-Emitter Leakage	I_{CEO}		1		nA	V_{CE} = 5 V		
Base-Emitter Voltage	V_{BE}		0.6		V	I_C = 10 µA, I_B = 70 nA		
Collector-Emitter Saturation Voltage	$V_{CE}(SAT)$		0.4		V	I_B = 1 µA, I_E = 10 µA		
Collector-Base Capacitance	C_{CB}		0.3		pF	f = 1 MHz, V_{CB} = 5 V		
Base-Emitter Capacitance	C_{BE}		0.4		pF	f = 1 MHz, V_{BE} = 0 V		
Thermal Resistance	Θ_{JC}		200		°C/W			

Notes:

1. 300 µs pulse width, 1 kHz pulse rate.
2. Derate Maximum Average Current linearly from 65°C by 6 mA/°C.
3. Without heat sinking from T_A = 65°C, derate Maximum Average Power linearly by 12 mW/°C.
4. Measured from a reflector coated with a 99% reflective white paint (Kodak 6080) positioned 4.27 mm (0.168 in.) from the reference plane.
5. Peak-to-Peak response to black and white bar patterns.
6. Center of maximum signal point image lies within a circle of diameter D relative to the center line of the package. A second emitter image (through the detector lens) is also visible. This image does not affect normal operation.
7. This measurement is made with the lens cusp parallel to the black-white transition.
8. Image size is defined as the distance for the 10%-90% response as the sensor moves over an abrupt black-white edge.
9. (+) indicates an increase in the distance from the reflector to the reference plane.
10. All voltages referenced to Pin 4.
11. CAUTION: The thermal constraints of the acrylic lens will not permit the use of conventional wave soldering procedures. The typical preheat and post cleaning temperatures and dwell times can subject the lens to thermal stresses beyond the absolute maximum ratings and can cause it to defocus.

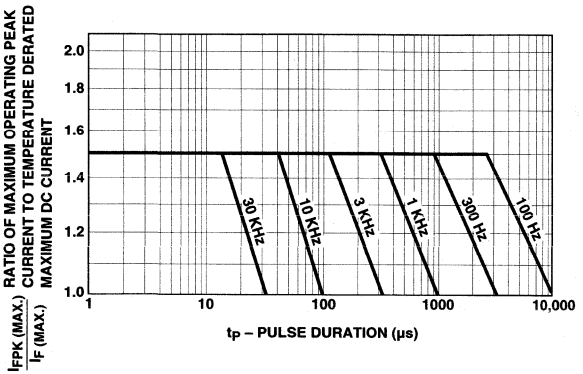


Figure 1. Maximum Tolerable Peak Current vs. Pulse Duration.

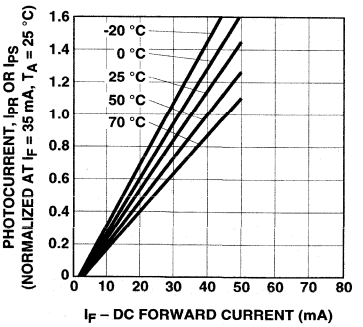


Figure 2. Relative Total Photocurrent vs. LED DC Forward Current.

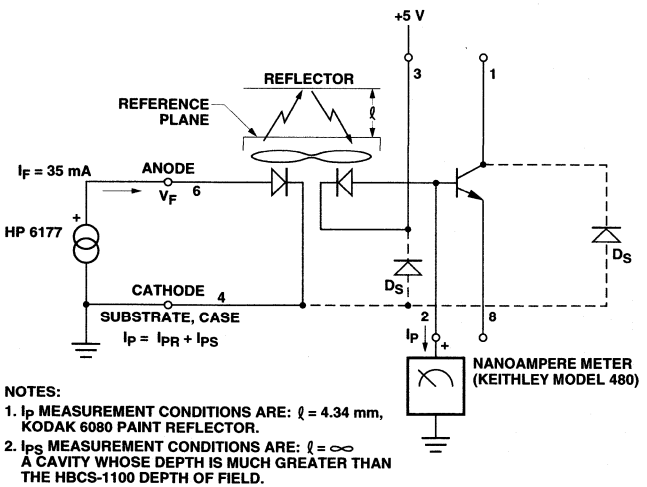


Figure 3. I_P Test Circuit.

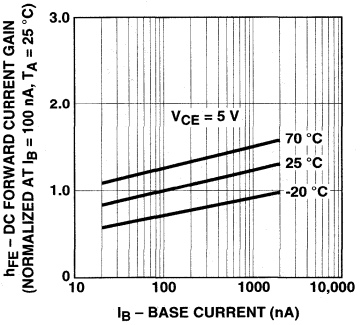


Figure 4. Normalized Transistor DC Forward Current Gain vs. Base Current at Temperature.

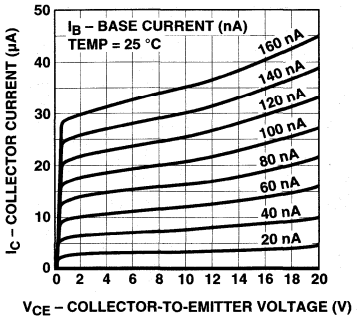


Figure 5. Common Emitter Collector Characteristics.

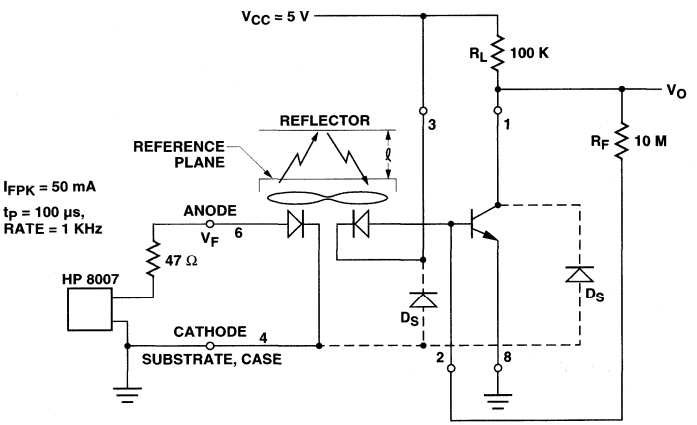


Figure 6. Slew Rate Measurement Circuit.

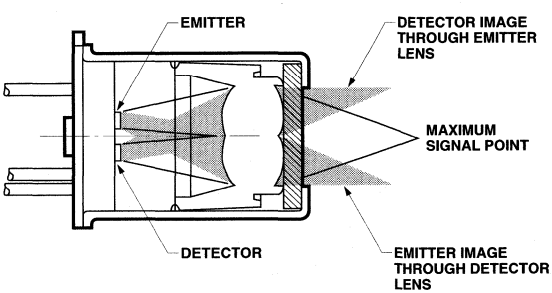


Figure 7. Image Location.

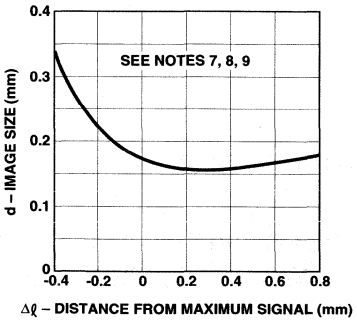


Figure 8. Image Size vs. Maximum Signal Point.

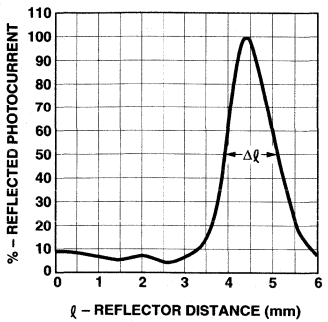


Figure 9. Reflector Distance vs. Percent Reflected Photocurrent.

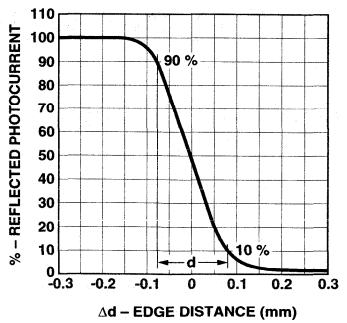


Figure 10. Step Edge Response.

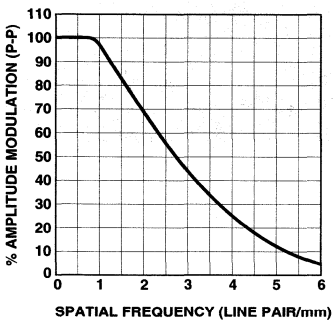


Figure 11. Modulation Transfer Function.

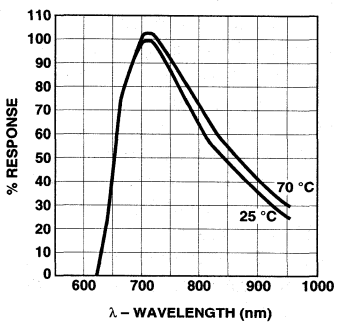


Figure 12. Detector Spectral Response.

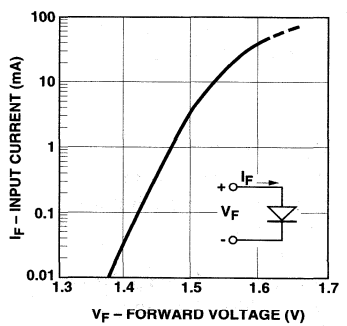


Figure 13. LED Forward Current vs. Forward Voltage Characteristics.

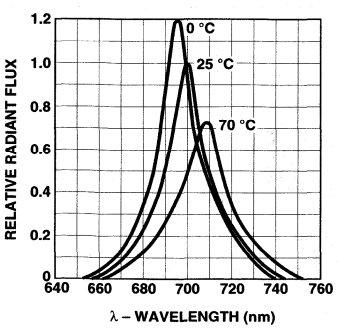


Figure 14. Relative Radiant Flux vs. Wavelength.

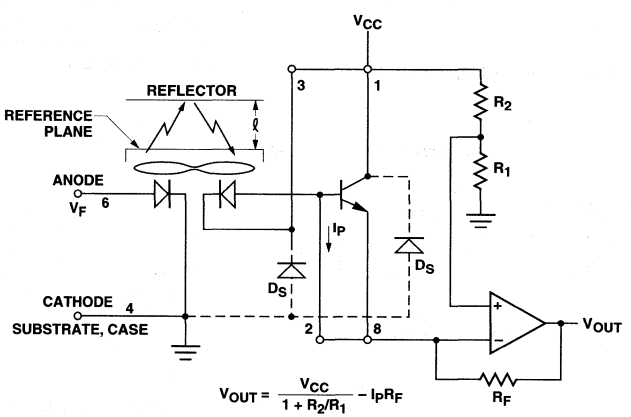


Figure 15. Photodiode Interconnection.

HEWLETT® PACKARD

Optical Reflective Sensors

Technical Data

HEDS-1200 High Resolution Infrared Sensor
HEDS-1300 Precision Resolution Sensor

Features

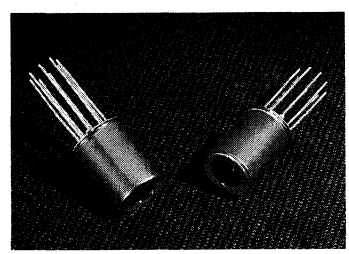
- **Focused Emitter and Detector in a Single Package**
- **TO5 Package**
- **Binning of Sensors by Photocurrent (Ipr)**

Applications

- **Bar Code Scanning**
- **Pattern Recognition and Verification**
- **Object Sizing**
- **Optical Limit Switching**
- **Optical/Surface Inspection**
- **Tachometry**
- **Edge/Line Sensing**
- **Dimensional Monitoring**

Description

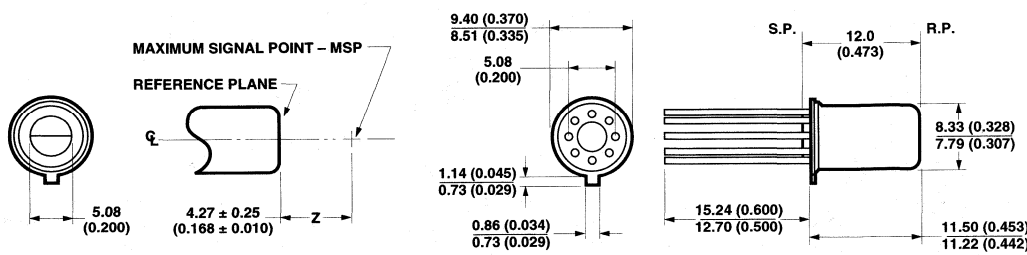
Both the HEDS-1200 and HEDS-1300 sensor are fully integrated modules designed for applications requiring optical reflective sensing. The modules contain an LED emitter (at the appropriate wavelengths) and a matched I.C. photodetector. A bifurcated aspheric lens is used to image the active areas of the emitter and the detector to a single spot that defines the resolution of the sensor. The output signal is a current generated by the photodiode.



Selection Guide

Sensor Part Number	HEDS-1200	HEDS-1300
Resolution	0.13 mm (0.005 in.)	0.19 mm (0.0075 in.)
LED Wavelength	820 nm	700 nm

Package Dimensions



NOTES:
1. ALL DIMENSIONS IN MILLIMETERS AND (INCHES).
2. ALL UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.
3. THE REFERENCE PLANE (R.P.) IS THE TOP SURFACE OF THE PACKAGE.
4. NICKEL CAN AND GOLD PLATED LEADS.
5. S.P. = SEATING PLANE.
6. THE LEAD DIAMETER IS 0.45 mm (0.018 IN.) TYP.

Mechanical Considerations

The HEDS-1200 and HEDS-1300 sensors are packaged in a high profile 8 pin TO5 metal can with a glass window. The emitter and photodetector chips are mounted on the header at the base of the package. Positioned above these active elements is a bifurcated aspheric acrylic lens that focuses them to the same point.

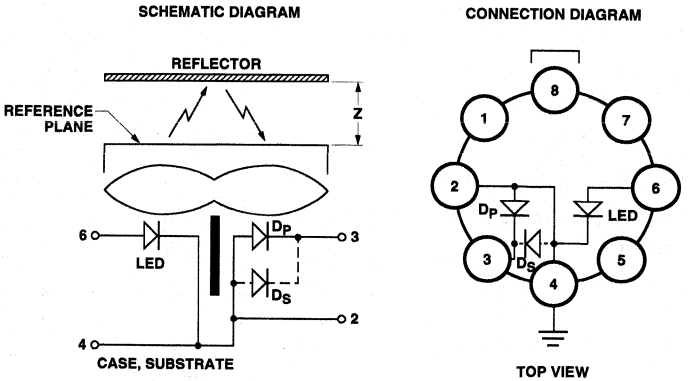
The sensors can be rigidly secured by commercially available TO5 style heat sinks, or 8 pin 0.200 inch diameter pin circle sockets. These fixtures provide a stable reference platform for affixing the sensors to a circuit board.

In applications requiring contact scanning, protective focusing tips are available. Focusing tips are available in either metal (HBCS-2999 or HBCS-4999) or polycarbonate (HBCS-A998 or HBCS-A999) packages using a rugged sapphire ball as the contact surface.

Electrical Operations

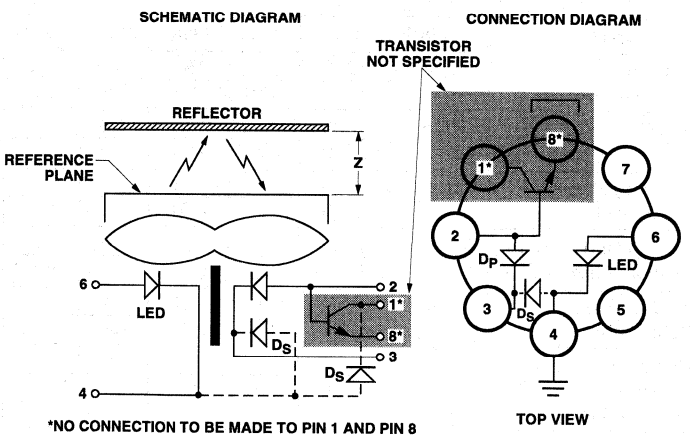
Both the HEDS-1200 and HEDS-1300 sensors have the following in common. The detector of the sensor is a single photodiode. The cathode of the emitter is physically and electrically connected to the case-substrate of the device. Applications that require modulation or switching of the LED should be designed to have the cathode connected to the electrical ground of the system. Refer to the Schematic and Connection Diagrams that follow.

HEDS-1200 Optical System



PIN #	FUNCTION (HEDS-1200)
2	PHOTODIODE ANODE, SUBSTRATE, CASE
3	PHOTODIODE CATHODE
4	LED CATHODE, SUBSTRATE, CASE
6	LED ANODE

HEDS-1300 Optical System



*NO CONNECTION TO BE MADE TO PIN 1 AND PIN 8

PIN #	FUNCTION (HEDS-1300)
2	PHOTODIODE ANODE
3	PHOTODIODE CATHODE
4	LED CATHODE, SUBSTRATE, CASE
6	LED ANODE

Absolute Maximum Ratings @ T_A = 25°C

Parameter	Symbol	HEDS-	Min.	Max.	Units	Fig.	Notes
Storage Temperature	Ts	1200	-40	+75	°C		
		1300	-40	+75	°C		
Operating Temperature	T_A	1200	-20	+70	°C		
		1300	-20	+70	°C		
Lead Soldering Temperature 1.6 mm from Seating Plane		1200		260°C for 10 sec.			1
		1300					1
Average LED Forward Current	If	1200	10	40	mA		3
		1300		50	mA		2
Peak LED Forward Current	Ifpk	1200		40	mA	7	4
		1300		75	mA	7	4
Reverse LED Input Voltage	Vr	1200		2.5	V		
		1300		5.0	V		
Photodiode Bias (Id = 100 µA max)	Vd	1200	-0.3	20	V		5
		1300	-0.3	20	V		5

Notes:
1. Caution: The thermal constraints of the acrylic lens will not permit the use of conventional wave soldering procedures. The typical preheat and post-cleaning temperatures and dwell times can subject the lens to thermal stresses beyond the absolute maximum ratings and can cause it to defocus.
2. Derate Maximum Average Current linearly from 65°C by 6 mA/°C [HEDS-1300 only].
3. Non-linear effects make operation of the HEDS-1200 below 10 mA not advisable.
4. 1 KHz pulse rate, 300 mS pulse width.
5. All voltages referenced to Pin 4.

System Electrical/Optical Characteristics @ T_A = 25°C

Parameter	Symbol	HEDS-	Min.	Typ.	Max.	Units	Conditions	Fig.	Notes
Reflected Photocurrent	Ipr	1200	150	280	650	nA	If = 35 mA, Vd = 0	1A, 2, 6	6
		1300	150	280	650	nA	See Binning Table	1B, 2, 6	6
Quality Factor	<Q>	1200	0.82	0.95	1.0		If = 35 mA	1A	6, 7
		1300	0.82	0.95	1.0			1B	6, 7
Ipr Temperature Coefficient	Ke	1200		-0.005		1/°C	If = 35 mA		8
		1300		-0.01		1/°C			8
System Optical Step Response Size (OSR)	d	1200		0.13		mm		9A	9
		1300		0.19		mm		9B	9
Maximum Signal Point (MSP)	Zm	1200	4.01	4.27	4.62	mm	Measured from Reference Plane	4	
		1300	4.01	4.27	4.52	mm		4	
Effective Numerical Aperture of Detector Lens	N.A.	1200		0.3					
		1300		0.3					

Notes:
6. Measured from a reflector coated with 99% diffuse reflective white paint (Kodak 6080) positioned 4.27 mm (0.168 in.) from the sensor's reference plane. Measured physically is the total photocurrent, Ipt, which consists of a signal (reflected from target) component, Ipr, and a component induced by reflections internal to the sensor (stray), Ips. Ipr = Ipt - Ips.
7. <Q> = Ipr/Ipt
8. Photocurrent variation with temperature follows a natural exponential law: Ip(T) = Ip(To)*exp[Ke(T-To)]
9. OSR size is defined as the distance for the 10%-90% "step" response of Ipr as the sensor moves over an abrupt black-white edge, or from opaque white to free space (no reflection).

Detector Electrical/Optical Characteristics @ T_A = 25°C

Parameter	Symbol	HEDS-	Min.	Typ.	Max.	Units	Conditions	Fig.	Notes
Dark Current	Id	1200		50	1000	pA	Vd = 5 V, If = 0		
		1300		50	1000	pA	Reflection = 0%		
Capacitance	Cd	1200		100		pF	Vd = 0 V, If = 0		
		1300		100		pF	f = 1 MHz		
Detector Area	Ad	1200		0.16		sq-mm	Square, with length		
		1300		0.16		sq-mm	= 0.4 mm per side		

Emitter Electrical/Optical Characteristics @ T_A = 25°C

Parameter	Symbol	HEDS-	Min.	Typ.	Max.	Units	Conditions	Fig.	Notes
Forward Voltage	Vf	1200		1.48	1.7	V	If = 35 mA	3	
		1300		1.6	1.8	V		3	
Reverse Breakdown Voltage	BVR	1200	2.5			V	Ir = 100 μA		
		1300	5.0			V			
Thermal Coefficient of Vf	ΔVf/ΔT	1200		-0.91		mV/°C	If = 35 mA		
		1300		-1.2		mV/°C			
Peak Wavelength	λ	1200	805	820	835	nm	If = 35 mA	5	
		1300	680	700	720	nm		5	
Emitting Area	Ae	1200		0.0062		sq-cm	0.0889 mm diameter junction (0.0035 in.)		
		1300		0.0285		sq-cm	0.185 mm diameter junction (0.0073 in.)		

Bin Table

Ipr Limits (nA)		
Bin #	**Min.**	**Max.**
2	150	200
3	195	245
4	240	293
5	288	355
6	350	430
7	425	520
8	515	650

Product Marking

The photocurrent binning of the sensor is included in the 8-digit code printed on the sensor can. The last digit in the code represents the bin number.

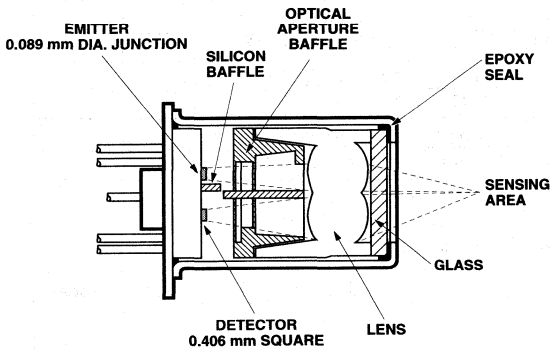
See Figure 8 for suggestions in the application of photocurrent bins.

Test algorithm bins units to the lowest bin number if a unit is in the overlap region. Such units can cross bin boundaries as temperature changes. (Ambient temperature affects LED efficiency slightly and may cause several percent changes in Ipr). Bin numbers are for "reference only" and do not constitute an absolute guarantee.

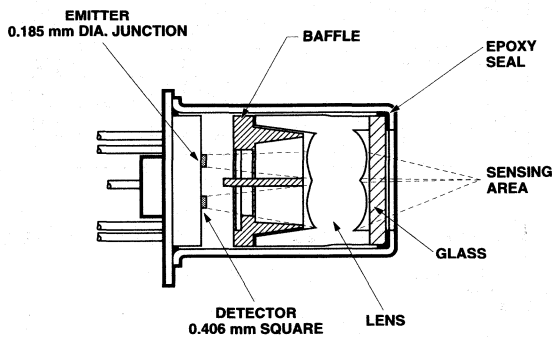
The output of all LEDs degrades with time, depending on drive conditions and temperature.

The entire available distribution of parts, appropriately marked, will be shipped. Single bin orders cannot be supplied.

HEDS-1200 Optical System



HEDS-1300 Optical System



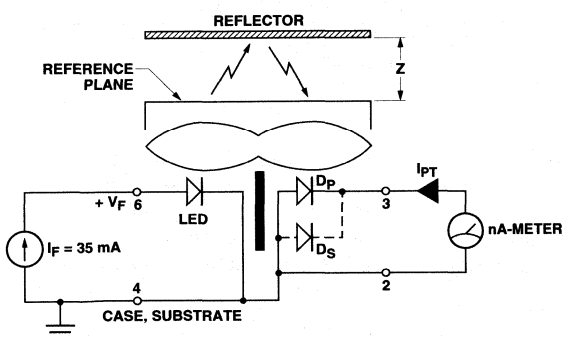


Figure 1A. HEDS-1200 Photocurrent Test Circuit.

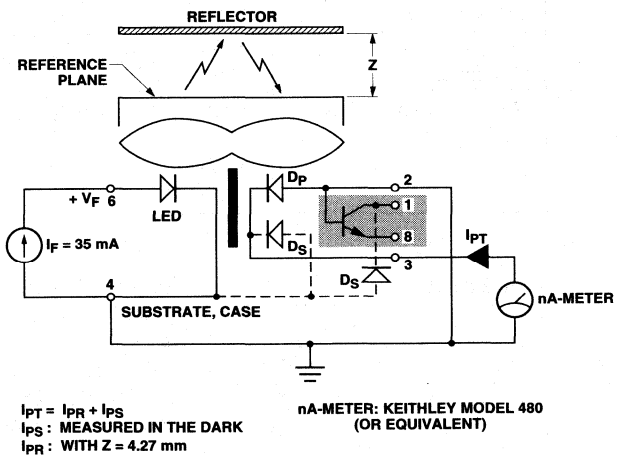


Figure 1B. HEDS-1300 Photocurrent Test Circuit.

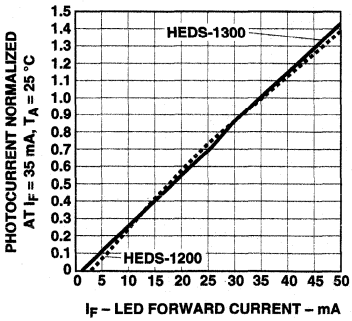


Figure 2. Relative Reflected Photocurrent.

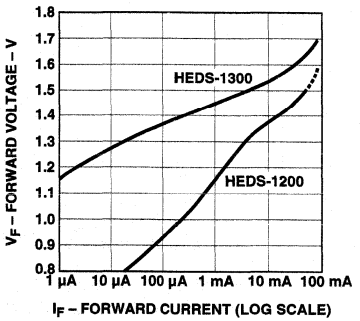


Figure 3. LED Forward Voltage vs. Forward Current.

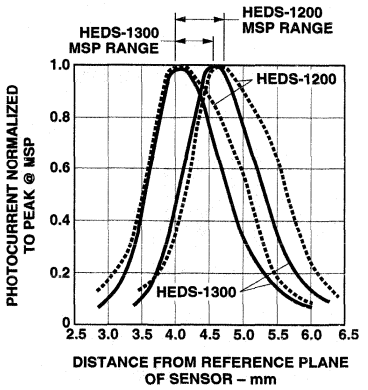


Figure 4. Photocurrent Variation with Distance.

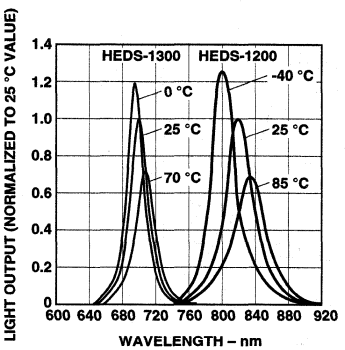


Figure 5. Typical Spectral Distribution of LEDs.

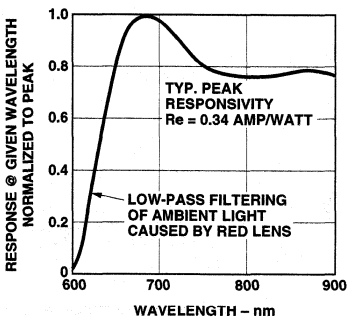


Figure 6. Relative Spectral Response of HEDS-1200 and HEDS-1300 Sensors.

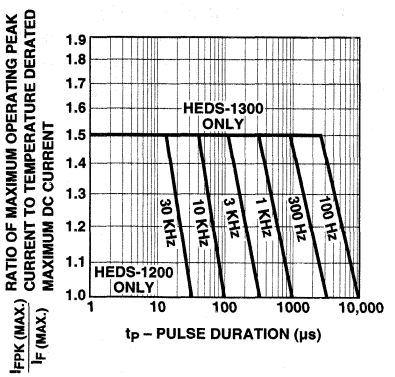
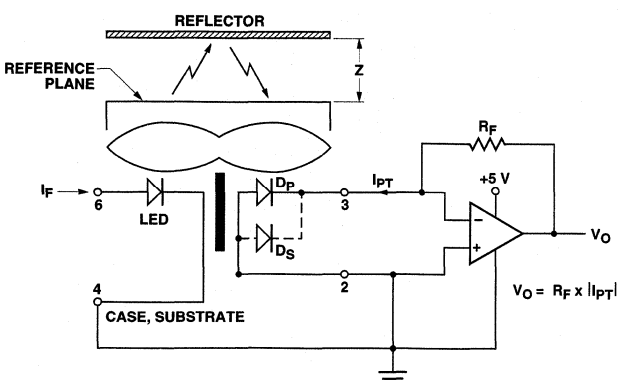


Figure 7. Sensor Pulse Drive Considerations. Max Tolerable Peak Pulse Current vs. Pulse Duration.

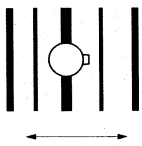


NOTE: FOR V_O (APPROX.) 1.9 – 2.4 VOLTS

SENSOR BIN NUMBER	RECOMMENDED VALUE OR R_F (OHMS)
2	15 M
3	12 M
4	10 M
5	8.2 M
6	6.8 M
7	5.6 M
8	4.7 M

Figure 8. Sensor with Transimpedance Amplifier.

Preferred Orientation



At maximum signal point (MSP) and/or when the sensor is in focus, the orientation of the sensor is unimportant. However, as one moves away from MSP and/or moves out of focus (either by distance or angle), the preferred orientation indicated above is recommended to maintain a higher resolution spot size.

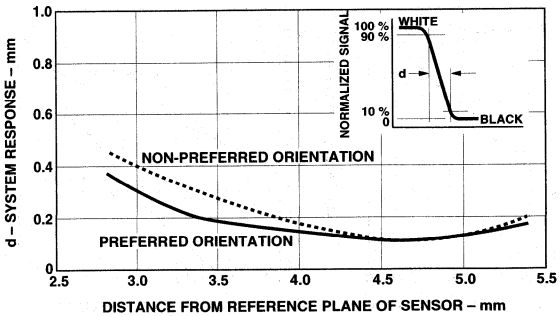


Figure 9A. HEDS-1200 System Optical Step Response Variation with Distance.

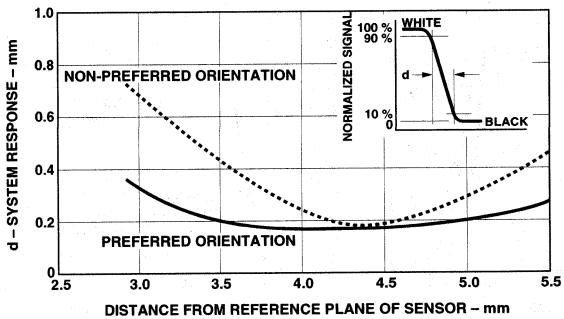


Figure 9B. HEDS-1300 System Optical Step Response Variation with Distance.

Warranty and Service

HP Optical Reflective Sensor is warranted for a period of one year after purchase covering defects in material and workmanship. Hewlett-Packard will repair or, at its option, replace products that prove to be defective in material or workmanship under proper use during the warranty period.

NO OTHER WARRANTIES ARE EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. HEWLETT-PACKARD IS NOT LIABLE FOR CONSEQUENTIAL DAMAGES.

For additional warranty or service information please contact your local Hewlett-Packard sales representative or authorized distributor.

HEWLETT® PACKARD

Bar Code Reader Tips and Optical Nest Assembly

Technical Data

HBCS-A998 HBCS-4999
HBCS-A999 HBCS-T999
HBCS-2999 HBCS-A995

Features

- **Rugged Sapphire Front End**
- **Enclosure Options: Polycarbonate, Anodized Aluminum, or Stainless Steel**
- **15 kV ESD Isolation for Polycarbonate Tips**
- **Compatible with HP Bar Code Wands and Sensors**
- **Self Cleaning**
- **Long Service Life**
- **External Threads**

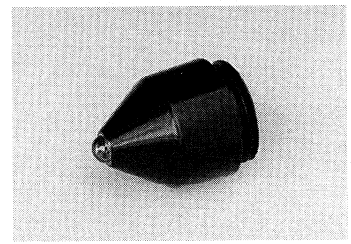
Bar Code Reader Tips Description

Hewlett-Packard offers a range of tips to be used in conjunction with HP optical reflective sensors and as replacement tips for the HP family of wand products. This combination results in a high performance optical system, which is unique in its size and precision. In addition to their optical performance, the tips protect the sensors and act as mechanical holders. With a rugged sapphire front end, these tips are generally self cleaning and should last for many years under normal use.

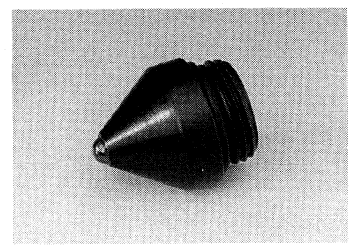
All tips have an internal reference ledge that positions the sensors so that the maximum signal point (MSP) occurs at the correct position, making the tips suitable for contact scanning.

HBCS-A995 Bar Code Reader Optical Nest Assembly

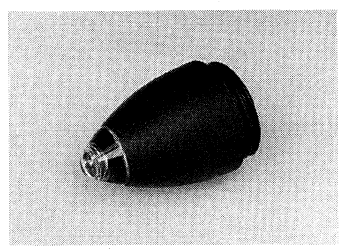
HP also offers the HBCS-A995 bar code reader optical nest assembly for custom applications. This device consists of a rugged sapphire ball bonded to a transparent polycarbonate assembly . The HBCS-A995 optical assembly is an integral part of the HBCS-A998/A999 tip and HBCS-AXXX wand construction. The HBCS-A995 can be bonded to a tip or a case by either press fitting or using a suitable adhesive. Ultrasonic bonding is not recommended. The HBCS-A995 polycarbonate assembly is UV opaque and is made of Lexan 303-11103.



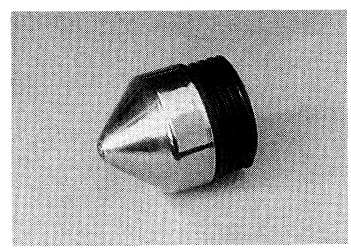
HBCS-2999 Tip



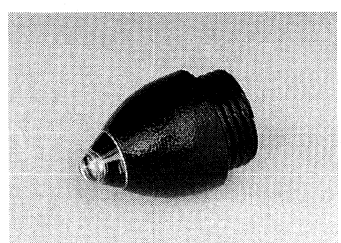
HBCS-4999 Tip



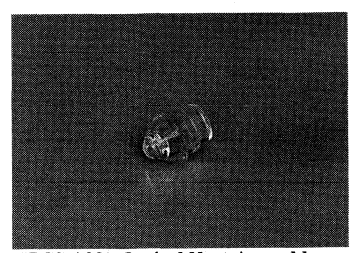
HBCS-A998 Tip



HBCS-T999 Tip



HBCS-A999 Tip



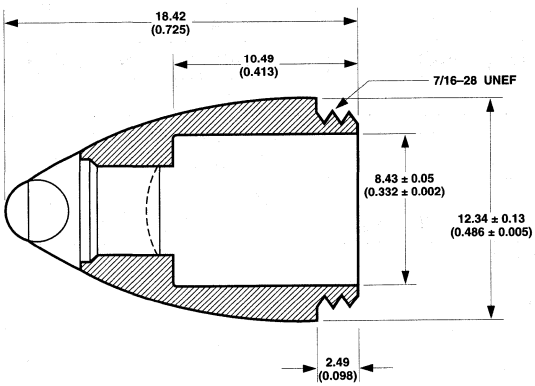
HBCS-A995 Optical Nest Assembly

Tip Selection Guide and Specifications

	Polycarbonate Tips		Metal Tips		
	HBCS-A998	**HBCS-A999**	**HBCS-2999**	**HBCS-4999**	**HBCS-T999***
ESD Isolation	15 kV		Not Applicable		
Overall Length	18.4 mm (0.725 in.)	18.3 mm (0.721 in.)	15.9 mm (0.625 in.)	15.7 mm (0.620 in.)	14.6 mm (0.576 in.)
Thread Engagement	2.5 mm (0.098 in.)	4.4 mm (0.172 in.)	2.5 mm (0.098 in.)	4.4 mm (0.172 in)	3.8 mm (0.151 in.)
Thread	7/16-28 UNEF				12 mm x 1.0
Outer Diameter	12.3 mm (0.486 in.)	13.2 mm (0.518 in.)	12.3 mm (0.485 in.)	13.2 mm (0.520 in.)	12.7 mm (0.500 in.)
Compatible HP Digitizer ICs	HBCC-0500/0600/0601				HBCC-0500
Compatible HP Bar Code Wands	Custom Applications**		HBCS-2XXX	HBCS-6XXX HBCS-8XXX	HBCS-TXXX
Compatible HP Bar Code Sensors	HBCS-1100, HEDS-1200/1300/1500, HBCC-1570/1580/1590				

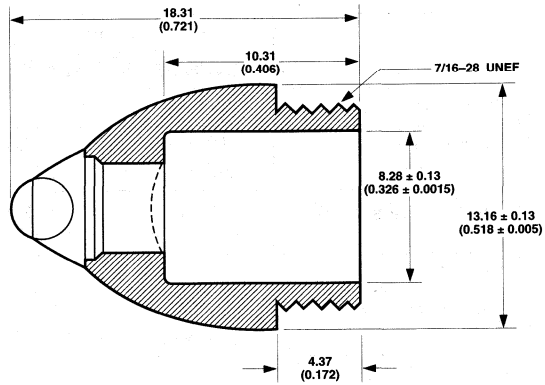
*HBCS-T999 has a stainless steel outer covering with plastic on the inside. The threads on this tip have a flat top.
**The HBCS-A998/A999 tip is an integral part of the case design of the HBCS-AXXX bar code wands.

HBCS-A998 Tip



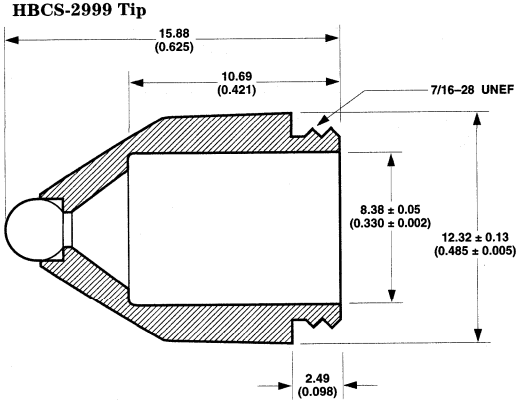
DIMENSIONS IN MILLIMETERS AND (INCHES)

HBCS-A999 Tip



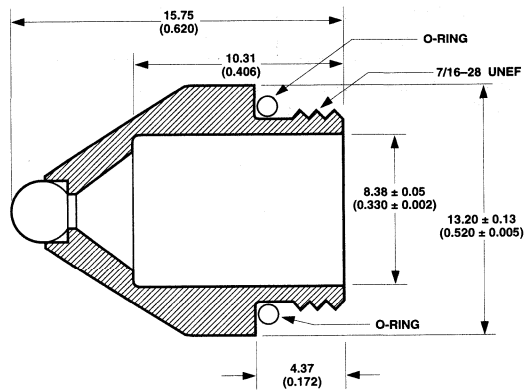
DIMENSIONS IN MILLIMETERS AND (INCHES)

HBCS-2999 Tip



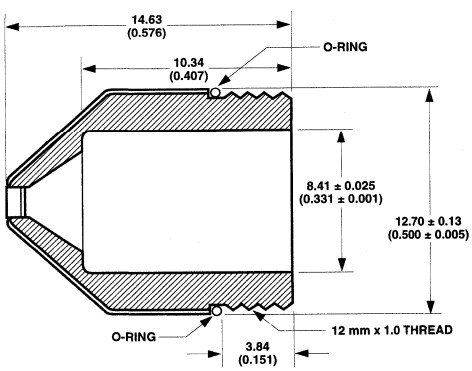
DIMENSIONS IN MILLIMETERS AND (INCHES)

HBCS-4999 Tip



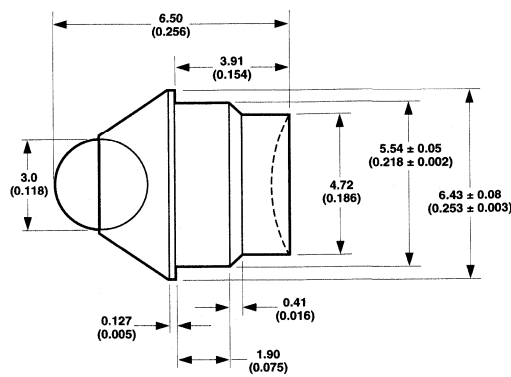
DIMENSIONS IN MILLIMETERS AND (INCHES)

HBCS-T999 Tip



DIMENSIONS IN MILLIMETERS AND (INCHES)

HBCS-A995 Optical Nest Assembly



HEWLETT® PACKARD

Low Current Bar Code Digitizer IC

Technical Data

HBCC-0500

Features

- **Compatible with HP Bar Code Sensors**
  - HBCC-1570 - 0.013 in. 0.33 mm
  - HBCC-1580 - 0.007 in. 0.185 mm
  - HBCC-1590 - 0.005 in. 0.13 mm
- **Ambient Light Rejection > 100 K Lux**
- **Accurate Digitizing of a Wide Range of Bar Code Labels**

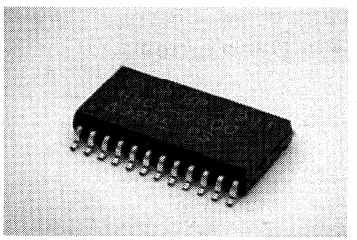
Description

The Hewlett-Packard Low Current Bar Code Digitizer IC allows designers to incorporate the high ambient light rejection and low power consumption features of the HBCS-AXXX/TXXX wands into their own bar code circuitry. The HBCC-0500 is packaged in a 24 pin SOIC plastic package.

Theory of Operation

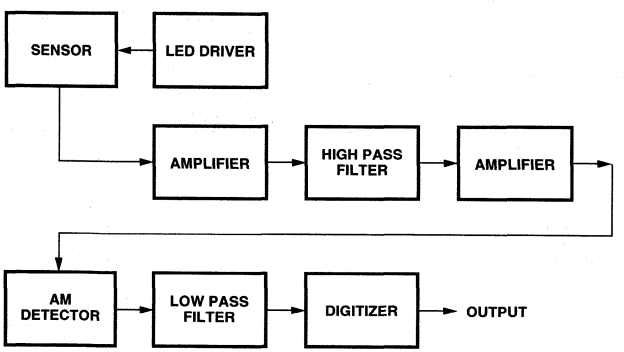
The digitizer IC uses the techniques in US Patent 4,682,015 to reduce power consumption and sensitivity to ambient light. Power is reduced by pulsing the LED every 33 microseconds with a 1 microsecond pulse. The output of different sensor "bins" is equalized by varying the amplitude of the LED drive current.

The sensor output has two components; DC due to ambient light, and AC from the bar code label. Photocurrent from the sensor is amplified and high pass filtered to remove the ambient light signal. The AC component is amplified and sent to an AM detector to recover the bar code information. The recovered bar code signal is low pass filtered to eliminate the 30 kHz carrier. The signal is input to a digitizer consisting of positive and negative



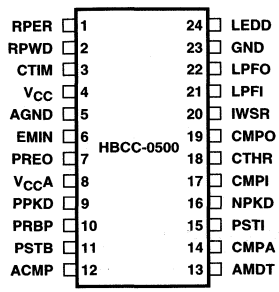
peak detectors and a comparator. The comparator threshold is generated from the peak detectors using a resistor ladder. This threshold, along with the current bar code signal, is input to a comparator. The output of the comparator drives an external output transistor.

Block Diagram

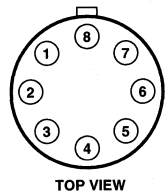


BAR CODE

Pinout



Sensor Pinout



TOP VIEW

Function	Pin #
LED Anode	6
LED Cathode	2
Detector Anode	8
Detector Cathode	1

Sensor Marking

Sensors are marked with an eight digit code, the last digit being the "bin" number. The bin number is used to determine the bin resistor, Rb, using the Bin Table.

Pin Description

Mnemonic	Description
RPER	Timer Period
RPWD	Timer Pulse Width
CTIM	Timer Capacitor
V_{CC}	Filtered Power
AGND	Analog Ground
EMIN	Preamp Emitter Input
PREO	Preamp Output
$V_{CC}A$	Analog Power
PPKD	Positive Peak Detector
PRBP	Preamp Bias Point
PSTB	Postamp Bypass
ACMP	Compensation Cap
AMDT	AM Detector
CMPA	Compensation Cap
PSTI	Postamp Input
NPKD	Negative Peak Detector
CMPI	Comparator Input
CTHR	Comparator Threshold
CMPO	Comparator Output
IWSR	White State Return Current
LPFI	Low Pass Filter Input
LPFO	Low Pass Filter Output
GND	Ground
LEDD	LED Drive

Parts List

Quantity	Part
1	Sensor
1	HBCC-0500
1	1N4148
1	2N3904
1	2N4403
1	2N5088
2	39 Ω
1	9.1 kΩ
2	20 kΩ
2	56 kΩ
1	390 kΩ
2	470 kΩ
1	680 kΩ
1	1.3 MΩ
1	2.0 MΩ
2	6.8 MΩ
1	Bin resistor R_b
1	12 pF
1	75 pF
1	330 pF
1	680 pF
2	1.0 nF
1	2.2 nF
1	8.2 nF
4	0.1 µF
3	0.22 µF
1	0.47 µF

Optional Parts List

Quantity	Part
1	1N4148
1	2N5088
1	2N3904
2	10 kΩ
1	220 kΩ
1	1.0 MΩ
1	2.0 MΩ
1	3.3 nF
1	1.0 µF

Bin Table

Bin #	1570, 1580 Rb Ω	1590 Rb Ω
1	8.2	22
2	11	27
3	15	36
4	18	47
5	24	56
6	30	75
7	36	91

Recommended Schematic

Shown is the recommended schematic for the HBCC-0500. Here are some construction tips.

1. Place the sensor, 2N4403, bin resistor, and the 0.47 µF cap close to each other to minimize loop area.
2. If the 0.47 µF cap is tantalum, its ESR must be used in series with R_b to determine the correct value for R_b.
3. A 1.0 µF ceramic cap may be used in place of the 0.47 µF cap.
4. Place the 0.22 µF cap attached to pins 4 and 23 close to the IC.
5. Use a single point ground close to pin 23.

Options

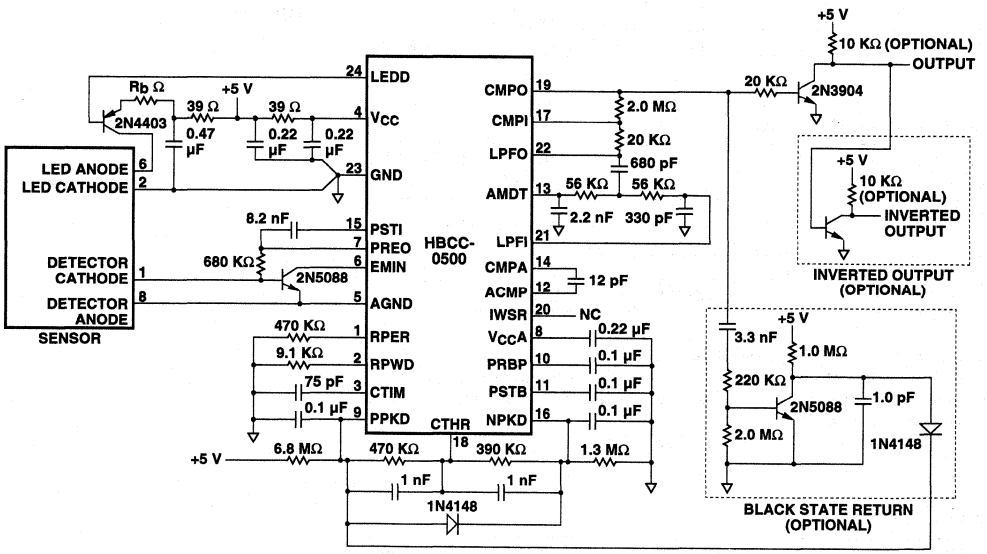
There are four options on the recommended schematic.

1. Output pull up resistor
2. Inverted output
3. Black state return
4. Threshold adjust

Pull Up Resistor

The 10 kΩ pull up resistor on the standard or inverted output transistor is optional. If the transistor is driving a cable, the resistor should be on the far end of the cable.

Schematic



BAR CODE

Inverted Output

The standard output of the HBCC-0500 is high when the sensor is looking at black bars, and low when the sensor is looking at white spaces. If inverted output is needed, add the extra circuitry in the inverted output block. Make sure that the 10 kΩ pull up resistor on the normal output transistor is loaded.

Black State Return

The HBCC-0500 normally returns to the white state 100 milliseconds after the last transition. The extra circuitry forces the black state after a time out period set by the 1.0 µF cap. The normal time out period is about 1.5 seconds. If a longer time is needed, increase the values of the 1.0 µF and the 3.3 nF caps. The ratio of values should be no more than 300:1.

Threshold Adjustment

The standard circuit uses a threshold designed for most bar codes. If the bar codes to be read *consistently* have narrow bars that are lighter than the wide bars, then the 470 kΩ and the 390 kΩ resistors attached to pin 18 should be swapped.

Warranty and Service

HP Digitizer ICs are warranted for a period of one year after purchase covering defects in material and workmanship. Hewlett-Packard will repair or, at its option, replace products that prove to be defective in material or workmanship under proper use during the warranty period.

NO OTHER WARRANTIES ARE EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. HEWLETT-PACKARD IS NOT LIABLE FOR CONSEQUENTIAL DAMAGES.

For additional warranty or service information, please contact your local Hewlett-Packard sales representative or authorized distributor.

Recommended Operating Conditions

Parameter	Min.	Max.	Units	Notes
Scan Velocity	7.6 (3)	76 (30)	cm/sec (in/sec)	1
Edge Contrast	40		%	2
V_{CC}	4.5	6.0	V	3
Ambient Temperature	-20	+65	°C	
Ambient Light		100,000	Lux	

Notes:

1. Narrow element width = 0.19 mm (0.0075 in.).
2. Contrast is defined as R_w - R_b, where R_w is the reflectance of the spaces in R_b is the reflectance of the bars, measured at the sensor wavelength (655 or 820 nm). 100% reflectance is barium sulfate.
3. Power supply ripple and noise should be less than 100 mV peak to peak.

Electrical Characteristics

Parameter	Symbol	Typical	Max.	Units	Notes
Supply Current, IC and Sensor	I_{CC}	2.7	4.0	mA	
High Level Output Current	I_{OH}		1.0	µA	
Low Level Output Voltage	V_{OL}		0.4	V	
Output Rise Time	t_r	4.5	20	µs	4
Output Fall Time	t_f	0.3	20	µs	4
Wake Up Time	t_w	50	200	ms	5

Notes:

4. Rise and fall time will be dependent upon the capacitance of the cable.
5. Wake up time is defined as the time from initial power turn on until the circuit is digitizing bar codes within data sheet limits.

HEWLETT® PACKARD

Single Chip Bar Code Decode IC

Technical Data

HBCR-1610
HBCR-1611
HBCR-1612

Features

- **Supports Five Industry Standard Bar Code Symbologies**
- **Automatic Code Recognition**
- **Choice of Parallel or Full Duplex Serial ASCII Interface**
- **Programmable via Escape Sequences or Pin Strapping**
- **CMOS**
- **Through Hole and Surface Mount Packages**
- **Audio and Visual Feedback Control**

Description

The Hewlett-Packard Single Chip Bar Code Decoder IC offers flexible bar code decoding that is designed to give OEMs the ability to address a growing number of industry segments and applications. Flexibility is made possible through firmware that allows the IC to automatically recognize and decode the most popular bar code symbologies. User implementation is easy since only a few supporting components are required.

The HBCR-1610 series decodes the most popular bar code symbologies used in applications in government, retail, industrial and medical markets. The IC automatically discriminates and decodes the following symbologies:

- Code 39 (Standard or Extended)
- Interleaved 2 of 5
- UPC A, E0, E1
- EAN/JAN 8, 13
- Codabar
- Code 128

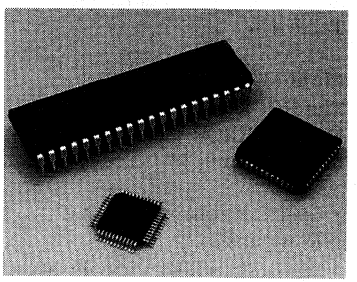
All bar codes may be scanned bidirectionally except for UPC/EAN/JAN bar codes with supplemental digits, which must be scanned so that the supplemental digits are scanned last.

Scanner Input

The HBCR-1610 decode ICs are designed to accept input from hand held digital scanners and slot readers. The maximum scan speed is 30 ips (73 cm/s).

Data Communications

The serial port supports a variety of baud rates, parity, and stop bits as described in Table 5. The IC has a "Single Read Mode" which allows the application program to stop data input until a "Next Read" command has been received. This allows the host computer to process data transmissions before enabling



subsequent reads. Control of data transmission is available using the standard XON/XOFF (D_1/D_3) handshake.

The parallel port is accomplished via an external 74HCT646 (octal bus transceiver) or two 74HCT574s (octal latches). There are handshake lines for both data and commands.

Feedback Features

Both audible and visual feedback are possible with the HBCR-1610 series. In both cases, the feedback outputs from the IC should be buffered before driving the transducer. An LED or beeper connected to the IC is either controlled directly by the IC, with signals generated by successful decodes, or controlled by the host system. The tone of the beeper can be configured to one of 16 tones, or can be silenced.

Power Requirements

The decoder IC is operated from a +5 volt DC power supply. The maximum current draw is 24 mA. The maximum power supply ripple voltage should be less than 100 mV, peak-to-peak.

Idle Mode

The IC automatically reduces power consumption whenever there is no scanning or decoding activity, or when there is no activity on the I/O port. See Table 4.

Manual

The HBCR-1610 Series Users Manual (HBCR-1697) covers the following topics:

- Specifications and Timing Diagrams
- Pin Definitions and Schematics
- General Scanning Tips
- Configuration and Operation
- Escape Sequence Programming
- Data Output Formats
- Sample Bar Codes
- I/O and Pacing Characteristics

IC Configuration

The default configuration is set when the IC powers up or when a Hard Reset command is received. Default configuration of many of the options is dependent on the logic states of IC pins, as shown in Table 5. A complete description of the pins and all possible configurations is in the Users Manual. More complete and flexible configuration is achieved using escape sequence commands.

There are two pins that cause significant changes in the IC operation.

Table 1. Recommended Operating Conditions

Parameter	Symbol	Minimum	Maximum	Units	Notes
Supply Voltage	V_{CC}	4.5	5.5	V	1
Ambient Temperature	T_A	0	+70	°C	
Oscillator Frequency	F_{OSC}	DC	16.000	MHz	2

Notes:

1. Maximum power supply ripple of 100 mV peak-to-peak.
2. The IC can use either an 11.059 or a 16.000 MHz crystal or ceramic resonator. The FRQ pin selects the frequency that matches the oscillator.

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_S	-65	+150	°C	
Supply Voltage	V_{CC}	-0.5	+7.0	V	
Pin Voltage	V_{IN}	-0.5	V_{CC} + 0.5	V	3

Note:

3. Voltage on any pin with respect to ground.

Table 3. Ordering Information

Part Number	Description
HBCR-1610	CMOS, 40 pin DIP, bulk shipment, no manual
HBCR-1611	CMOS, 44 pin PLCC, bulk shipment, no manual
HBCR-1612	CMOS, 40 pin QFP, bulk shipment, no manual
HBCR-1697	HBCR-1610 Series Users Manual
Option A01	IC individually bagged, no manual
Option B01	IC individually boxed with manual and data sheet

FRQ Pin

The FRQ pin is used to tell the IC what frequency oscillator is attached to the IC. Using the higher frequency allows greater maximum scan speeds, but causes the IC to draw slightly more supply current. If the state of the FRQ pin does not match the actual oscillator, beeper tones, LED flash length, parallel port timing, and serial port baud rates are adversely affected.

FRQ	Oscillator Frequency
0	16.000 MHz
1	11.059 MHz

IOM Pin

The IOM pin selects between the serial and parallel I/O mode of the IC. Depending on the state of the IOM pin, definitions of several configuration pins change or move to new positions.

IOM	I/O Mode
0	Parallel
1	Serial

Escape Sequences

The following set of escape sequences is used to control the IC and change its default configuration. Note that all configuration changes will be lost after a Hard Reset, or after power up. Detailed information on how to formulate and use escape sequences is given in the Users Manual.

Table 7. Escape Sequences

Escape Sequence	Function
Ec - y <n> b	Good Read Beep Tone
Ec - y <n> d	Serial Intercharacter Delay
Ec E	Hard Reset
Ec - y <n> f	Bar Code Symbology Selection
Ec - y <n> g	Check Character Options
Ec - y <n> h	Decoding Options
Ec - y <n> j	Single Read Mode
Ec - y <n> k	Single Read Control
Ec - y <n> l	LED Control
Ec - y <n> m	Interleaved 2 of 5 Length
Ec - y <n> O <n characters>	Trailer Selection
Ec - y <n> q	Code ID Characters
Ec - y <n> s	Status Request
Ec - y <n> t	Sound Tone
Ec - y <n> w	Scanner Enable

Table 4. DC Characteristics

HBCR-1610, 1611, 1612 (T_A = 0°C to +70°C, V_{CC} = 4.5 V to 5.5 V, V_{SS} = 0 V)

Symbol	Parameter	1610 Pins	1611 Pins	1612 Pins	Min.	Max.	Units	Test Conditions
V_{IL}	Input Low Voltage	all	all	all	-0.5	0.2 V_{CC} - 0.1	V	
V_{IH}	Input High Voltage	except 9, 19	except 10, 21	except 4, 15	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage	9, 19	10, 21	4, 15	0.7 V_{CC}	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage	1-8, 10-17, 21-28	2-9, 11, 13-19, 24-31	1-3, 5, 7-13 18-25, 40, 44		0.45	V	I_{OL} = 1.6 mA
V_{OL1}	Output Low Voltage	32-39	36-43	30-37		0.45	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage	1-8, 10-17, 21-28	2-9, 11, 13-19, 24-31	1-3, 5, 7-13 18-25, 40-44	2.4		V	I_{OH} = -60 µA
					0.75 V_{CC}		V	I_{OH} = -25 µA
					0.9 V_{CC}		V	I_{OH} = -10 µA
V_{OH1}	Output High Voltage	32-39	36-43	30-37	2.4		V	I_{OH} = -400 µA
					0.75 V_{CC}		V	I_{OH} = -150 µA
					0.9 V_{CC}		V	I_{OH} = -40 µA
I_{IL}	Input Low Current	1-8, 10-17, 21-28	2-9, 11, 13-19, 24-31	1-3, 5, 7-13, 18-25, 40-44		-50	µA	V_{IN} = 0.45 V
I_{LI}	Input Leakage Current	32-39	36-43	30-37		± 10	µA	$V_{SS} \le V_{IN} \le V_{CC}$
R_{RST}	Pulldown Resistor	9	10	4	50	150	KΩ	
I_{CC}	Supply Current 11.059 MHz	40	44	38		18	mA	Scanning
						4	mA	Idle
I_{CC}	Supply Current 16.000 MHz	40	44	38		24	mA	Scanning
						6	mA	Idle

Table 5. Summary of Features and Configurations – HBCR-1610 Series

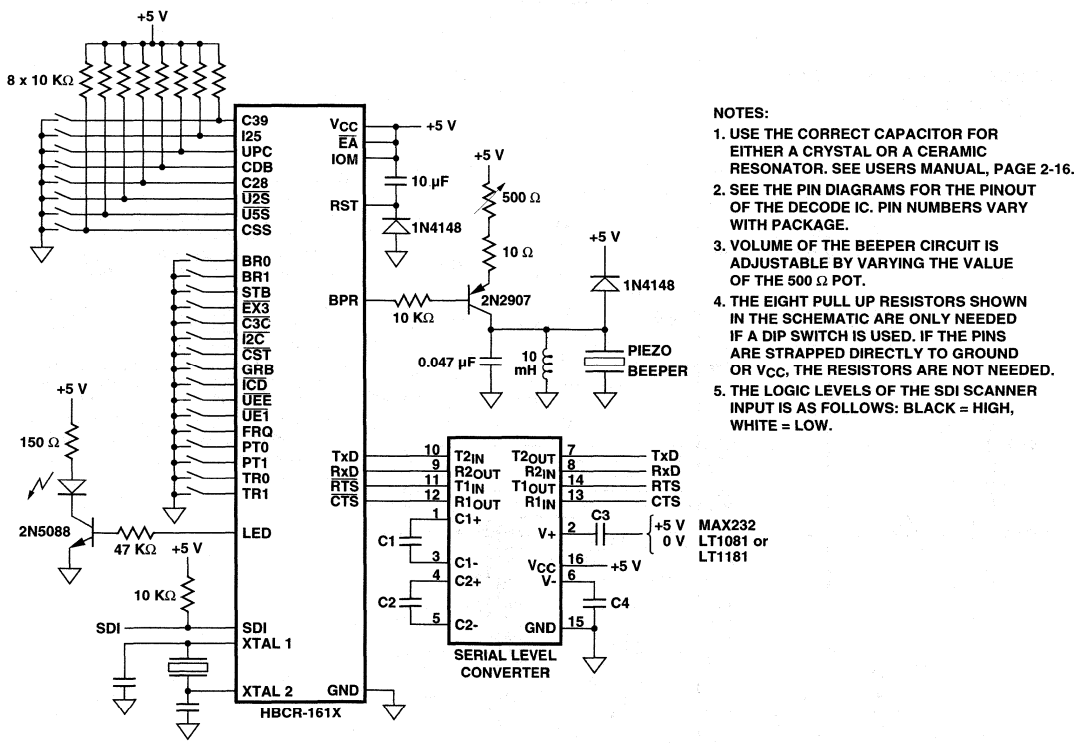
Feature	Function or Value	Default Setting	
		Serial Mode	Parallel Mode
Bar Code Symbology	When a symbology is enabled, bar codes of that type can be read, assuming other decoding options are satisfied.	Depends on pins: C39, I25, UPC CDB and C28.	All codes enabled
Interleaved 2 of 5 Label Length	Length variable from 4 to 32, or specific lengths from 2 to 32, or 6 or 14 only	Variable, 4-32	Variable, 4-32
Check Character Verification	For Code 39 For Interleaved 2 of 5 For Code 128† For UPC/EAN†	Depends on pin $\overline{\text{C3C}}$ Depends on pin $\overline{\text{I2C}}$ Enabled Enabled	Depends on pin $\overline{\text{C3C}}$ Depends on pin $\overline{\text{I2C}}$ Enabled Enabled
Check Character Transmission	For Code 39 and Interleaved 2 of 5 For UPC/EAN For Code 128†	Depends on pin $\overline{\text{CST}}$ Enabled Enabled	Depends on pin $\overline{\text{CST}}$ Enabled Enabled
Extended Code 39 Enable	Converts paired Code 39 data characters to Full ASCII characters	Depends on pin $\overline{\text{EX3}}$	Depends on pin $\overline{\text{EX3}}$
UPC/EAN Decoding Options	UPC vs. UPC/EAN UPC E expansion to UPC A UPC E Version 1 autodiscrimination UPC/EAN supplemental digits UPC/EAN check digit UPC/EAN output format	UPC/EAN Depends on pin $\overline{\text{UEE}}$ Depends on pin $\overline{\text{UE1}}$ Depends on pins $\overline{\text{US2}}$ and $\overline{\text{US5}}$ Transmitted Standard	UPC/EAN Depends on pin $\overline{\text{UEE}}$ Depends on pin $\overline{\text{UE1}}$ Disabled Transmitted Standard
Codabar Start/ Stop Transmission	Transmits or suppresses Codabar start/stop characters	Depends on pin CSS	Depends on pin CSS
Baud Rates	1200, 2400, 4800, 9600	Depends on pins BR0 and BR1	–
Parity	0s, 1s, even, odd	Depends on pins PT0 and PT1	0s
Stop Bits	1 or 2	Depends on pin STB	–
XON/XOFF Pacing†	Controls data flow on either port	Enabled	Enabled
Transmitted Character Delay Enable	Controls 10 millisecond intercharacter delay on the serial port	Depends on pin $\overline{\text{ICD}}$	–
Trailer Selection	String of characters appended to the decoded message (4 maximum)	C_R, C_R L_F, H_T, or none Depends on pins TR0 and TR1	C_R
Single Read Mode	Controls when labels can be read	Disabled	Disabled
Code ID Character Enable	Controls the transmission of the Code ID characters before decoded data	Disabled	Disabled
Good Read Beep Tone Selection	Controls the tone sounded when a bar code label is read	High or low pitch Depends on pin GRB	High or low pitch Depends on pin GRB
LED Control	Controls LED function: flash or turn off after a label is read	Auto Flash Mode	Auto Flash Mode

†Not configurable.

Table 6. Summary of Commands – HBCR-1610 Series

Feature	Description
Scanner Enable	When enabled, scans from a wand or a slot reader are decoded; otherwise, they are ignored.
Hard Reset	Resets the IC as though it were just powered up.
Self Test Failure Message	An error message is transmitted over the serial port at 9600 baud at power up if the IC self test fails.
Status Request	Returns the version number of the software.
Sound Tone	Causes the IC to sound a tone of the selected pitch for 120 milliseconds.

Stand Alone Decoder (Serial Mode)



NOTES:

1. USE THE CORRECT CAPACITOR FOR EITHER A CRYSTAL OR A CERAMIC RESONATOR. SEE USERS MANUAL, PAGE 2-16.
2. SEE THE PIN DIAGRAMS FOR THE PINOUT OF THE DECODE IC. PIN NUMBERS VARY WITH PACKAGE.
3. VOLUME OF THE BEEPER CIRCUIT IS ADJUSTABLE BY VARYING THE VALUE OF THE 500 Ω POT.
4. THE EIGHT PULL UP RESISTORS SHOWN IN THE SCHEMATIC ARE ONLY NEEDED IF A DIP SWITCH IS USED. IF THE PINS ARE STRAPPED DIRECTLY TO GROUND OR V_{CC}, THE RESISTORS ARE NOT NEEDED.
5. THE LOGIC LEVELS OF THE SDI SCANNER INPUT IS AS FOLLOWS: BLACK = HIGH, WHITE = LOW.

Surface Mount IC Drying

Whenever Vapor Phase or Infrared Reflow technologies are used to mount either of the surface mount packages, there is a possibility that previously absorbed moisture, heated very rapidly to the reflow temperatures, may cause the package to crack from internal stresses. There is a reliability concern that moisture may then enter the package over a period of time, and metal corrosion may take place, degrading the IC performance.

To reduce the amount of absorbed moisture and prevent cracking, all of the surface mount ICs should undergo one of the following baking cycles. The parts MUST then be mounted within 48 hours. If the parts are not mounted within 48 hours, they *must* be rebaked.

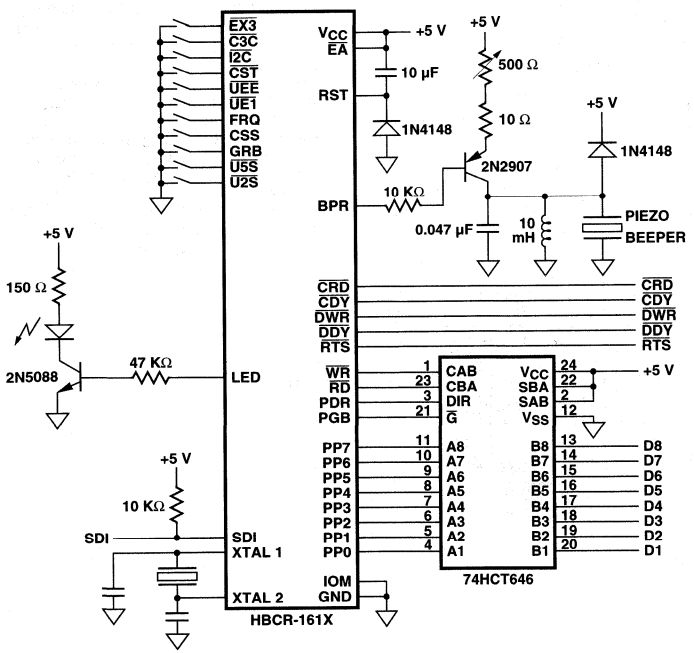
The total number of baking cycles must not exceed two (2). If the ICs are baked more than twice, Hewlett-Packard cannot guarantee the performance and reliability of the parts.

Neither bake cycle can be performed in the standard shipping tubes. The ICs must be baked in an ESD safe, mechanically stable container, such as an aluminum tube or pan.

Cycle	Temperature	Time
A	125°C	24 Hours
B	60°C	96 Hours

Note: Cycle B must be done in an atmosphere of <5% relative humidity air or nitrogen.

Stand Alone Decoder (Parallel Mode)

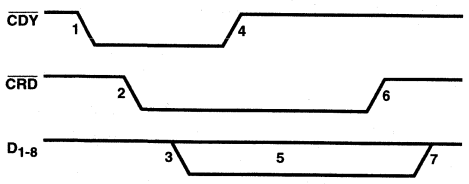


NOTES:

1. USE THE CORRECT CAPACITOR FOR EITHER A CRYSTAL OR A CERAMIC RESONATOR. SEE THE USERS MANUAL.
2. SEE PIN DIAGRAMS FOR THE PINOUT OF THE DECODE IC. PIN NUMBERS VARY WITH PACKAGE.
3. VOLUME OF THE BEEPER CIRCUIT IS ADJUSTABLE BY VARYING THE VALUE OF THE 500 Ω POT.
4. AN ALTERNATIVE CIRCUIT USING TWO 74HCT574 OCTAL LATCHES INSTEAD OF THE 74HCT646 IS IN THE USERS MANUAL.
5. THE LOGIC LEVELS OF THE SDI SCANNER INPUT IS AS FOLLOWS: BLACK = HIGH, WHITE = LOW.

Parallel I/O Handshake

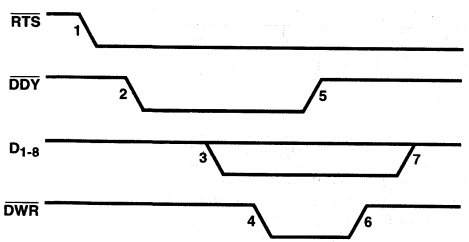
COMMANDS RECEIVED BY THE IC



PROTOCOL

1. THE HOST INDICATES THAT A COMMAND IS PENDING BY LOWERING $\overline{CDY}$.
2. THE IC INDICATES THAT IT IS READY FOR A COMMAND BY LOWERING $\overline{CRD}$.
3. THE HOST OUTPUTS THE COMMAND ONTO THE DATA BUS.
4. THE HOST INDICATES THAT THE DATA IS STABLE BY RAISING $\overline{CDY}$.
5. THE IC READS THE COMMAND FROM THE BUS.
6. THE IC INDICATES THAT THE COMMAND WAS ACCEPTED BY RAISING $\overline{CRD}$.
7. THE HOST REMOVES THE DATA FROM THE DATA BUS.

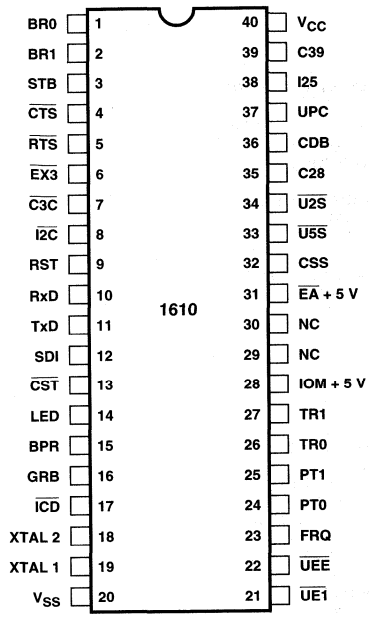
DATA TRANSMITTED FROM THE IC

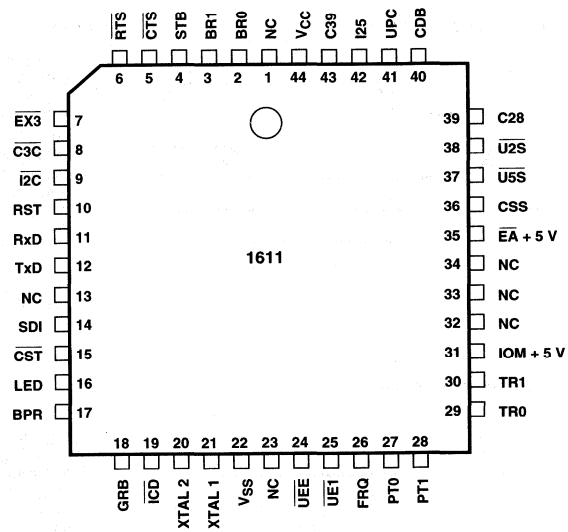


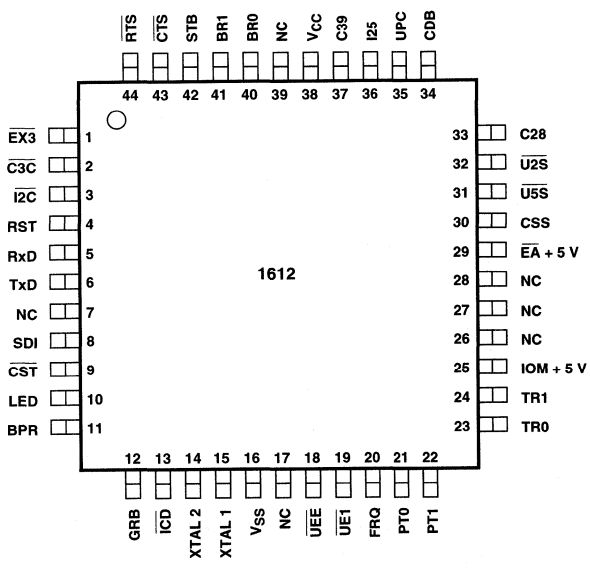
PROTOCOL

1. THE IC INDICATES DATA IS READY TO BE TRANSMITTED BY LOWERING $\overline{RTS}$; $\overline{RTS}$ STAYS LOW UNTIL THE LAST BYTE HAS BEEN TRANSMITTED.
2. THE HOST SIGNALS THE IC THAT IT IS READY FOR DATA BY LOWERING $\overline{DDY}$.
3. THE IC OUTPUTS DATA ONTO THE BUS.
4. THE IC INDICATES THAT THE DATA IS STABLE BY LOWERING $\overline{DWR}$.
5. THE HOST ACKNOWLEDGES THAT THE DATA IS RECEIVED BY RAISING $\overline{DDY}$.
6. THE IC INDICATES THE END OF THE OUTPUT CYCLE BY RAISING $\overline{DWR}$.
7. THE IC REMOVES DATA FROM THE BUS.

Serial Pinout

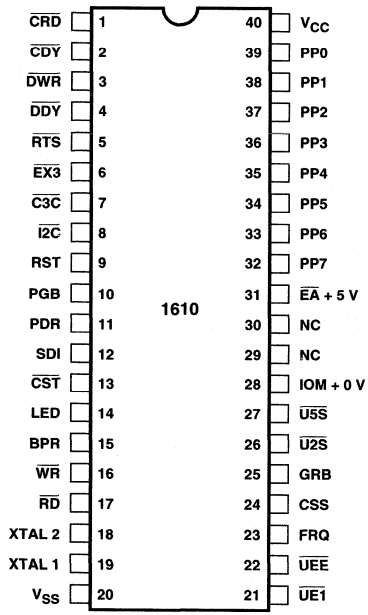


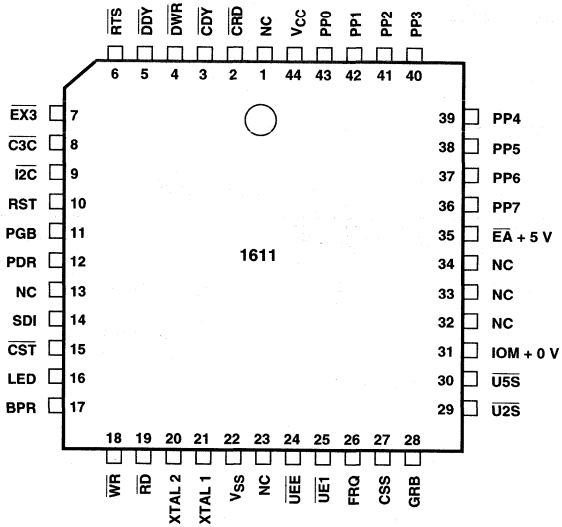


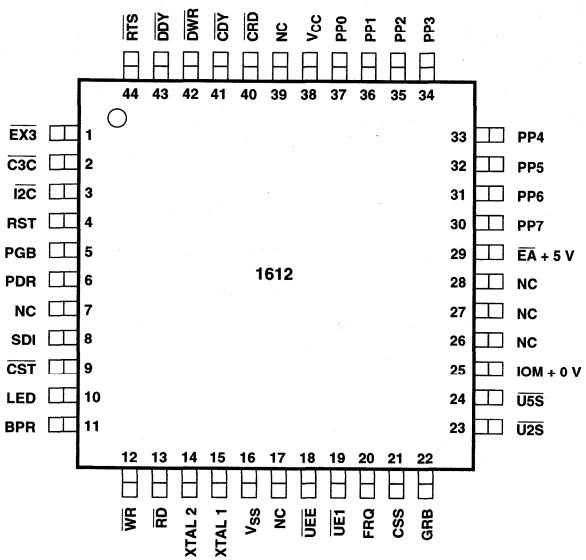


PIN MNEMONICS	
RxD	RECEIVED DATA
TxD	TRANSMITTED DATA
BR0-BR1	BAUD RATE SELECT
PT0-PT1	PARITY SELECT
TR0-TR1	TRAILER CHARACTERS SELECT
$\overline{CTS}$	CLEAR TO SEND
$\overline{RTS}$	REQUEST TO SEND
C39	CODE 39 ENABLE
$\overline{EX3}$	EXTENDED CODE 39 ENABLE
I25	INTERLEAVED 2 OF 5 ENABLE
UPC	UPC/EAN ENABLE
CDB	CODABAR ENABLE
C28	CODE 128 ENABLE
$\overline{UEE}$	UPC E EXPANSION ENABLE
$\overline{UE1}$	UPC E VERSION 1 ENABLE
$\overline{U2S}$	UPC 2 DIGIT SUPPLEMENTALS ENABLE
$\overline{U5S}$	UPC 5 DIGIT SUPPLEMENTALS ENABLE
CSS	CODABAR START/STOP CHAR. ENABLE
STB	STOP BITS SELECT
$\overline{C3C}$	CODE 39 CHECKSUM ENABLE
$\overline{I2C}$	INTERLEAVED 2 OF 5 CHECKSUM ENABLE
$\overline{CST}$	CHECKSUM TRANSMIT ENABLE
SDI	SCANNER DIGITAL INPUT
IOM	I/O MODE SELECT
RST	IC RESET
$\overline{EA}$	EXTERNAL PROGRAM MEMORY ENABLE
GRB	GOOD READ BEEP TONE SELECT
FRQ	OSCILLATOR FREQUENCY SELECT
LED	LED CONTROL LINE
BPR	BEEPER CONTROL LINE
$\overline{ICD}$	INTERCHARACTER DELAY ENABLE
XTAL1	OSCILLATOR INPUT
XTAL2	OSCILLATOR INPUT
V_{CC}	POWER
V_{SS}	GROUND

Parallel Pinout

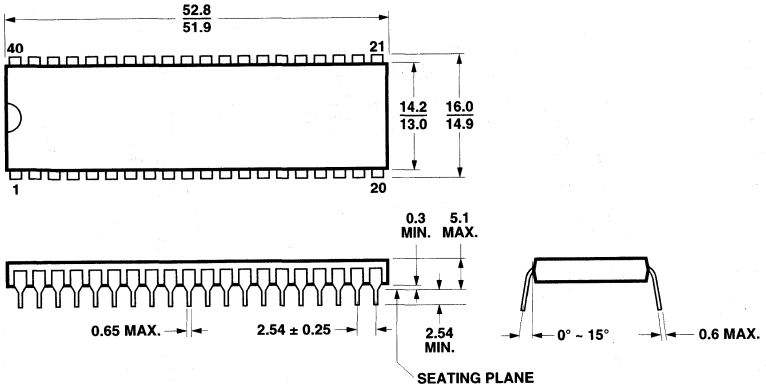




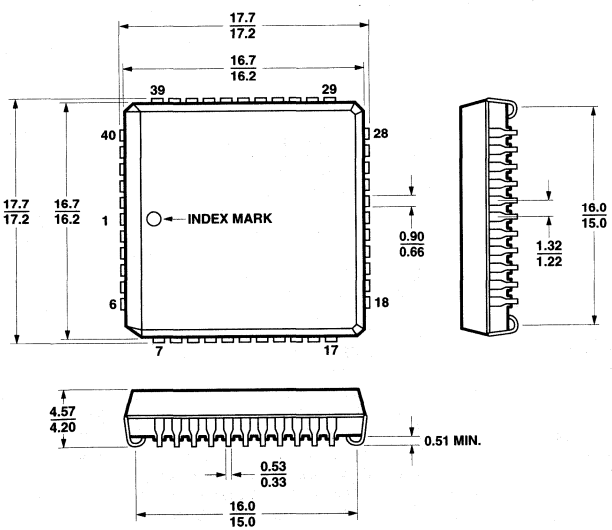


PIN MNEMONICS	
PP0-PP7	PARALLEL PORT BUS
DWR	DATA WRITE HANDSHAKE
DDY	READY FOR DATA HANDSHAKE
CRD	COMMAND READ HANDSHAKE
CDY	COMMAND READY HANDSHAKE
RTS	REQUEST TO SEND
C3C	CODE 39 CHECKSUM ENABLE
I2C	INTERLEAVED 2 OF 5 CHECKSUM ENABLE
CST	CHECKSUM TRANSMIT ENABLE
EX3	EXTENDED CODE 39 ENABLE
WR	DATA WRITE
RD	DATA READ
U2S	UPC 2 DIGIT SUPPLEMENTALS ENABLE
U5S	UPC 5 DIGIT SUPPLEMENTALS ENABLE
CSS	CODABAR START/STOP CHAR. ENABLE
PGB	TRANSCEIVER DRIVE ENABLE
PDR	TRANSCEIVER DIRECTION CONTROL
UEE	UPC E EXPANSION ENABLE
UE1	UPC E VERSION 1 ENABLE
SDI	SCANNER DIGITAL INPUT
IOM	I/O MODE SELECT
RST	IC RESET
EA	EXTERNAL PROGRAM MEMORY ENABLE
FRQ	OSCILLATOR FREQUENCY SELECT
GRB	GOOD READ BEEP TONE SELECT
LED	LED CONTROL LINE
BPR	BEEPER CONTROL LINE
XTAL1	OSCILLATOR INPUT
XTAL2	OSCILLATOR INPUT
VCC	POWER
VSS	GROUND

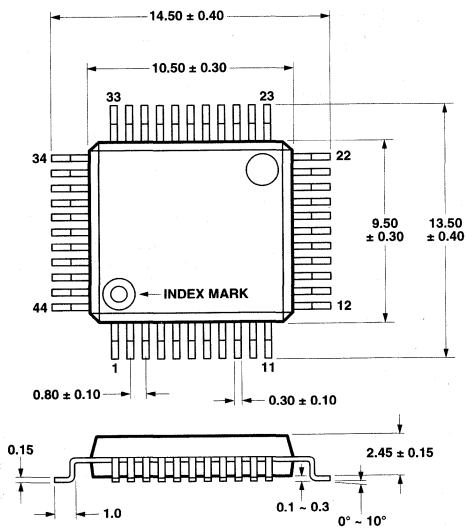
Mechanical Specifications – Units (mm)



HBCR-1610



HBCR-1611



HBCR-1612

HEWLETT® PACKARD

Programmable Bar Code Decode ICs

Technical Data

HBCR-2210
HBCR-2211

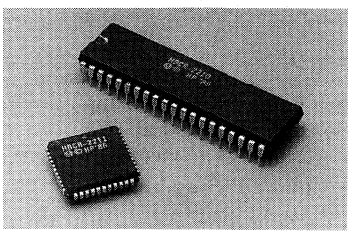
Features

- **Ideal for Hand Scanning and Non-contact Laser Scanning Applications**
- **Supports 7 Industry Standard Bar Code Symbologies**
- **Automatic Code Recognition**
- **Choice of Parallel or Serial Interface**
- **Full Duplex ASCII Interface**
- **Extensive Configuration Control**
- **Optical and Escape Sequence Configuration**
- **Input and Output Buffering**
- **Low Current (18 mA) CMOS Technology**
- **40 Pin DIP and 44 Pin PLCC Packages**
- **Audio and Visual Feedback Control**
- **EEPROM Support for Nonvolatile Configuration**
- **Single +5 Volt Supply**

Description

Hewlett-Packard's Bar Code Decoder ICs offer flexible bar code decoding capability that is designed to give OEMs the ability to address a growing number of industry segments and applications. Flexibility is made possible through sophisticated firmware which allows the ICs to accept data from a wide variety of scanners and to automatically recognize and decode the most popular bar code symbologies. User implementation of the decoder ICs is easy since it requires only a few supporting components and provides a standard I/O interface.

Manufacturers of data collection terminals, point of sale terminals, keyboards, weighing scales, medical equipment, test instrumentation, material handling equipment, and other systems having data collection needs are finding a growing demand for bar code reading capability in their products. The HBCR-2210 series decode ICs make it easy to add this capability without the need to invest in the development of bar code decoding software.



The bar code decoder ICs are compatible with most hand held scanners and some medium speed machine mounted laser heads. The HBCR-2210 series is compatible with fixed beam non-contact scanners, digital wands, and slot readers. In addition, the decoder is optimized for use with the Symbol Technologies moving beam laser scanners, but is also compatible with many other moving beam non-contact laser scanners with a similar interface protocol.

The HBCR-2210 series decoder ICs are excellent decoding solu

tions for a number of stationary scanning applications found in automated systems. The scan rate for moving beam applications should be similar to the scan rates for hand held laser scanners (35 to 45 scans per second). The scan speed for fixed beam applications should be similar to the scan speeds typical of wands and slot readers. For moving beam applications, it is necessary for the scanner to utilize the three laser control lines.

The HBCR-2210 series decodes the most popular bar code symbologies now in use in applications in the industrial, retail, government and medical markets:

- **Code 39 (Standard or Extended)**
- **Interleaved 2 of 5**
- **UPC A, E**
- **EAN/JAN 8, 13**
- **Codabar**
- **Code 128**
- **Code 11**
- **MSI Code**

When more than one symbology is enabled, the bar code being scanned will automatically be recognized and decoded, except for Standard versus Extended Code 39, which are mutually exclusive. Bi-directional scanning is allowed for all bar codes except UPC/EAN/JAN with supplemental digits, which must be scanned with the supplemental digits last.

The I/O for the decode IC is full duplex, 7 bit ASCII. Both serial and parallel interfacing are available. The serial interface can be converted to an RS232C interface or connected directly to another microprocessor for data processing. The parallel interface can be connected to a 74HC646 octal bus transceiver chip (or an equivalent part). Feedback to the operator is accomplished by signals for an LED and a beeper. In addition, there are many programmable functions that cover such items as code selection, good read beep tone, Header and Trailer buffers, laser scanning control, beeper tone, etc. See Table 2 for a complete list.

Performance Features

Bar Codes Supported

Code 39 is an alphanumeric code, while Extended Code 39 encodes the full 128 ASCII character set by pairing Code 39 characters. Both can be read bi-directionally with message lengths of up to 32 characters. An optional checksum character can be used with these codes, and the ICs can be configured to verify this character prior to data transmission.

Interleaved 2 of 5 code, a compact numeric only bar code, can also be read bi-directionally with message lengths from 4 to 32 characters. To enhance data accuracy, optional checksum character verification and/or message length checking can be enabled.

The following versions of UPC, EAN and JAN bar codes can be read bi-directionally: UPC-A, UPC-E, EAN-8, EAN-13, JAN-8, and JAN-13. All versions can be enabled simultaneously or decoding can be restricted to only the UPC codes. UPC, EAN, and JAN codes printed with complementary two or five digit supplemental encodations can be read in two different ways. If the codes are enabled without the supplemental encodations, then only the main part of symbols printed with supplemental encodations will be read. If the reading of supplemental encodations is enabled, then only symbols with these supplements will be read. When supplemental encodations are enabled, the bar code symbols must be read in a direction which results in the supplements being scanned last.

Codabar, a numeric only bar code with special characters, can be read bi-directionally for message lengths up to 32 characters. The decode IC can be configured to transmit or suppress the Codabar start/stop characters.

Code 128, a full ASCII symbology, can be scanned bi-directionally with message lengths of up to 32 characters.

Code 11 is a numeric, high density code with one special character, the hyphen (-). Verification of one or two check characters must be enabled, and the check character(s) are always transmitted. This code can be scanned bi-directionally.

MSI Code is a numeric, continuous code, with message lengths up to 32 characters. The check digit, a modulo 10 checksum, is always verified and transmitted. This code can be scanned bi-directionally.

Scanner Input

The HBCR-2210 decode IC is designed to accept data from hand held digital scanners or slot readers with the following logic state: black = high, white = low. The same decode IC also accepts

data from hand held laser scanners with the opposite logic states: black = low, white = high. The scanner type pin (SCT) on the HBCR-2210 series must be driven prior to power up or hard reset to identify the type of scanner connected.

In the HBCR-2210 series ICs, the automatic laser shutoff feature delay time is adjustable as a configuration option. Applications which require increased accuracy may need the redundancy check feature.

Scanner input can be disabled by software command. This allows an application program to control when an operator can enter data, preventing inadvertent data entry. It also allows the program to verify each scan before enabling subsequent scans. The HBCR-2210 series also offers two Single Read Modes which allow the application program to stop bar code data entry until a "Next Read" command is received, allowing the host computer to process data transmissions before enabling subsequent reads.

Configuration Control and Non-volatile Storage

Configuration of the decoder IC is done by any of three methods. A minimal subset of key options can be "hardwired" – controlled by electrically strapping specified pins on the decoder IC itself. Which pins affect configuration depends on the selection of serial or parallel interface. Alternatively, ASCII characters in the form of HP Escape Sequences (a format common to HP decoder ICs) can be sent to the serial or parallel I/O port; these commands can be used to control all configurable options. A third method is optical configuration, which makes use of special bar code menus supplied by HP. Menu labels can be created to modify any configurable options. A summary of the decoder IC features and applicable configuration methods for each is presented in Tables 2 and 3.

Once configuration has been set, it can be stored in an optional non-volatile memory, if included in the decoder circuit. When the EEP pin is tied high, the decoder IC drives I/O lines compatible with the widely available 9346/93C46 family of serial EEPROMS. The configuration is thereby saved during power down of the system and automatically reloaded at power up. Escape sequence commands allow explicit storage and recall of configuration settings. When using optical configuration, storage is automatic. If the EEP pin is tied low, the EEPROM is not used, so only hardwired configuration options are saved through powerdown; all others are set to default values at powerup. Table 2 shows default values of all features.

Data Communications

The serial port supports a wide range of baud rates, parities, and stop bits as described in Table 2. Software control of data transmission can be accomplished with a standard Xon/Xoff (DC1/DC3) handshake. The decode IC also supports an RTS/CTS hardware handshake.

The parallel port data has configurable parity. When the SMD pin is tied low, several pins pertaining to the serial port change function to control a parallel port instead. Pins 1 through 5 on DIP packages assume the function of handshake lines for the parallel port. The port itself is an external '646 family octal bus transceiver. Processor pins 10 and 11 (TXD and RXD in serial mode) now control the transceiver chip along with pins 16 and 17, RD and WR. Alternative circuits using SSI latch chips can be substituted for the '646 implementation to customize the function of the parallel port to a particular bus configuration.

Feedback Features

Both audio and visual feedback are possible with the HBCR-2210 series. In both cases, the outputs from the ICs should be buffered before driving the actual feedback transducer. An LED or beeper connected to the decoder IC can be controlled directly by the IC, with signals generated by successful decodes, or can be controlled by the host system. In addition, the tone of the beeper can be configured to be one of 16 different frequencies, or can be silenced.

Power Requirements

The decoder IC operates from a +5 volt DC power supply. The maximum current draw is 18 mA. The maximum power supply ripple voltage should be less than 100 mV, peak-to-peak.

Handling Precautions

The decoder ICs are extremely sensitive to electrostatic discharge (ESD). It is important that proper anti-static procedures be observed when handling the ICs. The package should not be

opened except in a static free environment.

Manuals

The decode IC Users Manual covers the following topics:

- Data output formats
- I/O interfaces
- Laser input timing diagrams
- Escape sequence syntax and functionality
- Example schematics
- All configurable options
- Bar code menus
- Scanner positioning and tilt
- Sample bar code symbols
- Appendices describing bar code symbologies

Table 1. Ordering Information

Part Number	Description
HBCR-2210	CMOS, 40 pin DIP, bulk ship, no manual
HBCR-2211	CMOS, 44 pin PLCC, bulk ship, no manual
OPT A01	IC individually boxed with manual and data sheet
HBCR-2297	HBCR-2210 Series Users Manual

Recommended Operating Conditions

Parameter	Symbol	Minimum	Maximum	Units	Notes
Supply Voltage	V_{CC}	4.0	6.0	V	1
Ambient Temperature	T_A	-40	+85	°C	
Crystal Frequency	XTAL	0 (DC)	11.059	MHz	2
Element Time Interval (Moving Beam)	ETI_M	13	555	µs	2, 3, 4
Element Time Interval (Contact Scanner)	ETI_C	50	71000	µs	3, 4

Notes:

1. Maximum power supply ripple of 100 mV peak to peak.
2. The HBCR-2210 series uses a 11.059 MHz crystal. For different crystal frequencies. multiply the specified baud rate and beeper frequencies by (crystal frequency/11.059 MHz) and multiply the element time interval ranges by (11.059 MHz/crystal frequency).
3. At the specified crystal frequency.
4. Corresponds to a scan rate of 35 to 45 scans per second.

Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_S	-55	+150	°C	
Supply Voltage	V_{CC}	-0.5	+7.0	V	5
Pin Voltage	V_{IN}	-0.5	V_{CC} + 0.5	V	5, 6

Notes:

5. T_A = 25°C.
6. Voltage on any pin with respect to ground.

DC Characteristics

HBCR-2210, 2211 **(T_A = 40°C to +85°C, V_{CC} = 4.5 V to 5.5 V, V_{SS} = 0 V)**

Symbol	Parameter	HBCR-2210 Pins	HBCR-2211 Pins	Min.	Max.	Units	Test Conditions
V_{IL}	Input Low Voltage	all	all	-0.5	0.2 V_{CC} - 0.1	V	
V_{IH}	Input High Voltage	except 9, 18	except 10, 20	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage	9, 18	10, 20	0.7 V_{CC}	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage	1-8, 10-17, 21-28	2-9, 11, 13-19, 24-31		0.45	V	I_{OL} = 1.6 mA
V_{OL1}	Output Low Voltage	30, 32-39	33, 36-43		0.45	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage	1-8, 10-17, 21-28	2-9, 11, 13-19, 24-31	2.4		V	I_{OH} = -60 µA
				0.75 V_{CC}		V	I_{OH} = -30 µA
				0.9 V_{CC}		V	I_{OH} = -10 µA
V_{OH}	Output High Voltage	30, 32-39	33, 36-43	2.4		V	I_{OH} = -400 µA
				0.75 V_{CC}		V	I_{OH} = -150 µA
				0.9 V_{CC}		V	I_{OH} = -40 µA
I_{IL}	Input Low Current	1-8, 10-17, 21-28	2-9, 11, 13-19, 24-31	-10	-200	µA	V_{IN} = 0.45 V
I_{IL2}	Input Low Current	18	20		-3.2	mA	V_{IN} = 0.45 V
I_{LI}	Input Leakage Current	32-39	36-43		± 10	µA	0.45 ≤ V_{IN} ≤ V_{CC}
R_{RST}	Pulldown Resistor	9	10	20	125	KΩ	
I_{CC}	Power Supply Current	–	–		18	mA	All Outputs disconnected
I_{CC}	Idle Mode Power Supply Current	–	–		9	mA	Note 7.

Note:

7. Applies only to HBCR-2210 and -2211 in Wand Mode or Laser Mode with Laser Idling enabled with no scanning or I/O operation in progress.

Table 2. Summary of Features and Configurations - HBCR-2210 Series

In the table below, the column entitled Selection is either:

Software	Escape Sequence and Optical Menu Programmability
Hardwire	Control of a feature by electrically strapping specified pins on the decoder IC itself
Both	Both Software and Hardwire

Feature	Function or Value	Selection	Default Setting
Code Selection	When a symbology is enabled, bar codes of that type can be read, assuming that other decoding options are satisfied.	Both	Decoding of all codes is enabled
Minimum/Maximum Label Length Selection	Code 39, Codabar, Code 128, Code 11, and MSI Code	Software	Min. = 1 Max. = 32
	Interleaved 2 of 5	Software	Min. = 4 Max. = 32
Interleaved 2 of 5 Specific Label Length Selection	Length variable from 4 to 32, or a specific even length between 2 and 32, or lengths 6 and 14 only	Software	4 to 32

(continued)

Feature	Function or Value	Selection	Default Setting
Check Character Verification Enable	For Code 39 For Interleaved 2 of 5 When enabled, the check character at the end of the bar code data is verified by the decoder	Software Software	Disabled Disabled
Check Character Transmission Enable	For both Code 39 and Interleaved 2 of 5, the check characters verified by the reader are included at the end of the decoded message	Software	Disabled
Code 39 Full ASCII Conversion Enable	Extended Code 39 data will be converted to ASCII characters	Software	Disabled
UPC/EAN/JAN Decoding Options Selection	UPC/EAN/JAN vs. UPC only Enable 2 or 5 digit supplements Autodiscrimination of tags with and without supplements	Software Software	UPC/EAN/JAN Enabled Supplements Disabled Disabled
Codabar Data Start/Stop Transmission Enable	Transmit or suppress start/stop characters	Software	Transmit
Code 11 Check Digit Verification Selection	Selection of 1 or 2 check digits	Software	1 check digit
Baud Rates	150, 300, 600, 1200, 2400, 4800, 9600, 19200	Both	Depends on pins BR1, BR0, and SMD
Parity	0s, 1s, Odd, Even	Both	Depends on pins EEP, PT1 and PT0
Stop Bits	1 or 2	Both	Depends on pins SMD and STB
RTS/CTS Pacing Enable	Request-To-Send/Clear-To-Send Pacing controls serial port data transmission	Software	Enabled
Xon/Xoff Pacing Enable	Controls data transmission on serial or parallel port by means of control characters sent to decoder IC	Software	Disabled
Transmitted Character Delay Enable	Specifies whether a delay is inserted between characters transmitted on the serial port	Software	Disabled
Transmitted Character Delay Selection	Specifies the number of milliseconds to insert between completion of transmission of one character and beginning of transmission of the next (1 to 250 ms)	Software	20 msec

(continued)

Feature	Function or Value	Selection	Default Setting
Header Selection	A string of characters pre-pended to the decoded message (10 characters, maximum)	Software	none
Trailer Selection	A string of characters appended to the decoded message (10 characters, maximum)	Software	C_R L_F
Reader Address Selection	Reader Address is transmitted at the beginning of decoded and No-Read messages for polling purposes. (1 character)	Software	none
Message Ready/Not Ready Response Selection	The Message Ready/Not Ready response is transmitted after the reader receives a status request type 3 and is used with Single Read Mode 2. (1 character each)	Software	ACK/NAK
No-Read Message Selection	The No-Read Message configured is transmitted each time there is an unsuccessful read (10 characters, maximum)	Software	none
No-Read Recognition Enable	Controls whether the decoder detects unsuccessful reads and sends the No-Read Message	Software	Disabled
Single Read Mode 1 Enable	Controls reading and automatic transmission of decoded messages	Software	Disabled
Single Read Mode 2 Enable	Controls separate reading of bar codes and triggering decoded message transmission	Software	Disabled
Output Buffering Enable	Characters to be transmitted are entered into a 256 character queue for use with a pacing protocol	Software	Disabled
Scanner Type Selection	Determines whether a wand or laser is to be used	Hardwire	Depends on pin SCT
Laser Shutoff Delay Selection	Defines laser on time prior to automatic shutoff, from 0 to 10 seconds in 100 ms steps	Software	3 seconds
Laser Redundancy Check Enable	Enables requirement for two consecutive, identical decodes for a good read	Software	Disabled
Continuous Laser Read Mode Enable	When enabled, the laser is turned on permanently instead of waiting for the trigger to be pulled	Software	Disabled

(continued)

Feature	Function or Value	Selection	Default Setting
Laser Connection Detection Enable	When enabled, the scanner type pin is ignored at powerup. Instead, the decoder tests for a laser scanner to determine scanner type	Software	Disabled
Laser Trigger Latch Mode Enable	When enabled, the laser scanner continues to scan after the trigger has been released until either the laser shutoff delay period elapses or a read occurs	Software	Disabled
Laser Idling Enable	When enabled, the processor idles while waiting for the trigger to be pulled, reducing current draw	Software	Disabled
Code ID Character Selection	Code ID character serves to identify the symbology of the decoded message	Software	Code 39 = a Int 2/5 = b UPC/EAN = c Codabar = d Code 128 = e Code 11 = f MSI Code = g
Code ID Character Transmission Enable	Code ID character can be added to the beginning of each decoded message	Software	Disabled
Bar Code Menu Scan Response Enable	Verification of individual configuration menu scans via transmission of response message	Software	Disabled
Hard Reset Message Enable	"Ready 12.4" C_R L_F will be transmitted to host upon hard reset	Software	Disabled
ROM, RAM Self Test Enable	When enabled, ROM and RAM are tested after a Hard Reset	Software	Enabled
Good Read Beep Tone Selection	Selects Good Read Beep tones (1 to 16)	Software	Tone 12
LED Control Selection	Controls the LED function: Automatic Flash Mode Automatic Feedback Mode		 Enabled Disabled
LED Active Level Selection	Defines logic level of LED ON state	Software	Active High
LED, Beeper Feedback Suppression Enable	Suppresses LED and Beeper operation for systems without those annunciators	Software	Not Suppressed
Wand Input Buffering Enable	Data from wand scans is collected continuously in an input buffer to increase throughput	Software	Disabled
Quiescent State of Address Line Selection	The quiescent state of the processor memory bus address lines A8, A9, A10 can be defined for additional I/O interfacing	Software	High

Table 3. Summary of Commands - HBCR-2210 Series

Features	Description
Scanner Enable	When enabled, scans with the wand or laser are decoded; otherwise, they are ignored
Hard Reset	Resets decoder IC as though it were just powered up
Soft Reset	Clears pacing conditions, errors
LED Control Selection	Controls the LED On/Off function
Status Requests	Cause the decoder to generate a status message • General status message showing symbology of last message read, error conditions, etc. • Message Ready/Not Ready response (for Single Read Mode 2)
Sound Tone	This command causes the reader to sound a tone at the selected pitch for approximately 100 milliseconds
Configuration Control	There are three operations that manipulate the decoder configuration as a block. • Set default configuration • Save configuration in non-volatile memory • Recall non-volatile configuration
Execute Pending Command	For use with laser scanning, this command causes immediate execution of previous commands that would otherwise be postponed until the laser scan finishes

Table 4. Summary of Other Features - HBCR-2210 Series

Power Idle Mode	Reduces current draw of processor from approximately 20 mA to 4 mA in wand mode when the wand is inactive
Laser Failure Timeout	Turns off the laser if the Scan Sync signal is missing after approximately 1 second, and sets the laser failure status bit
Self Test Failure Message	An appropriate message is transmitted at power up if the decoder Self Test fails. • ROM SELF TEST FAILED • EEPROM SELF TEST FAILED • RAM SELF TEST FAILED
EEPROM Fault Recognition	An appropriate message is transmitted at power up if the EEPROM checksum is incorrect. • EEPROM FAULT

Parallel Mode Handshake Timing

Handshake and Data Lines

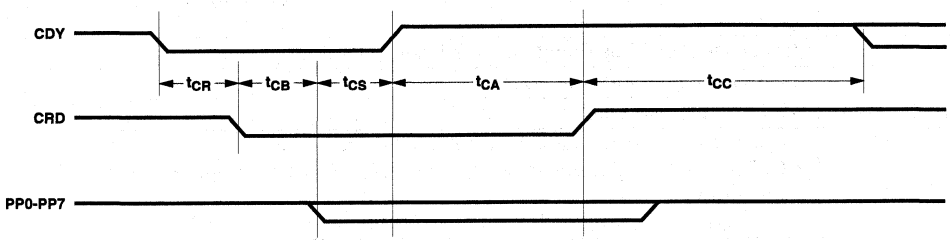


Figure 1. Host Commands Received by Decode IC (Reader).

Handshake Timing

t_{CR} = Falling edge of command ready to falling edge of command read. Max. = 30 µs for the first byte of transmission from host.
t_{CB} = Falling edge of command read to command valid. Min. = 0 µs
t_{CS} = Command valid set up to rising edge of command ready. Min. = 0 µs
t_{CA} = Rising edge of command ready to rising edge of command read. Max. = 8 µs
t_{CC} = Rising edge of command read to falling edge of command ready. Min. = 0 µs

Handshake and Data Lines

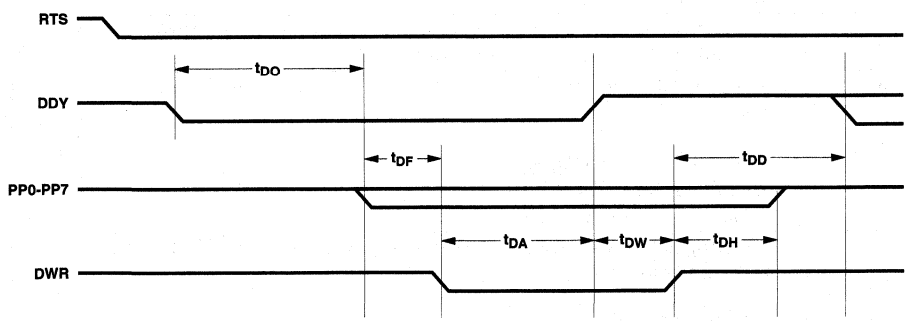


Figure 2. Decoder IC Data Sent to Host.

Handshake Timing

t_{DO} = Falling edge of data ready to data output to bus. Min. = 6 µs Typical Max. = 74 µs
Note: The maximum can be infinite if there is no data to be transmitted. RTS can be used to determine when there is data. If the scanner is active or escape sequence commands are being processed, (t_{DO} = t_{DF}) can extend by an indefinite amount.
t_{DF} = Data output to bus to falling edge of data write. Max. = 6 µs
t_{DA} = Falling edge of data write to rising edge of data ready. Min. = 0 µs
t_{DW} = Rising edge of data ready to rising edge of data write. Max. = 8 µs
t_{DH} = Data hold after rising edge of data write. Max. = 4 µs
t_{DD} = Rising edge of data write to falling edge of data ready. Min. = 0 µs

PLCC Drying

Whenever Vapor Phase or Infrared Reflow Technologies are used to mount the PLCC packages, there is a possibility that previously absorbed moisture, heated very rapidly to the reflow temperatures, may cause the package to crack from the internal stresses. There is a reliability concern that moisture may then enter the package over a period of time, and metal corrosion may take place, degrading the IC performance.

To reduce the amount of absorbed moisture and prevent cracking, all of the PLCC ICs should undergo one of the following baking cycles. The parts must then be mounted within 48 hours.

If the parts are not mounted within 48 hours, they must be re-baked.

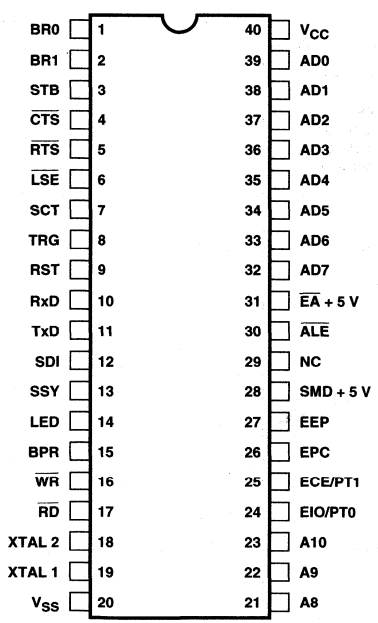
The total number of baking cycles must not exceed two. If the ICs are baked more than twice, Hewlett-Packard cannot guarantee the performance and reliability of the parts.

Neither bake cycle can be performed in the standard shipping tubes. The ICs must be baked in an ESD safe, mechanically stable container, such as an aluminum tube or pan.

Cycle	Temperature	Time	Notes
A	125°C	24 hrs	
B	60°C	96 hrs	8

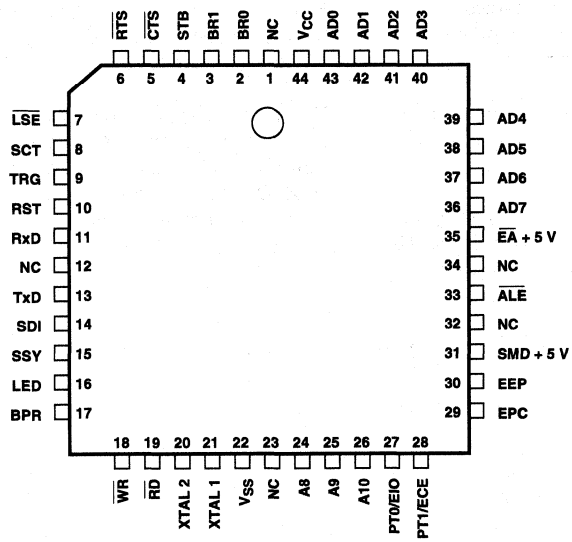
Note:
8. Cycle B must be done in atmosphere of <5% relative humidity air or nitrogen.

Pin Definitions



PIN MNEMONICS	
AD0-AD7	ADDRESS/DATA BUS
RxD	RECEIVED DATA
TxD	TRANSMITTED DATA
BR0-BR1	BAUD RATE
PT0-PT1	PARITY
STB	STOP BITS
LSE	LASER SCAN ENABLE
SCT	SCANNER TYPE
SDI	SCANNER DIGITAL INPUT
LED	LED CONTROL LINE
BPR	BEEPER CONTROL LINE
WR	DATA MEMORY WRITE
RD	DATA MEMORY READ
XTAL1	CRYSTAL INPUT
XTAL2	CRYSTAL INPUT
SMD	SERIAL MODE SELECT
RTS	REQUEST TO SEND
CTS	CLEAR TO SEND
RST	IC RESET
EEP	EEPROM SELECT
EPC	EEPROM CLOCK
ECE	EEPROM CHIP ENABLE
EIO	EEPROM I/O
TRG	LASER TRIGGER LINE
SSY	SCANNER SYNCHRONIZATION
A8	ADDRESS LINE #8
A9	ADDRESS LINE #9
A10	ADDRESS LINE #10
EA	EXTERNAL PROGRAM ENABLE
ALE	ADDRESS LATCH ENABLE
VCC	POWER
VSS	GROUND

Figure 3. HBCR-2210 Serial Pinout.



PIN MNEMONICS	
AD0-AD7	ADDRESS/DATA BUS
RxD	RECEIVED DATA
TxD	TRANSMITTED DATA
BR0-BR1	BAUD RATE
PT0-PT1	PARITY
STB	STOP BITS
LSE	LASER SCAN ENABLE
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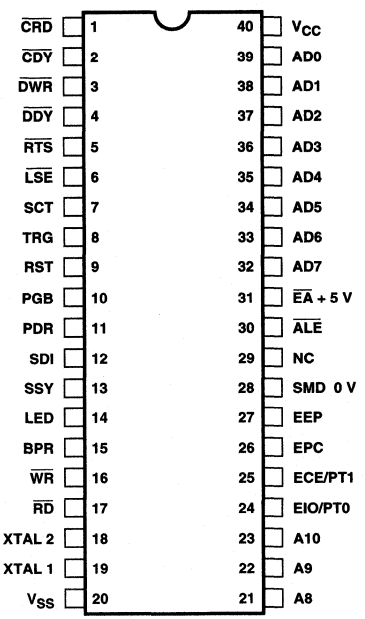
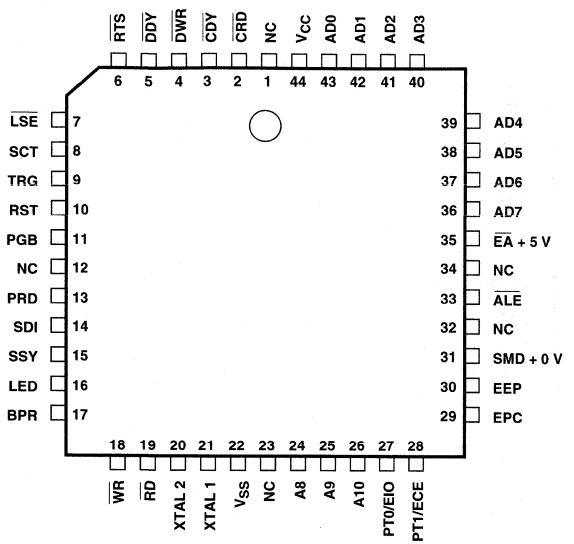
RST	IC RESET
EEP	EEPROM SELECT
EPC	EEPROM CLOCK
ECE	EEPROM CHIP ENABLE
EIO	EEPROM I/O
TRG	LASER TRIGGER LINE
SSY	SCANNER SYNCHRONIZATION
A8	ADDRESS LINE #8
A9	ADDRESS LINE #9
A10	ADDRESS LINE #10
EA	EXTERNAL PROGRAM ENABLE
ALE	ADDRESS LATCH ENABLE
VCC	POWER
VSS	GROUND

Figure 4. HBCR-2211 Serial Pinout.



PIN MNEMONICS	
AD0-AD7	ADDRESS/DATA BUS
DWR	DATA WRITE HANDSHAKE
DDY	READY FOR DATA HANDSHAKE
CRD	COMMAND READ HANDSHAKE
CDY	COMMAND READY HANDSHAKE
PT0-PT1	PARITY
LSE	LASER SCAN ENABLE
SCT	SCANNER TYPE
SDI	SCANNER DIGITAL INPUT
LED	LED CONTROL LINE
BPR	BEEPER CONTROL LINE
WR	DATA MEMORY WRITE
RD	DATA MEMORY READ
XTAL1	CRYSTAL INPUT
XTAL2	CRYSTAL INPUT
SMD	SERIAL MODE SELECT
PGB	TRANSCEIVER DRIVE ENABLE
PDR	TRANSCEIVER DIRECTION CONTROL
RST	IC RESET
EEP	EEPROM SELECT
EPC	EEPROM CLOCK
ECE	EEPROM CHIP ENABLE
EIO	EEPROM I/O
TRG	LASER TRIGGER LINE
SSY	SCANNER SYNCHRONIZATION
A8	ADDRESS LINE #8
A9	ADDRESS LINE #9
A10	ADDRESS LINE #10
EA	EXTERNAL PROGRAM ENABLE
ALE	ADDRESS LATCH ENABLE
RTS	REQUEST TO SEND
VCC	POWER
VSS	GROUND

Figure 5. HBCR-2210 Parallel Pinout.



PIN MNEMONICS	
AD0-AD7	ADDRESS/DATA BUS
$\overline{DWR}$	DATA WRITE HANDSHAKE
$\overline{DDY}$	READY FOR DATA HANDSHAKE
$\overline{CRD}$	COMMAND READ HANDSHAKE
$\overline{CDY}$	COMMAND READY HANDSHAKE
PT0-PT1	PARITY
$\overline{LSE}$	LASER SCAN ENABLE
SCT	SCANNER TYPE
SDI	SCANNER DIGITAL INPUT
LED	LED CONTROL LINE
BPR	BEEPER CONTROL LINE
$\overline{WR}$	DATA MEMORY WRITE
$\overline{RD}$	DATA MEMORY READ
XTAL1	CRYSTAL INPUT
XTAL2	CRYSTAL INPUT
SMD	SERIAL MODE SELECT
PGB	TRANSCEIVER DRIVE ENABLE
PDR	TRANSCEIVER DIRECTION CONTROL
RST	IC RESET
EEP	EEPROM SELECT
EPC	EEPROM CLOCK
ECE	EEPROM CHIP ENABLE
EIO	EEPROM I/O
TRG	LASER TRIGGER LINE
SSY	SCANNER SYNCHRONIZATION
A8	ADDRESS LINE #8
A9	ADDRESS LINE #9
A10	ADDRESS LINE #10
$\overline{EA}$	EXTERNAL PROGRAM ENABLE
$\overline{ALE}$	ADDRESS LATCH ENABLE
$\overline{RTS}$	REQUEST TO SEND
V_{CC}	POWER
V_{SS}	GROUND

Figure 6. HBCR-2211 Parallel Pinout.

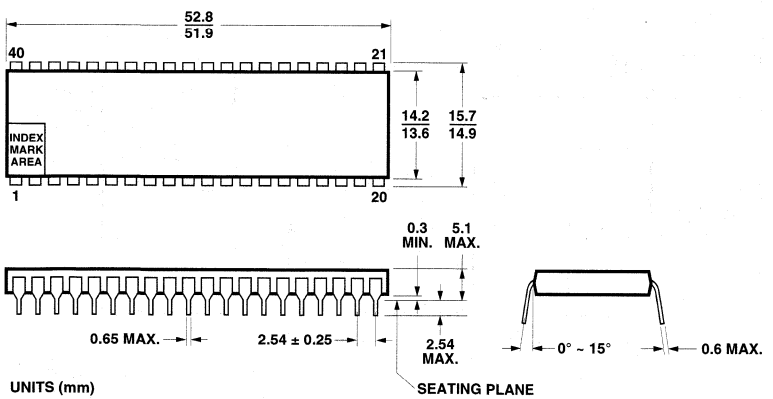


Figure 7. HBCR-2210 Mechanical Specifications.

BAR CODE

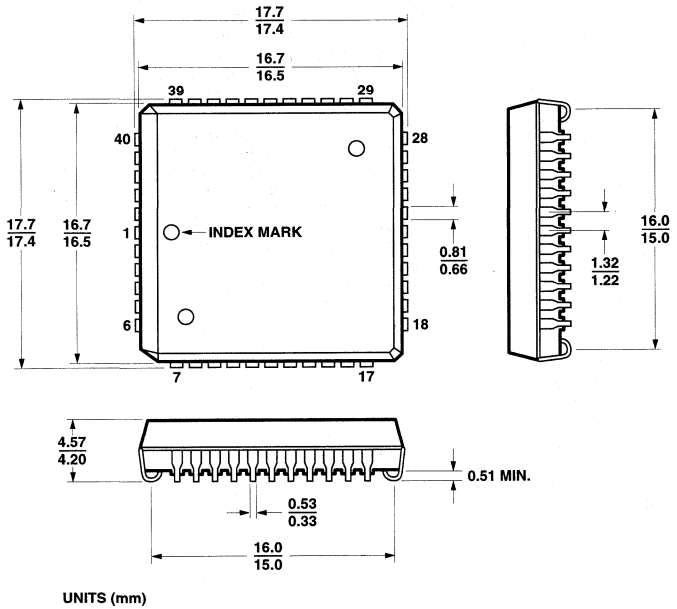


Figure 8. HBCR-2211 Mechanical Specifications.

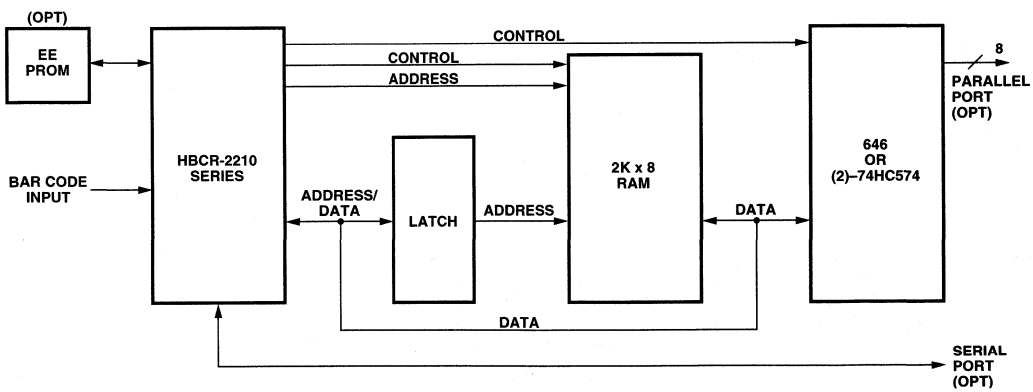


Figure 9. System Block Diagram.

Warranty and Service

The HP Bar Code Decode IC is warranted for a period of one year after purchase covering defects in material and workmanship. Hewlett-Packard will repair or, at its option, replace products that prove to be defective in material or workmanship under proper use during the warranty period.

NO OTHER WARRANTIES ARE EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. HEWLETT-PACKARD IS NOT LIABLE FOR CONSEQUENTIAL DAMAGES.

For additional warranty or service information please contact your local Hewlett-Packard sales representative or authorized distributor.

HEWLETT® PACKARD

Hewlett-Packard KeyWand Bar Code Reader

Technical Data

HBKW-1000 Series

Features

- **Works with IBM Compatible Computers**
- **Automatically Recognizes Mode and Code Set for Most PC Models**
- **Operates with or without a Keyboard Attached**
- **Powered from the PC**
- **Low Current Draw**
- **Automatically Discriminates 9 Bar Code Symbologies**
- **International Language Support**
- **Visual/Audible Feedback**
- **Programmable via Bar Code Menus**
- **Message Editing**
- **Rugged Polycarbonate Case**
- **Sapphire Tip**
- **15 KV ESD Case Isolation**
- **25 KV ESD Immunity**
- **Manufacturing - ISO 9002 Certified**
- **One Year Warranty**

Description

The Hewlett-Packard Programmable KeyWand Reader is an intelligent peripheral designed to easily add bar code reading capability to personal computers via the keyboard port. Power is provided by the PC, and the KeyWand Reader can operate with or without the keyboard attached. The KeyWand Reader is transparent to the application since data appears as keyboard input. Installing a KeyWand Reader does not require hardware or software modifications. The KeyWand Reader is also compatible with 17 keyboard languages.

All scanning, decoding, and I/O electronics are self-contained within the compact KeyWand Reader. The HBKW-1000 Series acknowledges a good scan with a flashing LED and/or by accessing the PC's internal beeper.

The KeyWand Reader automatically discriminates 9 standard bar code symbologies. A Message Editing feature allows the scanned data to be edited or reformatted prior to transmitting to the host. Bar code type identification, label length checking, and a check character verification are options that, when enabled, ensure a high level of data integrity.

Configuration parameters are stored in non-volatile memory so the KeyWand Reader retains the configuration when power is turned off. The KeyWand Reader autodiscriminates the PC type to which it is connected and whether or not Caps Lock is enabled.

IBM Compatible Computers

HP Vectra
IBM PC and Compatibles

Bar Code Symbologies

Code 39 Standard or Extended

Int. 2 of 5	Code 128
UPC A, E	EAN 8, 13
Codabar	Code 11
MSI Code	Code 93

International Language Support

The HP KeyWand Reader is menu programmable for 17 languages.

US English	Finnish
UK English	French Canadian
French	Latin American
German	Norwegian
Italian	Portuguese
Spanish	Swedish
Dutch	Swiss French
Belgian	Swiss German
(Flemish)	Danish

Visual/Audible Feedback

The HP KeyWand Reader employs the most flexible, programmable acknowledgment of a good scan to the user. The Visual Feedback LED is positioned close to the tip of the wand which makes it easy for the user to see. This is useful in noisy environments or where silence is required. For situations that require an audible acknowledgment, a TSR program stored and uploaded from the KeyWand Reader allows the user to program the pitch and duration of the PC beeper tone.

Programming via Bar Code Menus

The KeyWand Reader can be configured by scanning special bar code labels. This allows decoding, message editing, keyboard language, and other options to be tailored to a specific application. The reader can display its current configuration on the computer screen. See sample (below).

Applications

- **Manufacturing**
  Work-in-Process
  Inventory Control
  Shipping and Receiving
  Warehousing and Distribution
- **Retail POS**
- **Library Circulation**
- **Office Automation**
  Document Tracking
- **Health Industry**
  Medication Dispensation
  Blood banks
- **Transportation**
  Waybill Tracking

Configuration Display

```
                        CONFIGURATION DISPLAY
--- Version 14.3 ------------------------- (c) Hewlett-Packard 1986-1992
  CODE   |READ |CHECK CHAR | LENGTH | CODE ID  |  OTHER CONFIG. SETTINGS
         |     |verif_xmit_|min__max|xmit:[off]|-------------------------
Code 39  |[yes]|[no]  | yes |[1] [32]|   [a]    |Extended: [no]
Int. 2/5 |[yes]|[no]  | yes |[4] [32]|   [b]    |Length: [variable]
Codabar  |[yes]|[no]  | no  |[1] [32]|   [d]    |Include start/stop: [yes]
Code 128 |[yes]| yes  | no  |[1] [32]|   [e]    |
Code 11  |[yes]| [1]  | yes |[2] [32]|   [f]    |
MSI Code |[yes]| yes  | yes |[3] [32]|   [g]    |
Code 93  |[yes]| yes  | no  |[1] [32]|   [h]    |
UPC/EAN  |[yes]| yes  | yes | fixed  |   [c]    |[+ none]
 E:[0]   |     |      |     |        |          |EAN:[yes]   ID chars:[off]
----- MESSAGE COMPONENTS ---------------------------------------------------
     Ctrl character = ^ + letter       <<nn>> = Extended Key Index
Header:[<<61>>]
Trailer:[^M]
No-read:[<<61>><<61>>]
--- KEYCODES ----------OPERATOR FEEDBACK---------- MISCELLANEOUS -------
Key Delay:[1] ms  |Ready Signal:[on]          |[Wedge] (using keyboard)
[U.S. English]    |Menu Scan Responses:[on]   |No-read recognition:[off]
Code Set:[auto]->2|Good Read LED:[flashes]    |Family:[auto]->PC/AT,PS/2
ALT Sequence:[off]|                           |Cntl Chars:[ASCII]
-------------------------------------------------------------------------
```

All items within the square brackets [ ] are configurable.

Specifications

Scan Speed ..... 7.6 - 127 cm/s (3 to 50 in/s)
Tilt Angle ..... 5 to 40°
Minimum Contrast 45%
Light Wavelength:
HBKW-10XX 655 nm
HBKW-12XX 655 nm
HBKW-14XX 820 nm
Resolution:
HBKW-10XX 0.33 mm (0.013 in)
HBKW-12XX 0.19 mm (0.0075 in)
HBKW-14XX 0.13 mm (0.005 in)
Wand Diameter... 23 mm (0.9 in)
Wand length..... 160 mm (6.3 in)
Weight ..... 165 g (5.9 oz)
Color ..... Gray
Case ..... Polycarbonate
Tip ..... Sapphire

Environmental

Temperature:
Operating:
-20°C to +70°C (-4°F to +158°F)
Storage:
-40°C to +70°C (-40°F to +158°F)
Humidity (Non-condensing):
95% at +40°C (+104°F) max (non-condensing)
Ambient Light:
100 K lux (max)
Rain:
MIL-STD-810, Method 506, Procedure II
Dust:
MIL-STD-810, Method 510
Shock:
Ten drops to sealed concrete (random orientation) from 1.2 m (4 ft)

Typical Current Draw

Idle ..... 10 mA
Operating ..... 20 mA
LED Enable ..... +11 mA

FCC Certification

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Model	FCC Identification
HBKW-1000 Series	FCC ID: B94KDRZ

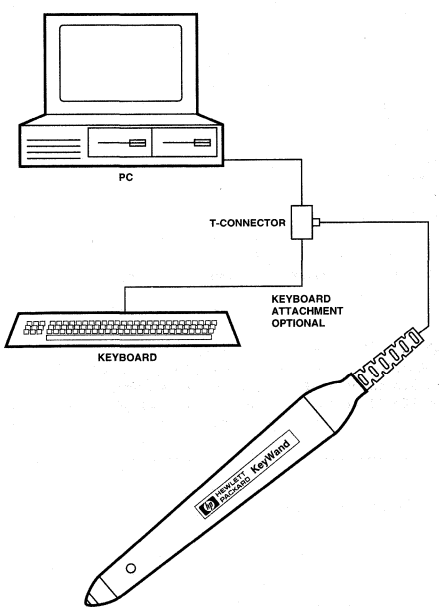


Figure 1. Systems Configuration.

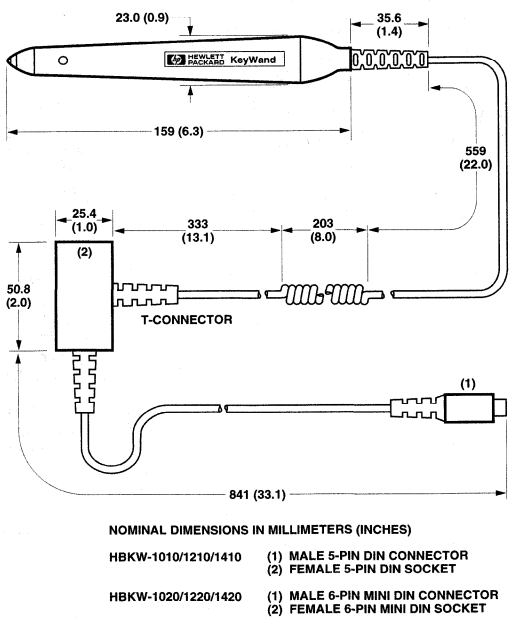


Figure 2. Wand Configuration.

Ordering Information

	Low Resolution 0.33 mm (0.013 in)	Medium Resolution 0.19 mm (0.0075 in)	High Resolution 0.13 mm(0.005 in)
LED Wavelength	655 nm (Visible Red)	655 nm (Visible Red)	820 nm (Infra Red)
5 PIN DIN Connector	HBKW-1010*	HBKW-1210	HBKW-1410*
6 PIN Mini-DIN Connector	HBKW-1020*	HBKW-1220	HBKW-1420*

*Low and High Resolution KeyWand Readers are built to order devices.

Universal KeyWand Kit

HBKW-1240 Will work with either 5-pin DIN or 6-pin Mini-DIN keyboard interfaces.
Kit includes: HBKW-1220 KeyWand Reader
HBKW-1910 Installation and Operation Guide
HBKW-1920 Wand Holder
HBKW-1925 Interface Adapters and Quick Start Instructions.

KeyWand Accessory Part Numbers

HBKW-1910 Installation and Operation Guide
HBKW-1920 Wand Holder
HBKW-1925 Interface Adapters (2) (5 pin DIN to 6 pin Mini-DIN)
HBKW-1991 Replacement Tip/Case
HBCS-A990 Case Replacement Tool

Warranty and Service

The Hewlett-Packard KeyWand Bar Code Reader is warranted for a period of one year from date of purchase covering defects in material and workmanship. Hewlett-Packard will repair or, at its option, replace products that prove to be defective in material or workmanship under proper use during the warranty period.

HEWLETT-PACKARD MAKES NO WARRANTY OF ANY KIND WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

Note: The shell of the connector must be tied to ground for proper operation of the HP KeyWand Reader.

The CE Mark demonstrates compliance with EC directives on EMC.

HEWLETT® PACKARD

Hewlett-Packard SmartWand Bar Code Reader

Technical Data

HBSW-8000 Series Polycarbonate or Metal Housing

Features

- **Automatically Decodes 9 Bar Code Symbologies**
  - Code 39 – Standard or Extended
  - Int. 2 of 5
  - UPC A, E
  - Codabar
  - MSI Code
  - Code 128
  - EAN 8, 13
  - Code 11
  - Code 93
- **LED Feedback**
- **Low Current Draw**
- **Programmable Either by Bar Code Labels or by Escape Sequences**
- **Configuration Stored in Non-Volatile Memory**
- **CMOS/TTL Interface**
  - Output 0 to 5 volts
  - Input up to ± 15 volts
- **Manufacturing - ISO 9002 Certified**
- **Full One Year Warranty**

Description

The Hewlett-Packard SmartWand Bar Code Reader is a bar code scanning wand with an integrated decoder. It transmits data to a computer via an asynchronous serial port, using CMOS level signals, at user definable baud rates. The SmartWand Reader's configuration may be changed by scanning special bar code menus, or by sending escape sequences to the wand from the host. The configuration is stored in non-volatile memory, allowing the SmartWand Reader to retain the configuration when the power is turned off. A Configuration Display option sends a summary of the configured options to the screen.

In its default configuration, the SmartWand Reader can automatically recognize and decode 9 standard bar code symbologies. Configurable options include: symbology selection, checksum verification, length checking, message editing, LED feedback control, Code 39 digital wand emulation mode, serial port configuration, and various I/O protocols such as single read modes, Xon/Xoff pacing and no-read recognition.

The polycarbonate-cased SmartWand Readers (HBSW-8000,8200,8400) have an LED near the tip that flashes after a good read. The LED also flashes during bar code menu programming and to signal any self-test failures after power-up.

All SmartWand Readers have an enhanced software version of Hewlett-Packard's proven

decoding algorithm. The SmartWands are also very suitable for portable computer or terminal applications due to its low current draw.

Visual Feedback LED

The SmartWand Readers with polycarbonate-cases have an easy-to-see Feedback LED near the scanner tip that acknowledges a good read. This is useful in a noisy environment or where silence is required. Since the state of the LED can be controlled by escape sequences, the host processor can turn the LED on or off at any time.

SmartWand Reader Configuration

The SmartWand Reader can be configured by scanning special bar code labels or by receiving escape sequence commands from the host. This allows decoding options and interface protocols to be tailored to a specific application. Configuration labels and a list of escape sequences are printed in the SmartWand User's Manual (P/N: HBSW-8997). The SmartWand Reader can display its current configuration on the host's screen. See sample.

Programmable Features

Bar code selection and decoding options
Check character verification and transmission
Serial port parameters and I/O protocols
Message editing
Header and terminators
LED operator feedback
Label length checking
No Read recognition
Digital wand Code 39 emulation

Wand Specifications

Scan Speed ..... 7.6 to 127 cm/s (3 to 50 in/s)
Tilt Angle ..... 5° to 40°
Minimum Contrast 45%
Color ..... Black
Wand Diameter ... 23 mm (0.9 in)
Wand Length .... 160 mm (6.3 in)
Weight:
Aluminum ..... 153 g (5.4 oz)
Polycarbonate ... 140 g (4.9 oz)
Tip ..... Sapphire

Environmental

Temperature:
Operating:
-20°C to 70°C (-4°F to 158°F)
Storage:
-40°C to 70°C (-40°F to 158°F)

Humidity (Non-condensing):
95% at 40°C (104°F) max.

Ambient Light:
100,000 lux (maximum)

Rain:
MIL-STD-810, Method 506, Procedure II (Polycarbonate)

Dust:
MIL-STD-810, Method 510

Shock:
Ten drops to sealed concrete (random orientation) from 1.2 m (4 ft)

Configuration Display

```
                    CONFIGURATION DISPLAY
 --- Version 12.5 ------------------------- (c) Hewlett-Packard 1986-1992
|  CODE   |READ |CHECK CHAR | LENGTH | CODE ID  |  OTHER CONFIG. SETTINGS  |
|         |     |verif_xmit_|min__max|xmit:[off]|--------------------------|
|Code 39  |[yes]|[no]  | yes |[1] [32]|   [a]    |Extended: [no]            |
|Int. 2/5 |[yes]|[no]  | yes |[4] [32]|   [b]    |Length: [variable]        |
|Codabar  |[yes]|[no]  | no  |[1] [32]|   [d]    |Include start/stop: [yes] |
|Code 128 |[yes]| yes  | no  |[1] [32]|   [e]    |                          |
|Code 11  |[yes]| [1]  | yes |[2] [32]|   [f]    |                          |
|MSI Code |[yes]| yes  | yes |[3] [32]|   [g]    |                          |
|Code 93  |[yes]| yes  | no  |[1] [32]|   [h]    |                          |
|UPC/EAN  |[yes]| yes  | yes |  fixed |   [c]    |[+ none]                  |
| E:[0]   |     |      |     |        |          |EAN:[yes]   ID chars:[off]|
|--- MESSAGE COMPONENTS (control character = ^ + letter) -----------------|
|Header:[]                              |No-read:[]                        |
|Trailer:[^M^J]                         |Message Ready:[^F]                |
|Reader Address:[]                      |Message Not Ready:[^U]            |
|-- SERIAL PORT --------- PACING ------------------ MISCELLANEOUS -------|
|Baud Rate:[9600]  |XON/XOFF Protocol:[off]    |No-Read Recognition:[off]  |
|Parity:[0's]      |Single Read Mode:[off]     |Scanner:[enabled]          |
|Stop Bits:[1]     |----- FEEDBACK: [on] ------|Buffering:[None]           |
|[20ms]Delay:[off] |LED:[flashes] Active:[high]|ROM/RAM Self Test:[off]    |
 ------------------------------------------------------------------------
```

All items within the square brackets [ ] are configurable.

Electrical Interface

V_{CC} Limits (V)	Min.	Max.
Operating	4.5	6.0
Absolute Rating	-0.3	6.0
Supply Ripple	100 mV peak to peak	

Typical Current Draw - I_{CC} (mA)

Mode	V_{CC}		
	4.5	5.0	6.0
Idle	8	9	12
Scanning	16	18	24
With LED on	25	29	38

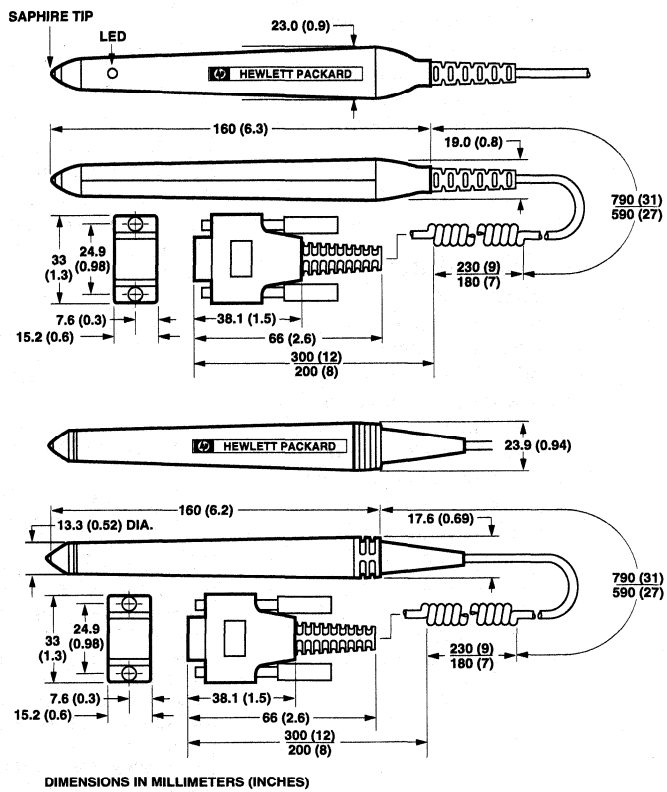
FCC Certification

HP's SmartWand Readers have received FCC certification for their standard configuration only. Any customer purchasing the product with stripped and tinned leads or a connector without adequate shielding has the responsibility to comply with FCC regulations. Moreover, if the HP SmartWand Reader is purchased without a connector, the product becomes defined as a sub-assembly and the FCC Identification number no longer applies. HP assumes no responsibility or liability for users of the HP SmartWand Readers without connectors that fail to comply with FCC regulations.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Model	FCC Identification
HBSW-8XXX Series	FCC ID: B94KDRZ

General Mechanical Specifications



DIMENSIONS IN MILLIMETERS (INCHES)

The CE Mark demonstrates compliance with EC directives on EMC.

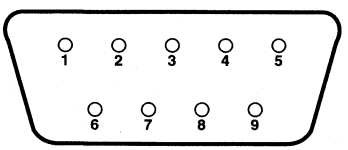
Connector

The standard connector is a 9 pin male D connector. There is also an option for the cable to have stripped and tinned wires.

Pin Diagram

Pin #	Wire Color	Function
1	-	N/C
2	White	TxD Transmitted Data (from the Reader)
3	Green	RxD Received Data (to the Reader)
4, 5, 6	-	N/C
7	Black	Ground
8	-	N/C
9	Red	V_{CC}
Shell	Braid	Shield

Shield and ground are tied together in the connector.



MALE 9 PIN SUBMINIATURE D CONNECTOR

Pin Description

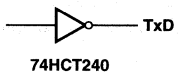
Pin 2 TxD - The data output signal TxD obeys standard serial asynchronous data formats, but uses zero to five volts CMOS logic levels. It can be described as CMOS level RS-232. The TxD output circuit is shown in the figure below. It will drive TTL, LSTTL, CMOS, HC, and HCT inputs.

TxD Output Specifications

(V_{CC} = 4.5 V, T_A = 25°C)

	Min.	Max.
V_{OH}	4.4 V @ 20 µA 3.8 V @ 6 mA	
V_{OL}		0.10 V @ -20 µA 0.33 V @ -6 mA
I_{OL}		35 mA

TxD Circuit



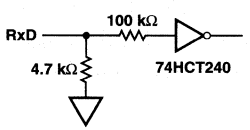
Pin 3 RxD - The received data signal RxD expects the standard asynchronous serial data format. It will accept either CMOS level or true RS-232 level signals. The figure below shows the equivalent input circuit.

RxD Input Specifications

(V_{CC} = 5.0 V, T_A = 25°C)

V_{IH}	2.0 V 500 µA
V_{IL}	0.8 V @ 1 µA

RxD Circuit



Note: If the part is purchased with stripped and tinned wires, or if the connector is removed, the ground and shield wires must be connected together for proper operation.

Ordering Information

Part Number	Housing	Resolution	LED Wavelength
HBSW-8000*	Polycarbonate	Low –	655 nm
HBSW-8100*	Metal	0.33 mm (0.013 in)	
HBSW-8200	Polycarbonate	Medium –	655 nm
HBSW-8300	Metal	0.19 mm (0.0075 in)	
HBSW-8400*	Polycarbonate	High –	820 nm
HBSW-8500*	Metal	0.13 mm (0.005 in)	

* Low and High Resolution SmartWand Readers are built to order devices.

SmartWand Kits

HBSW-8205 - Polycarbonate SmartWand Kit
Includes: HBSW-8200 General Purpose Reader
HBSW-8997 User's Manual
HBCS-2998 Black Wand Holder

HBSW-8305 - Metal SmartWand Kit
Includes: HBSW-8300 General Purpose Reader
HBSW-8997 User's Manual
HBCS-2998 Black Wand Holder

SmartWand Accessory Part Numbers

HBSW-8997 User's Manual
HBCS-2998 Wand Holder (black polycarbonate)
HBSW-8991 Replacement Polycarbonate Case with LED Window and Tip
HBCS-4999 Replacement Tip for Metal Case
HBCS-A990 Plastic Case Replacement Tool

Warranty and Service

The Hewlett-Packard SmartWand Bar Code Reader is warranted for a period of one year from date of purchase covering defects in material and workmanship. Hewlett-Packard will repair or, at its option, replace products that prove to be defective in material or workmanship under proper use during the warranty period.

HEWLETT-PACKARD MAKES NO WARRANTY OF ANY KIND WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

HEWLETT® PACKARD

Low Current Digital Bar Code Wand

Technical Data

HBCS-A000 Series

Features

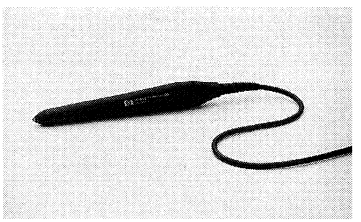
- **Rugged Polycarbonate Case, Switched or Unswitched**
- **Ultra Low Continuous Current Draw**
- **Available in 3 Resolutions to Meet a Variety of Scanning Needs**
- **High Ambient Light Rejection–Operates in Direct Sunlight**
- **Visible Red (655 nm) and Infrared (820 nm) Versions Available**
- **Scan Angle: 0° to 45° Typical**
- **Manufacturing: ISO 9002 Certified**

Description

The HBCS-A000 series low current digital wands are hand held scanners optimized to provide excellent scanning of all common bar code formats. The patented low current, high ambient light rejection circuitry is packaged in a rugged polycarbonate case.

Available in three resolutions, these wands are capable of reading a wide range of bar code printing. Visible red and infrared versions are available for reading a wide range of print types and colors.

The wands are available with or without a switch to control the wand operation.



Applications

The HBCS-A000 series wands are highly effective alternatives to keyboard data entry. These devices are especially designed for battery powered applications where low power drain is a primary concern. In addition to their low current draw, these wands are also designed to work in high ambient light, such as outdoors or near windows.

BAR CODE

Selection Guide

Wand Type	Switched			Unswitched		
Typical Resolution	0.33 mm (0.013 in.)	0.19 mm (0.0075 in.)	0.13 mm (0.005 in.)	0.33 mm (0.013 in.)	0.19 mm (0.0075 in.)	0.13 mm (0.005 in.)
LED Wavelength	655 nm		820 nm	655 nm		820 nm
5-Pin DIN Connector	HBCS-A000*	HBCS-A200	HBCS-A400*	HBCS-A100*	HBCS-A300	HBCS-A500*
9-Pin D-Sub Connector	HBCS-A008*	HBCS-A208*	HBCS-A408*	HBCS-A108*	HBCS-A308*	HBCS-A508*
No connector: Strip and Tin Leads	HBCS-A007*	HBCS-A207*	HBCS-A407*	HBCS-A107*	HBCS-A307*	HBCS-A507*
Individually Boxed Wand	Order Option #A01 with the above referenced part number. The wand is shipped in a "kraft" box, including an HBCS-A000 series data sheet.					

***Note:** Build to order product only. Minimum stock is available for engineering evaluation purchases.

Specifications (T_A = 25°C Typical)

Parameter	Minimum	Maximum	Units	Notes
Scan Velocity	7.6 (3)	127 (50)	cm/sec (in/sec)	
Edge Contrast	45		%	1
Supply Voltage (V_{CC})	4.5	5.5	V	
Supply Ripple		100	mV_{pp}	
Temperature	-20	+65	°C	
Ambient Light		100,000	lux	

Absolute Maximum Ratings

Parameter	Minimum	Maximum	Units
Storage Temperature	-40	+75	°C
Operating Temperature	-20	+65	°C
Supply Voltage	-0.5	+6	V
Output Transistor Power		150	mW
Output Collector Voltage	-0.5	+20	V

Electrical Characteristics (T_A = 25°C)

Parameter	Min.	Typ.	Max.	Units	Conditions	Notes
Supply Current	2.5	3.5	5.0	mA	V_S = 5.0 V	2
High Level Output Current			1.0	A	V_{OH} = 2.4 V	
Low Level Output Voltage			0.4	V	I_{OL} = 16 mA	
Output Rise Time		3.4	20	µs		3
Output Fall Time		1.2	20	µs		3
Switch Bounce		0.5	5.0	ms		4
ESD Immunity		25		kV		5
ESD Isolation Unswitched Wands		15		kV		5
ESD Isolation–Switched Wands		8		kV		5
Wake-Up Time		50	200	ms		6

Notes:

1. Contrast is defined as $R_W - R_B$ where R_W is the reflectance of the white spaces and R_B is the reflectance of the black bars, measured at the emitter wavelength (655 nm or 820 nm). Contrast is related to PCS by PCS = $(R_W - R_B)/R_W$ or $R_W - R_B$ = PCS * R_W.
2. Not including the pull-up resistor current.
3. 10% to 90% transitions.
4. Switch bounce causes a series of sub millisecond pulses to appear on the output.
5. Shield must be properly terminated. The human body is modelled by discharging a 300 pF capacitor through a 500 Ω resistor. No damage to the wand will occur at the specified discharge level. The energy will be passed through the shield to the host device.
6. After this time, the wand is operational.

Electrical Operation

The HBCS-A000 series digital bar code wands consist of a precision optical sensor and an electronic circuit that creates a digital output of the bar code pattern. The open collector transistor requires only a pull-up resistor to provide a TTL compatible output.

A non-reflecting black bar results in a logic high (1) level output, while a reflecting white space will cause a logic low (0) level output. The initial state will be indeterminate. However, if no bar code is scanned, after a short period, (typically less than 1 second), the wand will assume a logic low state.

The wands provide a case, cable and connector shield which must be terminated to logic ground, or preferably, to both logic ground and earth ground. The shield is connected to the metal housing of the 5 pin DIN connector.

Certification

FCC Certification (US Only)

Hewlett-Packard products have received FCC certification for its standard configuration only. Any customer purchasing the product with stripped and tinned leads or a connector without adequate shielding has the responsibility to comply with FCC regulations. Moreover, if the Hewlett-Packard Low Current Bar Code Wands are purchased without a connector, the product becomes defined as a subassembly and the FCC identification number no longer applies. Hewlett-Packard assumes no responsibility or liability for users of the Hewlett Packard Low Current Digital Bar Code Wands without connectors that fail to comply with FCC regulations.

This equipment complies with Part 15, Class B, of the FCC Rules. Operation is subject to the following two conditions:

1) This equipment may not cause harmful interference,
2) This equipment must accept any interference that may cause undesired operation.

Model	FCC Identification
HBCS-A000 through -A099	FCC ID: B948JAHBCS-A000 HEWLETT-PACKARD
HBCS-A100 through -A199	FCC ID: B948JAHBCS-A000 HEWLETT-PACKARD
HBCS-A200 through -A299	FCC ID: B948JAHBCS-A200 HEWLETT-PACKARD
HBCS-A300 through -A399	FCC ID: B948JAHBCS-A300 HEWLETT-PACKARD
HBCS-A400 through -A499	FCC ID: B948JAHBCS-A400 HEWLETT-PACKARD
HBCS-A500 through -A599	FCC ID: B948JAHBCS-A500 HEWLETT-PACKARD

The CE Mark demonstrates compliance with EC directives on EMC.

VCCI Registration: Pending

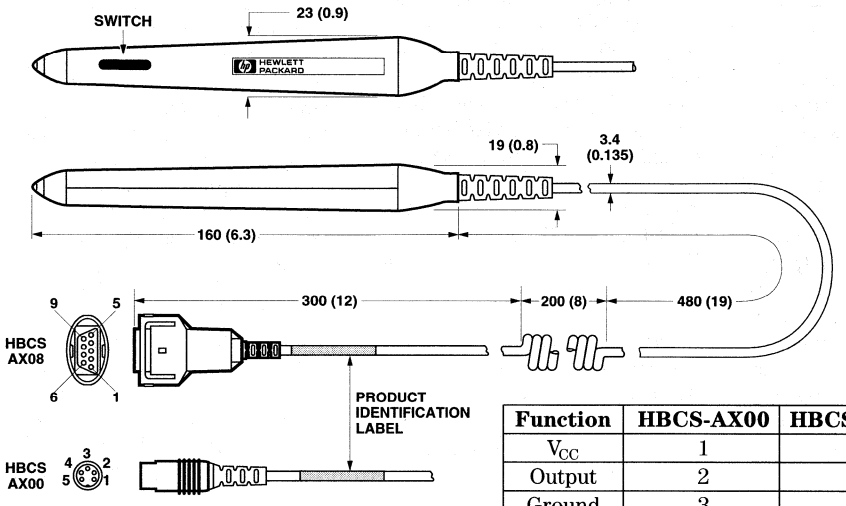
Warranty and Service

Hewlett-Packard Low Current Digital Bar Code Wands are warranted for a period of one year after purchase covering defects in material and workmanship. Hewlett-Packard will repair, or at its option, replace products that prove to be defective in material or workmanship under proper use during the warranty period.

NO OTHER WARRANTIES ARE EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. HEWLETT-PACKARD IS NOT LIABLE FOR CONSEQUENTIAL DAMAGES.

For additional warranty or service information please contact your local Hewlett-Packard sales representative or authorized distributor.

Wand Dimensions and Connector Configurations



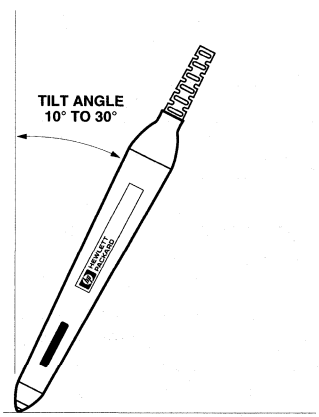
ALL DIMENSIONS IN MILLIMETERS (INCHES)

Function	HBCS-AX00	HBCS-AX08	Wire Color
V_{CC}	1	9	Red
Output	2	2	White
Ground	3	7	Black
Shield	Shell	8	Braid
All other pins are N/C			

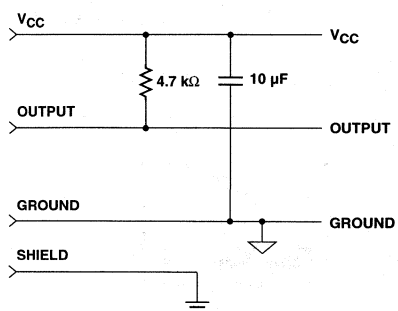
Shield and ground are tied together in the connector.

Note: If the part is purchased with stripped and tinned wires, or if the connector is removed, the ground and shield wires must be connected together for proper operation.

Preferred Orientation



Preferred Electrical Connection



HEWLETT® PACKARD

Industrial Digital Bar Code Slot Reader

Technical Data

HBCS-7100 Series

Features

- **Multi Resolution**
  Compatible with virtually all bar code resolutions
- **Large Slot Width**
  Allows reading thickly laminated cards
- **Sealed Metal Case (IP 66/67)**
  Can be installed outdoors or in wet environments
- **Tamper Proof Design**
  Ideal for security applications
- **Minimal First Bar Distortion**
- **880 nm Light**
- **Wide Operating Temperature Range**
  -40°C to +70°C
- **Wide Scan Speed Range**
- **Black Textured Epoxy Finish**
- **Digital Output**
  Open collector output compatible with TTL and CMOS logic
- **Single +5 Volt Supply**

Description

Hewlett-Packard's Industrial Digital Slot Reader is designed to provide excellent scanning performance on a wide variety of bar coded cards and badges. It contains a unique optical/electrical system that integrates over a large vertical area of the bar/space pattern, providing a greatly improved first read rate even on poorly printed bar codes.

The HBCS-7100 Series uses an infrared (880 nm) light with 0.19 mm (0.0075 in.) resolution.

The extra large depth of field allows the slot reader to have a slot width of 3.2 mm (0.125 in.), thus making it possible to read even thickly laminated cards and badges. When used as a stand alone optics module, the maximum depth of field is dependent upon resolution.

The optics and electronics are housed in a rugged metal case. The case is fully gasketed and sealed, making it suitable for use in outdoor or wet environments. The black epoxy coating adds a durable, finished look to the Digital Slot Reader. When installed using the rear screw holes, the units become tamper proof, making an excellent choice for security access control.

The optical system is centered in the slot track, allowing the user to easily scan from either direction. The wide slot width makes it easy to insert and slide the cards. The optical system is covered with a recessed window to prevent contamination and reduce the wear on the cards.

The standard slot reader comes with the optics module mounted on a base plate with an opposite rail and 122 cm (48 in.) straight cord. Two standard connectors are available: a male 5 pin, 240°, locking DIN (HBCS-7100); or a female, 9 pin D-sub squeeze to release, (HBCS-7108).

The optics module (HBCS-7150) is available which can be integrated into other equipment or used as a stand alone sensor assembly.

Applications

The digital bar code slot reader is a highly effective alternative to

BAR CODE

keyboard data entry. Bar code scanning is faster and more accurate than key entry and provides far greater throughput. In addition, bar code scanning typically has a higher first read rate and greater data accuracy than optical character recognition. When compared to magnetic stripe encoding, bar code offers significant advantages in flexibility of media, symbol placement and immunity to electromagnetic fields.

Hewlett-Packard's Industrial Digital Slot Reader is designed for applications where high first read rate and durability are important factors. The epoxy coated metal case with its tamper proof mounting system, makes these slot readers ideal choices for security access control, time and attendance recording and other bar coded badge and card reading applications.

Electrical Operation

The HBCS-71XX family of digital slot readers consists of a precision optical system, an analog amplifier, a digitizing circuit, and an output transistor. These elements provide a TTL compatible output from a single 4.5 V to 5.5 V DC power supply. The open collector transistor requires a pull-up resistor for proper operation.

A non-reflecting black bar results in a logic high (1) level output, while a reflecting white space will cause a logic low (0) level output. After power up, the slot reader will be fully operational after approximately 6 seconds. During operation, the slot reader will assume a logic low state after a short period (typically 1 second) if no bar code is scanned. This feature allows multiple scanners (slot readers and wands) to be connected together with a simple OR gate.

The slot reader connector provides a shield which is connected to signal ground. The shield is connected either to the metal housing of the 5 pin DIN connector, or to pin 8 of the 9 pin D-sub connector. A good connection to earth ground is recommended.

The maximum recommended cable length is 7.6 m (25 ft.).

WARNING:

OBSERVING THE INFRARED LIGHT SOURCE IN THE HBCS-7150 AT CLOSE DISTANCES FOR PROLONGED PERIODS OF TIME MAY CAUSE INJURY TO THE EYE. When mounted with the rail in place, the infrared output flux is radiologically safe. With the rail removed, precautions should be taken to avoid prolonged visual observation.

Mounting Considerations

Slot Reader

The slot reader (HBCS-7100/7108) is designed to be virtually tamper proof when mounted using the two rear mounting holes. In this case, the cable must be routed from the rear of the slot reader through the mounting surface (wall, door, etc.).

When mounting the slot reader, the cable may be routed through the mounting surface (see above), or it may be routed along grooves in the base and exit the side of the slot reader at any of four points. This allows flexibility in the mounting orientation.

Optics Module

The optics/electronics module (HBCS-7150) is designed for applications which require a different slot width, integration into a larger housing, or a fixed beam stationary scanner. When using the optics module, the operating distance from the front surface of the module to the symbol will vary depending on the symbol resolution. Figure 1 shows the relationship between operating range and *minimum* symbol resolution for a typical optics module.

This relationship was applied in the design of the slot reader, where a slot width of 3.2 mm (0.125 in.) insures excellent performance reading bar code symbols which have a nominal resolution of 0.19 mm (0.0075 in.) and include normal printing errors.

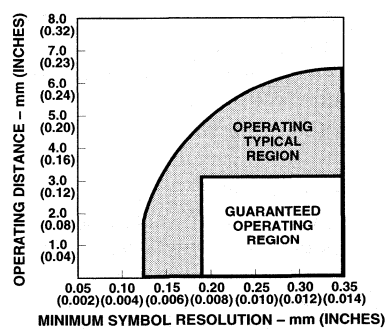


Figure 1.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Notes
Nominal Narrow Element Width		0.19 (0.0075)		mm (in.)	
Scan Velocity	V_{scan}	20 (8)	254 (100)	mm (in.)	1
Contrast	R_W-R_B	45		%	2
Supply Voltage	V_S	4.5	5.5	V	3
Ambient Temperature	T_A	-40	+70	°C	4
Ambient Light	E_V		100,000	lux	5

Absolute Maximum Ratings T_A = 25°C (unless specified otherwise)

Parameter	Symbol	Min.	Max.	Units	Notes
Storage Temperature	T_S	-40	+80	°C	
Supply Voltage	V_S	-0.3	+7.0	V	
Output Transistor Power	P_T		200	mW	
Output Collector Voltage	V_O	-0.3	+20	V	

Electrical Characteristics

T_A = 25°C, V_S = 4.5 V to 5.5 V (unless specified otherwise)

Parameter	Symbol	Typ.	Max.	Units	Conditions	Notes
Supply Current	I_S	56	100	mA	V_S = 5.0 V	
High Level Output Current	I_{OH}		1.0	µA	V_{OH} = 2.4 V	
Low Level Output Voltage	V_{OL}		0.4	V	I_{OL} = 16 mA	
Output Rise Time	t_r	0.9	5.0	µs	10% - 90% transition RL = 1 kΩ	
Output Fall Time	t_f	0.07	5.0	µs		
Electrostatic Discharge Immunity	ESD	25		kV		6

Notes:

1. Measured scanning a symbol with 0.19 mm narrow elements. For larger narrow element widths, the maximum scan speed will increase proportionally.
2. Contrast is defined as R_W-R_B where R_W is the reflectance of the white spaces and R_B is the reflectance of the black bars, measured at 880 nm.
3. Allowable power supply ripple and noise is frequency dependent. See Figure 5.
4. Non-condensing. If there is frost or dew over the optics window, it should be removed for optimal scanning performance.
5. Direct sunlight at any illumination angle.
6. The shield must be properly terminated (See Figure 2). The human body is modeled by discharging a 300 pF capacitor through a 500 Ω resistor. No damage to the slot reader will occur at the specified level.

Interface Specifications

The slot reader has two different standard connectors: a 5 pin, 240 metal locking DIN; or a 9 pin female D-sub squeeze to release. The recommended interface is shown in Figure 2. The mechanical specifications for the 5 pin DIN are shown in Figure 3. The mechanical specifications for the 9 pin D-sub are shown in Figure 4.

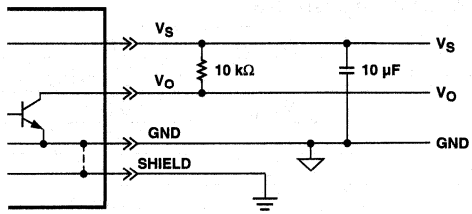


Figure 2. Recommended Interface.

Pinout

Function	5 pin DIN	9 pin D-sub
V_S	1	9
Output	2	2
Ground	4	7
Shield	Case	8
No Connect	3,5	1,3,4,5,6

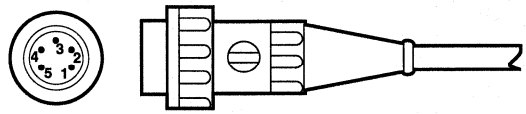


Figure 3. Connector Configuration for HBCS-71X0.

Shield and ground are tied together in the connector.

Note: If the part is purchased with stripped and tinned wires, or if the connector is removed, the ground and shield wires must be connected together for proper operation.

Wire Color

Function	Color
V_S	Red
Output	Yellow/White
Ground	Black
Shield	Braid

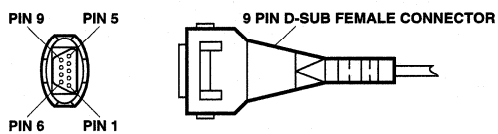


Figure 4. Connector Configuration for HBCS-71X8.

PSRR Performance

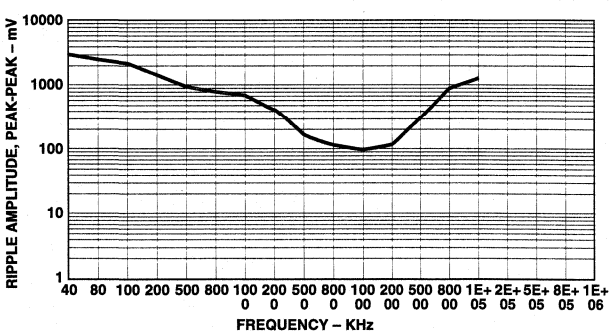
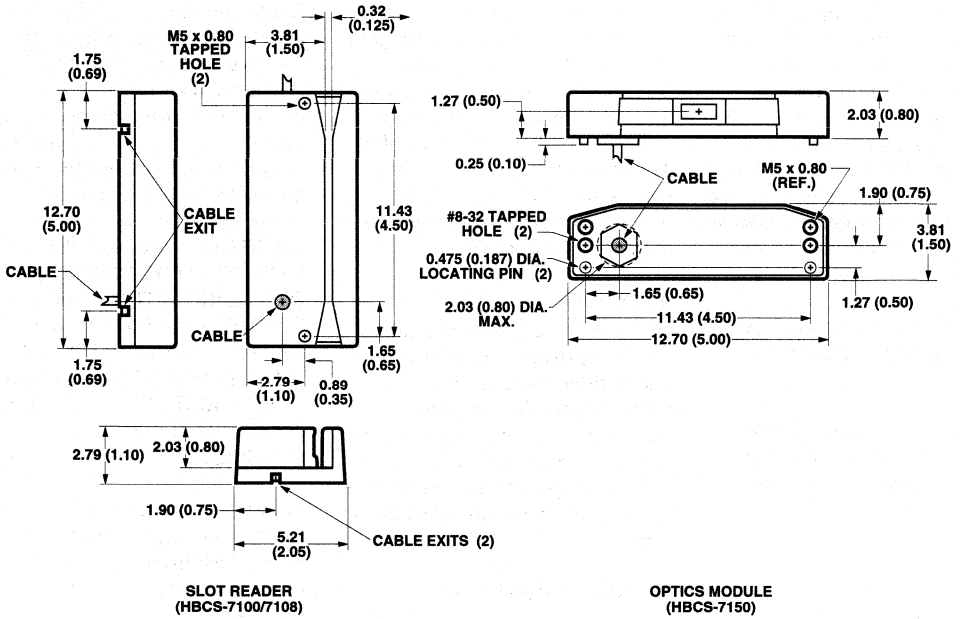


Figure 5. Ripple Noise Needed to Switch Output.

CE 96

The CE Mark demonstrates compliance with EC directives on EMC.

Dimensions



Notes:

7. Mounting holes on the HBCS-7100/7108 are suitable for either #10-32 or M5-0.80 screws.
8. Mounting holes on the HBCS-7150 are for #8-32 screws.
9. Slot readers and optics modules have a black textured epoxy finish.
10. All dimensions are nominal and are stated in millimeters and (inches).

Selection Guide

	HBCS-7100	HBCS-7150
5 pin DIN Connector	Standard	Standard
9 pin D-Sub Connector	HBCS-7108	NA
No Connector Strip and Tin Leads	HBCS-7104*	HBCS-7154*
Individually Boxed Slot Reader	Order Option #A01 with the above referenced part-number. The slot reader is shipped in a "kraft" box, including an HBCS-7100 series data sheet.	

*Build to order product only. Minimum stock available for engineering evaluation purchases.

Symbol Placement

The center of the slot reader's optical system is located 12.7 mm (0.50 in.) from the bottom of the slot. Consequently, bar code symbols to be read by the slot reader must be positioned on the card(s) or document(s) at a height which insures that all bars and spaces will cross a line located 12.7 mm from the bottom edge of the card(s) or document(s). For optimal performance, all bars and spaces should cross the area between 1.14 mm (0.45 in.) and 1.40 mm (0.55 in.) from the bottom edge.

The bars and spaces should be perpendicular to the bottom edge, however, a skew of ± 4 degrees from the perpendicular is acceptable.

Maintenance Considerations

The slot reader and optics module include a window which is slightly recessed in order to prevent direct contact with the bar code symbol. This reduces the wear on both the window and the symbol. The window may become dirty over a period of time. If this occurs, clean the window with a commercial glass cleaner.

Testing

All Hewlett-Packard slot readers are 100% tested for performance and digitizing accuracy after manufacture. This insures a consistent quality product. More information about Hewlett-Packard's test procedures, test set up, and test limits are available on request.

Optional Features

For options such as special cables or connectors, contact your nearest Hewlett-Packard sales office or authorized representative.

Warranty and Service

Hewlett Packard Slot Readers are warranted for a period of one year after purchase covering defects in material and workmanship. Hewlett-Packard will repair or, at its option, replace products that prove to be defective in material or workmanship under proper use during the warranty period.

NO OTHER WARRANTIES ARE EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. HEWLETT-PACKARD IS NOT LIABLE FOR CONSEQUENTIAL DAMAGES.

For additional warranty or service information, please contact your local Hewlett-Packard sales representative or authorized distributor.

Applications

The following abstracts represent application notes that are not published in this catalog. These application notes can be obtained from your local Hewlett-Packard sales office or authorized HP distributor or representative (see section 5).

Application Bulletin 75
ESD Control in Portable Bar Code Readers
This AB, which is applicable to the HBCS-AXXX series wands, provides information to help the designer of portable bar code decoders to harden their system to electrostatic discharge (ESD).

Ordering No. 5954-2170

AN 1008
Optical Sensing with the HBCS-1100
This AN gives the basic optical flux coupling design for discrete emitters and detectors. It presents the concepts of modulation transfer function, depth of field, and reflective sensor design. It also discusses the optical and electrical operation of the HBCS-1100 High-Resolution optical sensor. Finally, it presents electrical design techniques that allow the HBCS-1100 to interface with popular logic families.

Ordering No. 5091-7363E

AN 1013
Elements of a Bar Code System
This AN, which is applicable to all HP digital wands, describes in detail the elements that make up most bar code systems. Included is a discussion of the fundamental system design, detailed discussion of seven popular code symbologies, a section on symbol generation, and methods of data entry. A glossary of terms and a reference section are also included. This is an excellent publication for people who are just learning about bar code or for those who need a more comprehensive understanding of the subject.

Ordering No. 5953-9387

AN 1040
Ambient Light Rejection Circuit for the HEDS-1500
Bright ambient light causes the resolution of the HEDS-1500 sensor to degrade when the sensor is dc driven. This AN presents a circuit schematic that allows full resolution in bright ambient light. Included are graphs showing limits of current and voltage, and frequency responses under specific conditions.

Ordering No. 5952-2228

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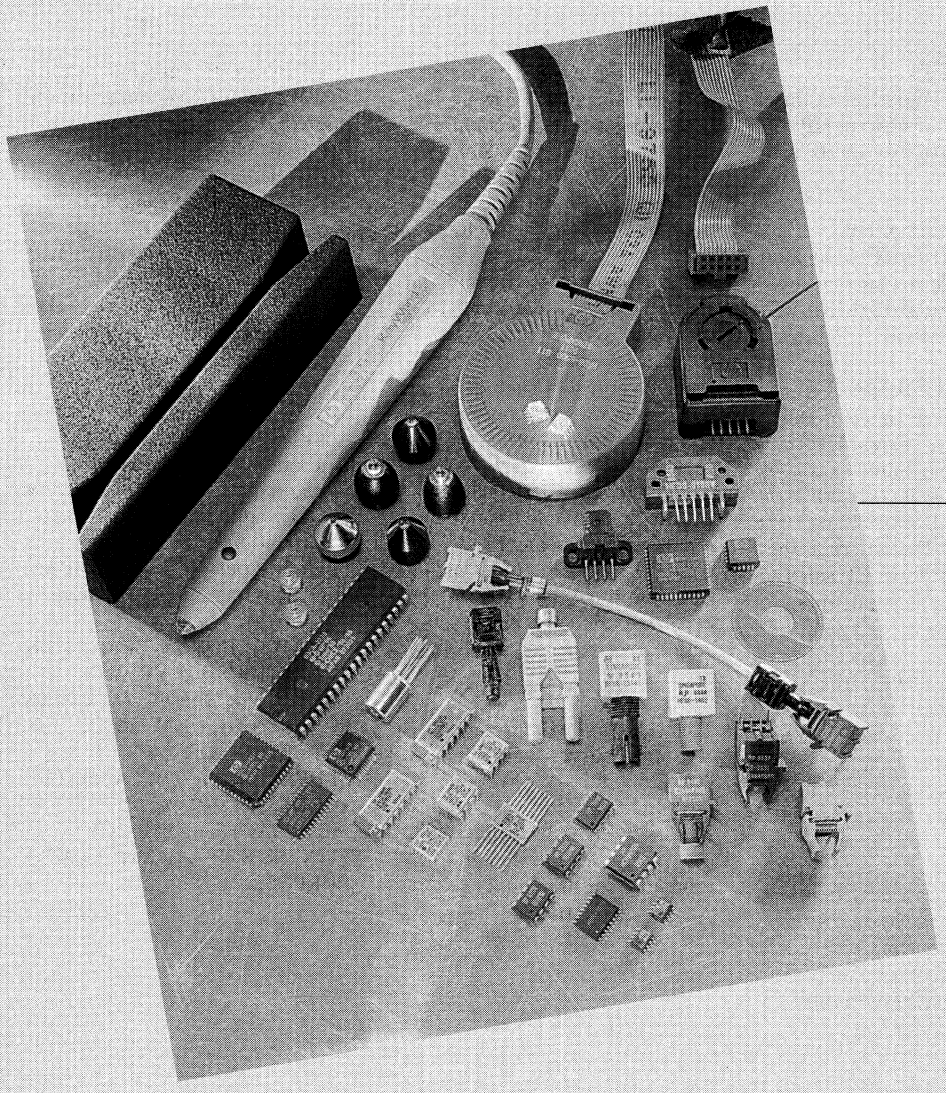
Ordering & Service Information 5-2
Authorized Distributor
& Representative Listing..... 5-3
HP Sales & Support Listing 5-11



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To order any component in this catalog, call your nearest HP authorized distributor or HP sales office.

A complete listing of HP authorized distributors is located on page 5-3. These distributors can offer off-the-shelf delivery for most HP components.

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For additional technical literature not available in this catalog, try our fax-back service (US and Canada only) at: 1-800-450-9455.

Information regarding Hewlett-Packard Components Group products is available on the World Wide Web via the Components Group home page at: **http://www.hp.com/go/components**

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c) Unless HP agrees in writing that Customer has configuration control, HP may make process or materials changes affecting the performance or other characteristics of Products. Products supplied after such a change will continue to meet HP's published minimum/maximum specifications, but may not be identical to Products supplied as samples or under prior orders.

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